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Issue 2

AT&T 3B2 Computer

Technical Reference Manual

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Chapter 1: INTRODUCTION

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INTRODUCTION

PURPOSE OF TECHNICAL REFERENCE MANUAL

This manual is intended for use by a sophisticated user, an Original Equipment Manufacturer (OEM), or a Value Added Retailer (VAR) who need physical and functional information on the AT&T 3B2 computer series (300, 310, 400, 500, 600, 700, and 1000) and associated peripheral add-ons.

MANUAL ORGANIZATION

This manual is structured so you can easily find information without having to read the entire text. The remainder of this manual is organized as follows.

- Chapter 2, "EQUIPMENT DESCRIPTION," is a hardware-oriented physical description of the 3B2 computers and peripherals.
- Chapter 3, "FUNCTIONAL DESCRIPTION," describes how the 3B2 computer operates. The peripherals operation and important information is also given.
- Appendix A, "VIRTUAL ADDRESS SPACE," gives the virtual memory address spectrum for the 3B2 computer.
- Appendix B, "CONNECTOR AND CABLING INFORMATION," provides card signal and connector information.

RELATED DOCUMENTATION

Other documents for OEM/VAR use are the following:

Crash Analysis Guide
: This guide describes the use of the **crash** command to examine the UNIX® system memory images following a system panic.

Feature Card Interface Design Manual
: This manual provides the information necessary to design a feature card for the 3B2 computer. Detailed information is provided on the Input/Output (I/O) bus.

Error Message Manual
: This manual contains error message descriptions and recommended actions for the various 3B2 computer error messages.

Off-Line Diagnostics Manual
: This manual describes the diagnostic phases and gives test descriptions for all 3B2 computer and feature card diagnostics.

Driver Design Guide
: This guide provides information for creating device drivers. Descriptions include firmware interfaces, how to write a block and character device driver, and how to install a driver.

Application Software Packaging Guide
: This guide identifies the requirements, guidelines, and templates for developers to use when creating software applications for inexperienced end users.

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EQUIPMENT DESCRIPTION

This chapter provides a **physical** description of the 3B2 computer system to a circuit card (board) level and defines the 3B2 computer hardware architecture.

The common system equipment configurations are defined by solution packages. The various solution packages for the 3B2 computer and AT&T Expansion Module (AT&T/XM) are detailed in the AT&T marketing information.

SYSTEM (EQUIPMENT) CONFIGURATIONS

Computer Models

The 3B2 computer is designed to support a wide range of processing needs. Features and capabilities are easily added to a basic configuration to create a system supporting a particular application (solution package).

The 3B2 computer family consists of seven models:

3B2/300 computer (Manufacturer discontinued.)

Entry level model providing:

- One integral floppy disk drive
- One integral hard disk drive
- Four feature card slots
- System Board, ED-4C637-30,G1 equipped with a WE® 32100 Microprocessor, WE 32101 Memory Management Unit, and a 8.2-MHz system clock. Early models use a CM190A System Board equipped with a WE 32002 Processor Module and a 7.2-MHz system clock (28.8-MHz oscillator divide by four).

3B2/310 computer

Current entry level model providing:

- One integral floppy disk drive
- One integral hard disk drive
- Four feature card slots
- System Board, ED-4C637-30,G3 or G4 equipped with a WE 32100 Microprocessor, WE 32101 Memory Management Unit, 10-MHz oscillator (system clock), and a WE 32106 Math Acceleration Unit (optional, G4).

3B2/400 computer

Beginning midrange model providing:

- One integral floppy disk drive
- One or two integral hard disk drives
- One cartridge tape drive
- Twelve feature card slots
- System Board, ED-4C637-30,G2 or G5 equipped with a WE 32100 Microprocessor, WE 32101 Memory Management Unit, 10-MHz oscillator (system clock), and a WE 32106 Math Acceleration Unit (optional, G5).

3B2/500 computer

Expanded midrange model providing:

- One integral floppy disk drive
- One Small Computer System Interface (SCSI) hard disk drive
- One cartridge tape drive
- Seven feature card slots
- Five performance card slots
- System Board (CM518A) equipped with a WE 32100 Microprocessor, WE 32101 Memory Management Unit, 18-MHz oscillator (system clock), and a WE 32106 Math Acceleration Unit.

3B2/600 computer

Larger midrange model providing:

- One integral floppy disk drive
- Two SCSI hard disk drives
- One cartridge tape drive
- Twelve feature card slots
- Twelve performance card slots
- System board equipped with a WE 32100 Microprocessor, WE 32101 Memory Management Unit, 18-MHz oscillator (system clock), and a WE 32106 Math Acceleration Unit.

3B2/700 computer

Enhanced larger model providing:

- One integral floppy disk drive
- Two SCSI hard disk drives
- One cartridge tape drive
- Twelve feature card slots
- Twelve performance card slots
- System board equipped with a WE 32200 Microprocessor, WE 32201 Memory Management Unit, 22-MHz oscillator (system clock), and a WE 32206 Math Acceleration Unit.

3B2/1000 computer

Top of the line model providing:

- One integral floppy disk drive
- Up to three SCSI hard disk drives
- One cartridge tape drive
- Twelve feature card slots
- Twelve performance card slots
- System board equipped with a WE 32200 Microprocessor, two WE 32201 Memory Management Units, 24-MHz oscillator (system clock), and a WE 32206 Math Acceleration Unit.

Minimum 3B2 Computer Equipment Configuration

The minimum 3B2 computer equipment configuration consists of a 3B2/300 computer equipped with the following:

- System Board, ED-4C637-30,G1 equipped with a WE 32100 Microprocessor, WE 32101 Memory Management Unit, 8.2-MHz system clock. Early models use a CM190A System Board equipped with a WE 32002 Processor Module and a 7.2-MHz system clock (28.8-MHz oscillator divide by four).
- One 5.25 inch, 720-kilobyte (formatted), double-sided, 96 tracks-per-inch floppy disk drive.
- One 10-megabyte (formatted) hard disk drive.
- A 0.5-megabyte Random Access Memory (RAM). Four expansion slots are provided for the equipage of feature cards.
- A data terminal connected to the CONSOLE port.

To this minimum 3B2/300 computer configuration, additional hard disk drives, floppy disk drives, and cartridge tape drives can be added via the equipage of one or more AT&T/XM cabinets. The integral hard disk drive configuration can also be expanded by changing the hard disk to a large capacity drive. A maximum of 432 megabytes of ST-506 hard disk memory (six 72-megabyte hard disk drives) can be equipped with a 3B2/300 or 3B2/310 computer and AT&T/XM cabinets. The size of the RAM can be expanded to a maximum of 4 megabytes. (Computers equipped with a red ON/STANDBY switch require a power supply upgrade to expand RAM above 2 megabytes.) A SCSI Host Adapter card (CM195W) can be used to interface a wide range of mass storage peripheral devices. Refer to the *AT&T SCSI (Small Computer System Interface) Definition,* (Select Code 305-013), for additional information on this capability.

Maximum 3B2 Computer Equipment Configuration

The maximum 3B2 computer equipment configuration consists of a 3B2/1000-80 computer fully equipped with the following:

- A system board equipped with WE 32200 Microprocessor, two WE 32201 Memory Management Units, 24-MHz oscillator (system clock), and a WE 32206 Math Acceleration Unit.
- One 5.25-inch, 720-kilobyte (formatted), double-sided, 96 tracks-per-inch floppy disk drive.
- Three 300-megabyte (formatted) SCSI hard disk drives.
- A 64-megabyte RAM.
- One 120-megabyte SCSI Cartridge Tape Drive.
- Twelve expansion slots. One expansion slot is used for the SCSI Host Adapter card. The other eleven expansion slots can be used for additional Host Adapter cards or other feature cards.

To the 3B2/1000-80 computer configuration, additional hard disk drives, 9-track tape drives, and cartridge tape drives can be added via the SCSI Host Adapter card (CM195W or CM521A). This card can be used to interface a wide range of mass storage peripheral devices. Over 14 gigabytes of external hard disk memory can be equipped with a 3B2/1000-80 computer and SCSI expansion cabinets. Refer to the *AT&T SCSI (Small Computer System Interface) Definition,* (Select Code 305-013), for additional information on this capability.

Add-On Features

The following equipment and features can be added to a 3B2 computer configuration.

Data Terminal/Communications Equipment

Various terminals, printers, and other peripheral devices can be connected to a 3B2 computer. Some of these devices are briefly described in the following paragraphs.

AT&T Automatic Dial Modem. The AT&T Automatic Dial Modem is an intelligent, asynchronous, autodial/autoanswer modem operating at user selectable speeds of 300/1200 baud. The modem can be connected to either a data terminal or to the host computer.

TELETYPE® Model 5410/AT&T Model 4410 Terminal. The TELETYPE Model 5410/AT&T Model 4410 terminal is an asynchronous, serial, video display terminal. It features a selectable 80- or 132-column screen. The low-profile keyboard has a standard typewriter layout with eight programmable function keys.

TELETYPE Model 5420/AT&T Model 4415 Terminal. The Model 5420/4415 terminal has been replaced by the 5425/4425 terminal.

TELETYPE Model 5425/AT&T Model 4425 Terminal. The Model 5425/4425 terminal has all the features of the 5410/4410 terminal plus features such as full screen windowing, five different character sets, a fully buffered auxiliary printer port, and up to 38 downloadable function keys. An optional feature available with this terminal is an integral 300/1200 baud modem/dialer with five autodial strings. This terminal has replaced the TELETYPE 5420/AT&T Model 4415 buffered terminal.

TELETYPE Model 5620 Dot-Mapped Display Terminal. The Model 5620 terminal is a Dot-Mapped Display terminal featuring the WE 32000 Microprocessor System. This terminal features 256-kilobyte or 1-megabyte Dual Port Random Access Memory (DPRAM) with transparent refresh and 1000 dots-per-square-inch resolution on a 15-inch diagonal, nonglare screen. A dot addressable screen gives the user the capability to create full graphics, define character fonts, and make line drawings. The electronic mouse on this terminal can be used to create and control up to six window displays when used with supporting software on the host computer system.

AT&T 605 Terminals. The AT&T 605 Business Communications Terminal (BCT) offers the features of basic terminals. It is PC compatible, has 80- or 132- column operation, and a 102-key keyboard with 36 programmable function keys. There are two RS32-C ports, one for host communications and one for a printer.

AT&T 615 Terminals. The AT&T 615 Multitasking Terminal (MT) is an interactive, character-at-a-time keyboard/display terminal optimized for windowing capabilities. Multitasking feature allows simultaneous access for up to three applications. There is also a slot for optional input/output cards. The AT&T 615 MT also supports an autodialer card.

AT&T 620 Terminals. The AT&T 620 Multitasking Terminal with Graphics (MTG) is a full featured terminal with a bit-mapped screen. It offers the same features as the AT&T 615 MT plus 256 kilobytes of RAM (512 kilobytes optional), up to six active layers, a three-button mouse, and built-in emulation.

AT&T 630 Terminals. The AT&T 630 MTG has the same capability of the TELETYPE Model 5620. The user interface offers more advanced features like cut and paste between windows, scrolling of lines in a window, and resident fonts. The 630 MTG has a three-button mouse, 640 kilobytes of RAM, 384 kilobytes of Erasable Programmable Read Only Memory (EPROM), a 68000 microprocessor, and cartridge Read Only Memory (ROM) expansion capabilities. The 16-inch diagonal monitor has 1024 dots-per-inch resolution on a coated, nonglare screen.

Model DQP-10 Printer. The Model DQP-10 printer is a dot-matrix, serial, impact printer capable of bidirectional printing at 120 characters per second. At six or eight vertical lines per inch, the DQP-10 printer will print up to 80 characters per line with 10 characters per inch. Single sheet (8.5 x 11 inches) or continuous fanfold paper, up to 10 inches wide, can be used.

Model 470 and 475 Printers. The Model 470 and 475 printers are compact, desktop, dot-matrix, impact printers. They are capable of bidirectional printing at speeds up to 120 characters per second. They can print up to 132 characters per line, in a compressed font mode, at 16.8 characters per inch. The friction paper feed and integral tractor/pin feed mechanism can handle paper up to 10 inches wide. The only difference between the two printers is the type of interface. The Model 470 printer is equipped with a 36-pin parallel interface; the Model 475 printer is equipped with a serial RS-232C interface.

Model 5310 and 5320 Printers. The Model 5310 and 5320 printers are dot-matrix, bidirectional, logic-seeking printers offering sophisticated graphics capabilities. They can print up to 200 characters per second. These printers offer a wide range of form and paper handling options. Carriage size and maximum characters per line are the differences between the two printers. The Model 5310 has a 80-column carriage; the Model 5320 has a 132-column carriage. The Model 5310 can print up to 132 characters per line; the Model 5320 can print up to 220 characters per line.

Model LQP-40 Printer. The Model LQP-40 printer is a daisy-wheel, letter-quality, serial/parallel printer with a 48,000-byte data buffer. At six or eight vertical lines per inch, the LQP-40 printer uses proportional fonts with speeds up to 18 characters per second. Single sheet (8.5 x 11 inches) or continuous fanfold paper, up to 16.5 inches wide, can be used.

Model 455 Printer. The Model 455 printer is a daisy-wheel, letter-quality printer capable of speeds up to 55 characters per second. The printer is compatible with both serial and parallel interfaces. Friction and tractor feeds will handle paper up to 15 inches wide. As many as 197 characters can be printed on a single line, and a variety of font styles can be obtained by changing the daisy wheel.

RAM Expansion

The 3B2/300, 310, and 400 computers can be equipped with a maximum of two memory cards to form the RAM. RAM is expandable in 1-megabyte increments to the maximum size of 4 megabytes. A power supply upgrade is required for 3B2/300 computers with a red ON/STANDBY switch to expand RAM to 3 or 4 megabytes.

A 3B2/500 computer can be equipped with a maximum of two memory cards. These memory cards can be 2 megabytes or 4 megabytes, up to the maximum capacity of 8 megabytes.

The 3B2/600, 700, and 1000 computers can be equipped with a maximum of four memory cards. RAM is expandable in 2-megabyte increments to the maximum size of 16 megabytes for the 3B2/600 computer or 64 megabytes for the 3B2/700 and 1000 computers.

Hard Disk Expansion

Additional hard disk drives can be added to an existing 3B2 computer. The hard disks are either ST-506 type hard disks or SCSI hard disks, according to the associated computer. Two sizes of ST-506 hard disk drives are available: 30 megabytes and 72 megabytes (formatted). The 3B2/300 and 310 computers can support a maximum of six hard disk drives (one in the computer cabinet and five in two AT&T/XM cabinets) for a maximum of 432 megabytes of ST-506 hard disk memory. The 3B2/400 computer can support a maximum of ten hard disk drives (two in the computer cabinet and eight in AT&T/XM cabinets) for a maximum of 720 megabytes of ST-506 hard disk memory. Each AT&T/XM cabinet can house a maximum of three hard disk drives.

Additional hard disk drives can be added to an existing 3B2 computer using a SCSI. A SCSI Host Adapter card provides the interface between the computer and the SCSI bus. The SCSI hard disks are either 147 megabytes (formatted), 300 megabytes (formatted), or 600 megabytes (formatted). Many combinations of the different sizes of hard disks can be produced for over 14 gigabytes of external

storage. Refer to the *AT&T SCSI (Small Computer System Interface) Definition,* (Select Code 305-013), for additional information on this capability.

Removable Media Expansion

There are various forms of removable media available with 3B2 computers. Some are standard equipment while others are optional.

Floppy Disk. A second 720-kilobyte, double-sided, 96 tracks-per-inch, floppy disk drive can be equipped in an AT&T/XM. Connection to the host 3B2 computer is via a CM195H Cartridge Tape Controller (CTC) Card. While it is possible to equip more than two floppy disk drives on a system, equipage of more than two floppy disk drives is not practical. Two floppy disk drives provide drive-to-drive operational capabilities that are considered to be the optimum floppy disk drive equipage.

23-Megabyte Cartridge Tape. One or more 23-megabyte cartridge tape drives can be added to a 3B2 computer. The drive can be mounted in an AT&T/XM cabinet or by itself in a Tape Module cabinet. Each cartridge tape drive connects to the host 3B2 computer via a CM195H Cartridge Tape Controller Card that is installed in a 3B2 computer feature card slot. For a 3B2/400, the first cartridge tape controller is equipped in slot 2. Each CM195H CTC Card can interface two peripheral devices (one floppy disk and one cartridge tape drive). Simultaneous access of the two devices connected to the same CM195H CTC Card is not possible.

60- and 120-Megabyte Cartridge Tape. Additional 60- and 120-megabyte cartridge tape drives can be added to an existing 3B2 computer using a SCSI. A CM195W SCSI Host Adapter Card provides the interface between the computer and the SCSI bus. Refer to the *AT&T SCSI (Small Computer System Interface) Definition,* (Select Code 305-013), for additional information on this capability.

Rewritable Optical Disk. The SCSI Rewritable Optical Disk Module can be added to an existing 3B2 computer. The optical disk removable media provides approximately 584 megabytes (292 megabytes per side) of formatted storage capacity. A CM195W SCSI Host Adapter Card provides the interface between the computer and the SCSI bus. Refer to the *AT&T SCSI (Small Computer System Interface) Definition,* (Select Code 305-013), for additional information on this capability.

AT&T 3BNET Local Area Network

The AT&T 3B2 computers can serve as nodes on the AT&T 3BNET Local Area Network (3BNET LAN). The 3BNET LAN is an Ethernet compatible network operating at 10 megabits per second using the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithm. The lowest level protocols conform to the Institute of Electrical and Electronics Engineers (IEEE) 802.3 standards for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) local area networking. The connection of a 3B2 computer to the 3BNET is via a CM195A Network Interface Card that is installed in a 3B2 computer feature card slot.

AT&T STARLAN Network

The AT&T STARLAN network is a low-cost, local area network for linking MS-DOS* and UNIX system-based computers. The STARLAN network runs at 1 megabit per second on twisted pair wiring. The wiring is based on AT&T's Premises Distribution System (PDS). The high-level protocols support applications written for Microsoft Networks.

Connection to STARLAN from a 3B2 computer is provided by a CM195U Network Access Unit (NAU) Card that plugs into a 3B2 computer feature card slot.

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* Registered trademark of Microsoft Corp.

The AT&T STARLAN 3B2 Computer Network Program provides file transfer and electronic mail services for AT&T 3B2 computers and UNIX Personal Computer (PC) workstations. The STARLAN network PC interface supports the following capabilities:

- Enables MS-DOS machines to do file sharing and print sharing with other MS-DOS machines.
- Enables MS-DOS machines to store files on UNIX system machines.
- Enables MS-DOS machines to use peripheral devices associated with UNIX system machines.
- Enables UNIX system machines to do file transfers and exchange mail.
- Enables UNIX system machines to share remote printers associated with other UNIX system machines.
- Provides print queue query and other administrative services.
- Provides security features to restrict access to network resources.

Debug Monitor (DEMON)

The DEbug MONitor (DEMON) is a firmware resident option for Version 2 3B2 computers. The DEMON is a development aid in verifying hardware operation and debugging software or firmware. Refer to the *AT&T 3B2 Computer Debug Monitor Guide,* (Select Code 305-442), for more information.

HARDWARE OVERVIEW

Domestic 3B2/300 Computer Cabinet (ED-4C492-30)

Major Assemblies

Figure 2-1 shows a typical domestic 3B2/300 computer. The major assemblies include the following:

- Power Supply Unit (TRW #095-10011-XX1 or TRW #095-10060-00) set for 115 volt AC operation
- One Floppy Disk Drive, KS-23114,L4
- One Hard Disk Drive:
  - 10-megabyte, KS-23023,L1
  - 30-megabyte, KS-23054,L1
  - 72-megabyte, KS-23054,L2.
- CM190A System Board (Discontinued Availability)
  or
  System Board, ED-4C637-30,G1
- CM193A/B Backplane and card cage
- Memory card(s)
- Auxiliary Disk Interface, ED-4C632-30
- Dual Universal Asynchronous Receiver/Transmitter (DUART) Connector-2 Interface, ED-4C492-35,G5 and G5A
- Backup battery.

Domestic 3B2/300 Computer Equipment Characteristics

Physical.

Height	3.6 inches
Width	22 inches
Depth	17 inches
Weight	Approximately 30 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	115 V AC, 4 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 200 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	640 Btu/hour (maximum) 188 watts
Noise Level	Approximately 40 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	6 to 10
CPU Benchmark	0.61 Million Instructions Per Second (MIPS)

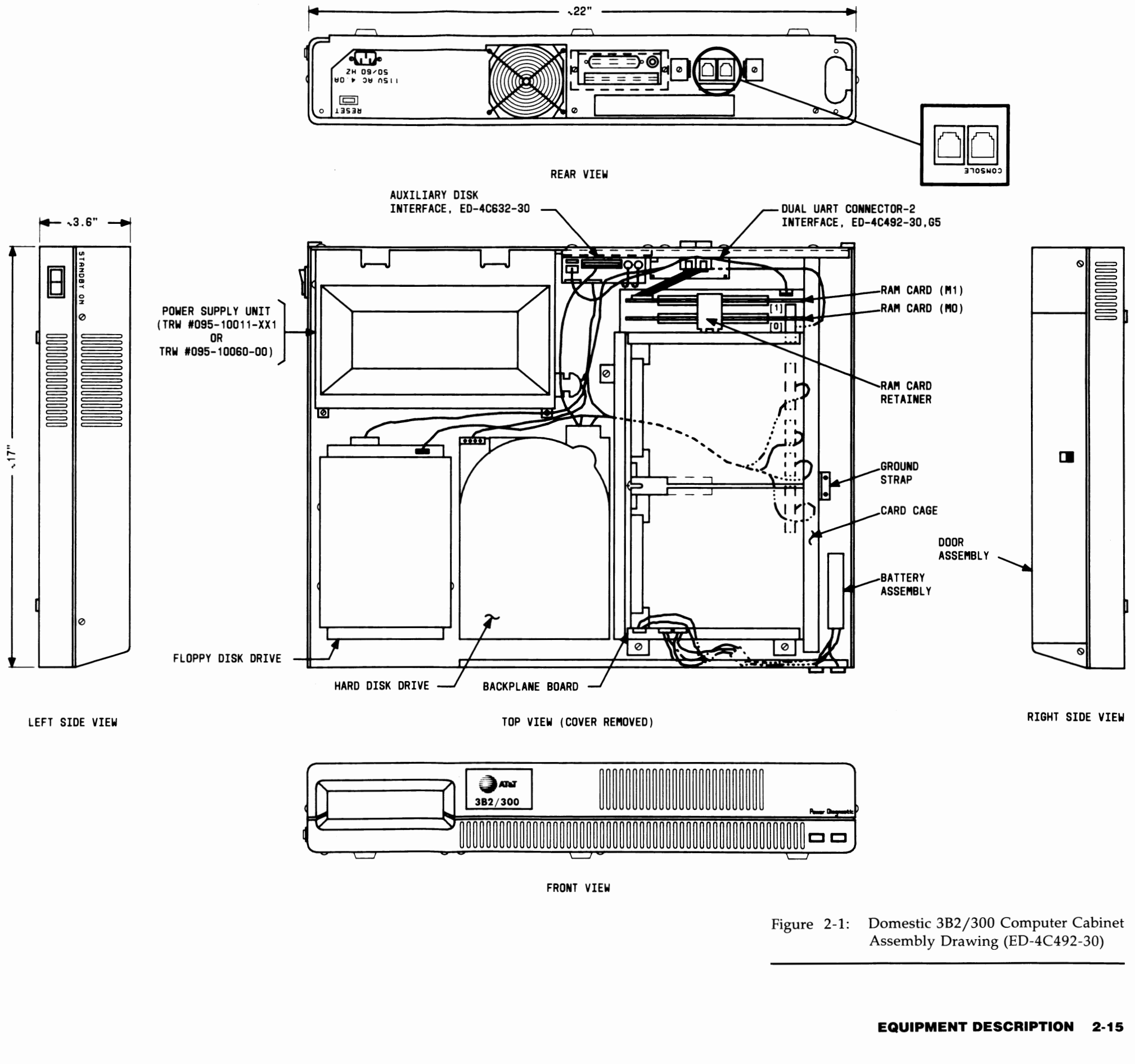


Figure 2-1: Domestic 3B2/300 Computer Cabinet Assembly Drawing (ED-4C492-30)

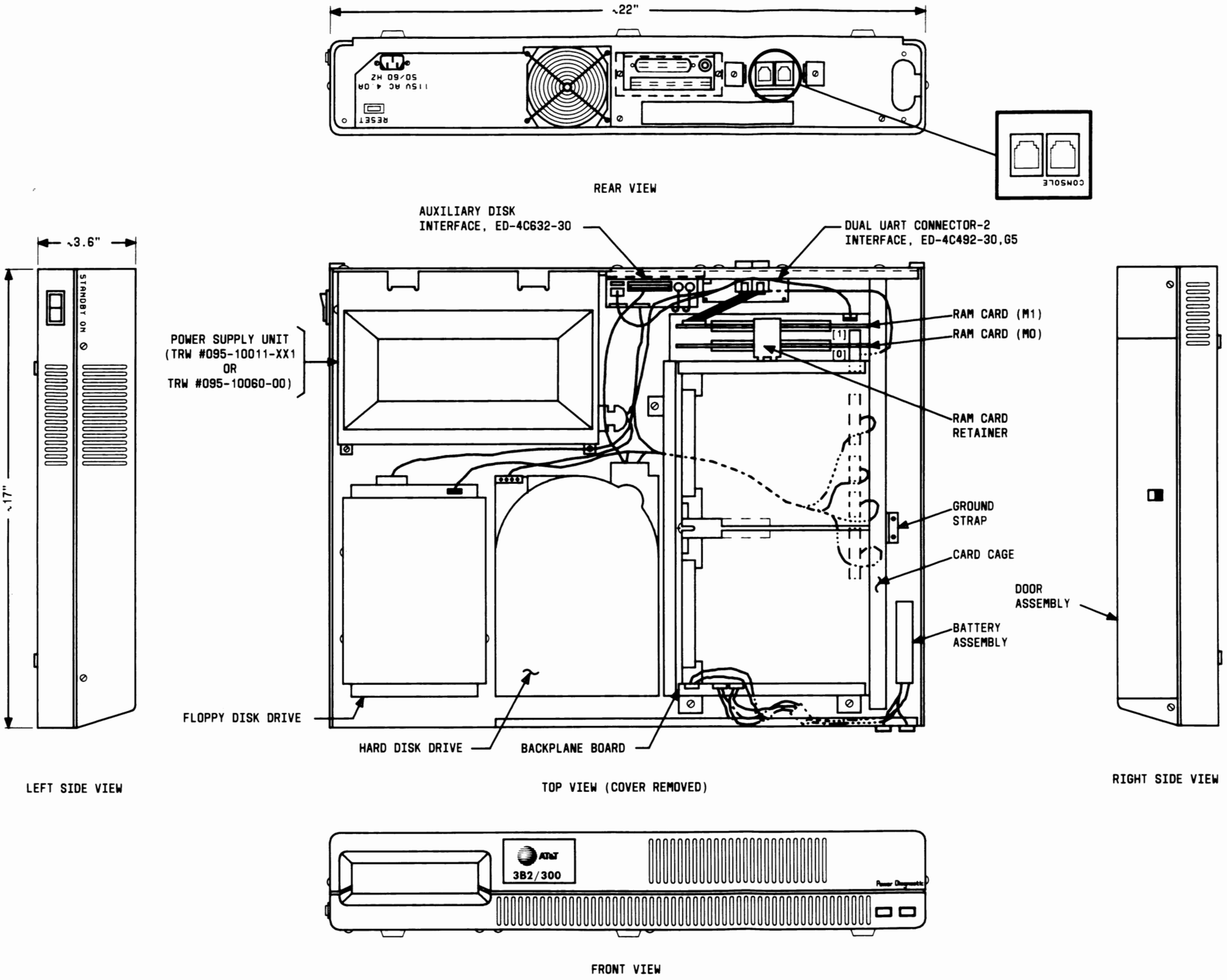


Figure 2-1: Domestic 3B2/300 Computer Cabinet Assembly Drawing (ED-4C492-30)

International 3B2/300 Computer Cabinet (ED-4C560-30)

Major Assemblies

Figure 2-2 shows a typical international 3B2/300 computer. The major assemblies include the following:

- Power Supply Unit (TRW #095-10011-XX2 or TRW #095-10061-00) set for 220 to 240 volt AC operation
- One Floppy Disk Drive, KS-23114,L4
- One Hard Disk Drive:
  - 10-megabyte, KS-23023,L1
  - 30-megabyte, KS-23054,L1
  - 72-megabyte, KS-23054,L2.
- CM190A System Board (Discontinued Availability)
  or
  System Board, ED-4C637-30,G1
- CM193A/B Backplane and card cage
- Memory card(s)
- Auxiliary Disk Interface, ED-4C632-30
- DUART Connector-2 Interface, ED-4C492-35,G5 and G5A
- Backup battery.

International 3B2/300 Computer Equipment Characteristics

Physical.

Height	3.6 inches
Width	22 inches
Depth	17 inches
Weight	Approximately 30 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	220 to 240 V AC, 2 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 200 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	640 Btu/hour (maximum) 188 watts
Noise Level	Approximately 40 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	6 to 10
CPU Benchmark	0.61 Million Instructions Per Second (MIPS)

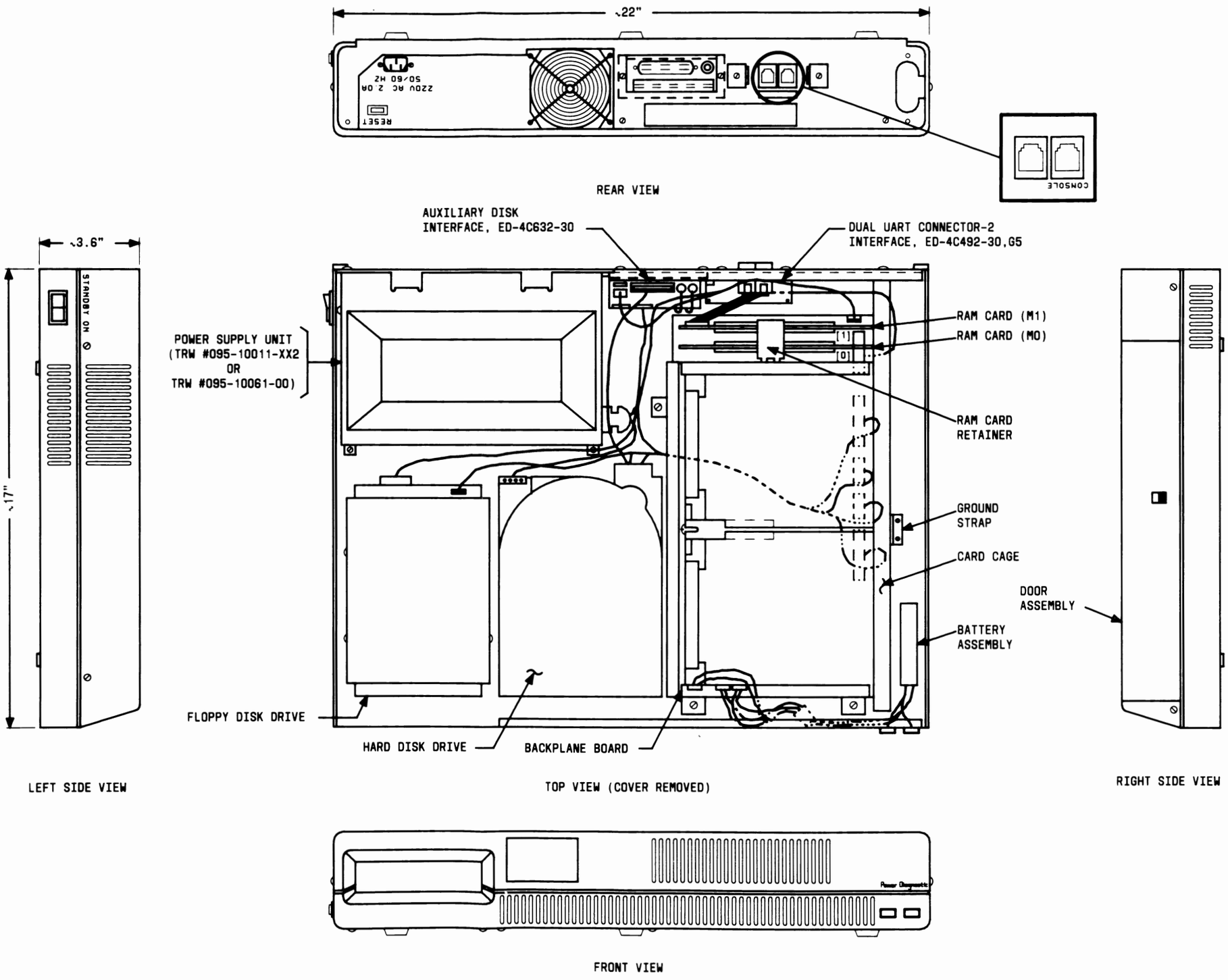


Figure 2-2: International 3B2/300 Computer Cabinet Assembly Drawing (ED-4C560-30)

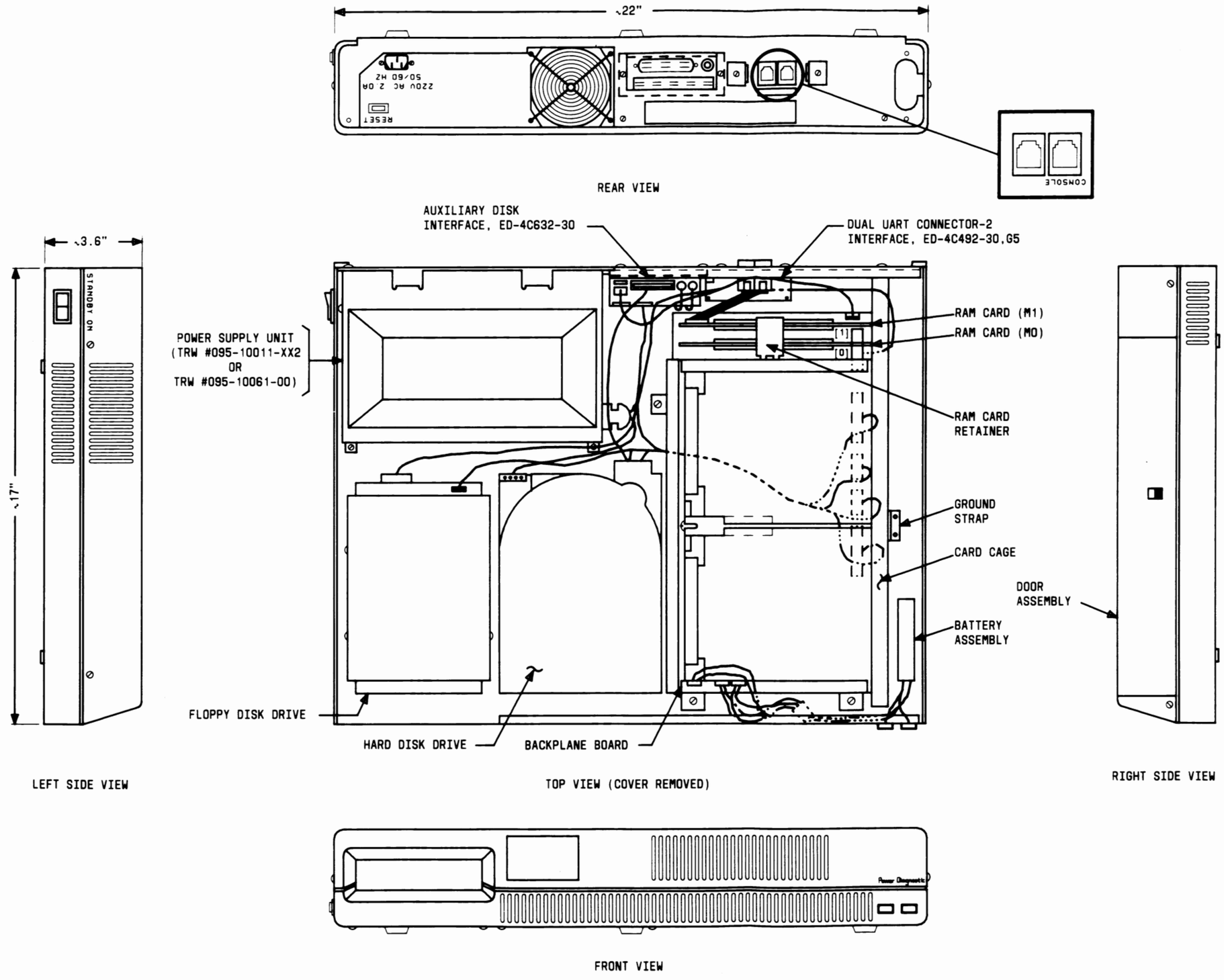


Figure 2-2: International 3B2/300 Computer Cabinet Assembly Drawing (ED-4C560-30)

Domestic 3B2/310 Computer Cabinet (ED-4C645-30)

Major Assemblies

Figure 2-3 shows a typical domestic 3B2/310 computer. The major assemblies include the following:

- Power Supply Unit (TRW #095-10011-XX1 or TRW #095-10060-00) set for 115 volt AC operation
- One Floppy Disk Drive, KS-23114,L4
- One Hard Disk Drive:
  - 30-megabyte, KS-23054,L1
  - 72-megabyte, KS-23054,L2.
- System Board ED-4C637-30,G3 [without Math Acceleration Unit (MAU)] or ED-4C637-30,G4 (with MAU)
- CM193A/B Backplane and card cage
- Memory card(s)
- Auxiliary Disk Interface, ED-4C632-30
- DUART Connector-2 Interface, ED-4C492-35,G5 and G5A
- Backup battery.

Domestic 3B2/310 Computer Equipment Characteristics

Physical.

Height	3.6 inches
Width	22 inches
Depth	17 inches
Weight	Approximately 30 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	115 V AC, 4 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 200 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	640 Btu/hour (maximum) 188 watts
Noise Level	Approximately 40 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	6 to 14
CPU Benchmark	1.12 Million Instructions Per Second (MIPS)

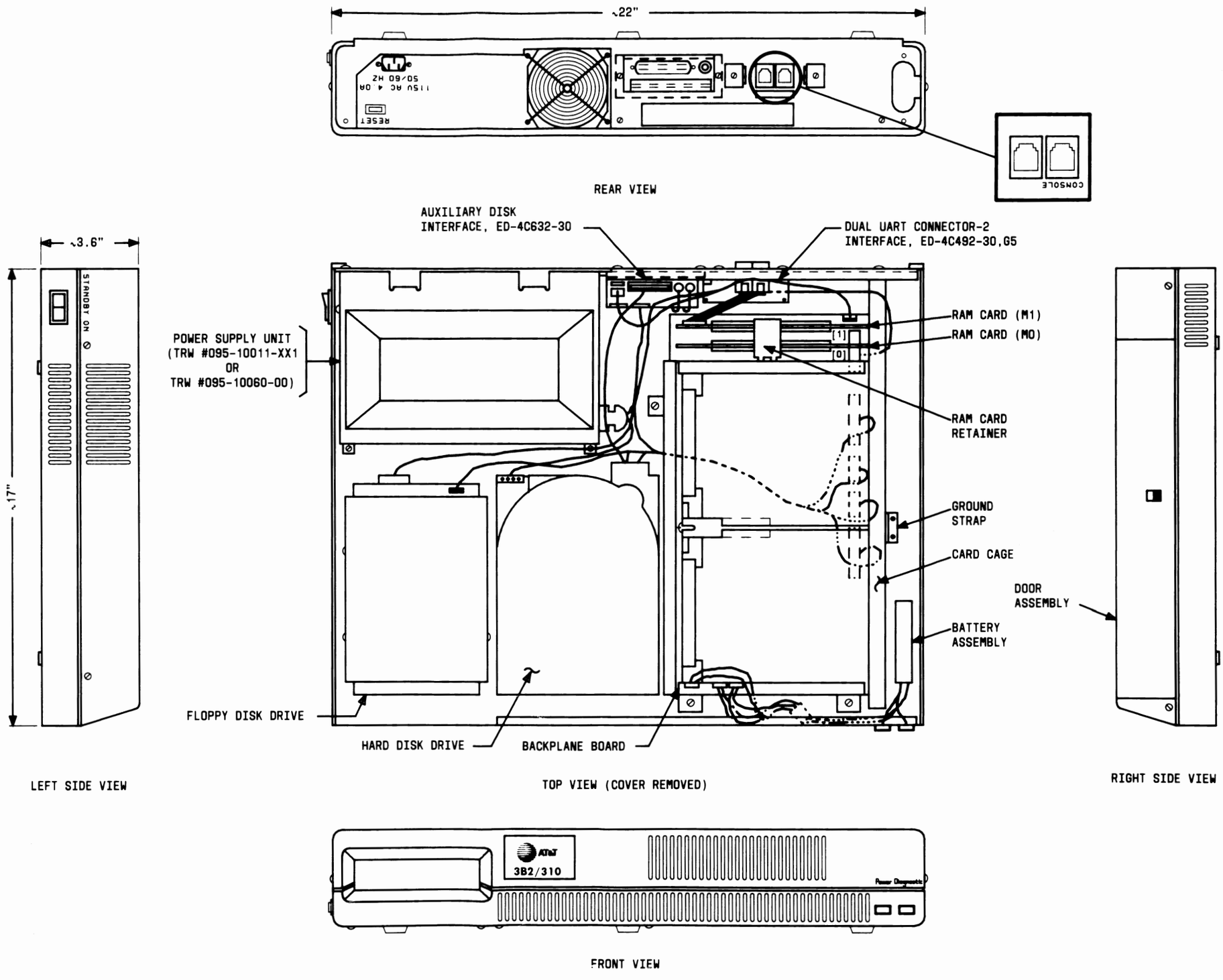


Figure 2-3: Domestic 3B2/310 Computer Cabinet Assembly Drawing (ED-4C645-30)

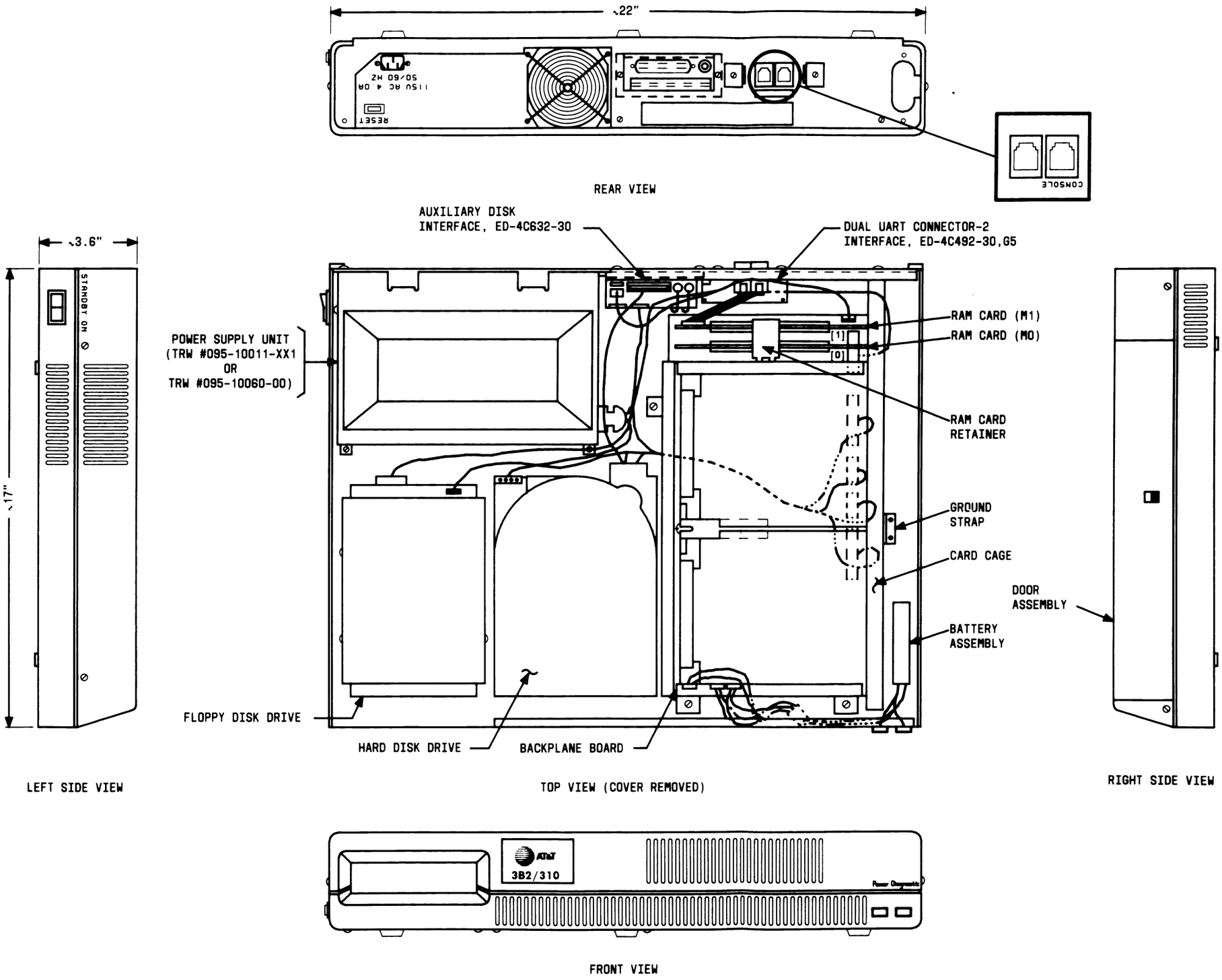


Figure 2-3: Domestic 3B2/310 Computer Cabinet Assembly Drawing (ED-4C645-30)

International 3B2/310 Computer Cabinet (ED-4C646-30)

Major Assemblies

Figure 2-4 shows a typical international 3B2/310 computer. The major assemblies include the following:

- Power Supply Unit (TRW #095-10011-XX2 or TRW #095-10061-00) set for 220 to 240 volt AC operation
- One Floppy Disk Drive, KS-23114,L4
- One Hard Disk Drive:
  - 30-megabyte, KS-23054,L1
  - 72-megabyte, KS-23054,L2.
- System Board ED-4C637-30,G3 (without MAU) or ED-4C637-30,G4 (with MAU)
- CM193A/B Backplane and card cage
- Memory card(s)
- Auxiliary Disk Interface, ED-4C632-30
- DUART Connector-2 Interface, ED-4C492-35,G5 and G5A
- Backup battery.

International 3B2/310 Computer Equipment Characteristics

Physical.

Height	3.6 inches
Width	22 inches
Depth	17 inches
Weight	Approximately 30 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	220 to 240 V AC, 2 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 200 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	640 Btu/hour (maximum) 188 watts
Noise Level	Approximately 40 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	6 to 14
CPU Benchmark	1.12 Million Instructions Per Second (MIPS)

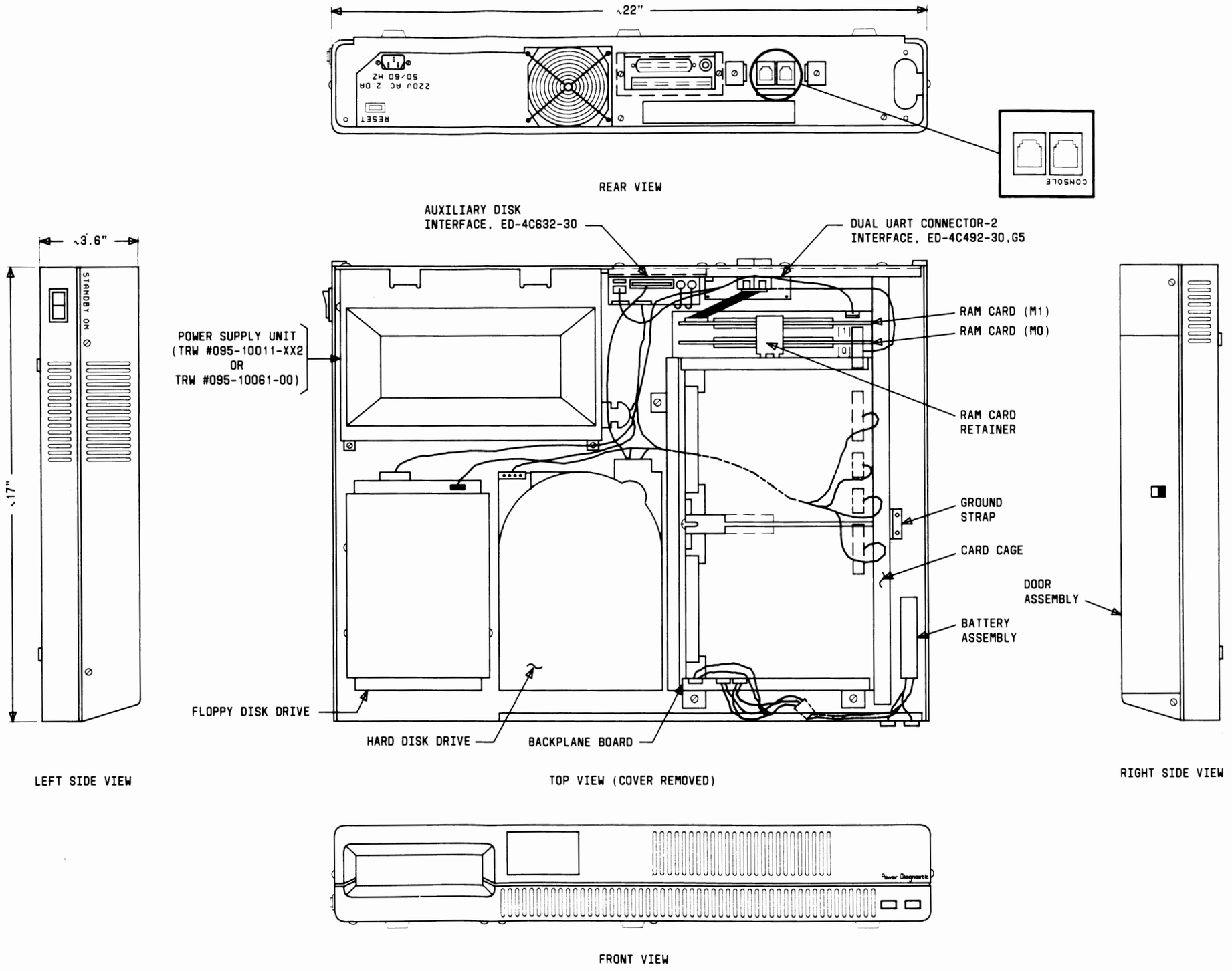


Figure 2-4: International 3B2/310 Computer Cabinet Assembly Drawing (ED-4C646-30)

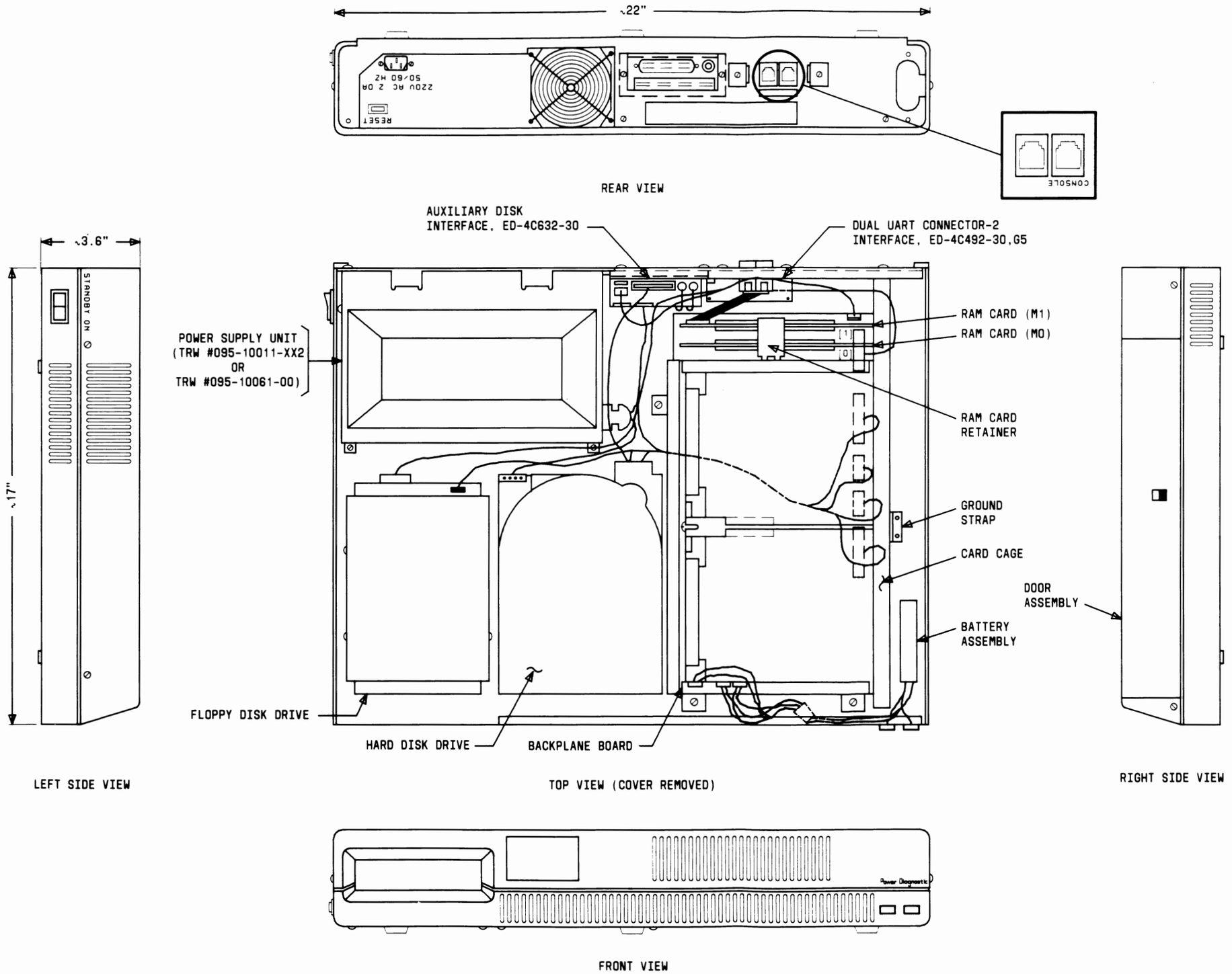


Figure 2-4: International 3B2/310 Computer Cabinet Assembly Drawing (ED-4C646-30)

Domestic 3B2/400 Computer Cabinet (ED-4C631-30)

Major Assemblies

Figure 2-5 shows a typical domestic 3B2/400 computer. The major assemblies include the following:

- Power Supply Unit (TRW #095-10035-XX1) set for 115 volt AC operation
- One Floppy Disk Drive, KS-23114,L4
- One or two Hard Disk Drives:
  - 30-megabyte, KS-23054,L1
  - 72-megabyte, KS-23054,L2.
- One 23-megabyte Cartridge Tape Drive, KS-23165,L1
- System Board ED-4C637-30,G2 (without MAU) or ED-4C637-30,G5 (with MAU)
- CM194B Backplane and card cage
- Memory card(s)
- DUART Connector-2 Interface, ED-4C631-35,G2
- Backup battery.

Domestic 3B2/400 Computer Equipment Characteristics

Physical.

Height	7.2 inches
Width	22 inches
Depth	18 inches
Weight	Approximately 60 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	115 V AC, 6 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 350 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	1200 Btu/hour (maximum) 352 watts
Noise Level	Approximately 45 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	10 to 25
CPU Benchmark	1.12 Million Instructions Per Second (MIPS)

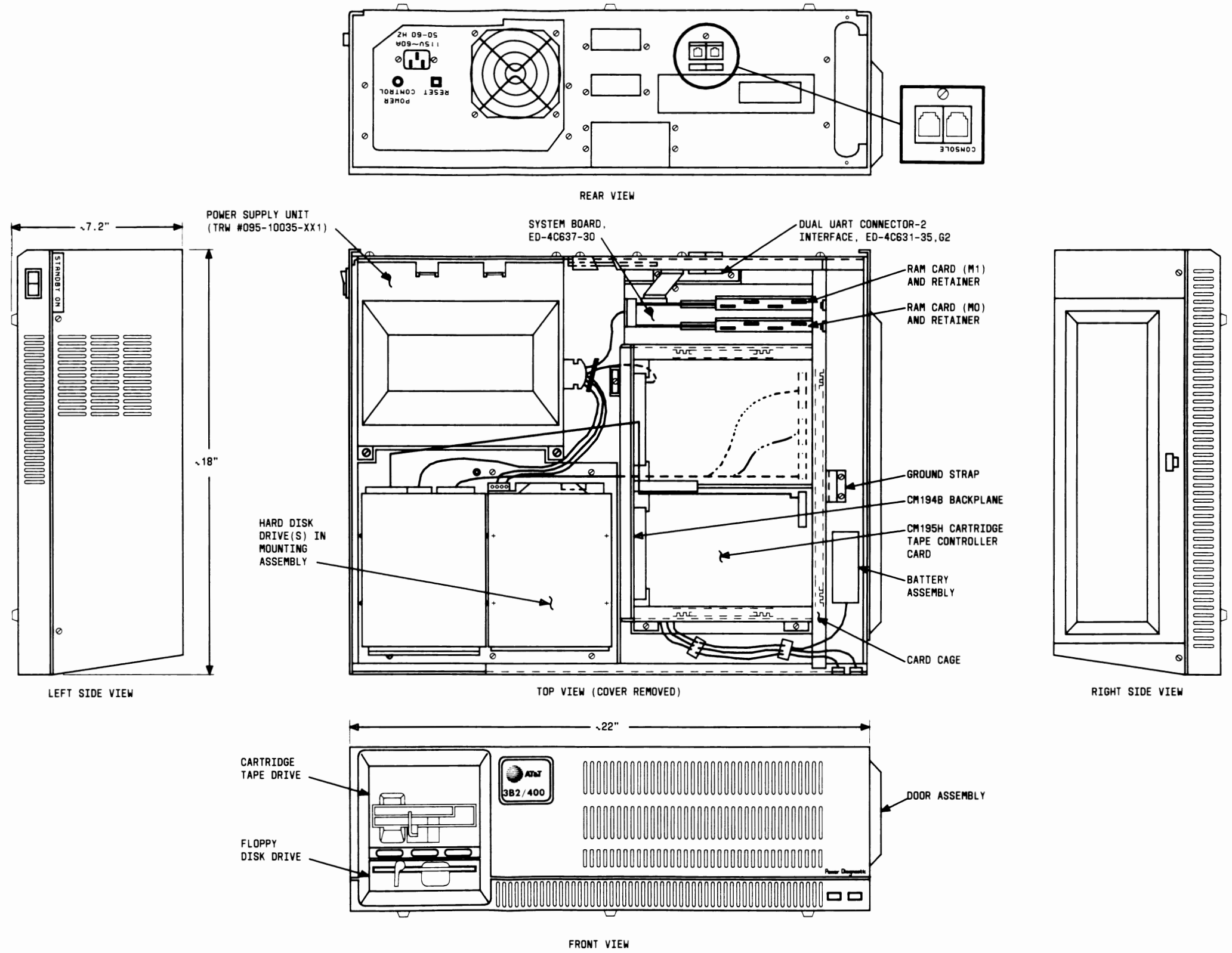


Figure 2-5: Domestic 3B2/400 Computer Cabinet Assembly Drawing (ED-4C631-30)

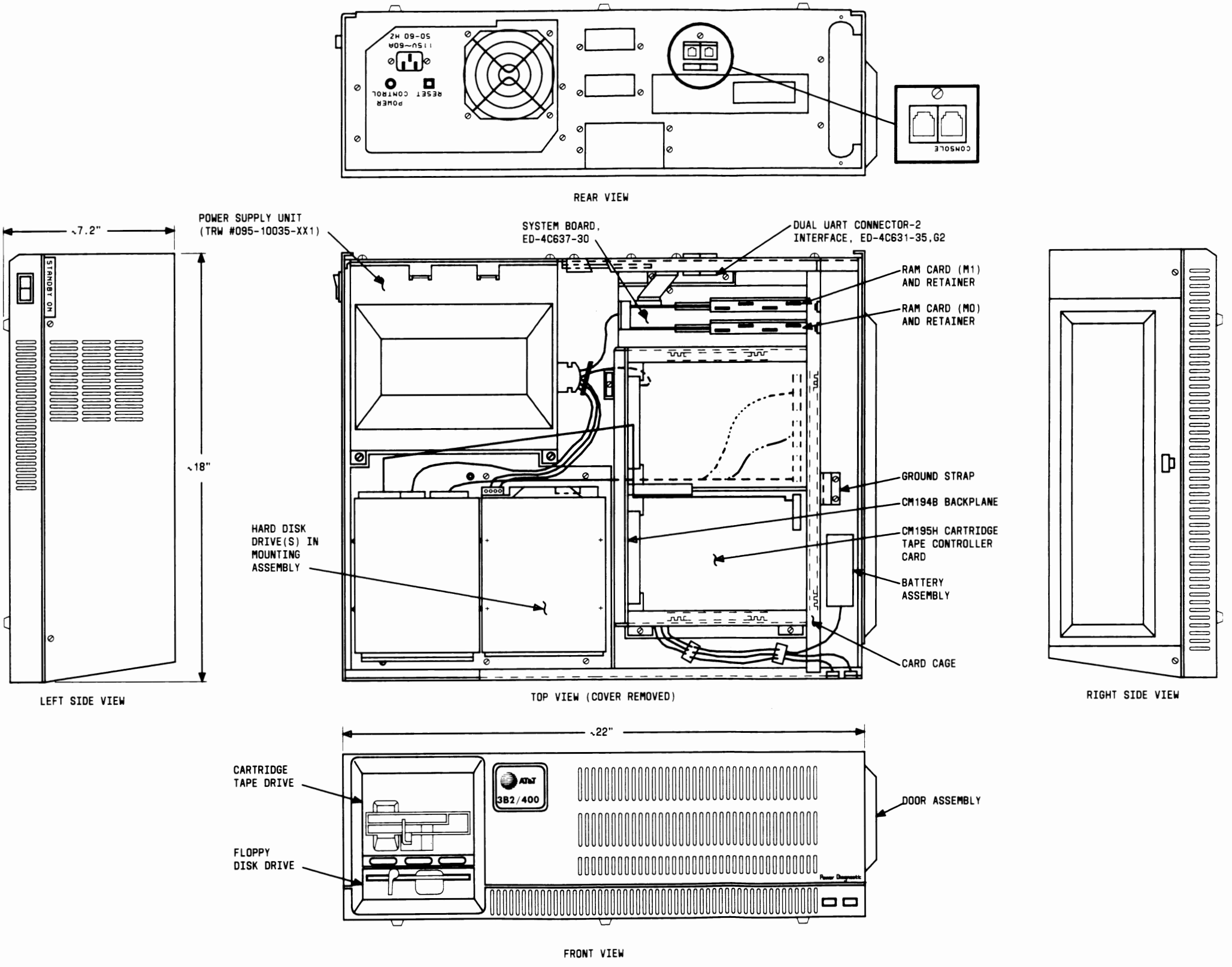


Figure 2-5: Domestic 3B2/400 Computer Cabinet Assembly Drawing (ED-4C631-30)

International 3B2/400 Computer Cabinet (ED-4C638-30)

Major Assemblies

Figure 2-6 shows a typical international 3B2/400 computer. The major assemblies include the following:

- Power Supply Unit (TRW #095-10035-XX2) set for 220 to 240 volt AC operation
- One Floppy Disk Drive, KS-23114,L4
- One or two Hard Disk Drives:
  - 30-megabyte, KS-23054,L1
  - 72-megabyte, KS-23054,L2.
- One 23-megabyte Cartridge Tape Drive, KS-23165,L1
- System Board ED-4C637-30,G2 (without MAU) or ED-4C637-30,G5 (with MAU)
- CM194B Backplane and card cage
- Memory card(s)
- DUART Connector-2 Interface, ED-4C631-35,G2
- Backup battery.

International 3B2/400 Computer Equipment Characteristics

Physical.

Height	7.2 inches
Width	22 inches
Depth	18 inches
Weight	Approximately 60 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

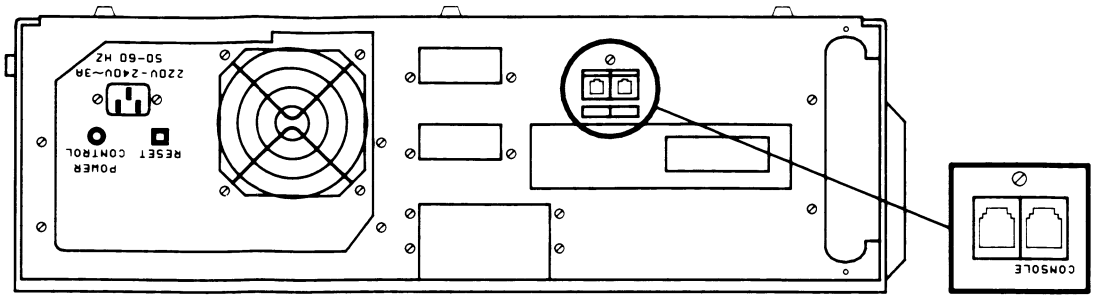
Voltage	220 to 240 V AC, 3 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 350 watts (maximum)

Environmental.

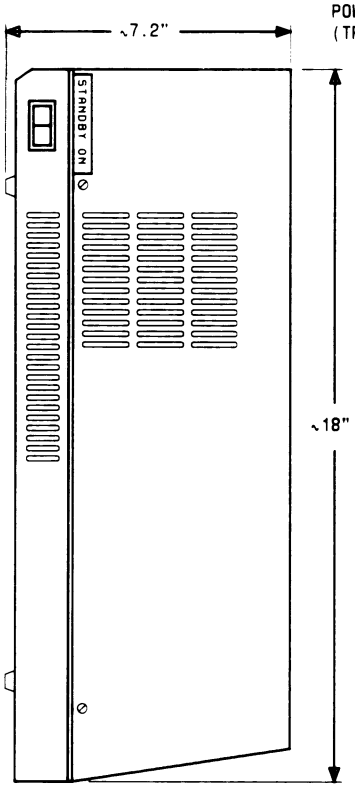
Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	1200 Btu/hour (maximum) 352 watts
Noise Level	Approximately 45 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

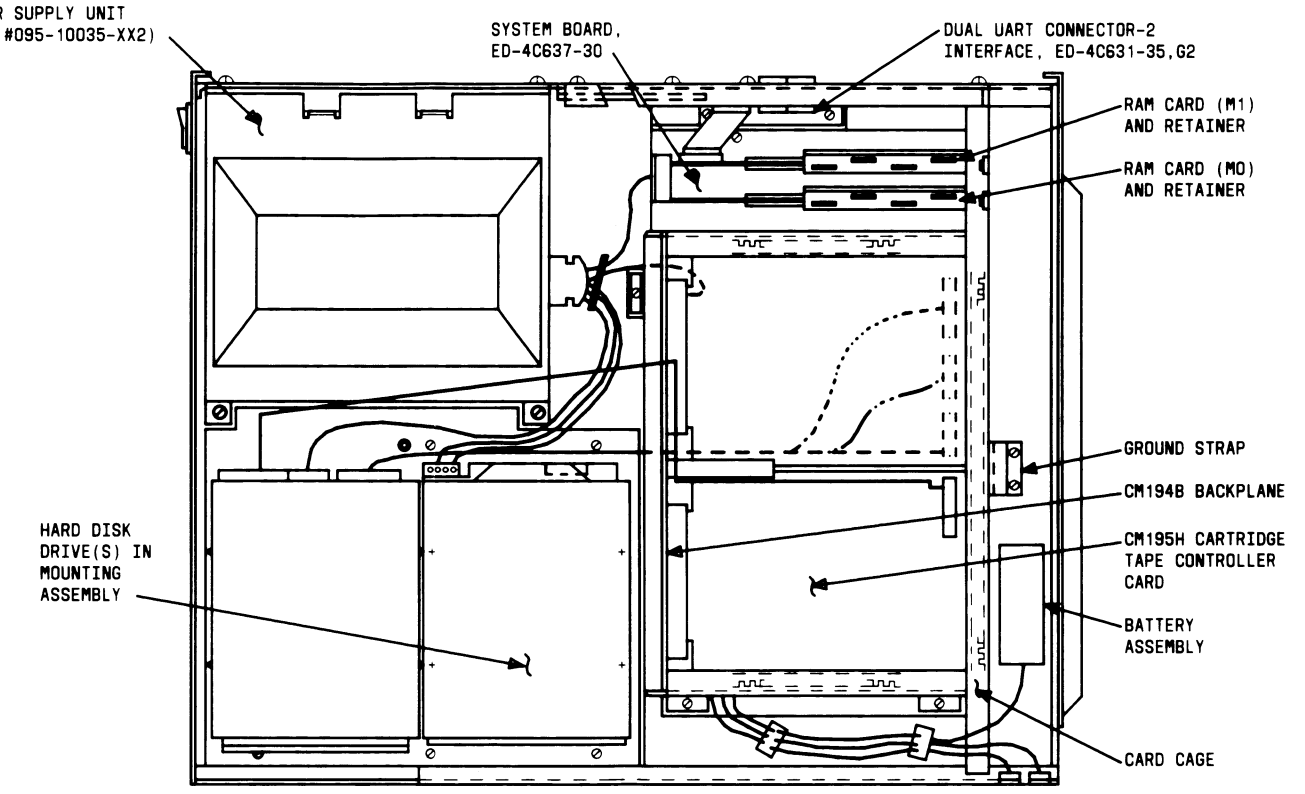
Concurrent Users	10 to 25
CPU Benchmark	1.12 Million Instructions Per Second (MIPS)



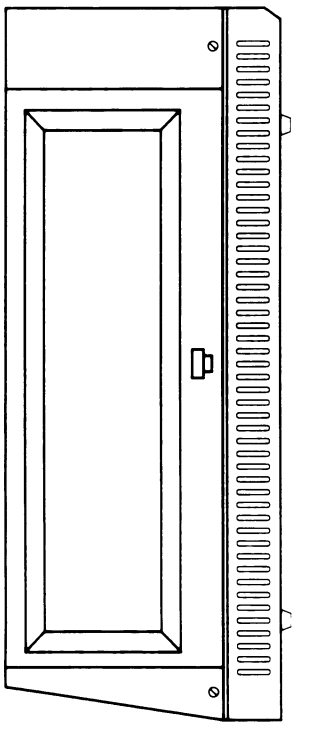
REAR VIEW



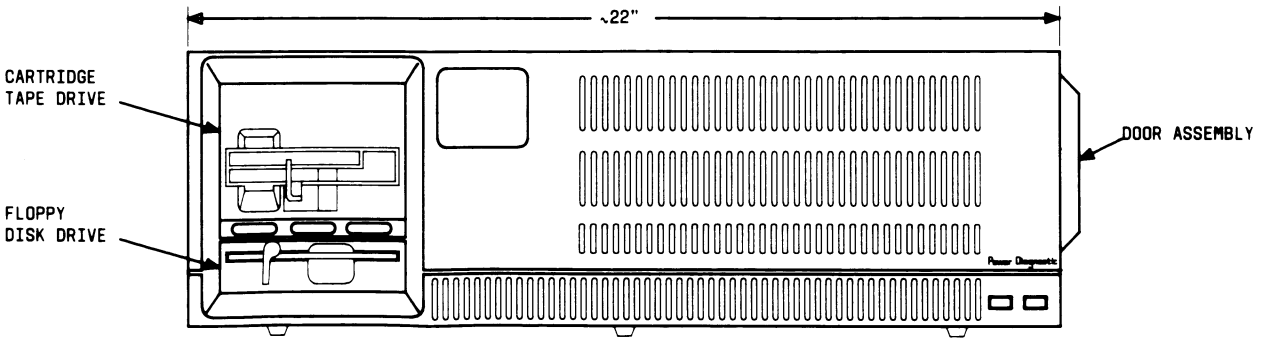
LEFT SIDE VIEW



TOP VIEW (COVER REMOVED)

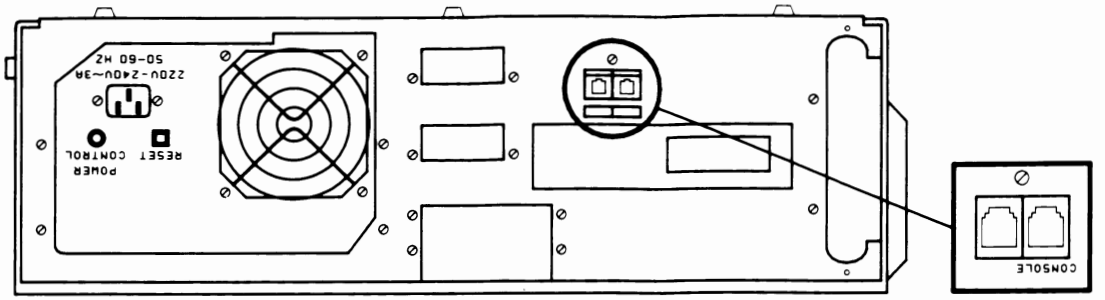


RIGHT SIDE VIEW

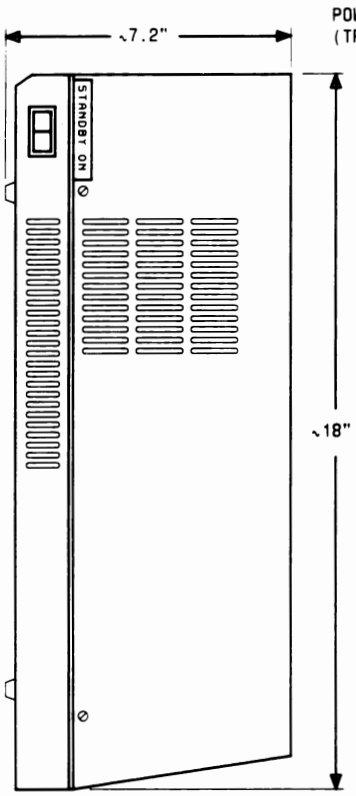


FRONT VIEW

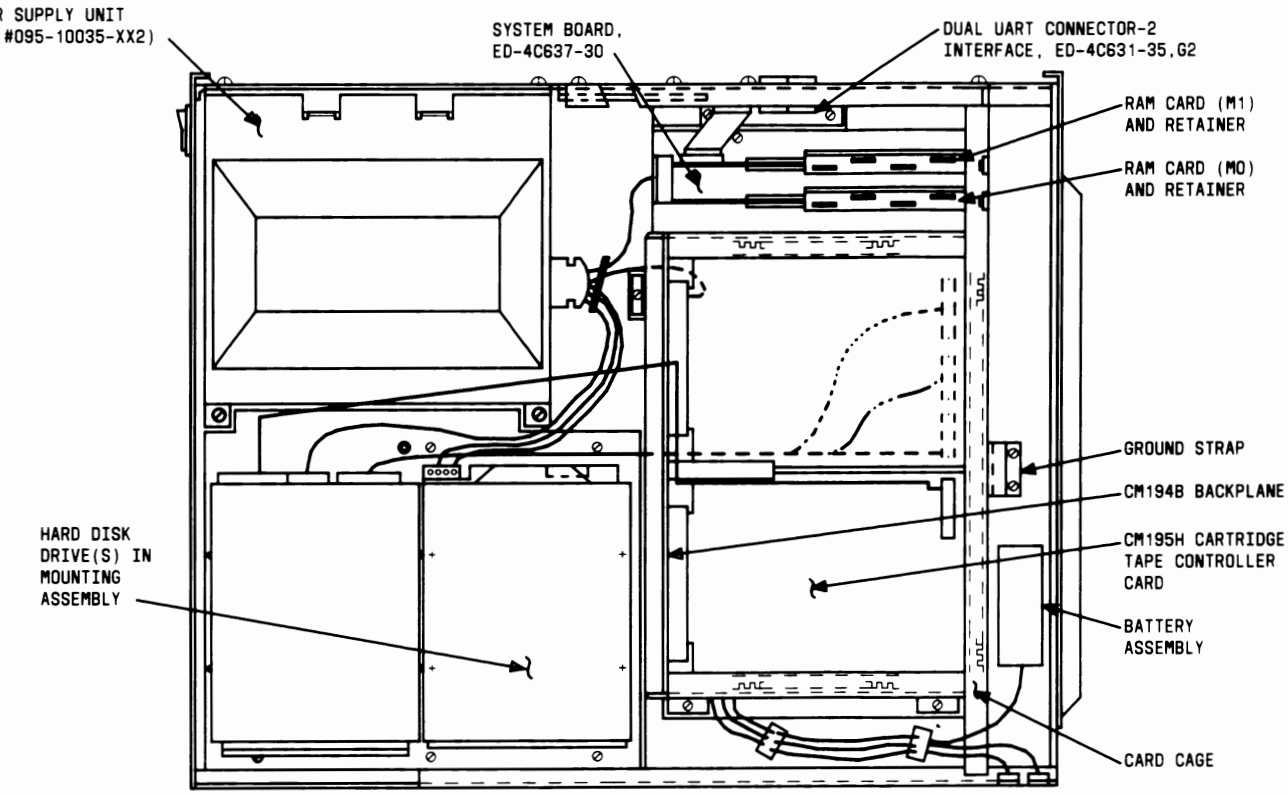
Figure 2-6: International 3B2/400 Computer Cabinet Assembly Drawing (ED-4C638-30)



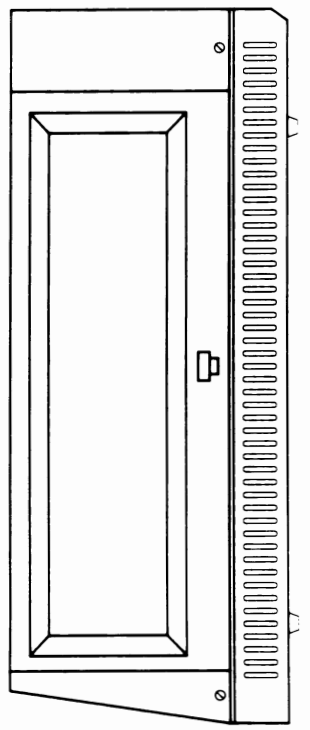
REAR VIEW



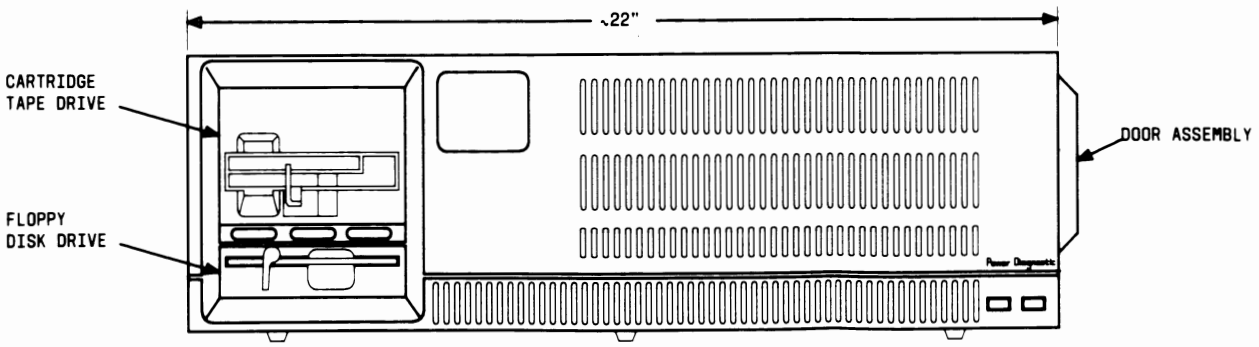
LEFT SIDE VIEW



TOP VIEW (COVER REMOVED)



RIGHT SIDE VIEW



FRONT VIEW

Figure 2-6: International 3B2/400 Computer Cabinet Assembly Drawing (ED-4C638-30)

3B2/500 Computer Cabinet (ED-3T043-30)

Major Assemblies

Figure 2-7 shows a typical 3B2/500 computer. Since the 3B2/500 computer is equipped with a "smart" power supply, there is no noticeable difference in the domestic and international versions. The major assemblies include the following:

- Power Supply Unit (ACS752A)
- One Floppy Disk Drive, KS-23114,L4
- One Hard Disk Drive:
  - 147-megabyte, KS-23371,L17
  - 155-megabyte, KS-23483,L25
  - 300-megabyte, KS-23483,L1B.
- One 60- or 120-megabyte Cartridge Tape Drive, KS-23417,L1 or KS-23465,L14
- System Board CM518A
- CM520A Backplane and card cage
- Memory card(s)
- DUART Connector-2 Interface, ED-4C631-35,G2
- Backup battery.

3B2/500 Computer Equipment Characteristics

Physical.

Height	7.6 inches
Width	22.5 inches
Depth	18 inches
Weight	Approximately 55 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

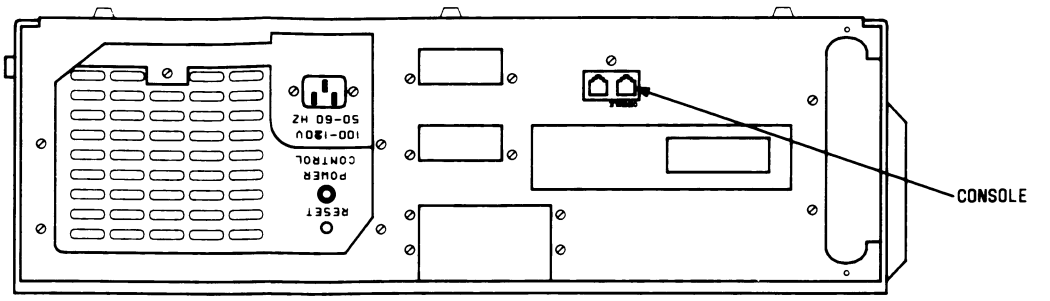
Voltage	115 V AC, 7 Amperes Domestic 220 to 240 V AC, 4 Amperes International
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 500 watts (maximum)

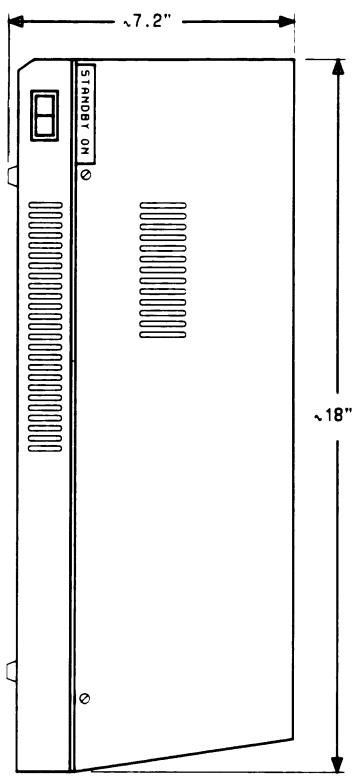
Environmental.

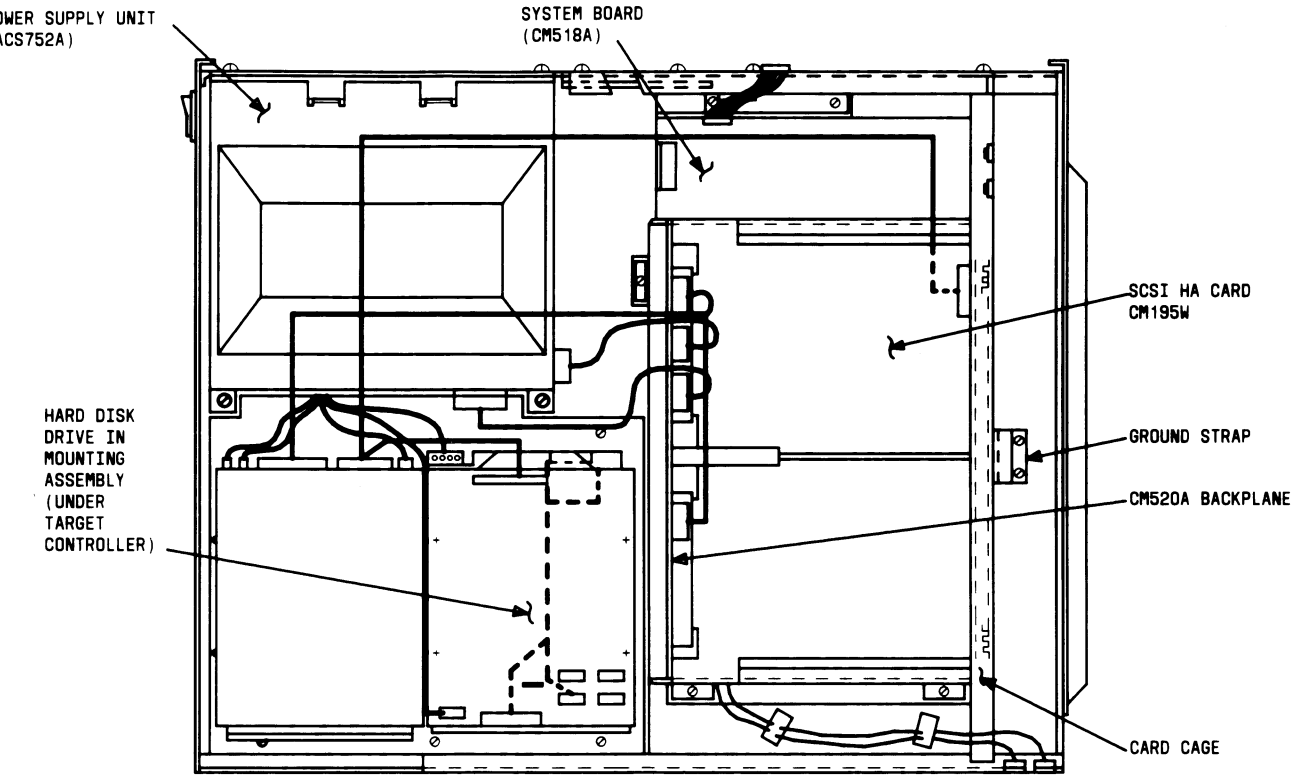
Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	1275 Btu/hour (maximum) 374 watts
Noise Level	Approximately 42 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

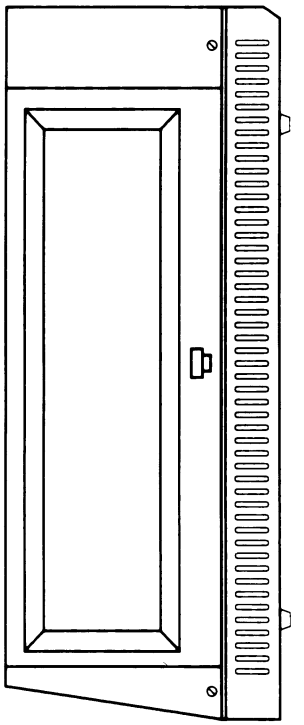
Performance.

Concurrent Users	25 to 40
CPU Benchmark	2.1 Million Instructions Per Second (MIPS)









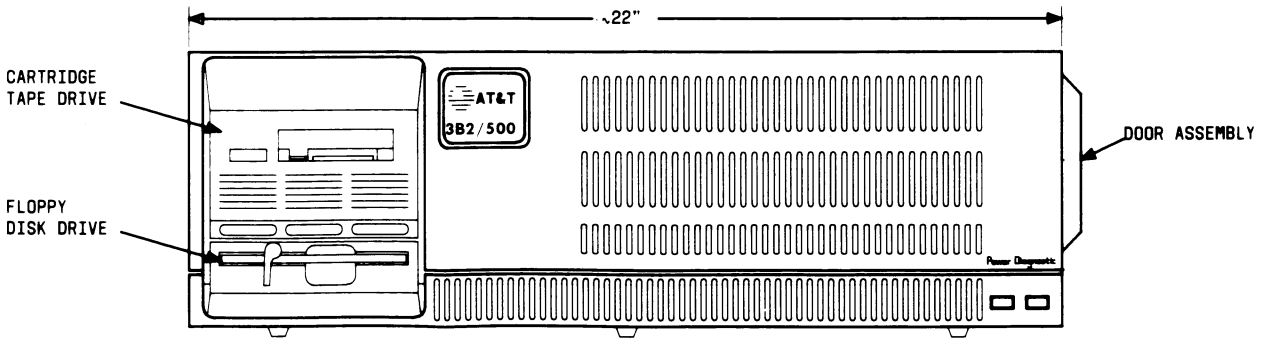
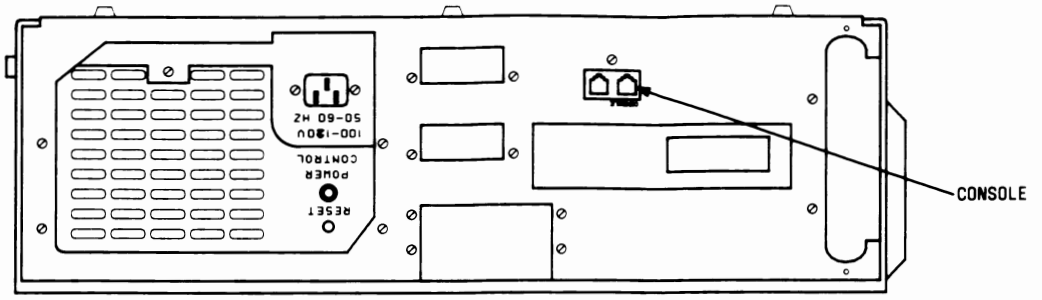
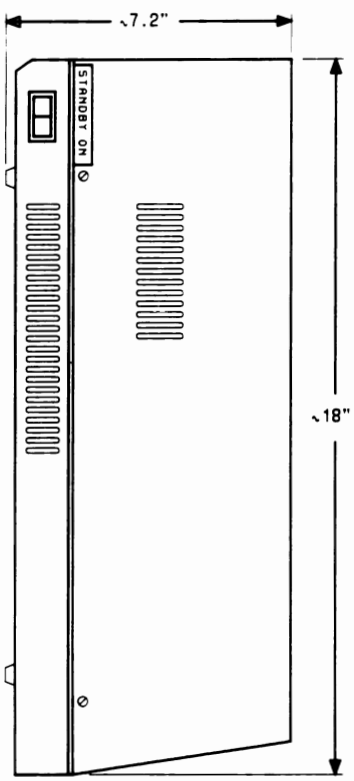


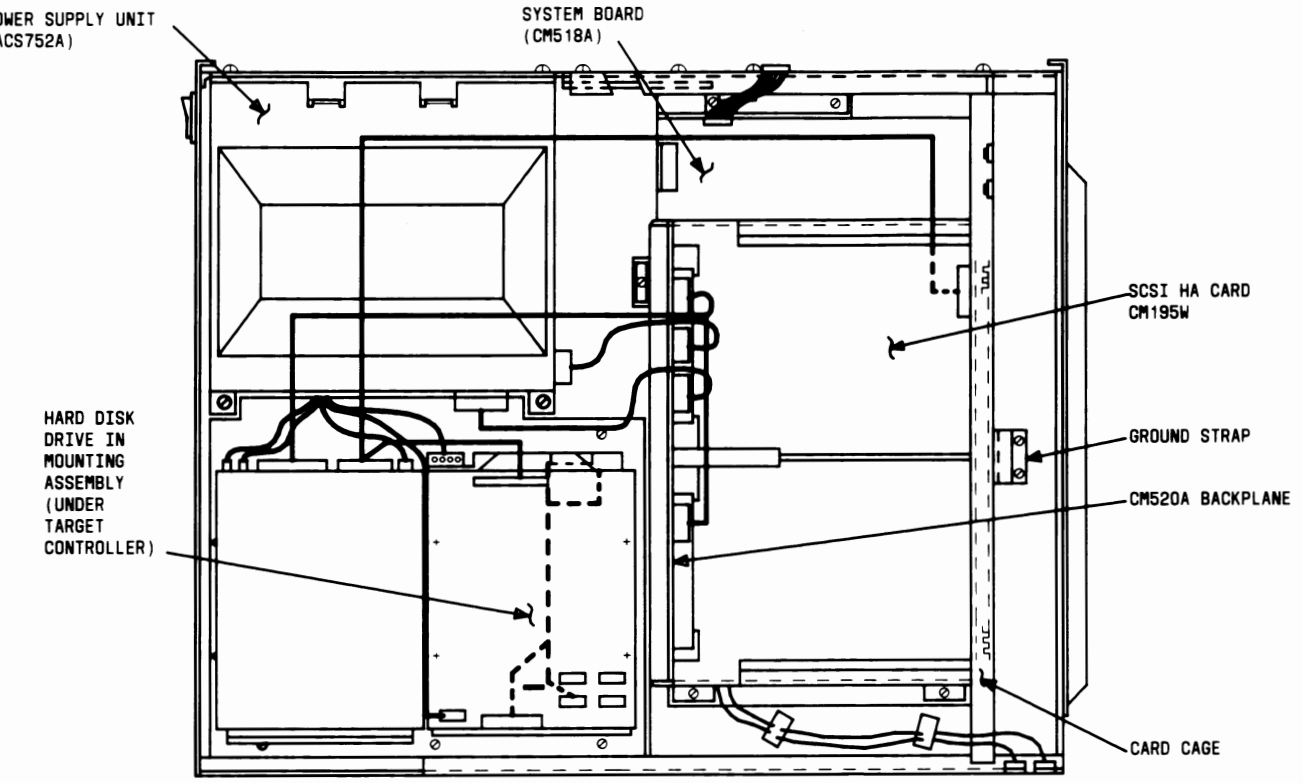
Figure 2-7: 3B2/500 Computer Cabinet Assembly Drawing (ED-3T043-30)



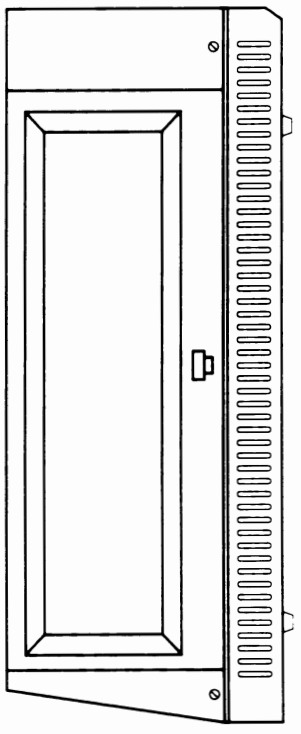
REAR VIEW



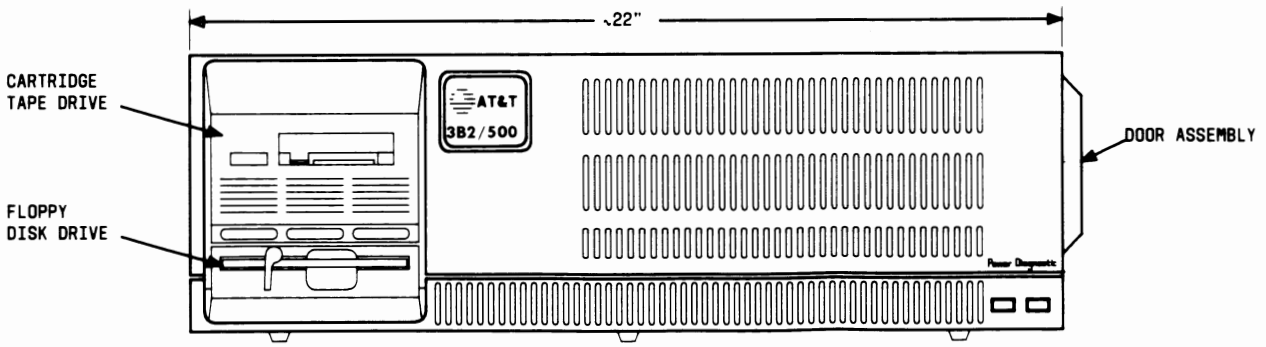
LEFT SIDE VIEW



TOP VIEW (COVER REMOVED)



RIGHT SIDE VIEW



FRONT VIEW

Figure 2-7: 3B2/500 Computer Cabinet Assembly Drawing (ED-3T043-30)

3B2/600 Computer Cabinet (ED-3T023-30)

Major Assemblies

Figure 2-8 shows a typical 3B2/600 computer. Since the 3B2/600 computer is equipped with a "smart" power supply, there is no noticeable difference in the domestic and international versions. The major assemblies include the following:

- Power Supply Unit (ACS782A-0)
- One Floppy Disk Drive, KS-23114,L4
- One or two Hard Disk Drives:
  - 147-megabyte, KS-23371,L17
  - 155-megabyte, KS-23483,L25.
- One 60-megabyte Cartridge Tape Drive, KS-23417,L1
- System Board CM518A
- CM519A Backplane and card cage
- Memory card(s)
- Backup battery.

3B2/600 Computer Equipment Characteristics

Physical.

Height	13 inches
Width	17 inches
Depth	24 inches
Weight	Approximately 82 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	115 V AC, 12 Amperes Domestic 220 to 240 V AC, 8.5 Amperes International
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 1300 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	3000 Btu/hour (maximum) 879 watts
Noise Level	Approximately 50 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	25 to 64
CPU Benchmark	2.61 Million Instructions Per Second (MIPS)

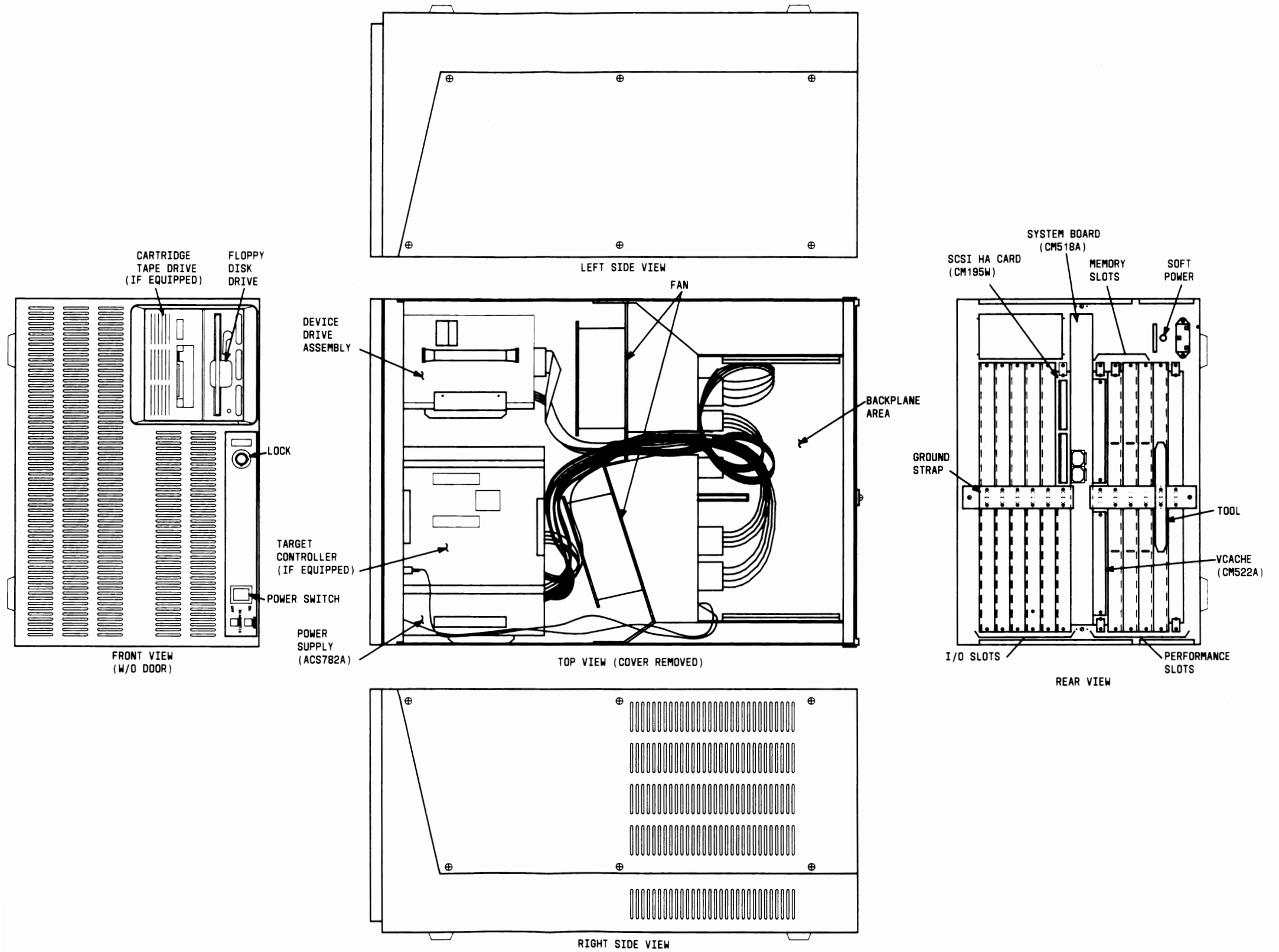


Figure 2-8: 3B2/600 Computer Cabinet Assembly Drawing (ED-3T023-30)

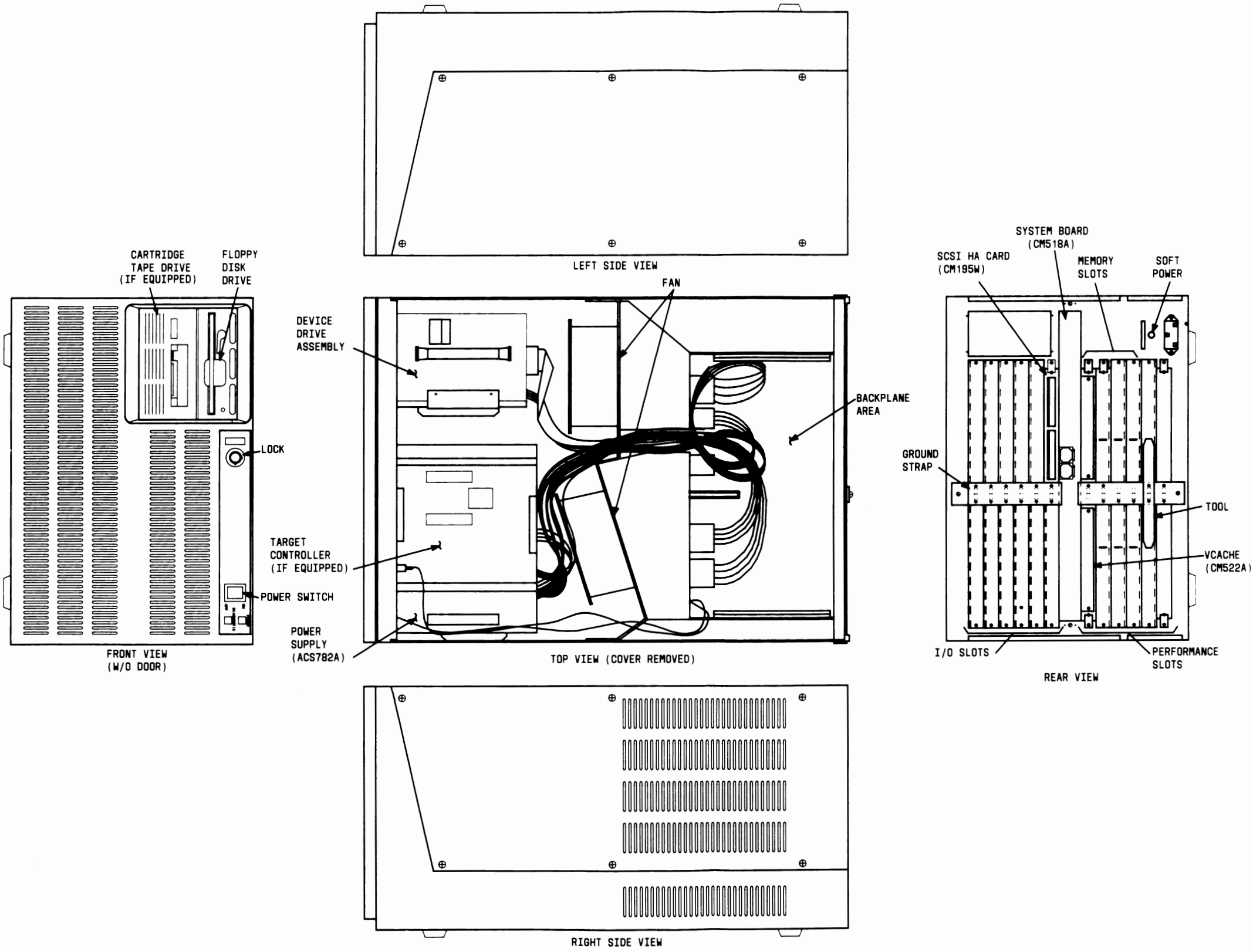


Figure 2-8: 3B2/600 Computer Cabinet Assembly Drawing (ED-3T023-30)

3B2/700 Computer Cabinet (ED-3T047-30)

Major Assemblies

Figure 2-9 shows a typical 3B2/700 computer. Since the 3B2/700 computer is equipped with a "smart" power supply, there is no noticeable difference in the domestic and international versions. The major assemblies include the following:

- Power Supply Unit (ACS782A-0)
- One Floppy Disk Drive, KS-23114,L4
- One or two Hard Disk Drives:
  - 300-megabyte, KS-23483,L1B
  - 300-megabyte with Enhanced Small Disk Interface (ESDI), KS-23371,L31.
- One 120-megabyte Cartridge Tape Drive, KS-23465,L1A
- System Board CM518B
- CM519A Backplane and card cage
- Memory card(s)
- Backup battery.

3B2/700 Computer Equipment Characteristics

Physical.

Height	13 inches
Width	17 inches
Depth	24 inches
Weight	Approximately 82 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	115 V AC, 12 Amperes Domestic 220 to 240 V AC, 8.5 Amperes International
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 1300 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	3000 Btu/hour (maximum) 879 watts
Noise Level	Approximately 50 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	64 to 80
CPU Benchmark	4.0 Million Instructions Per Second (MIPS)

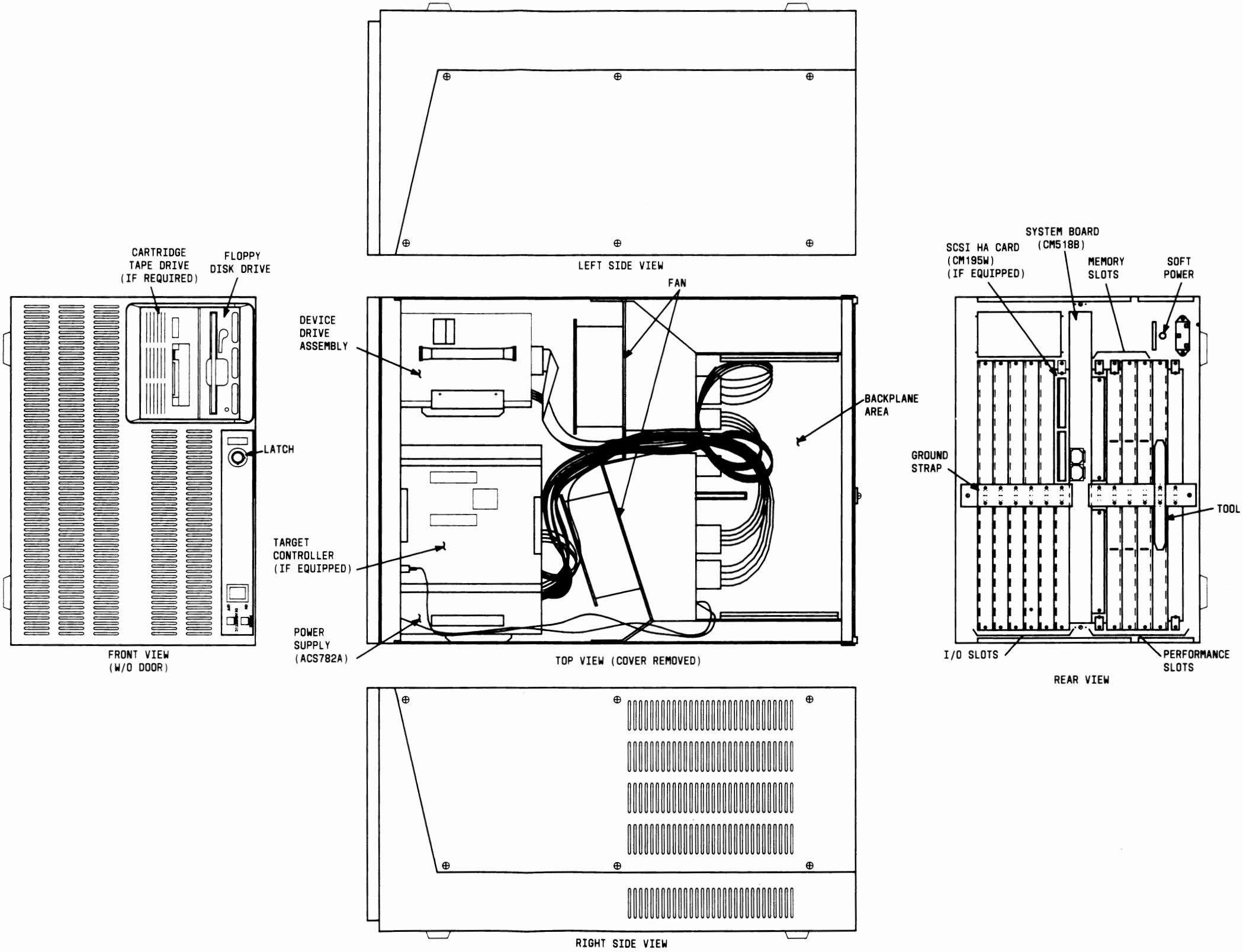


Figure 2-9: 3B2/700 Computer Cabinet Assembly Drawing (ED-3T047-30)

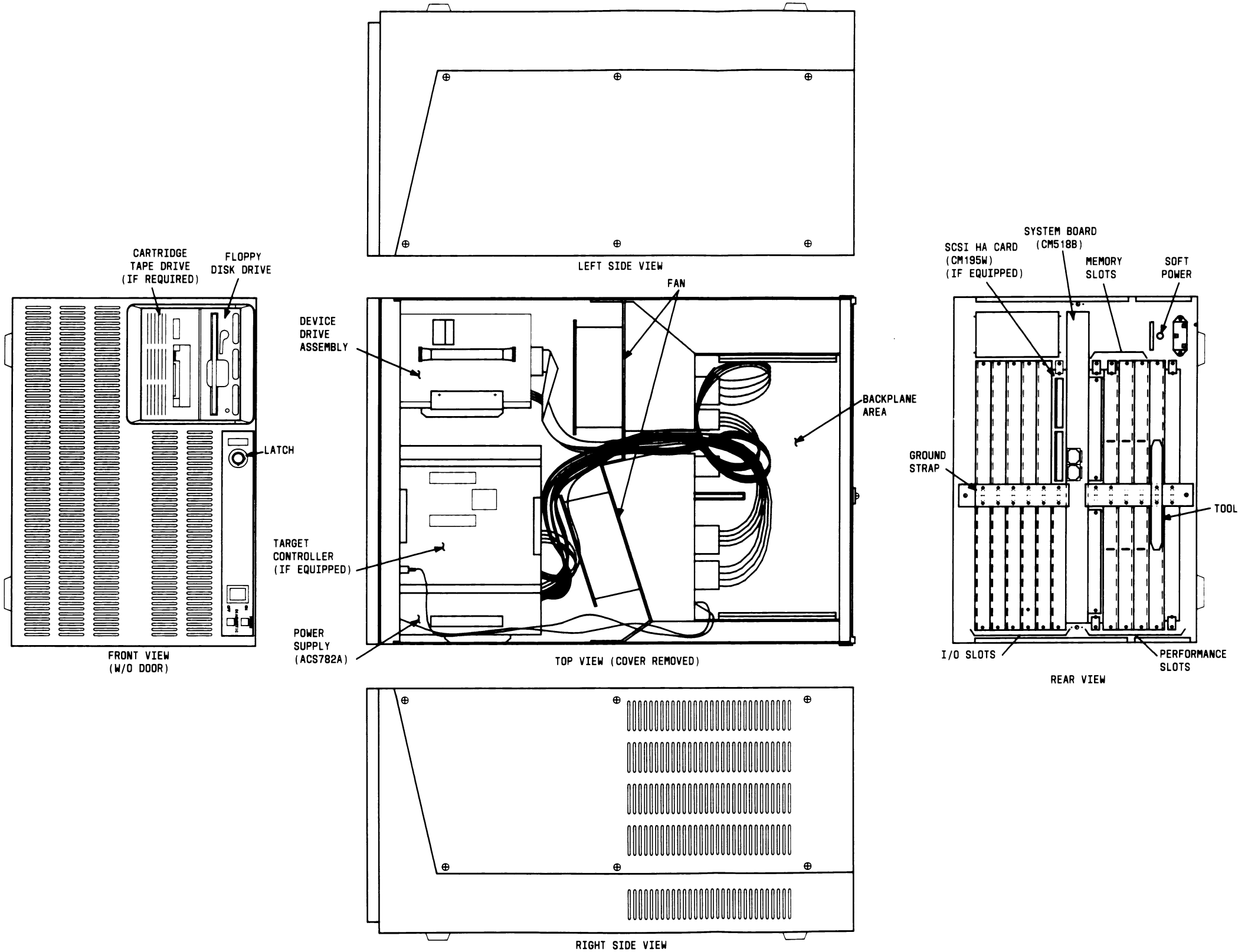


Figure 2-9: 3B2/700 Computer Cabinet Assembly Drawing (ED-3T047-30)

3B2/1000 Computer Cabinet (ED-3T056-30)

Major Assemblies

Figure 2-10 shows a typical 3B2/1000 computer. The 3B2/1000 is available in three different models: 60, 70, and 80. Each model is slightly different in its configuration.

However, each 3B2/1000 computer is equipped with a "smart" power supply so there is no noticeable difference in the domestic and international versions. The major assemblies include the following:

- Power Supply Unit (ACS782A-0)
- One Floppy Disk Drive, KS-23114,L4
- One, two, or three 300-megabyte Hard Disk Drives, KS-23483,L3
- One 120-megabyte Cartridge Tape Drive, KS-23465,L1A
- System Board CM518C
- CM519B Backplane and card cage
- Memory card(s)
- Backup battery.

3B2/1000 Computer Equipment Characteristics

Physical.

Height	13 inches
Width	17 inches
Depth	24 inches
Weight	Approximately 82 pounds
Cabinet Load	Supports external loads to 60 pounds

Electrical.

Voltage	115 V AC, 12 Amperes Domestic 220 to 240 V AC, 8.5 Amperes International
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 1300 watts (maximum)

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	3000 Btu/hour (maximum) 879 watts
Noise Level	Approximately 50 dB(A) Sound Pressure Level (ANSI S12.10—Bystander Position)

Performance.

Concurrent Users	64 to 80
CPU Benchmark	4.1 Million Instructions Per Second (MIPS)

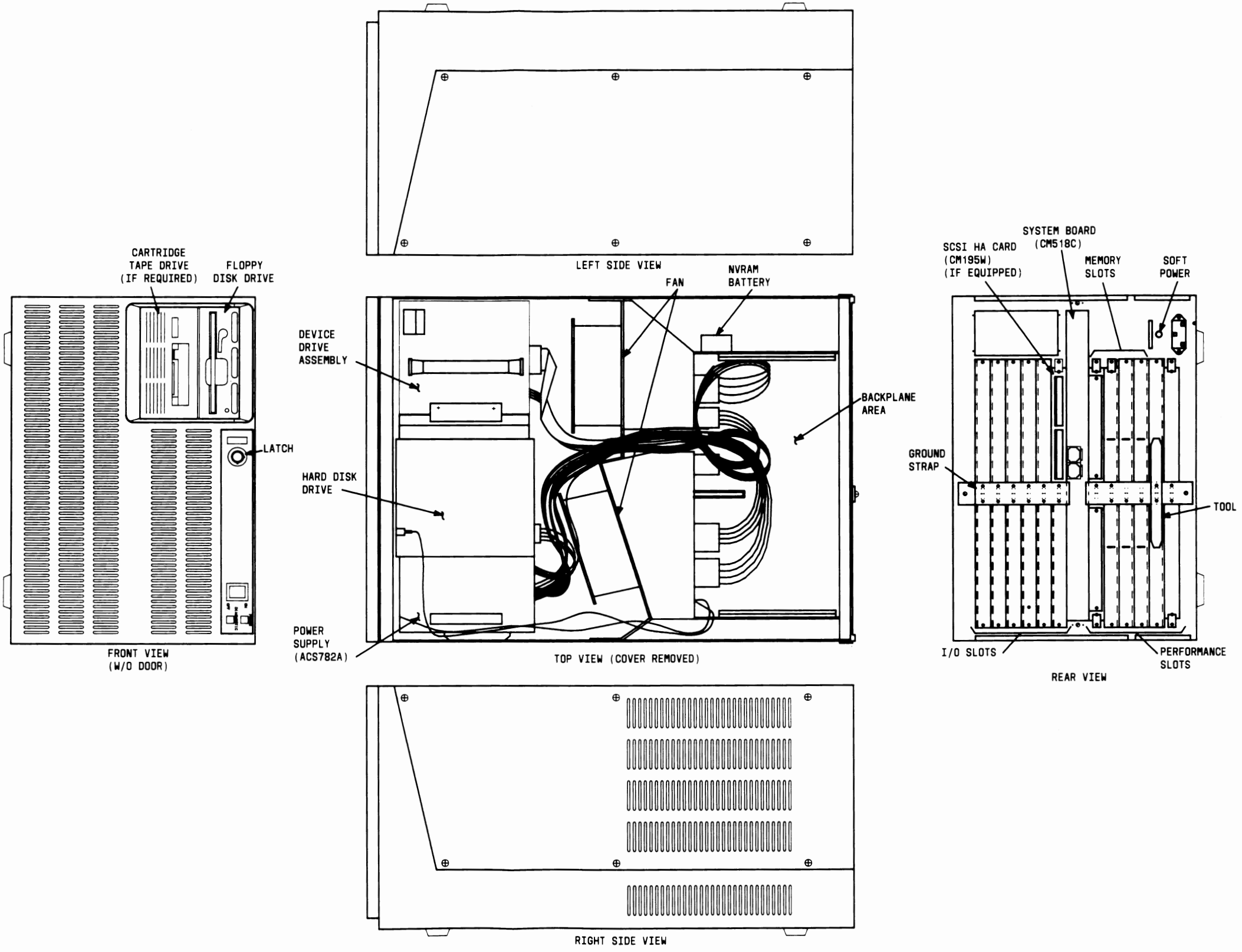


Figure 2-10: 3B2/1000 Computer Cabinet Assembly Drawing (ED-3T056-30)

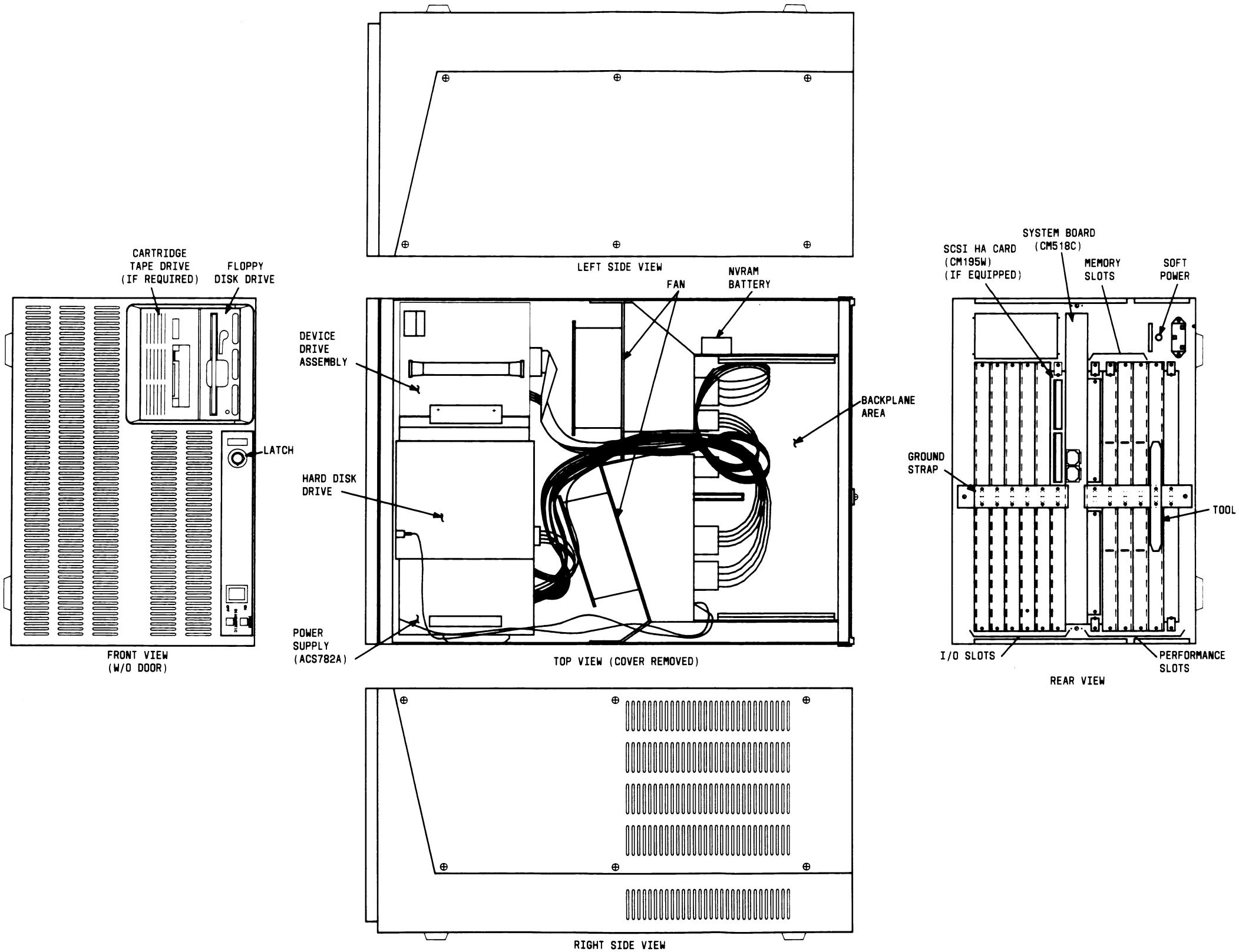


Figure 2-10: 3B2/1000 Computer Cabinet Assembly Drawing (ED-3T056-30)

Domestic AT&T/XM (ED-4C580-30)

Major Assemblies

Figure 2-11 shows a typical domestic AT&T/XM. The major assemblies include a power supply and various combinations of floppy disk drives, cartridge tape drives, and hard disk drives. A maximum of three hard disk drives can be housed in the cabinet. The major assemblies are listed below:

- Power Supply Unit (TRW #095-10040-XX1) set for 115 volt AC operation
- Devices (drives):
  - Floppy Disk Drive, KS-23114,L4
  - 30-megabyte Hard Disk Drive, KS-23054,L1
  - 72-megabyte Hard Disk Drive, KS-23054,L2
  - 23-megabyte Cartridge Tape Drive, KS-23165,L1
  - 60-megabyte Cartridge Tape Drive, KS-23417,L2.

Domestic AT&T/XM Equipment Characteristics

Physical.

Height	4.6 inches
Width	22 inches
Depth	17 inches

Electrical.

Voltage	115 V AC, 5 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 298 watts

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	1000 Btu/hour (maximum)
Noise Level	45 dB(A) (steady state), 55 dB(A) (maximum)

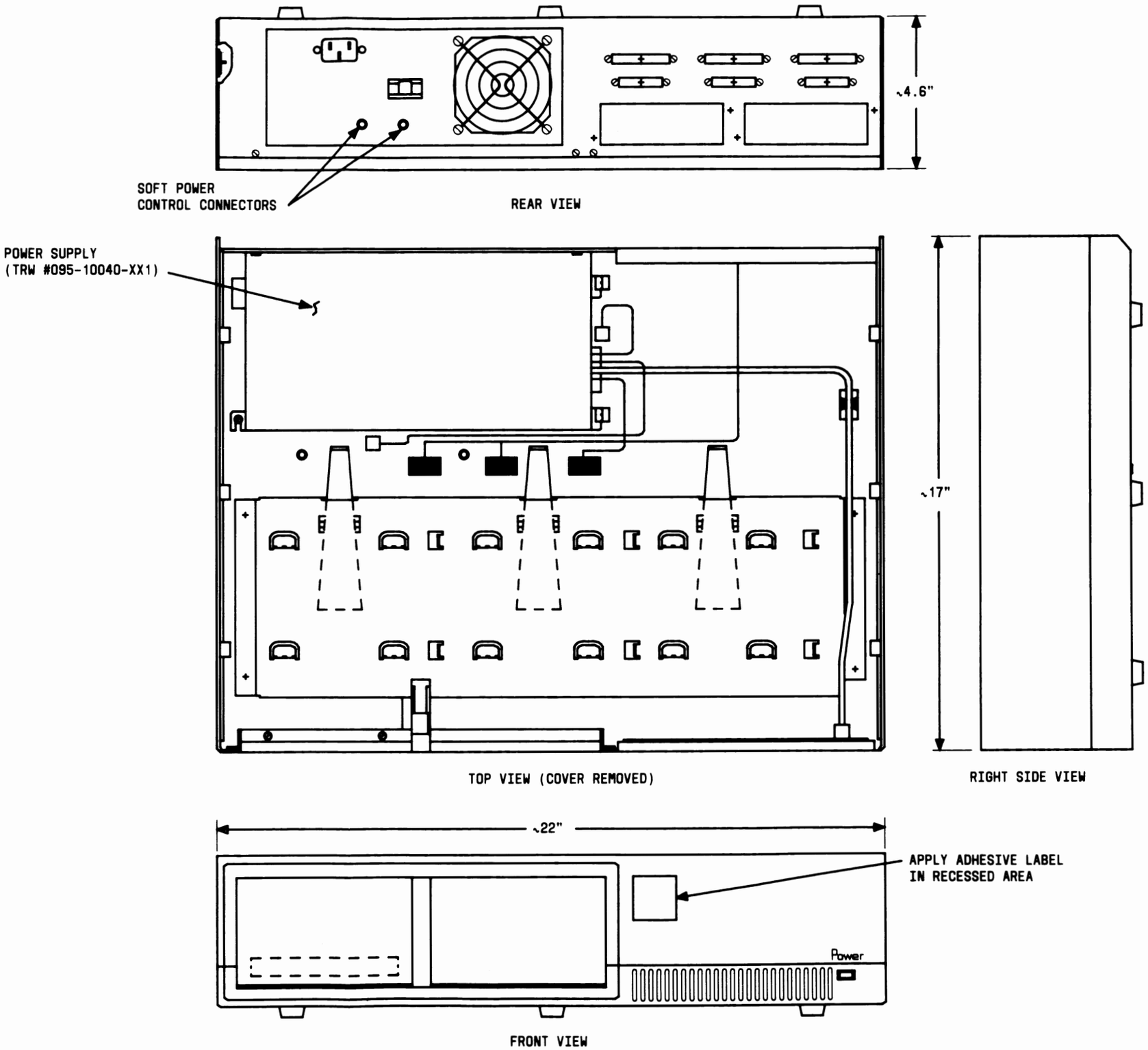


Figure 2-11: Domestic AT&T/XM Cabinet Assembly Drawing (ED-4C580-30)

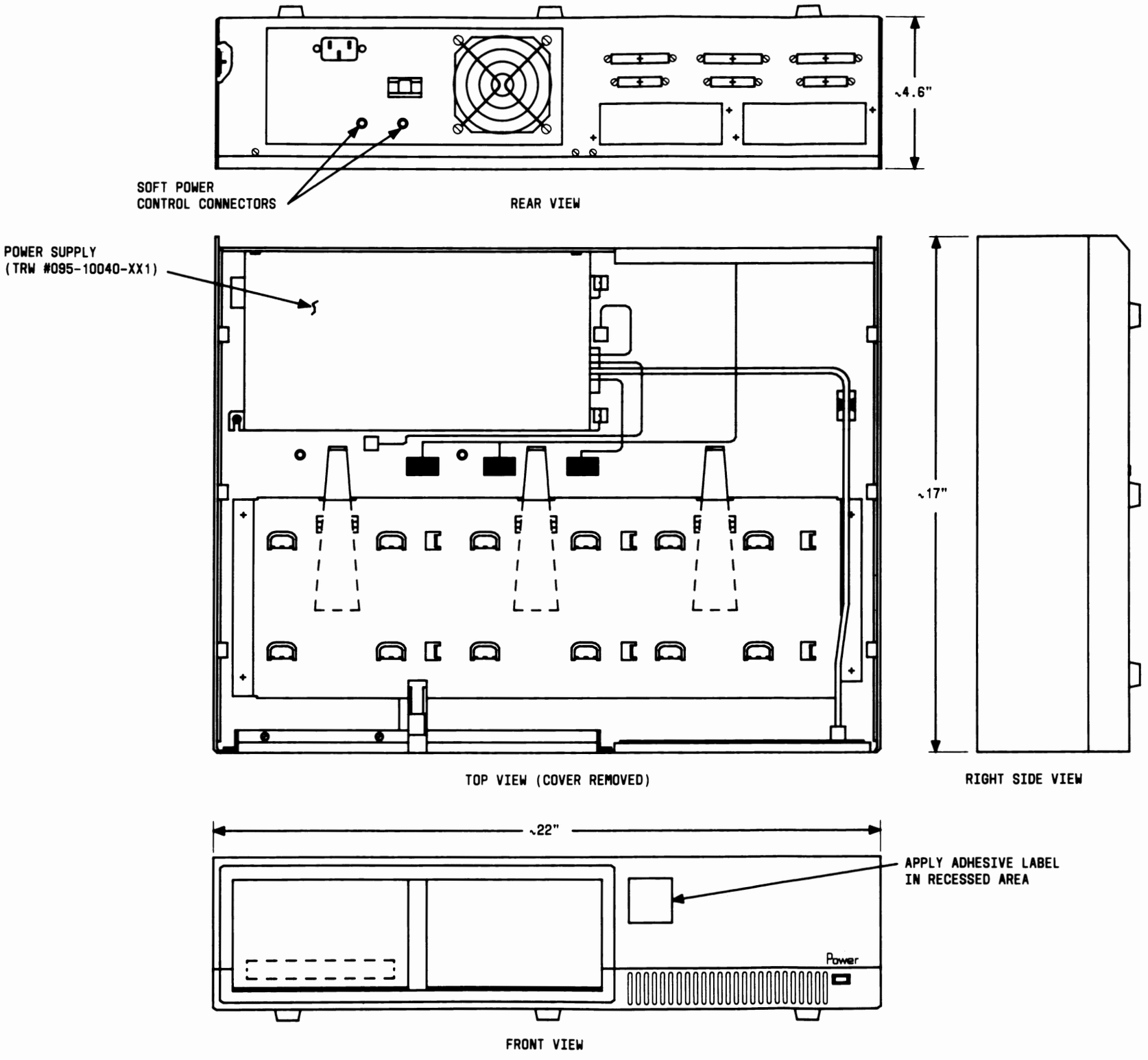


Figure 2-11: Domestic AT&T/XM Cabinet Assembly Drawing (ED-4C580-30)

International AT&T/XM (ED-4C635-30)

Major Assemblies

Figure 2-12 shows a typical international AT&T/XM. The major assemblies include a power supply and various combinations of floppy disk drives, cartridge tape drives, or hard disk drives. A maximum of three hard disk drives can be housed in the cabinet. The major assemblies are listed below:

- Power Supply Unit (TRW #095-10040-XX2 or equivalent) set for 220 volt AC operation
- Devices (drives):
  - Floppy Disk Drive, KS-23114,L4
  - 30-megabyte Hard Disk Drive, KS-23054,L1
  - 72-megabyte Hard Disk Drive, KS-23054,L2
  - 23-megabyte Cartridge Tape Drive, KS-23165,L1
  - 60-megabyte Cartridge Tape Drive, KS-23417,L2.

International AT&T/XM Equipment Characteristics

Physical.

Height	4.6 inches
Width	22 inches
Depth	17 inches

Electrical.

Voltage	220 to 240 V AC, 2.5 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 298 watts

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	1000 Btu/hour (maximum)
Noise Level	45 dB(A) (steady state), 55 dB(A) (maximum)

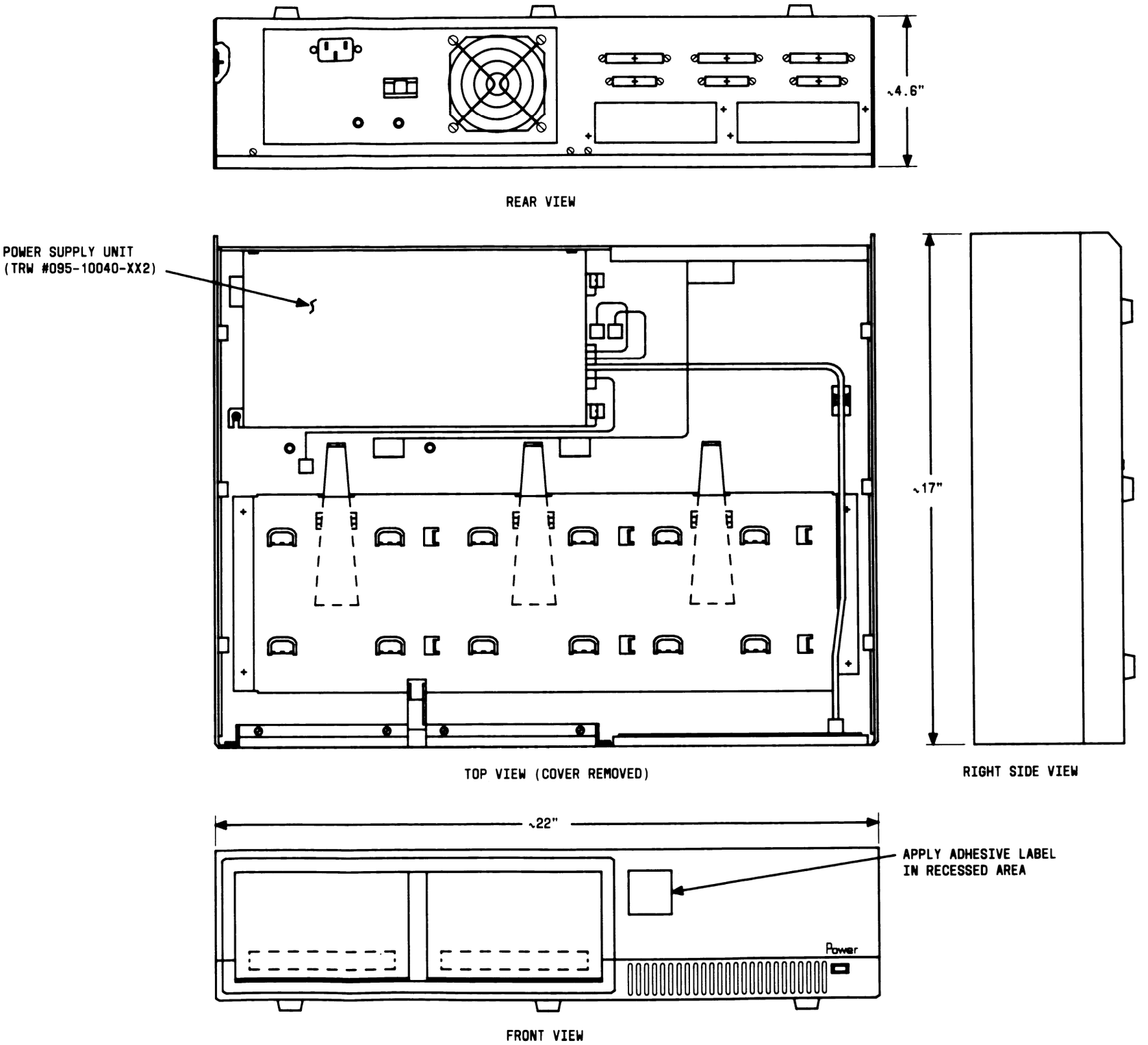


Figure 2-12: International AT&T/XM Cabinet Assembly Drawing (ED-4C635-30)

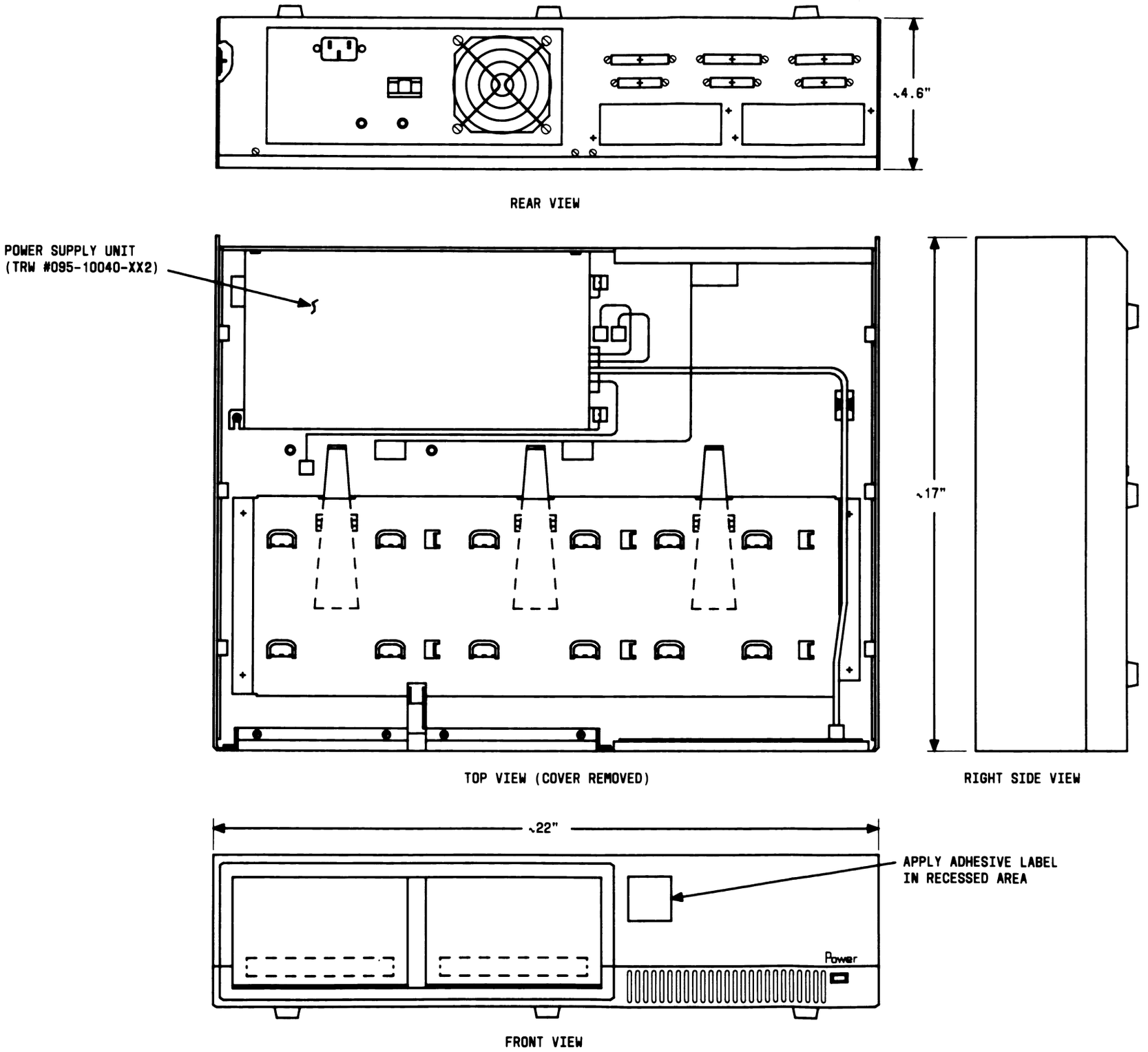


Figure 2-12: International AT&T/XM Cabinet Assembly Drawing (ED-4C635-30)

Domestic AT&T XM/405S/900S (ED-3T010-30)

Major Assemblies

Figure 2-13 shows a typical domestic AT&T XM/405S/900S. The major assemblies include a power supply, a bridge controller, and three hard disk drives. The major assemblies are listed below:

- Power Supply Unit (TRW #095-10064-02) set for 115 volt AC operation
- Bridge Controller (WP91205,L3)
- Three 135-megabyte (total of 405 megabytes) Hard Disk Drives, KS-23371,L13
  or
  Three 300-megabyte (total of 900 megabytes) ESDI Hard Disk Drives, KS-23371,L31 and L33.

Domestic AT&T XM/405S/900S Equipment Characteristics

Physical.

Height	4.6 inches
Width	22 inches
Depth	17 inches

Electrical.

Voltage	115 V AC, 5 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 298 watts

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	1000 Btu/hour (maximum)
Noise Level	45 dB(A) (steady state), 55 dB(A) (maximum)

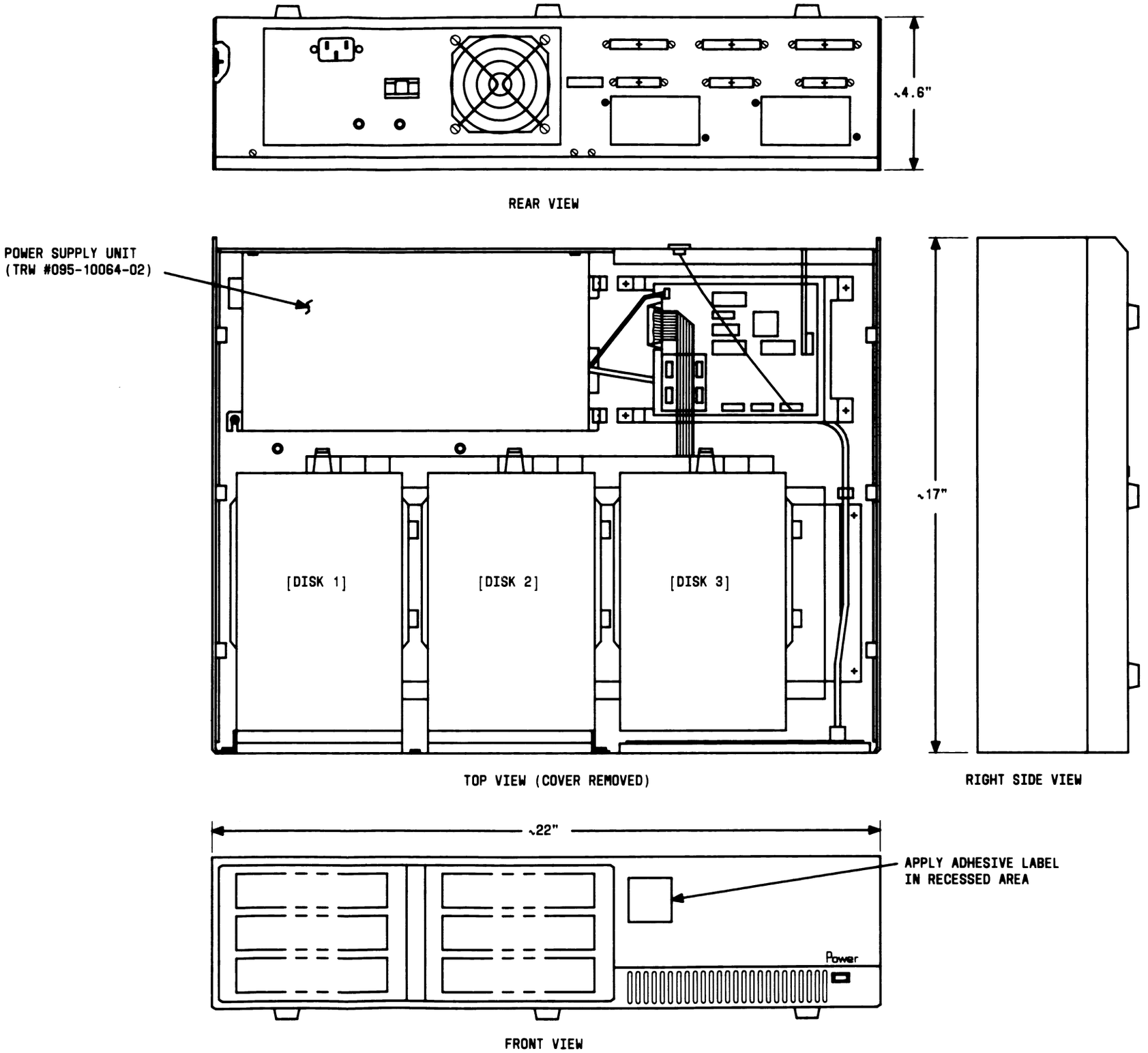


Figure 2-13: Domestic AT&T XM/405S/900S Cabinet Assembly Drawing (ED-3T010-30)

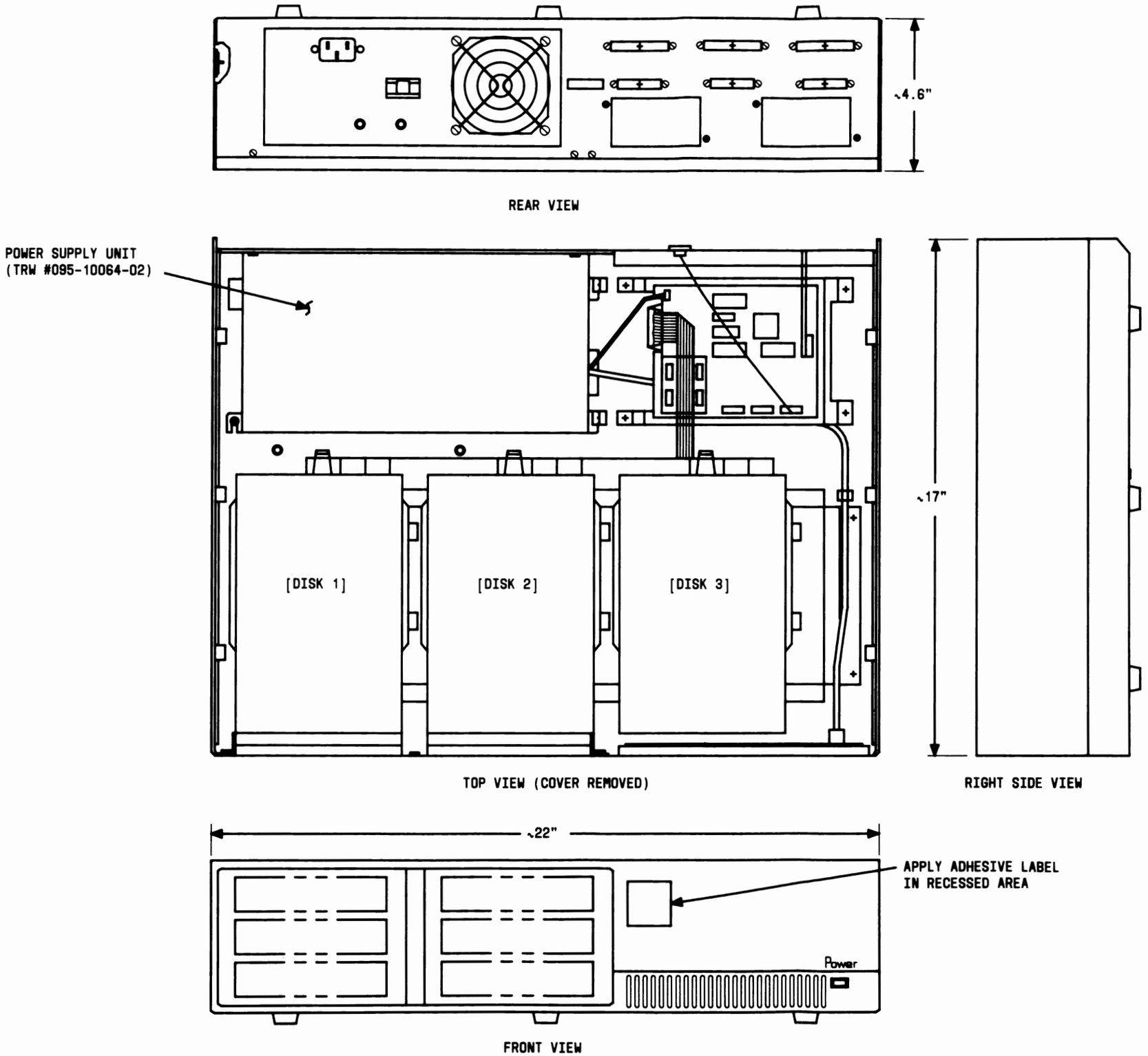


Figure 2-13: Domestic AT&T XM/405S/900S Cabinet Assembly Drawing (ED-3T010-30)

International AT&T XM/405S/900S (ED-3T027-30)

Major Assemblies

Figure 2-14 shows a typical international AT&T XM/405S/900S. The major assemblies include a power supply, a bridge controller, and three hard disk drives. The major assemblies are listed below:

- Power Supply Unit (TRW #095-10073 or equivalent) set for 220 volt AC operation
- Bridge Controller (WP91205,L3)
- Three 135-megabyte (total of 405 megabytes) Hard Disk Drives, KS-23371,L13
  or
  Three 300-megabyte (total of 900 megabytes) ESDI Hard Disk Drives, KS-23371,L31 or L33.

International AT&T XM/405S/900S Equipment Characteristics

Physical.

Height	4.6 inches
Width	22 inches
Depth	17 inches

Electrical.

Voltage	220 to 240 V AC, 2.5 Amperes
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	Less than 298 watts

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing
System Power Consumption	1000 Btu/hour (maximum)
Noise Level	45 dB(A) (steady state), 55 dB(A) (maximum)

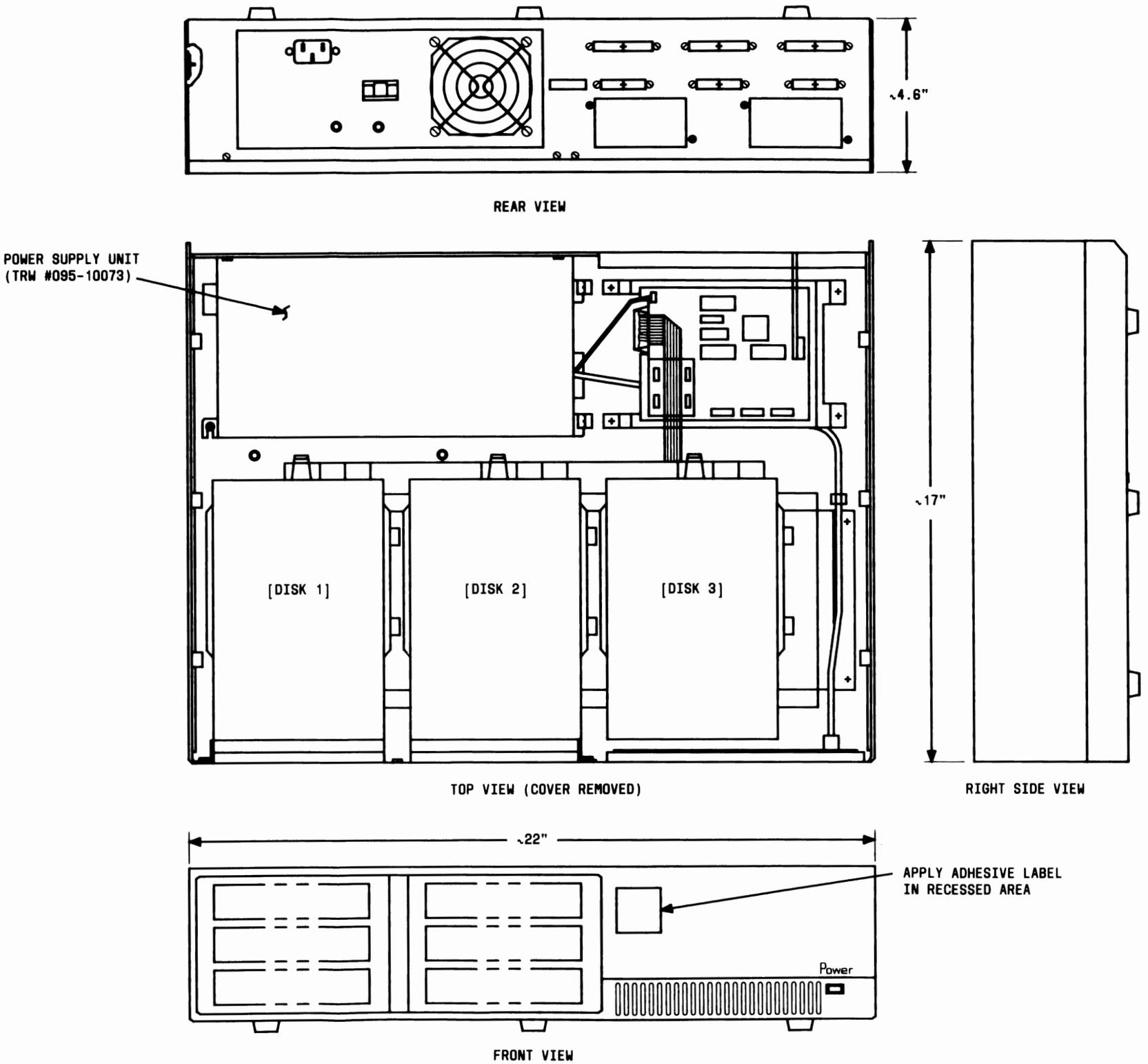


Figure 2-14: International AT&T XM/405S/900S Cabinet Assembly Drawing (ED-3T027-30)

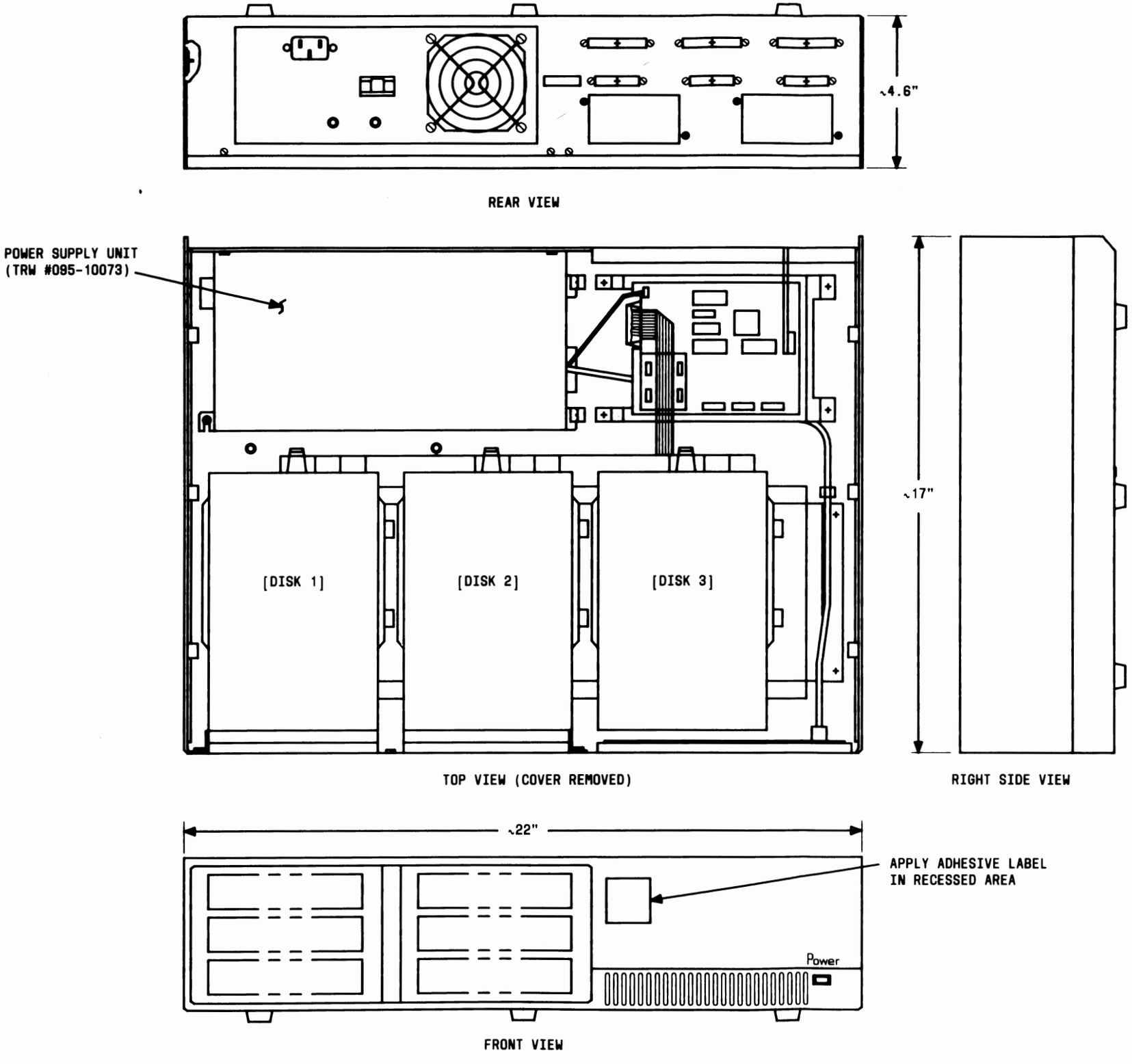


Figure 2-14: International AT&T XM/405S/900S Cabinet Assembly Drawing (ED-3T027-30)

AT&T Disk Controller Module/4E (ED-3T011-30,G1)

Major Assemblies

Figure 2-15 shows an AT&T Disk Controller Module (DCM/4E). The DCM/4E cabinet contains an ESDI bridge controller and power supply. The DCM/4E acts as one tap on the SCSI single-ended bus and can control up to four Disk Modules (DMs). The DCM/4E bridges the single-ended SCSI bus of the Host Adapter to the ESDI of the disk drives. The major assemblies are listed below:

- Power Supply (TRW #095-10065)
- Target Bridge Controller (WP91205,L3).

AT&T DCM/4E Equipment Characteristics

Physical.

Height	4 inches
Width	11 inches
Depth	12.5 inches

Electrical.

Voltage	120 V AC, 1.5 Amperes Domestic 240 V AC, 0.75 Amperes International
Frequency	50/60 Hz

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing

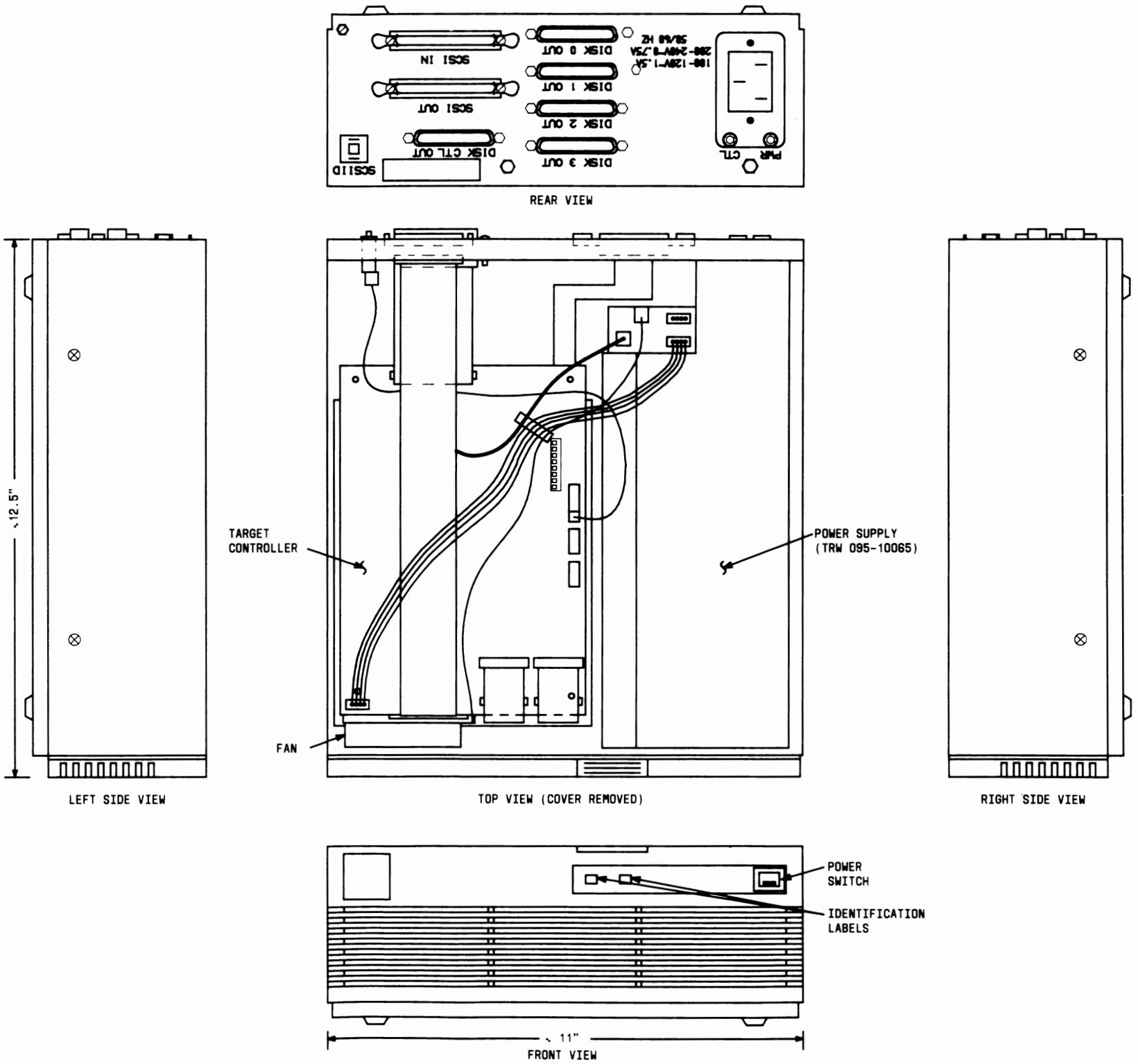


Figure 2-15: AT&T DCM/4E Cabinet Assembly Drawing (ED-3T011-30,G1)

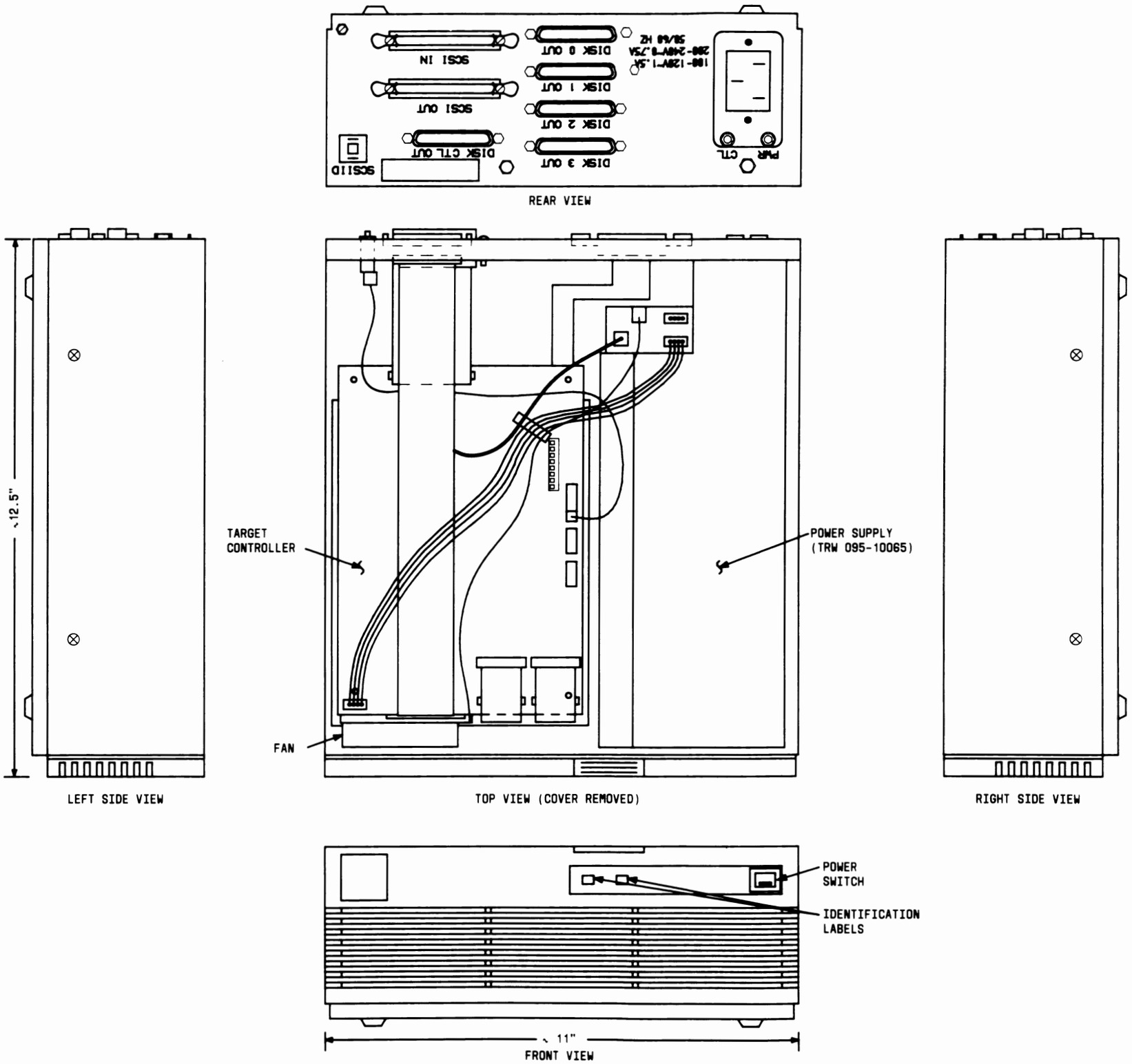


Figure 2-15: AT&T DCM/4E Cabinet Assembly Drawing (ED-3T011-30,G1)

AT&T Disk Module (ED-3T011-30,G2, G3, G5, G6)

Major Assemblies

Figure 2-16 shows an AT&T Disk Module (DM). The DM cabinet contains a single ESDI hard disk drive and power supply. The disk drive can be one of several formatted capacities. The major assemblies are listed below:

- Power Supply (TRW #095-10065)
- Disk Drive:
  - 94-megabyte, KS-23371,L7
  - 147-megabyte, KS-23371,L17
  - 300-megabyte, KS-23371,L31.

AT&T DM Equipment Characteristics

Physical.

Height	4 inches
Width	11 inches
Depth	12.5 inches

Electrical.

Voltage	120 V AC, 1.5 Amperes Domestic 240 V AC, 0.75 Amperes International
Frequency	50/60 Hz

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing

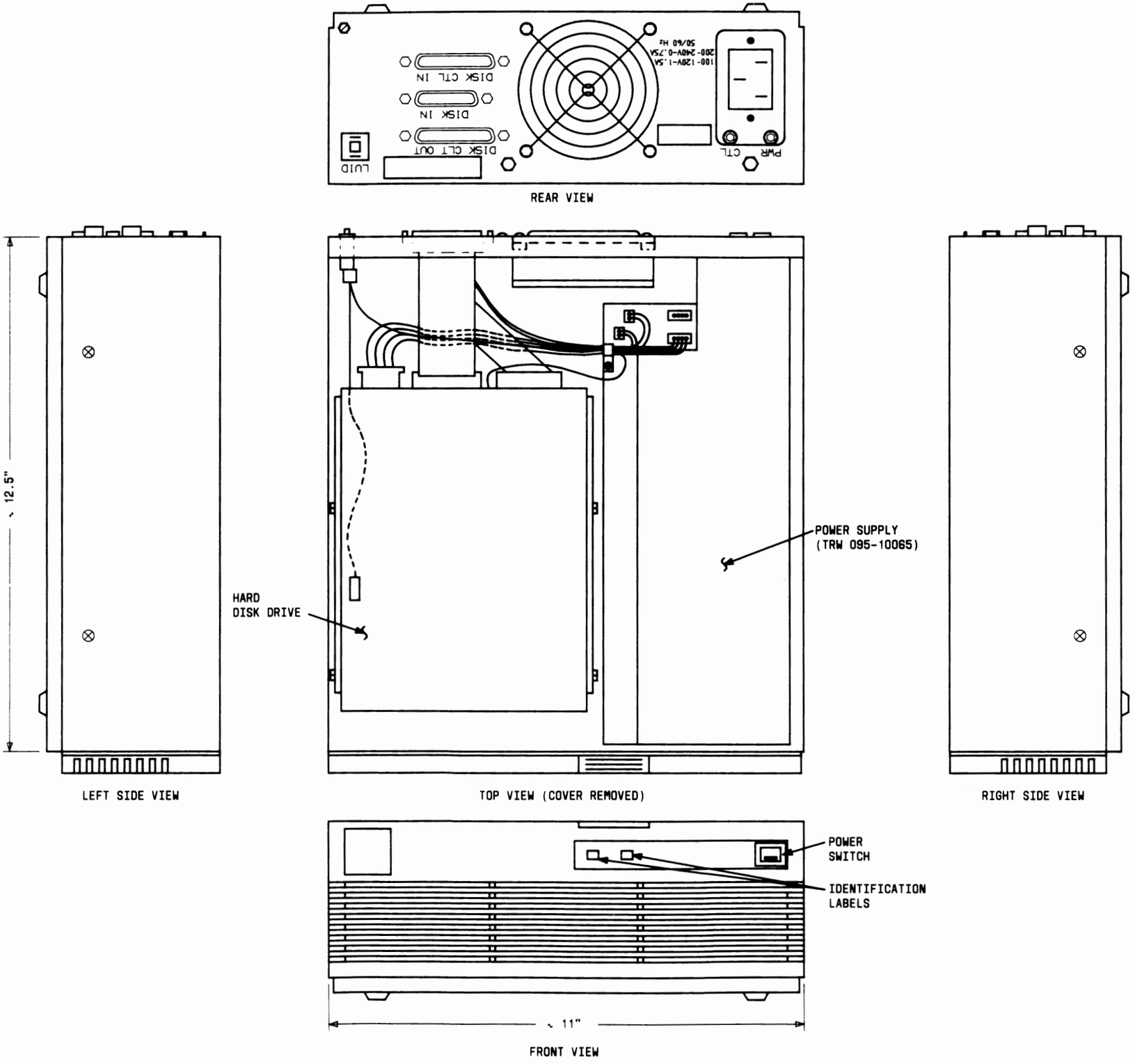


Figure 2-16: AT&T DM Cabinet Assembly Drawing (ED-3T011-30, G2, G3, G5, G6)

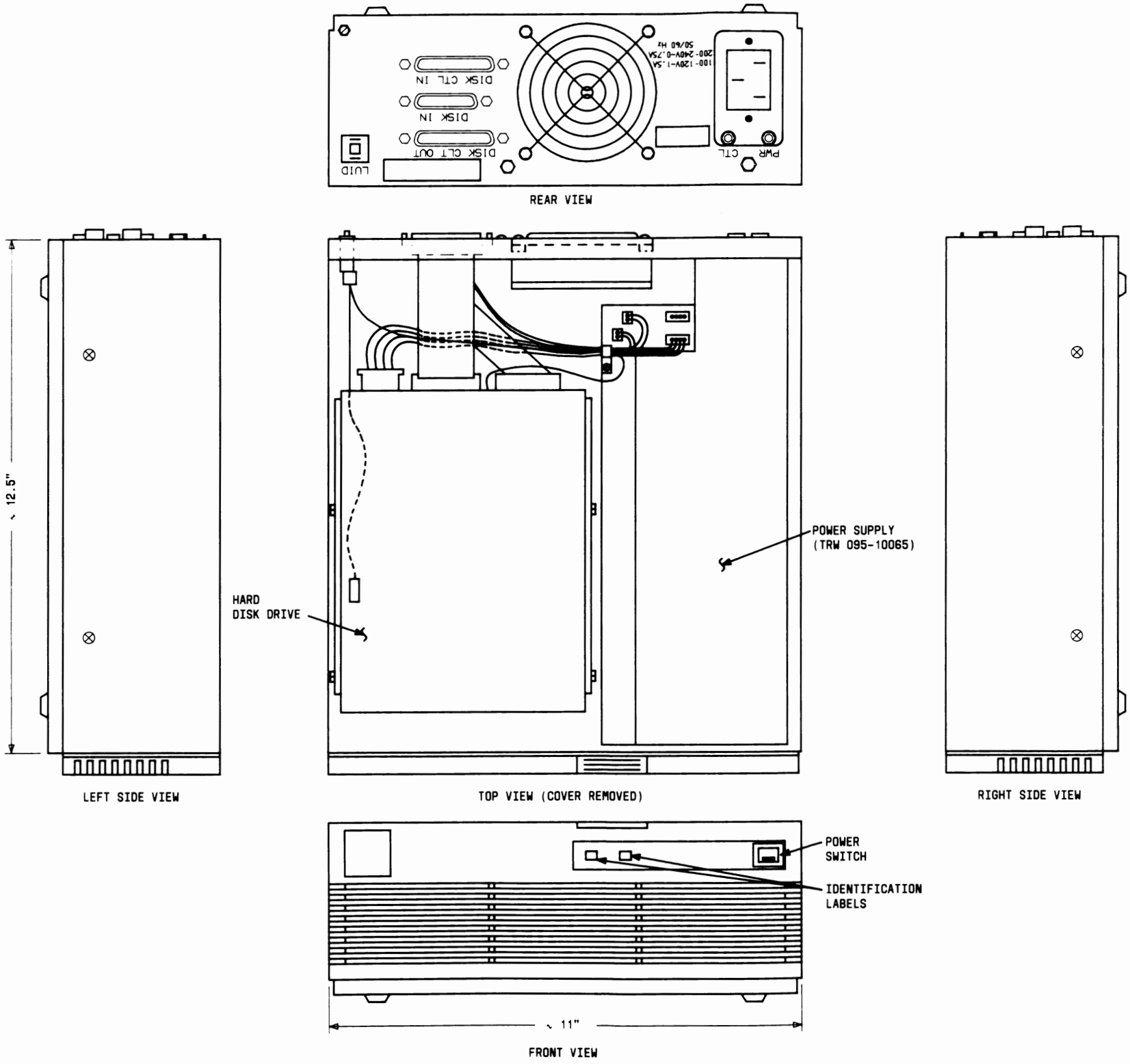


Figure 2-16: AT&T DM Cabinet Assembly Drawing (ED-3T011-30, G2, G3, G5, G6)

AT&T Embedded Disk Modules (ED-3T011-30,G8, G9, G11)

Major Assemblies

Figure 2-17 shows an AT&T Disk Module (DM/S or DM/DS). The DM/S cabinet contains a single-ended, embedded SCSI hard disk drive and power supply. The DM/DS cabinet contains a differential, embedded SCSI disk drive. The major assemblies are listed below:

- Power Supply (TRW #095-10065)
- Disk Drive:
  - Single-ended 300-megabyte disk drive, KS-23483,L1B
  - Differential 300-megabyte disk drive, KS-23483,L11B
  - Differential 600-megabyte disk drive, KS-23483,L15.

AT&T DM/S or DM/DS Equipment Characteristics

Physical.

Height	4 inches
Width	11 inches
Depth	12.5 inches

Electrical.

Voltage	120 V AC, 1.5 Amperes Domestic 240 V AC, 0.75 Amperes International
Frequency	50/60 Hz

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing

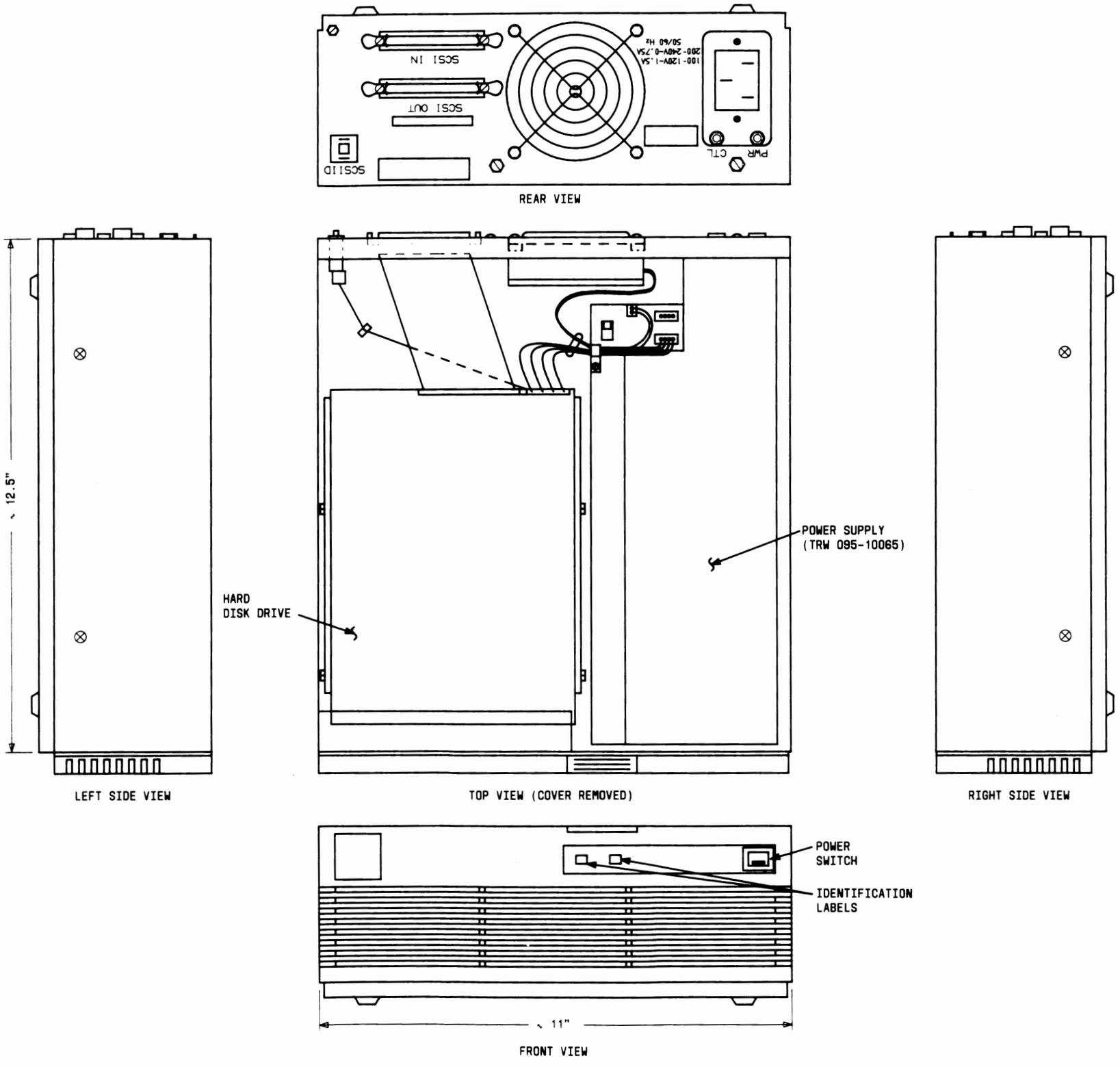


Figure 2-17: AT&T DM/S or DM/DS Cabinet Assembly Drawing (ED-3T011-30, G8, G9, G11)

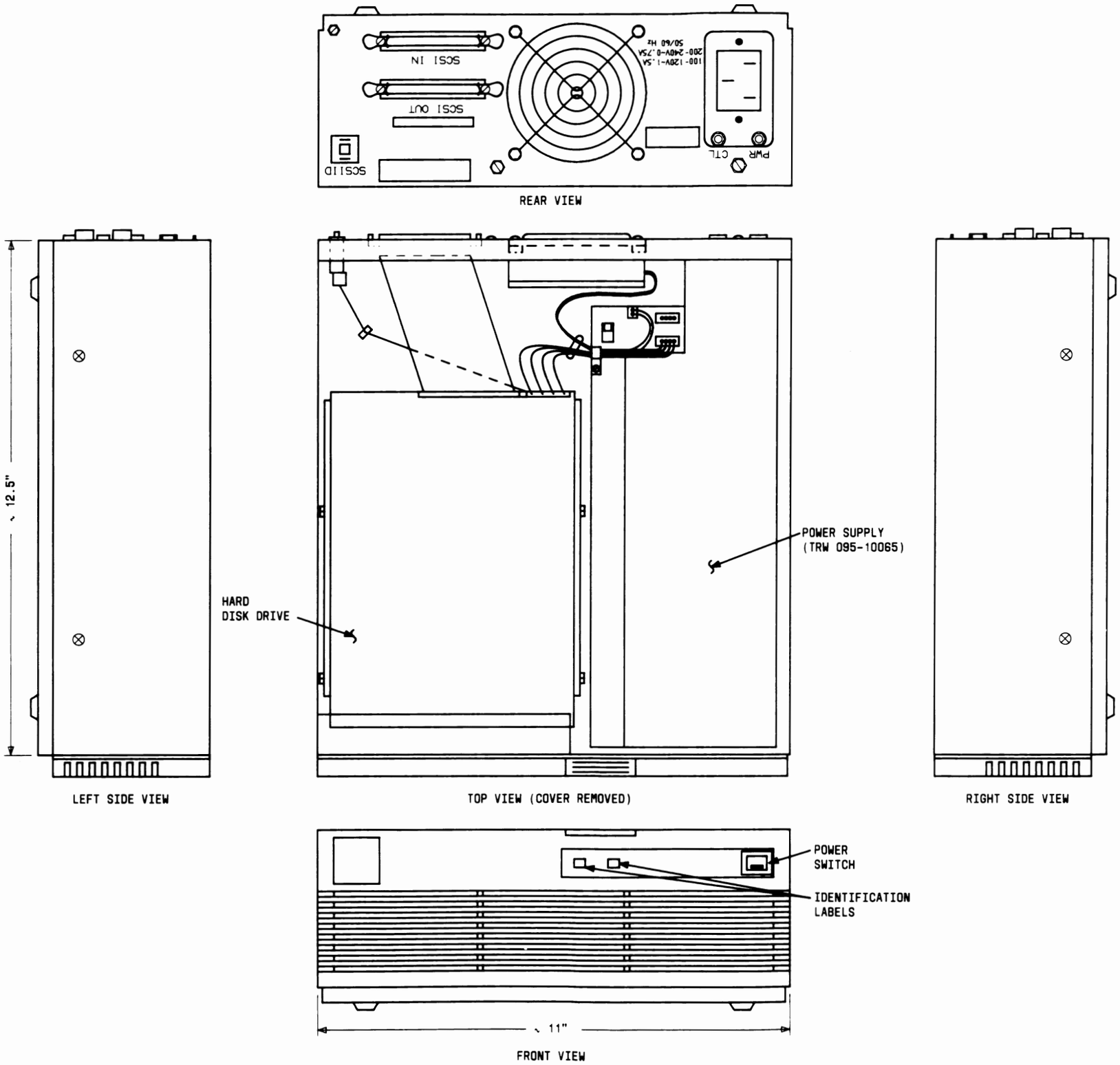


Figure 2-17: AT&T DM/S or DM/DS Cabinet Assembly Drawing (ED-3T011-30, G8, G9, G11)

AT&T SCSI Rewritable Optical Disk Module

Major Assemblies

Figure 2-18 shows an AT&T SCSI Rewritable Optical Disk Module. The optical disk can be used as a storage media or as another hard disk drive. The SCSI Rewritable Optical Disk Module cabinet contains a rewritable optical disk drive, embedded SCSI controller, and power supply. The major assemblies are listed below:

- Power Supply
- Optical Disk Drive.

AT&T SCSI Rewritable Optical Disk Equipment Characteristics

Physical.

Height	4.25 inches
Width	12.8 inches
Depth	11.2 inches

If the optical disk is formatted to operate as a hard disk drive, the format is similar to the WREN* III hard disk drives. The pertinent information is as follows:

Rotational Speed	2400 revolutions per minute
Bytes/Sector	512
Sectors/Track	32
Tracks/Cylinder	64
Cylinders	279 Accessible, 281 Total
Formatted Size	571,392 blocks (512 bytes)

Operational.

Interface	SCSI (Single-ended only)
Transfer Rate	5.44 megabits per second (680 kilobytes per second, read) 2.72 megabits per second (340 kilobytes per second, write)
Seek Time	95 milliseconds, average 185 milliseconds, maximum

Electrical.

Voltage	120 V AC, 1.5 Amperes Domestic 240 V AC, 0.75 Amperes International
Frequency	50/60 Hz

Environmental.

Temperature	50°F to 104°F 10°C to 40°C
Humidity	10% to 90%, noncondensing

* Registered trademark of Control Data Corp.

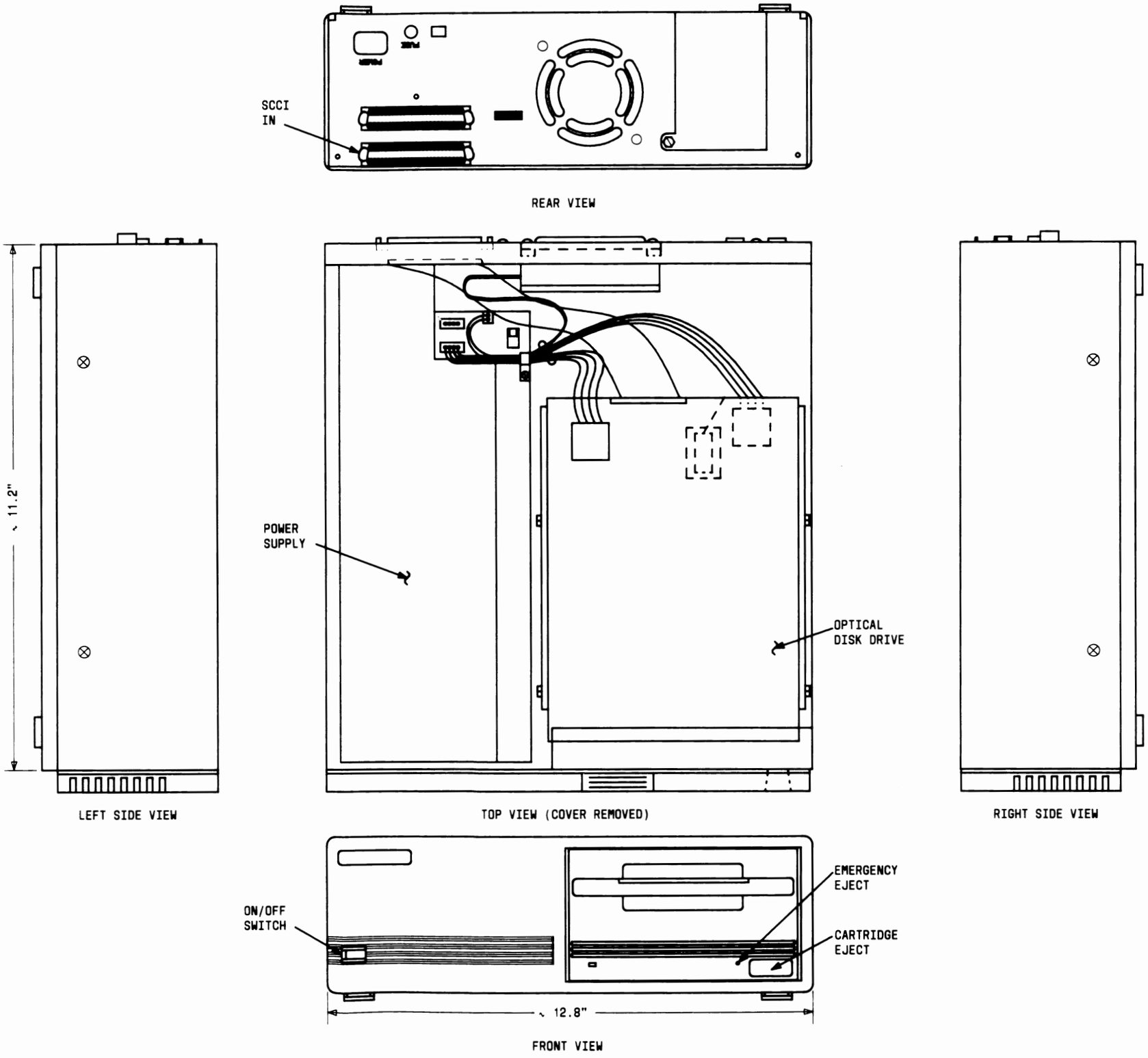


Figure 2-18: AT&T SCSI Rewritable Optical Disk Cabinet Assembly Drawing

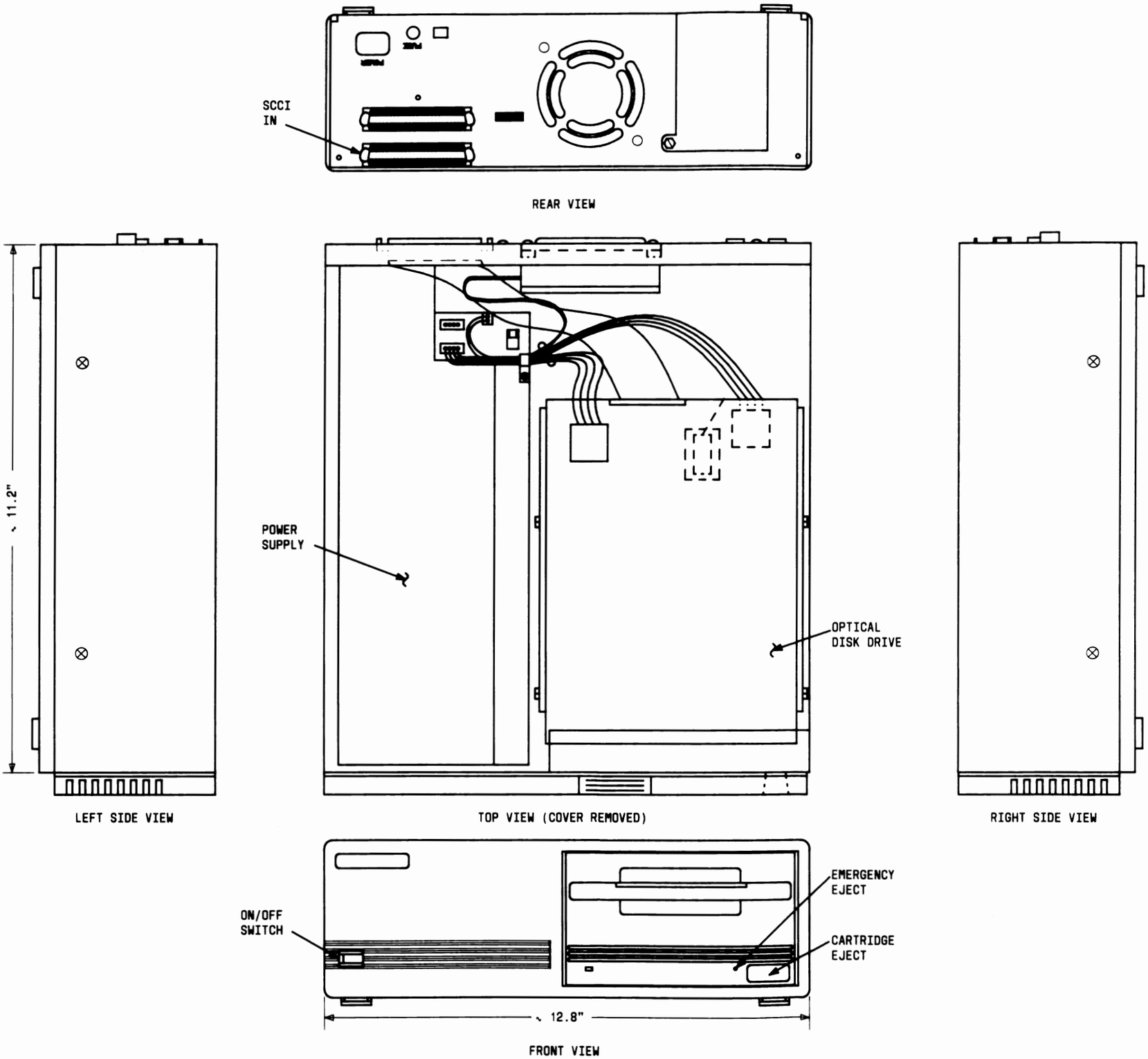


Figure 2-18: AT&T SCSI Rewritable Optical Disk Cabinet Assembly Drawing

AT&T SCSI 9-Track Tape

The AT&T SCSI 9-Track Tape Drives are standard 9-track, reel-to-reel devices which permit transfer of data between AT&T computers that support SCSI. These drives are also media compatible with other vendors' computers. Although a SCSI 9-Track Tape Drive is intended primarily as a data transfer mechanism, it can also be used as a mass storage backup device.

All SCSI 9-Track Tape Drives have an embedded SCSI controller which connects directly to the SCSI bus. There are two SCSI 9-Track Tape Drives:

- Desktop, autoloading, dual density (1600/6250 BPI)
- Manual-loading, single density (1600 BPI).

Figures 2-19 and 2-20 show the two types of SCSI 9-Track Tape Drives.

AT&T SCSI 9-Track Tape Drive Equipment Characteristics

Electrical.

Voltage	120 V AC, 1.5 Amperes Domestic 240 V AC, 0.75 Amperes International
Frequency	50/60 Hz

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing

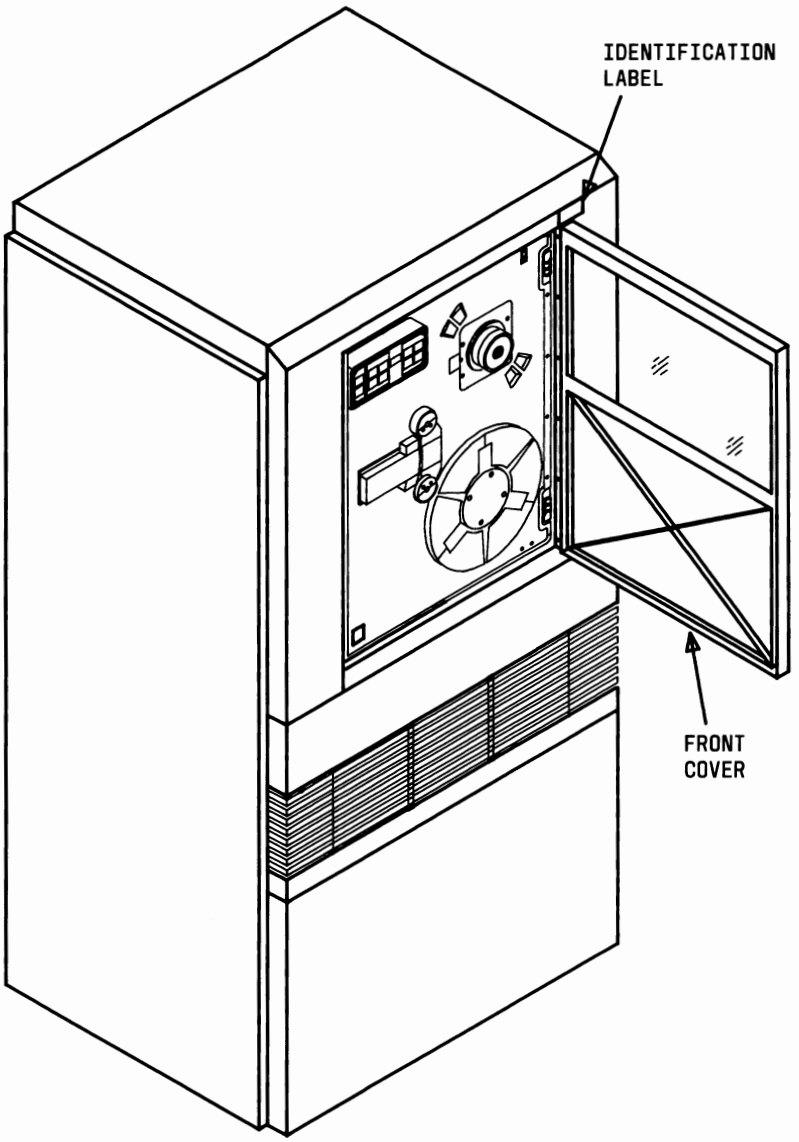


Figure 2-19: SCSI Manual Loading 9-Track Tape Cabinet

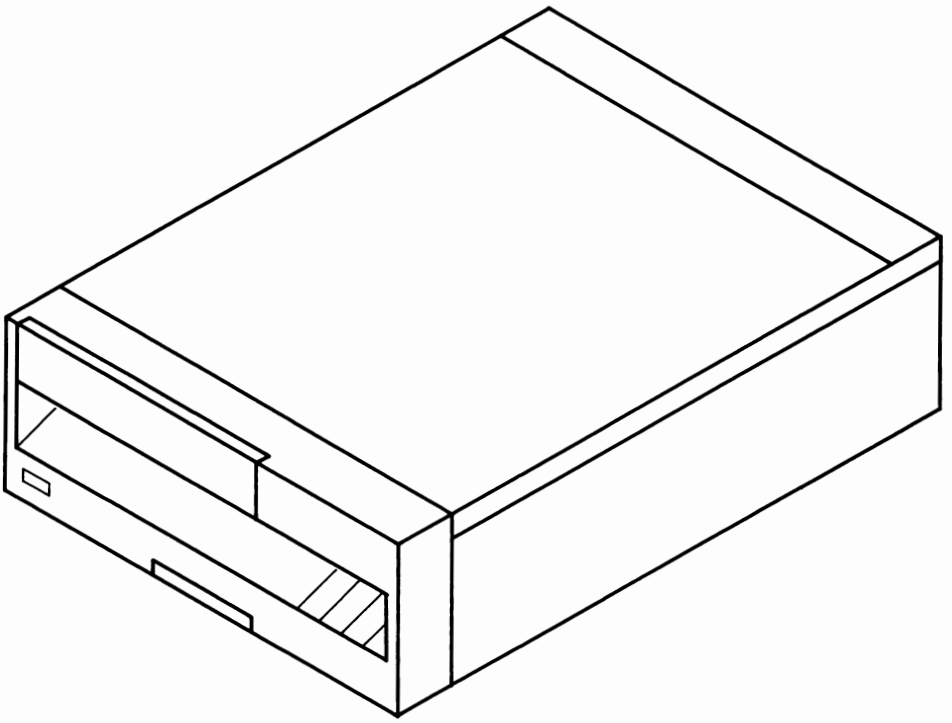


Figure 2-20: SCSI Autoloading 9-Track Tape Cabinet

AT&T SCSI Tape Module (ED-3T011-30,G4, G7)

Major Assemblies

Figure 2-21 shows an AT&T SCSI Tape Module (TM). The TM cabinet contains a 60- or 120-megabyte, embedded SCSI Cartridge Tape Drive and power supply. The major assemblies are listed below:

- Power Supply (TRW #095-10065)
- Tape Drive:
  - 60-megabyte SCSI Cartridge Tape Drive, KS-23417,L1 or L3
  - 120-megabyte SCSI Cartridge Tape Drive, KS-23465,L1, L31, or L51.

AT&T SCSI TM Equipment Characteristics

Physical.

Height	4 inches
Width	11 inches
Depth	12.5 inches

Electrical.

Voltage	120 V AC, 1.5 Amperes Domestic 240 V AC, 0.75 Amperes International
Frequency	50/60 Hz

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing

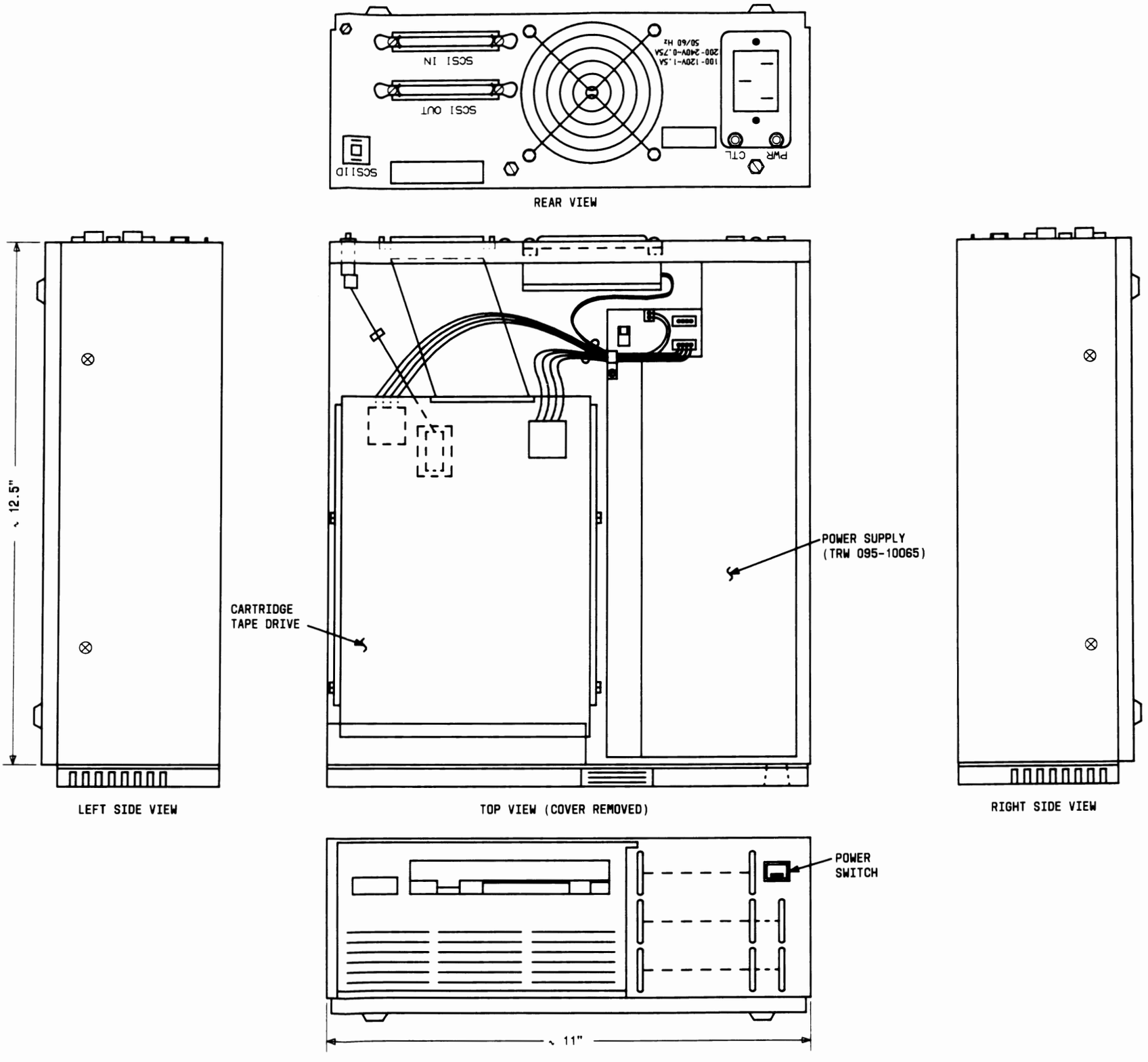


Figure 2-21: AT&T SCSI TM Cabinet Assembly Drawing (ED-3T011-30, G4, G7)

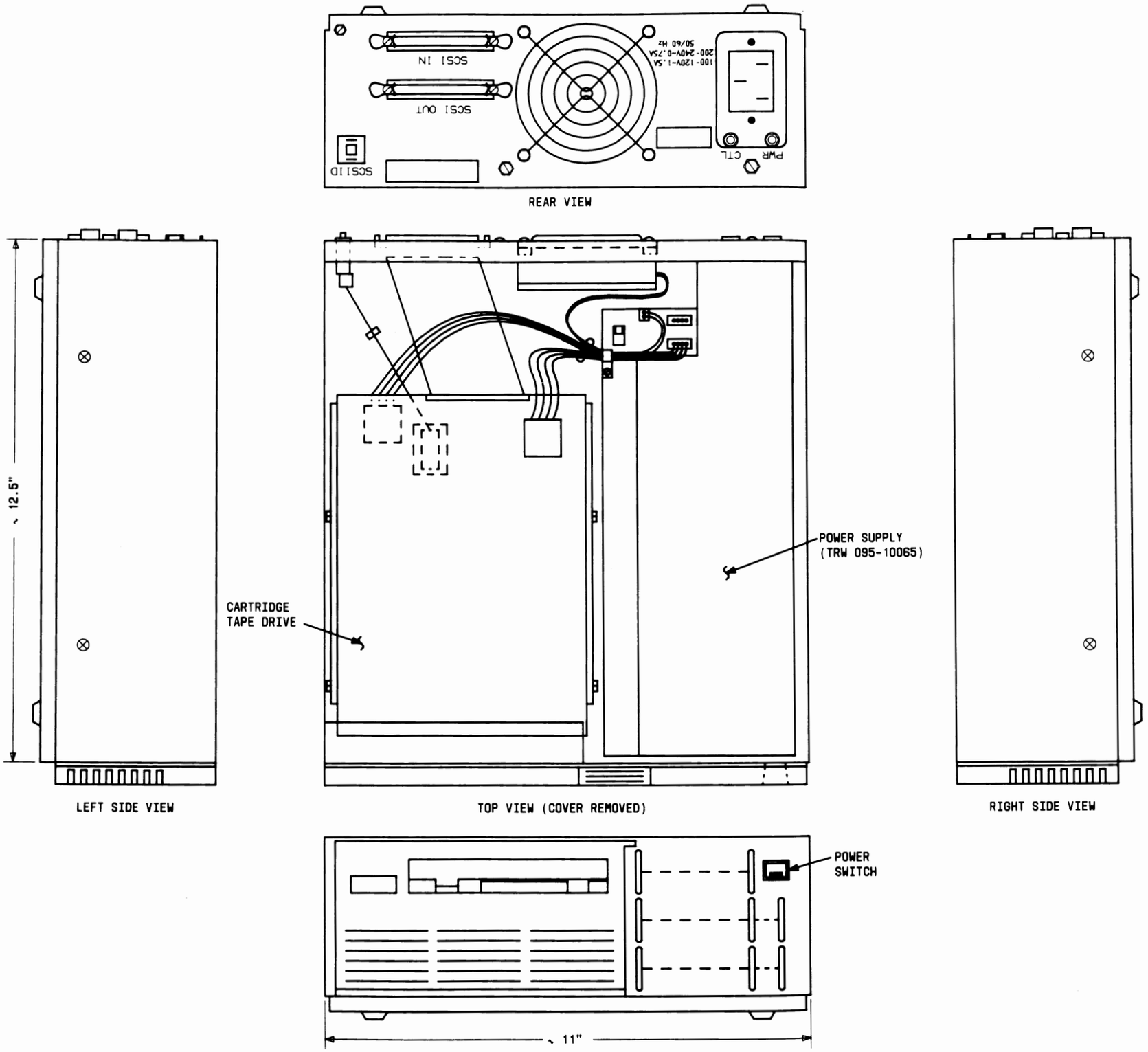


Figure 2-21: AT&T SCSI TM Cabinet Assembly Drawing (ED-3T011-30,G4, G7)

AT&T Cartridge Tape Module

Major Assemblies

The AT&T Cartridge Tape Module is a 3B2 computer external cartridge tape unit with built-in power supply. The cartridge tape module cabinet houses one 23-megabyte cartridge tape drive and a power supply. The cartridge tape unit is the same tape unit used in the AT&T/XM and 3B2/400. A cartridge tape drive connects to the host 3B2 computer via a CM195H Cartridge Tape Controller Card. The CM195H is installed in a 3B2 computer feature card slot. The AT&T Tape Module is a low-cost alternative to using an AT&T/XM to provide cartridge tape backup capability when the additional hard disk drive expansion is not required. Soft power control is not provided with the AT&T Tape Module. The AT&T Tape Module is available only with a power supply for 115 volts AC operation.

AT&T Cartridge Tape Module Equipment Characteristics

Physical.

Height	5 inches
Width	7.75 inches
Depth	15.5 inches

Electrical.

Voltage	120 V AC, 1 Ampere
Frequency	50/60 Hz
Total Power Consumption (Heat Dissipation)	120 watts (or less)

Environmental.

Temperature	40°F to 112°F 5°C to 45°C
Humidity	20% to 80% relative humidity (noncondensing) with a maximum wet bulb temperature of 26°C
Altitude	10,000 feet above sea level
Noise	40 dB(A) (idle), 43 dB(A) (running)

AT&T Peripheral Power Control Unit (ED-3T011-30,G10)

Major Assemblies

Figure 2-22 shows an AT&T Peripheral Power Control Unit (PPCU). The PPCU allows multiple host computers to control shared peripheral unit power. Inside the cabinet is the CFW1 Circuit Card that makes the power control connections.

AT&T PPCU Equipment Characteristics

Physical.

Height	4 inches
Width	11 inches
Depth	12.5 inches

Environmental.

Temperature	40°F to 100°F 5°C to 38°C
Humidity	20% to 80%, noncondensing

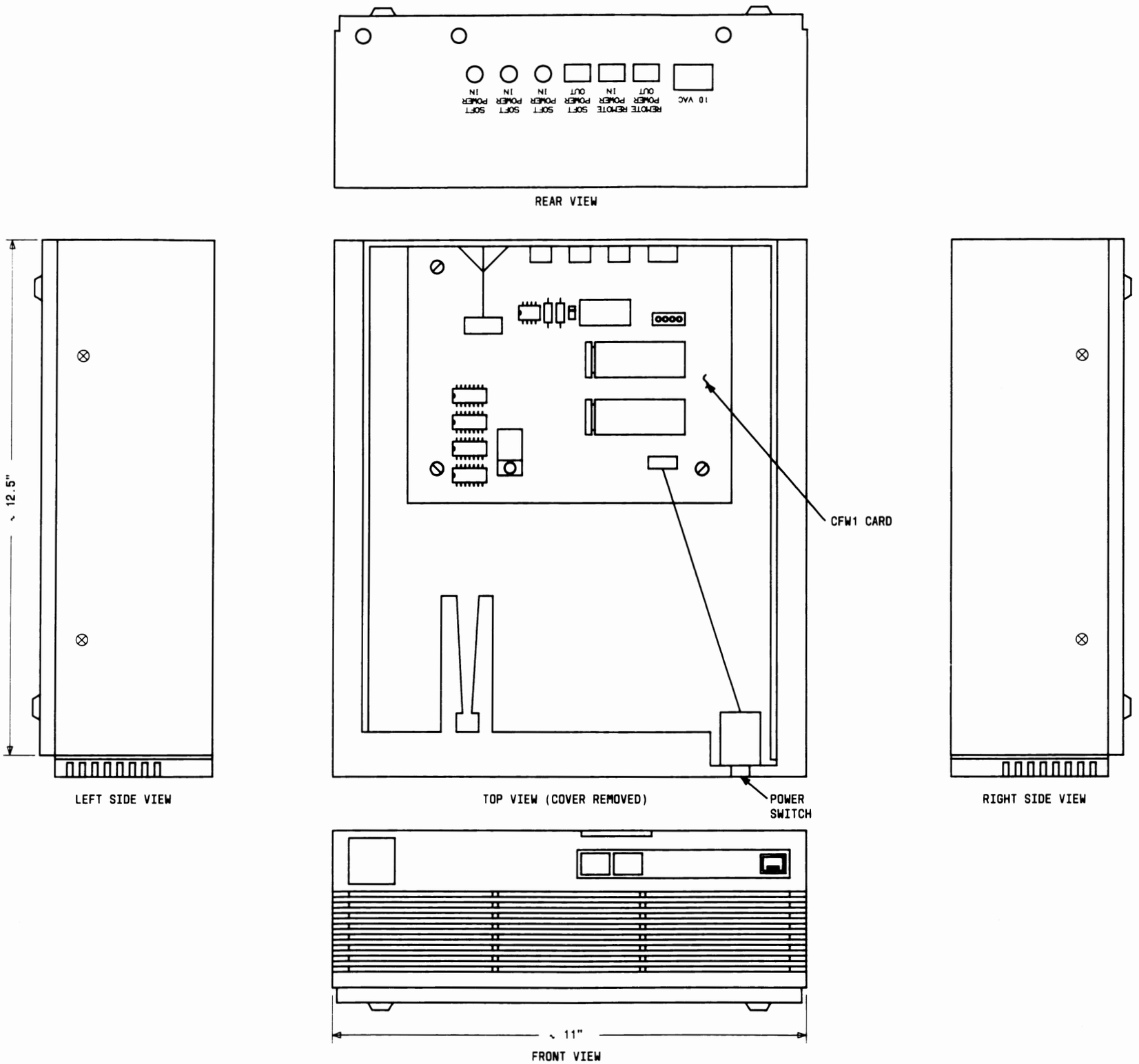


Figure 2-22: AT&T PPCU Cabinet Assembly Drawing (ED-3T011-30,G10)

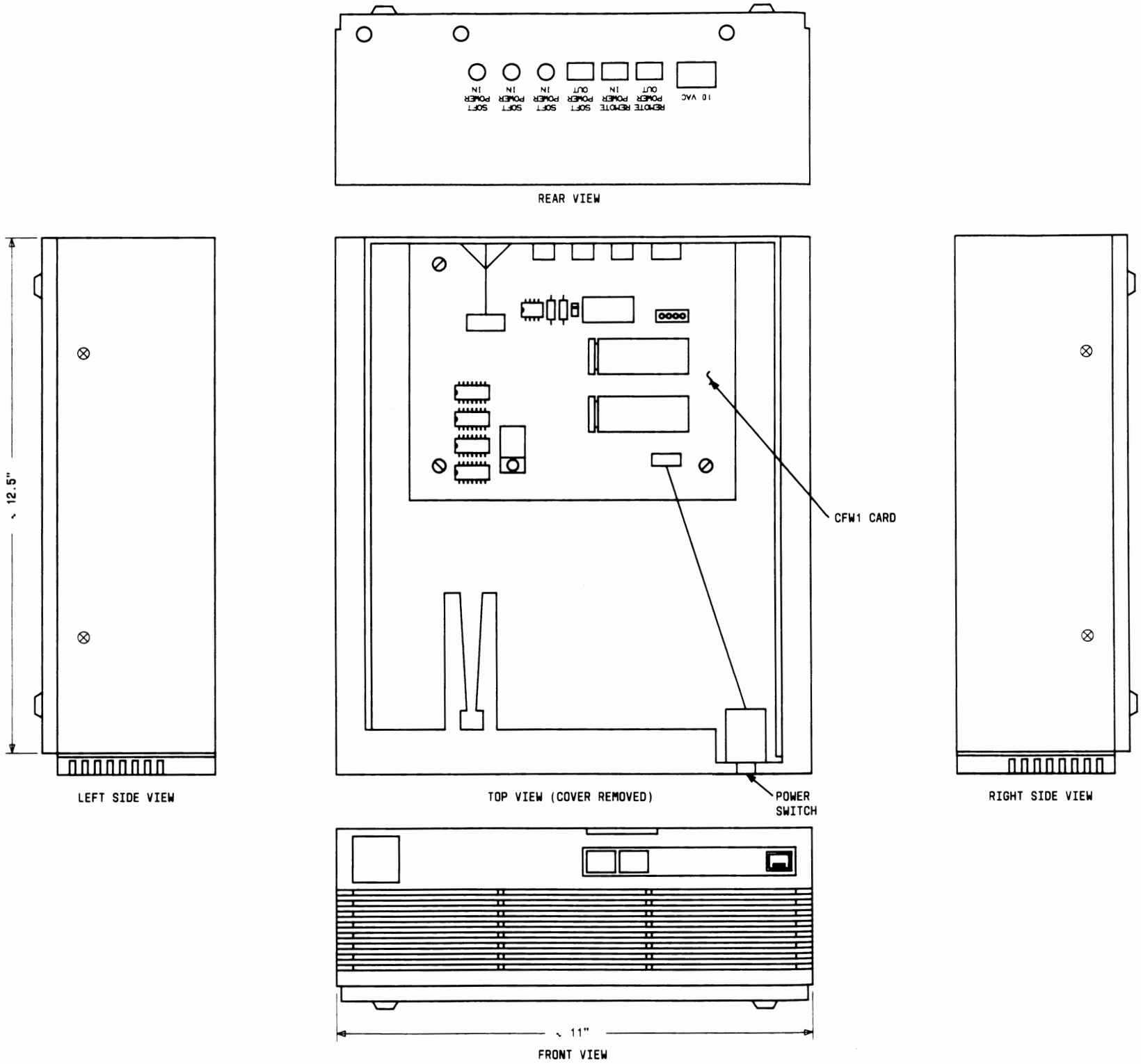


Figure 2-22: AT&T PPCU Cabinet Assembly Drawing (ED-3T011-30,G10)

SYSTEM BOARDS

CM190A System Board

CM190A System Board Layout

Figure 2-23 shows the layout of the component side of a CM190A System Board. The system board is a multilayer board measuring 7.7 inches wide by 14.8 inches deep. Refer to Appendix B for connector pinout information. All system board interfaces are connectorized as follows:

- CONSOLE and CONTTY RS-232C Ports (J01)
- Backplane Board (J02 and J03)
- Power (J04)
- Random Access Memory (RAM) Cards (M0/J05 and M1/J06)
- Integral Hard Disk Control Bus (J07)
- Integral Hard Disk Data Bus 0 (J08)
- Integral Hard Disk Data Bus 1 (J09)
- Integral Floppy Disk Data and Control Bus (J10)
- Nonvolatile Random Access Memory (NVRAM) Power (J11)
- Diagnostic and Power Indicators (J12 and J13).

The following major components on the system board are connectorized:

- Read Only Memory (ROM) (four Dual Inline Packages)
- WE 32002 Processor Module
- 28.8-MHz Oscillator (divided by four for 7.2-MHz system clock).

CM190A Versions (Series Information)

The CM190A System Board is used in early production 3B2/300 computers. The CM190A System Board has been discontinued and replaced by the System Board, ED-4C637-30.

Artmaster 5 and later CM190A System Boards are required to run the UNIX System V Release 2.0 and later releases of the operating system. Artmaster 6 and later system boards are required to support a 72-megabyte hard disk drive as an integral disk.

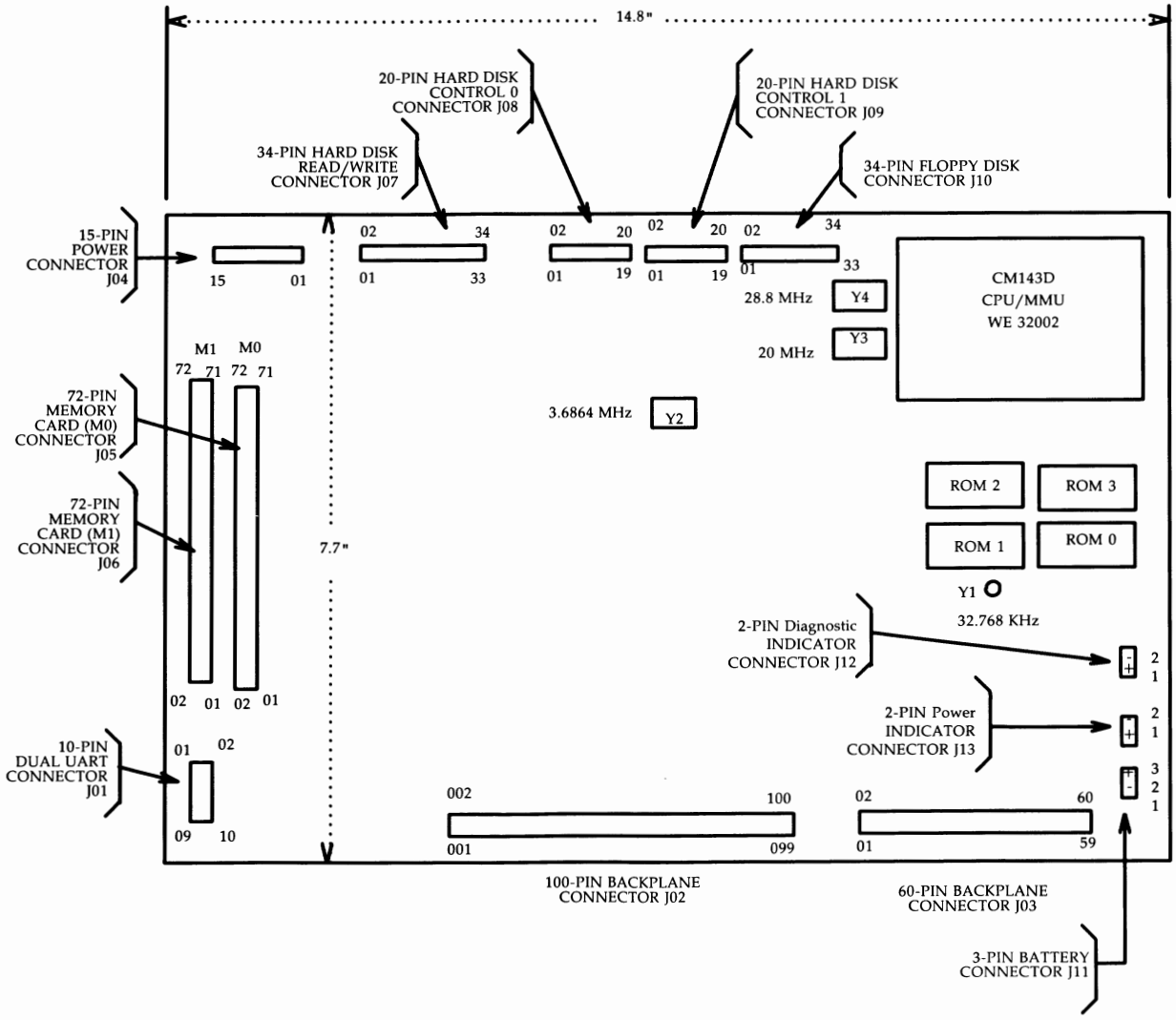


Figure 2-23: CM190A System Board Layout (Discontinued Availability)

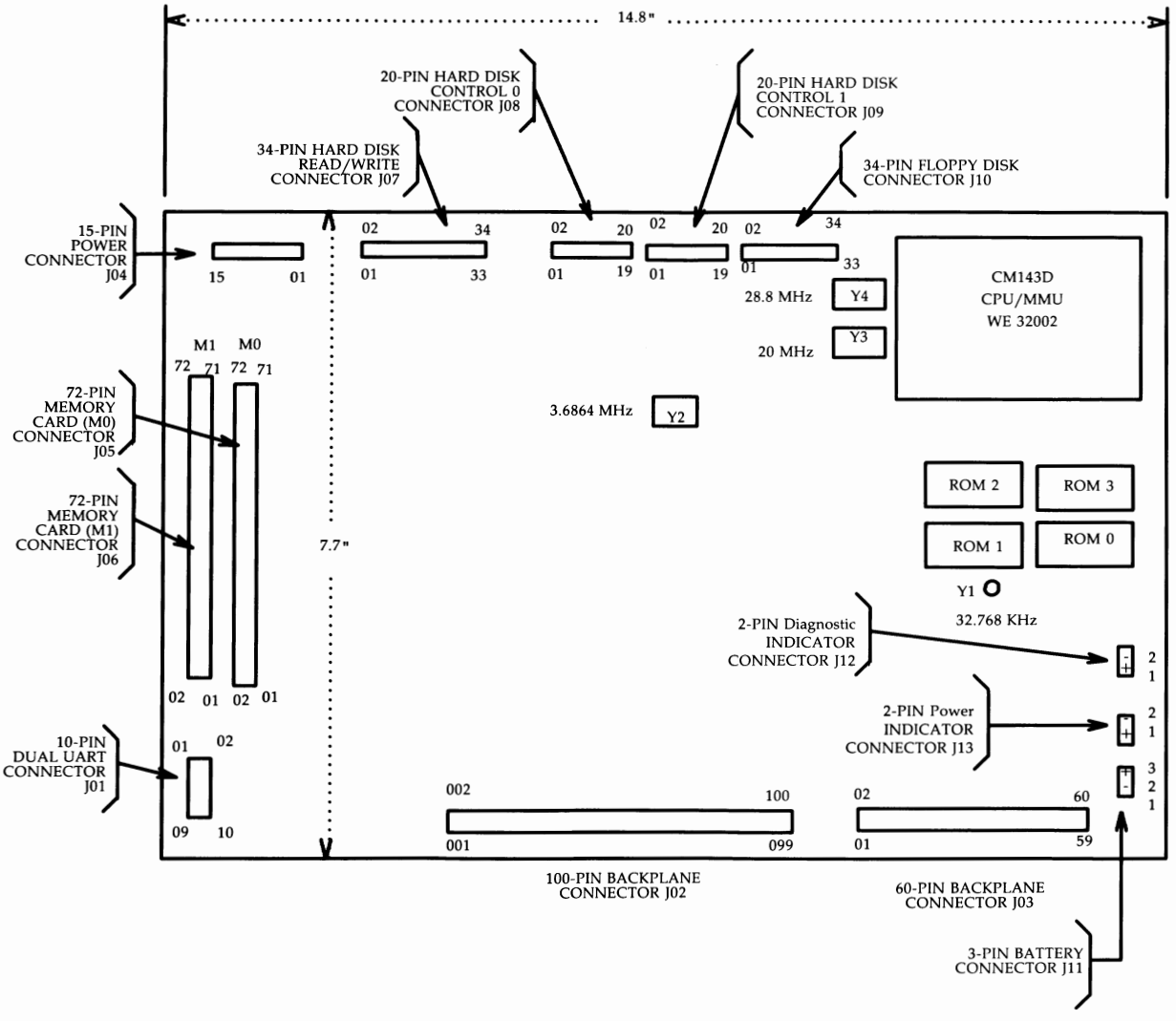


Figure 2-23: CM190A System Board Layout (Discontinued Availability)

ED-4C637-30 System Board

ED-4C637-30 System Board Layout

Figure 2-24 shows the layout of the component side of a typical System Board, ED-4C637-30. The system board is a multilayer board measuring 7.7 inches wide by 14.8 inches deep. Refer to Appendix B for connector pinout information. All system board interfaces are connectorized as follows:

- CONSOLE and CONTTY RS-232C Ports (J01)
- Backplane Board (J02 and J03)
- Power (J04)
- Random Access Memory (RAM) Cards (M0/J05 and M1/J06)
- Integral Hard Disk Control Bus (J07)
- Integral Hard Disk Data Bus 0 (J08)
- Integral Hard Disk Data Bus 1 (J09)
- Integral Floppy Disk Data and Control Bus (J10)
- Nonvolatile Random Access Memory (NVRAM) Power (J11)
- Diagnostic and Power Indicators (J12 and J13)
- Auxiliary Disk Interface Soft Power (J14).

The following major components on the system board are connectorized:

- Read Only Memory (ROM) (four Dual Inline Packages)
- WE 32100 Microprocessor Central Processor Unit (CPU)
- WE 32101 Memory Management Unit (MMU)
- 8.2/10-MHz Oscillator
- WE 32106 Math Acceleration Unit (MAU) (optional).

ED-4C637-30 System Board Versions (Series Information)

Different versions (groups) are used for the various 3B2 computer models. The differences among the groups are the system clock (8.2 MHz or 10 MHz) and equipage of the WE 32101 MAU. The system board groups are identified in the following table by the model of computer, system clock rate, and MAU equipage. Not identified in the table is ED-4C637-30,G6 that is a stripped board (no ROM or MAU) used for system board sparing.

SYSTEM BOARD	COMPUTER MODEL	SYSTEM CLOCK	MAU
ED-4C637-30,G1	3B2/300	8.2 MHz	—
ED-4C637-30,G2	3B2/400	10 MHz	NO
ED-4C637-30,G3	3B2/310	10 MHz	NO
ED-4C637-30,G4	3B2/310	10 MHz	YES
ED-4C637-30,G5	3B2/400	10 MHz	YES

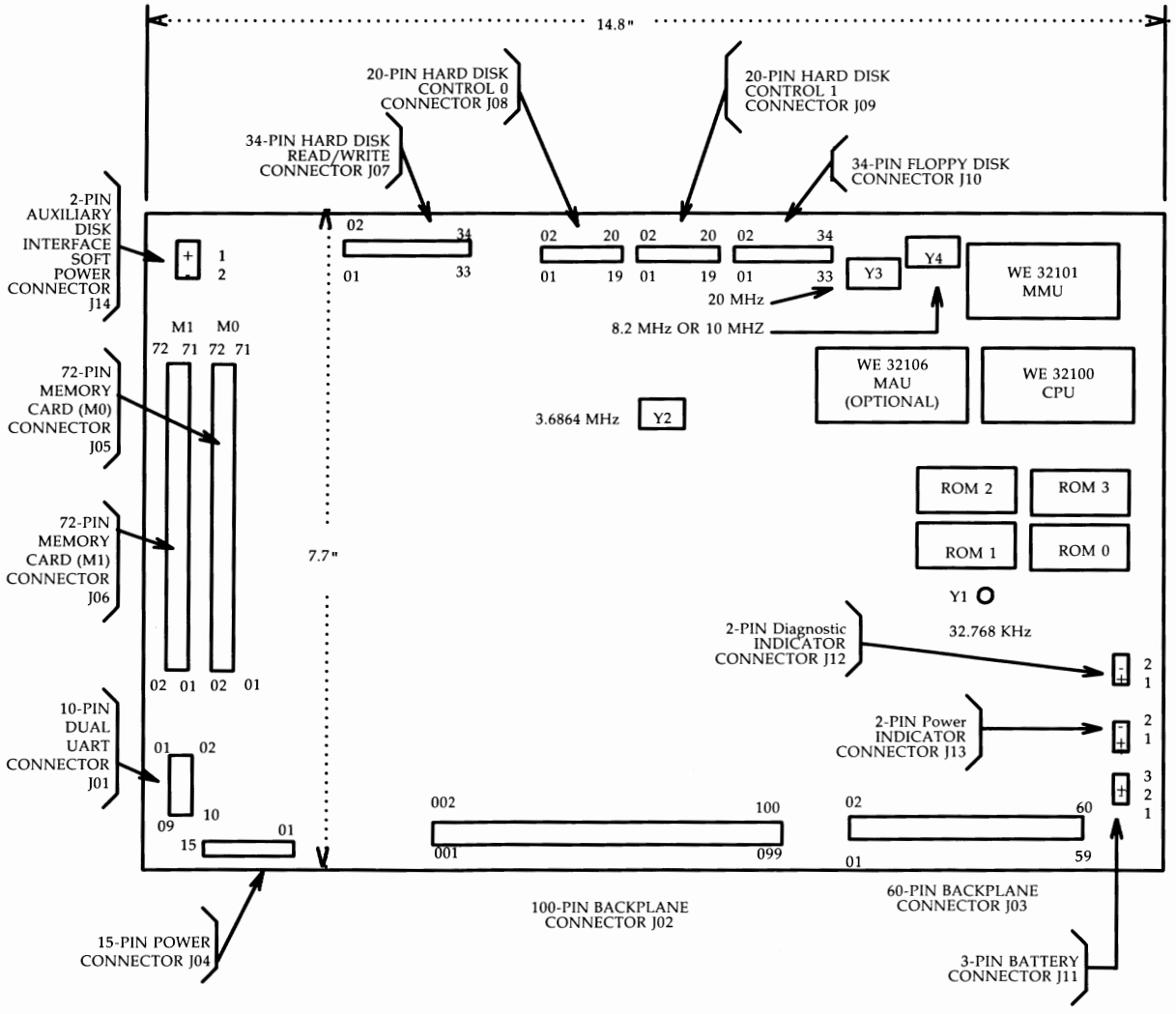


Figure 2-24: System Board, ED-4C637-30 Layout

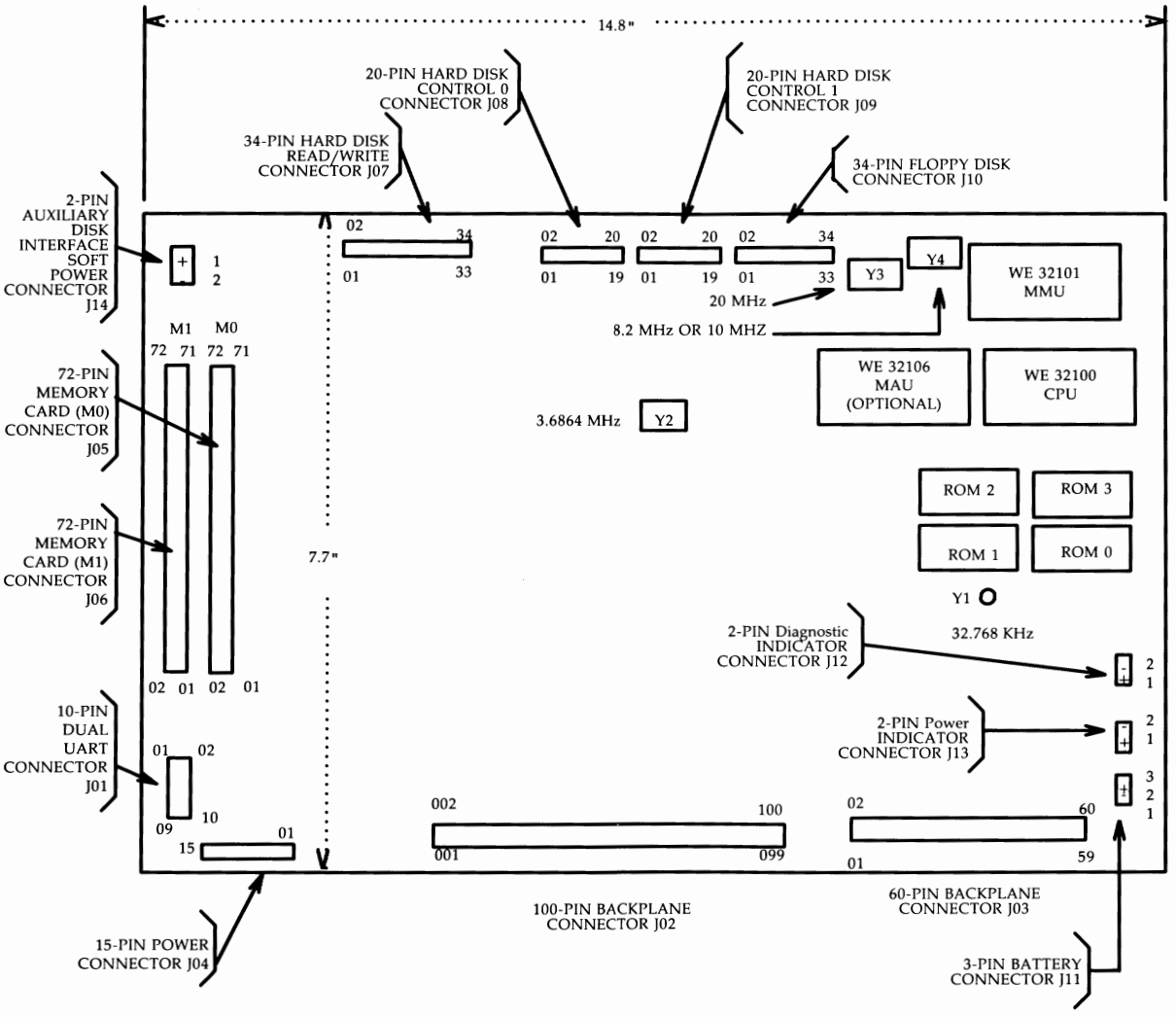


Figure 2-24: System Board, ED-4C637-30 Layout

CM518A System Board

CM518A System Board Layout

Figure 2-25 shows the layout of the component side of a typical CM518A System Board. The system board is a multilayer board measuring 14.8 inches wide by 7.7 inches deep. All system board interfaces are connectorized as follows:

- CONSOLE and CONTTY RS-232C Ports (J4 and J5)
- Alternate CONSOLE and CONTTY RS-232C Ports (J1)
- Backplane Connector (J2)
- Battery Connector (J3).

The following major components on the system board are connectorized:

- Read Only Memory (ROM) (four Dual Inline Packages)
- 82HS321A Integrated Circuit (Artmaster 2 only).

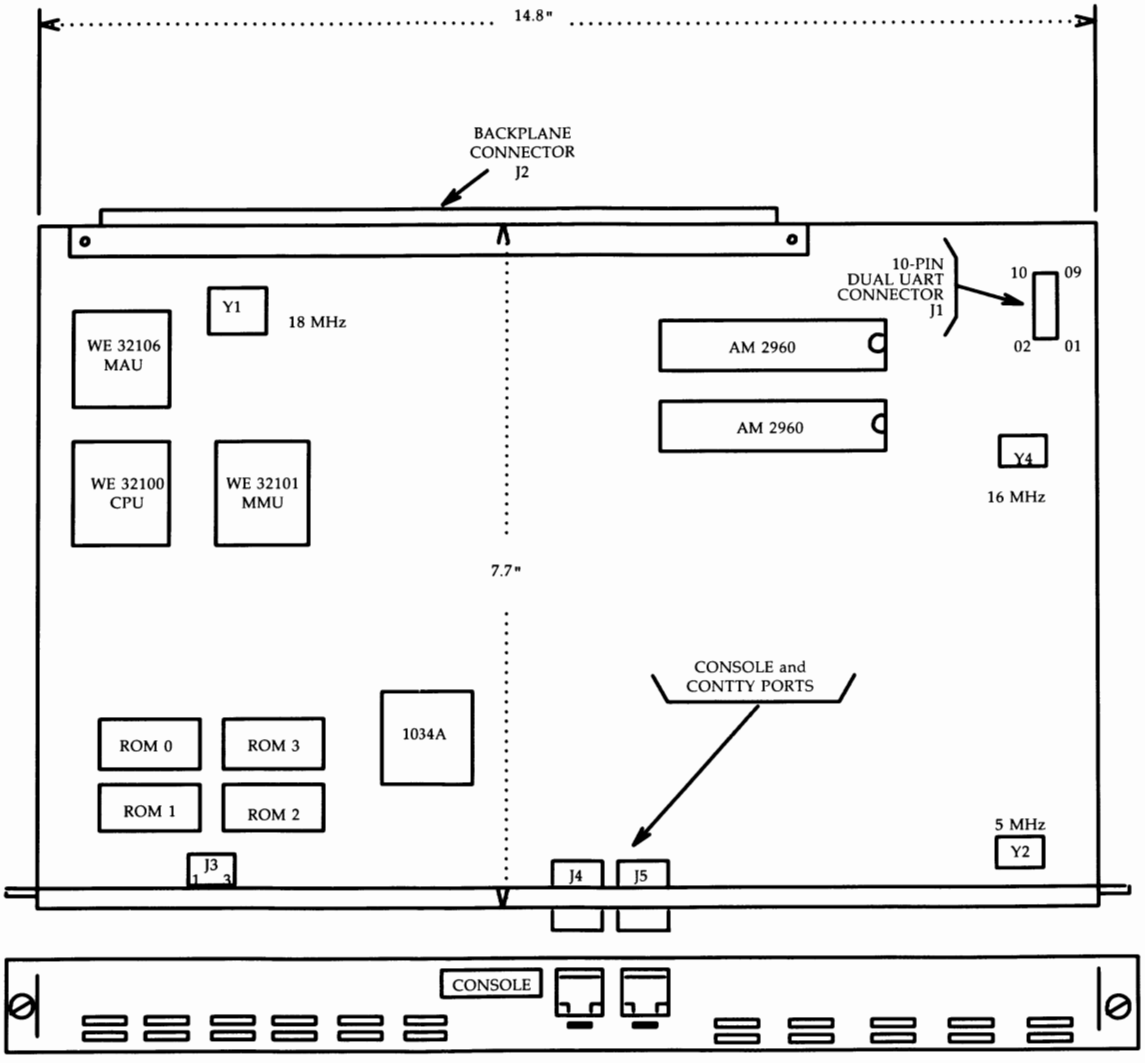


Figure 2-25: CM518A System Board Layout

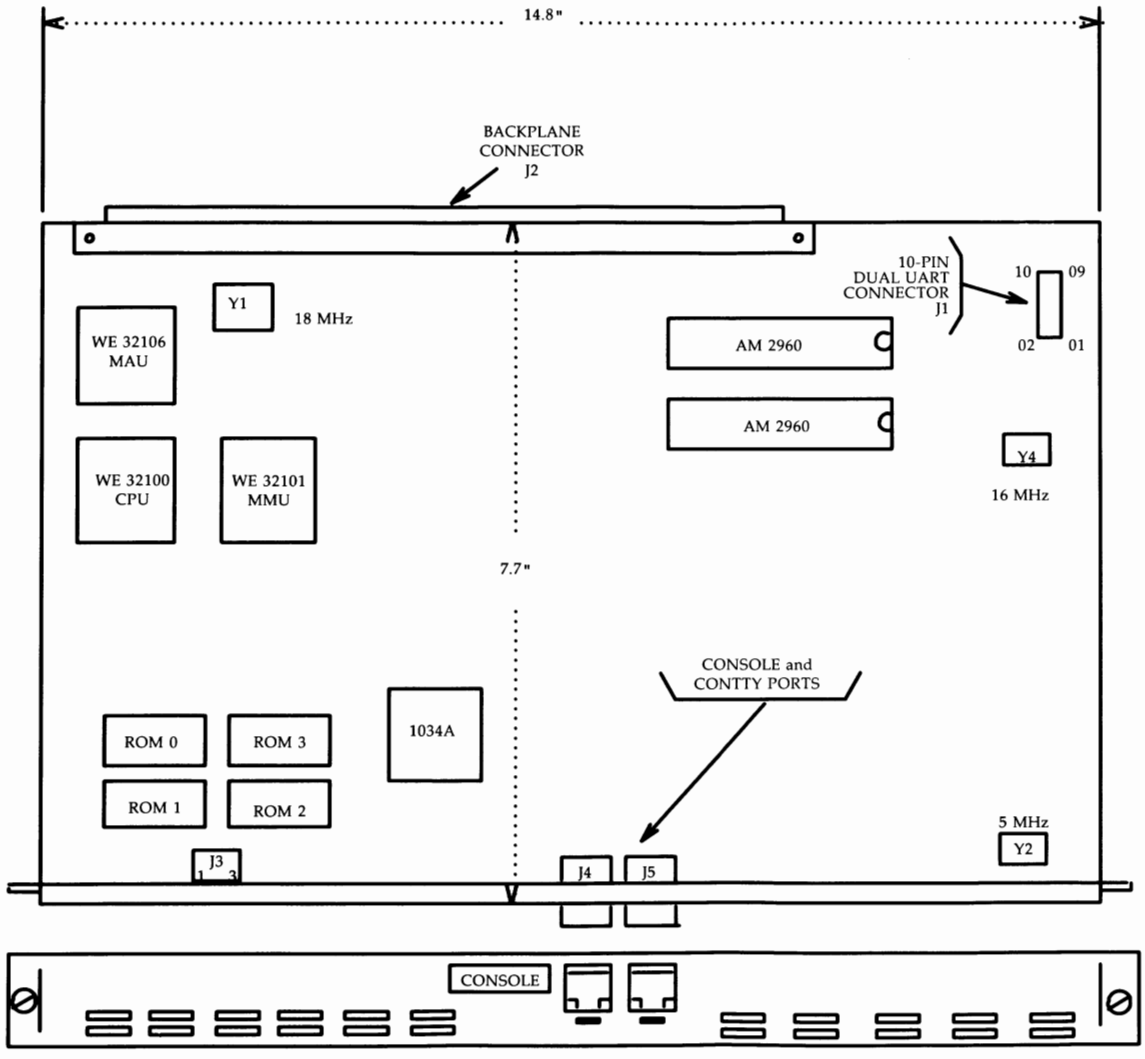


Figure 2-25: CM518A System Board Layout

CM518B System Board

CM518B System Board Layout

Figure 2-26 shows the layout of the component side of a typical CM518B System Board. The system board is a multilayer board measuring 14.8 inches wide by 7.7 inches deep. All system board interfaces are connectorized as follows:

- CONSOLE and CONTTY RS-232C Ports (J4 and J5)
- Alternate CONSOLE and CONTTY RS-232C Ports (J1)
- Backplane Connector (J2).

The following major components on the system board are connectorized:

- Read Only Memory (ROM) (four Dual Inline Packages)
- WE 32200 Microprocessor Central Processor Unit (CPU)
- WE 32201 Memory Management Unit (MMU)
- WE 32206 Math Acceleration Unit (MAU).

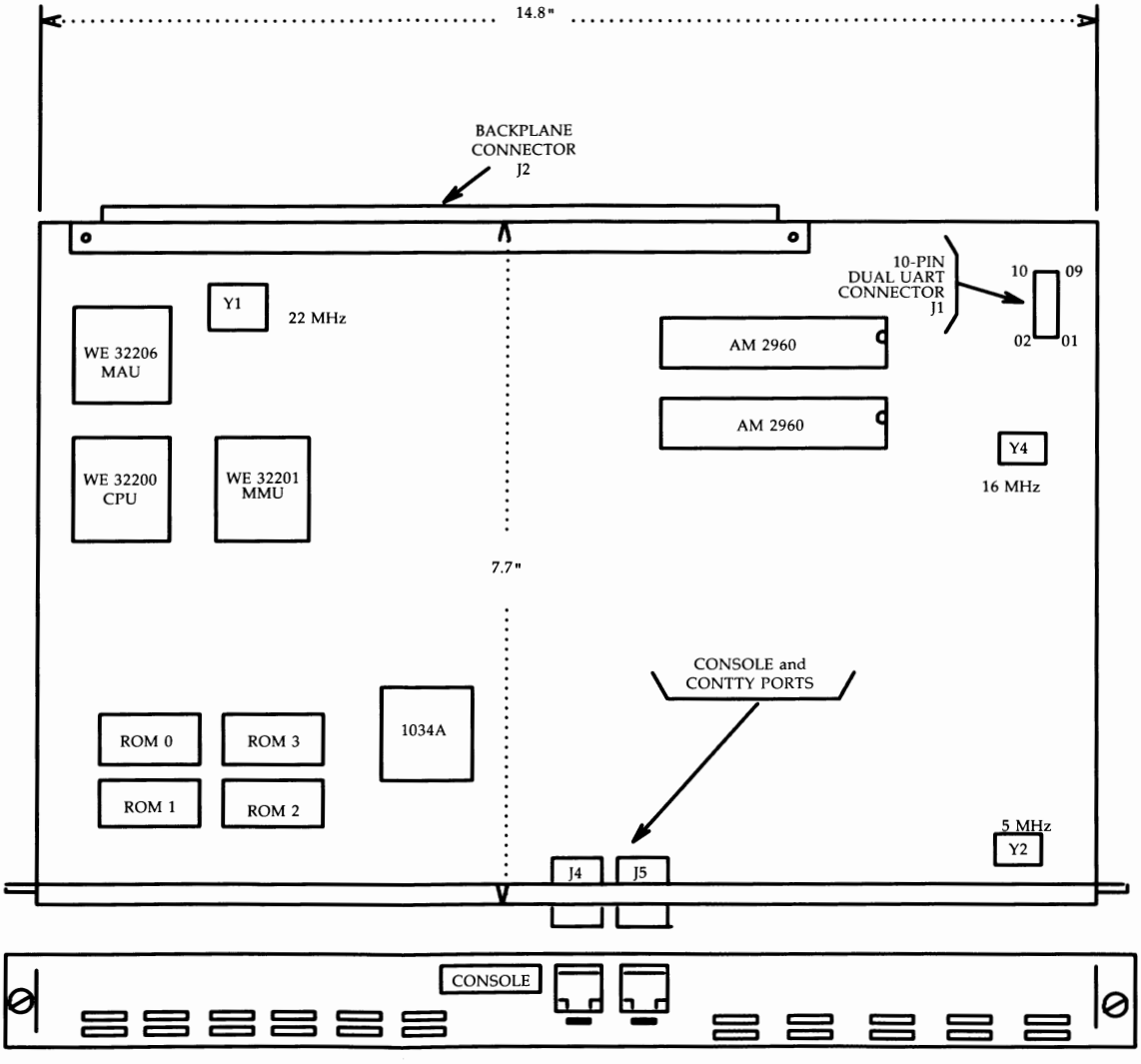


Figure 2-26: CM518B System Board Layout

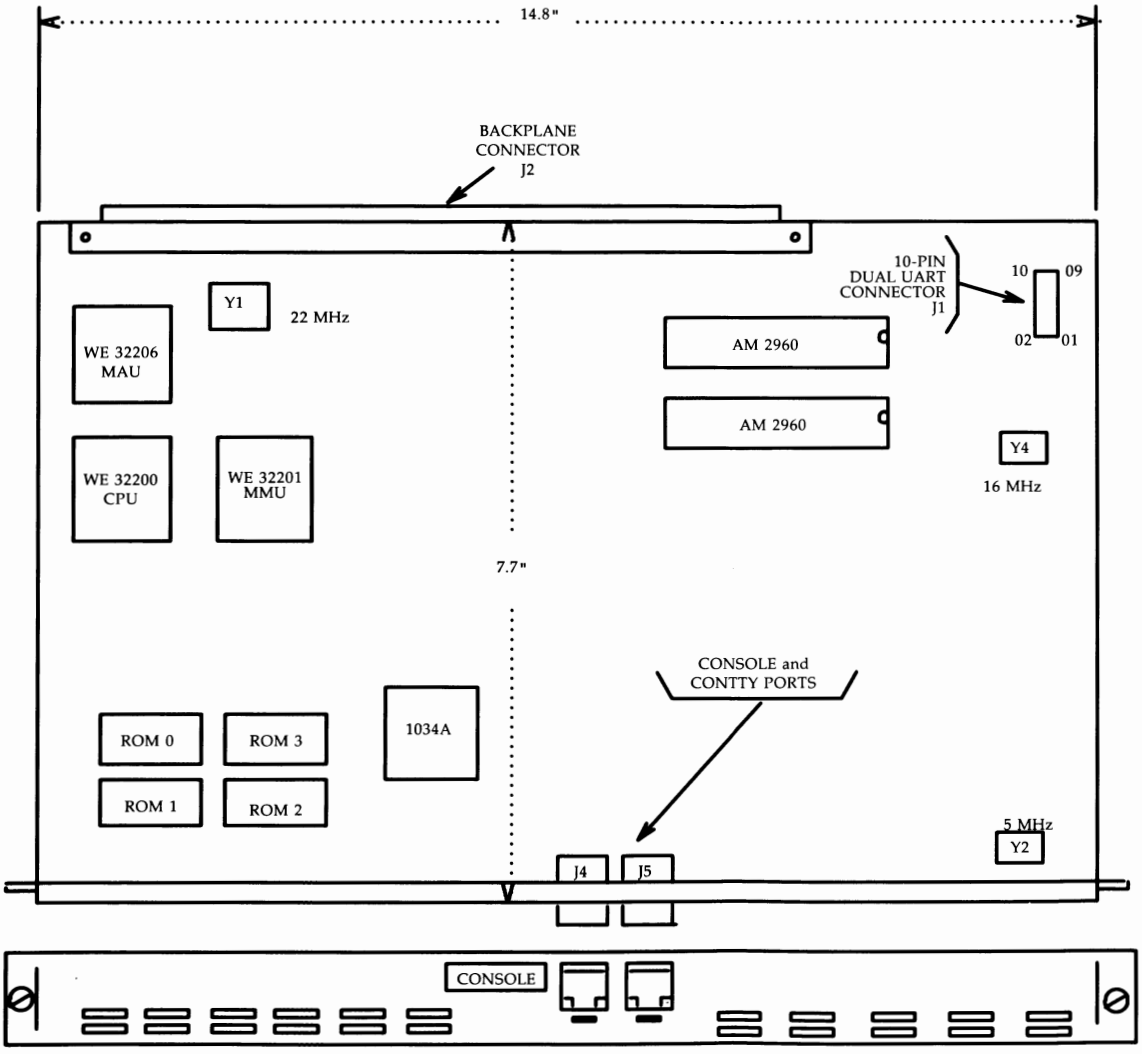


Figure 2-26: CM518B System Board Layout

CM518C System Board

CM518C System Board Layout

Figure 2-27 shows the layout of the component side of a typical CM518C System Board. The system board is a multilayer board measuring 14.8 inches wide by 7.7 inches deep. All system board interfaces are connectorized as follows:

- CONSOLE and CONTTY RS-232C Ports (J4 and J5)
- Alternate CONSOLE and CONTTY RS-232C Ports (J1)
- Backplane Connector (J2).

The following major components on the system board are connectorized:

- Read Only Memory (ROM) (two Dual Inline Packages)
- WE 32200 Microprocessor Central Processor Unit (CPU)
- Two WE 32201 Memory Management Unit (MMU)
- WE 32206 Math Acceleration Unit (MAU)
- 24-MHz Oscillator.

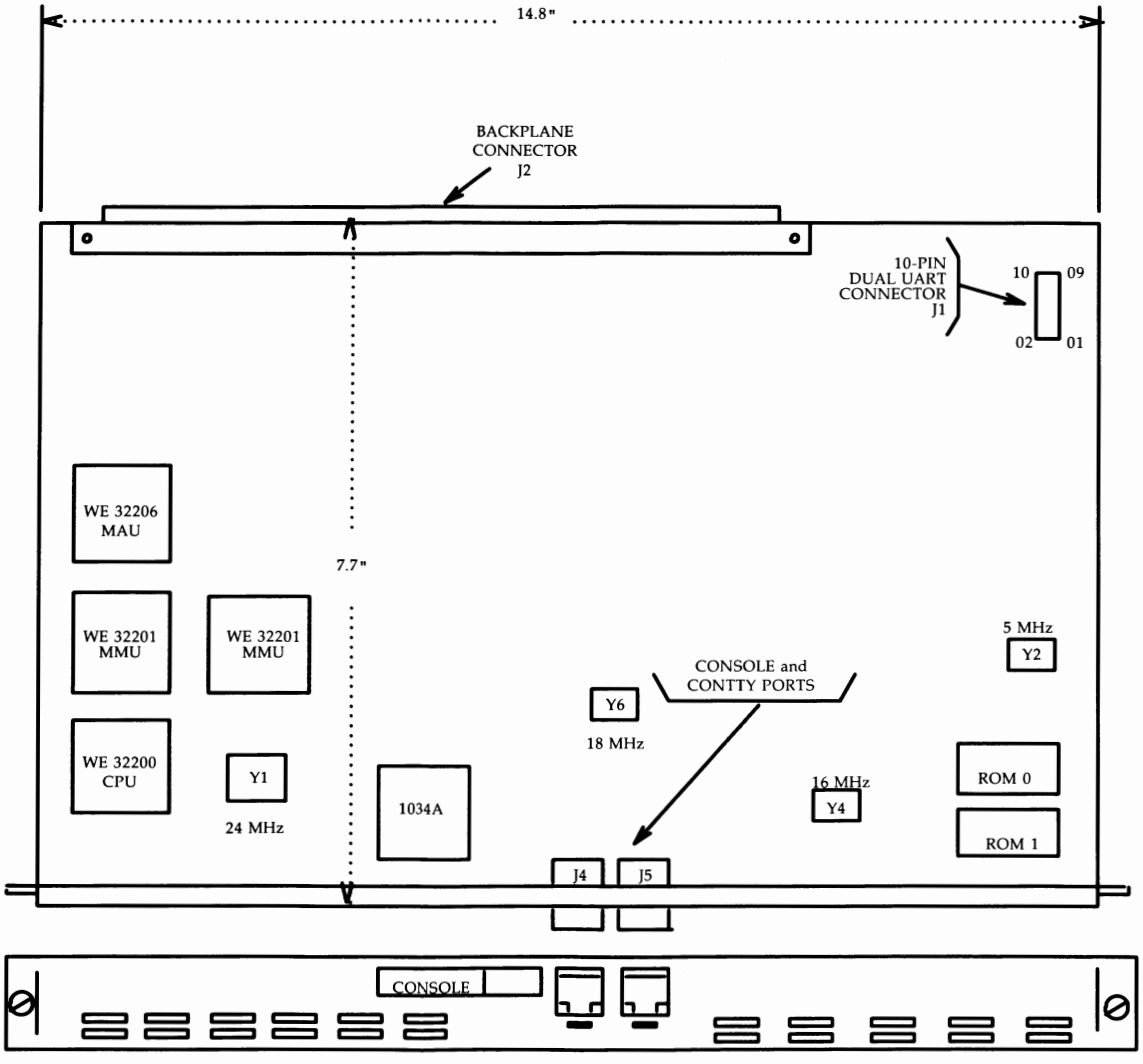


Figure 2-27: CM518C System Board Layout

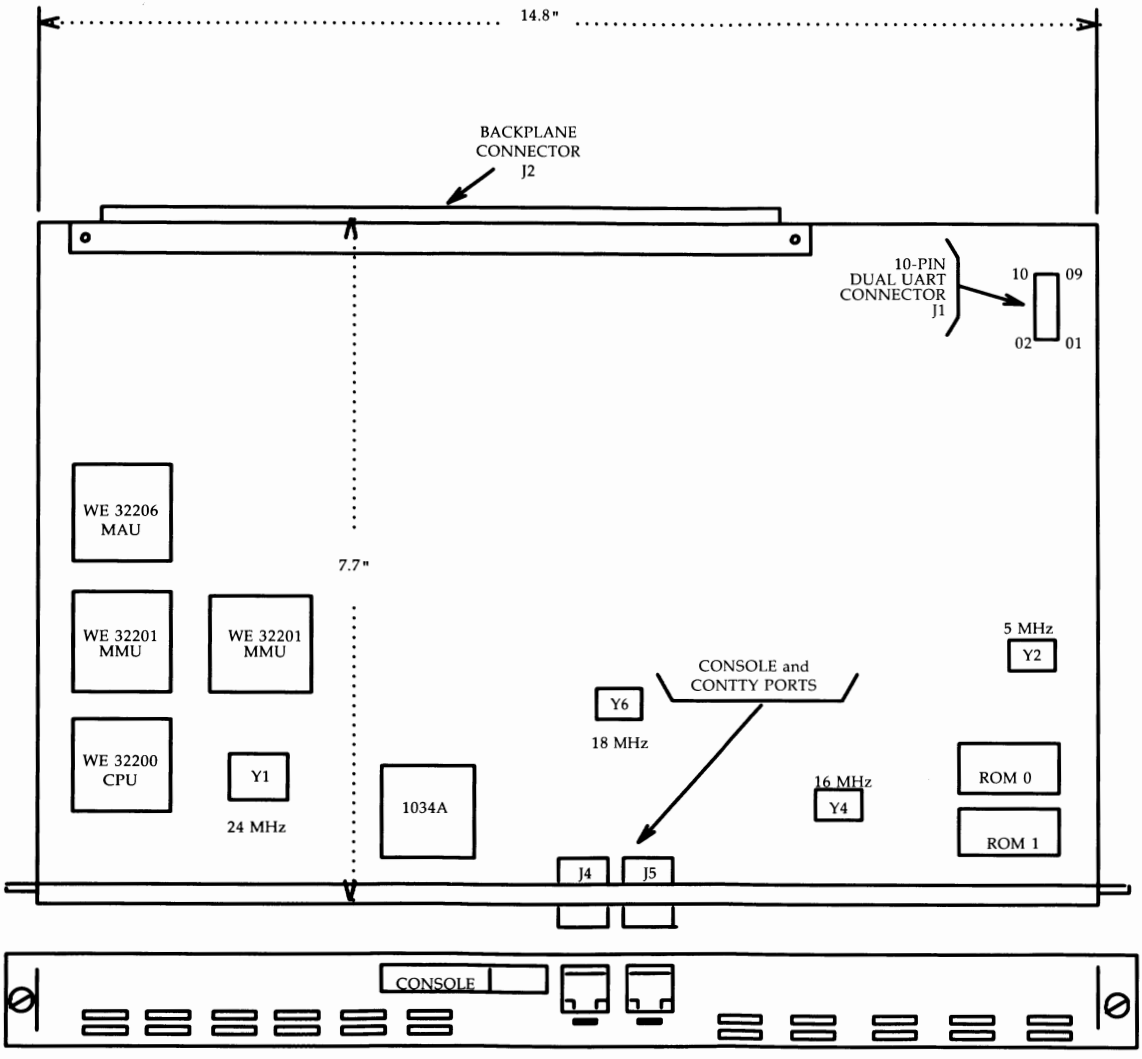


Figure 2-27: CM518C System Board Layout

RANDOM ACCESS MEMORY CARDS

Memory Card Types

The various Random Access Memory (RAM) card types are listed below:

CM191A	0.25-megabyte card (used in 3B2/300 computers, only)
CM191B	1-megabyte card
CM191C	1-megabyte card (half height, surface mounted technology)
CM191D	2-megabyte card (half height, surface mounted technology)
CM192B	2-megabyte card [used in 3B2/400 computers (replaced by CM191D)]
CM523A	4-megabyte card (used in Version 3 computers; 256-kilobyte devices)
CM523AA	4-megabyte card (used in Version 3 computers; 1-megabyte devices)
CM523B	2-megabyte card (used in Version 3 computers)
CM523D	16-megabyte card (used in Version 3 computers).

Each of these cards is described in the following paragraphs. A CM192A Card does not exist. Refer to the *AT&T 3B2 Computer Random Access Memory Expansion Manual,* (Select Code 305-532), for additional information. Card interconnections (pinouts) are defined in Appendix B.

RAM Equipage Considerations

Version 3 computers may be equipped with as much memory as the backplane will allow. However, Version 2 computers have certain considerations that must be followed.

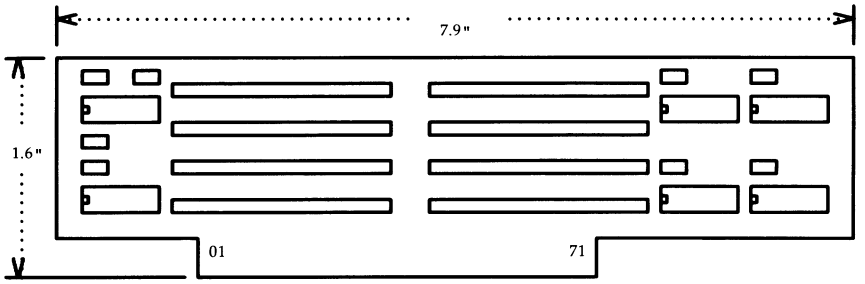
The 1- and 2-megabyte cards can be equipped in the same machine; however, the 2-megabyte card must be in connector M0. Four-slot computers (3B2/300 and 3B2/310) equipped with power supplies having a red ON/STANDBY switch are limited to 2 megabytes of RAM. To expand these machines to 3 or 4 megabytes of RAM requires the replacement of the power supply. Only early production units are equipped with power supply units having a red ON/STANDBY switch. The following table summarizes the equipage of RAM cards in Version 2 computers.

RAM CARD CONFIGURATION SUMMARY

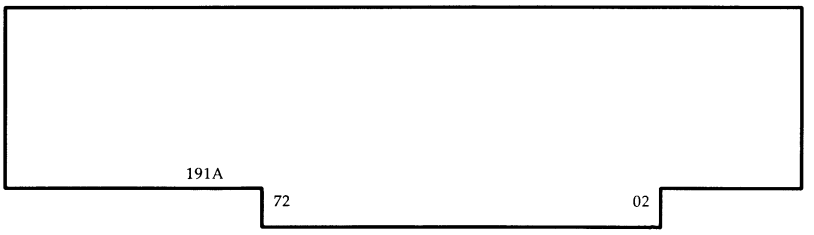
MEMORY SIZE	M0 CONNECTOR	M1 CONNECTOR
0.5 MEGABYTES (3B2/300, only)	0.25-MEGABYTE CARD	0.25-MEGABYTE CARD
1.0 MEGABYTES	1-MEGABYTE CARD	—
2.0 MEGABYTES 2.0 MEGABYTES	1-MEGABYTE CARD 2-MEGABYTE CARD	1-MEGABYTE CARD —
3.0 MEGABYTES	2-MEGABYTE CARD	1-MEGABYTE CARD
4.0 MEGABYTES	2-MEGABYTE CARD	2-MEGABYTE CARD

CM191A 0.25-Megabyte RAM Card

The CM191A 0.25-Megabyte RAM Card is a multilayer board containing eight 64K by 4-bit Dynamic RAM (DRAM) Single Inline Packages (SIPs) (for data), four 64K by 1-bit DRAM chips (for byte parity), and two driver chips. Fourteen bypass capacitors and one resistor network are also on the board. All components are mounted on the front side of the board. Connection to the system board is via a 72-pin edge connector. Card pinout information is provided in Appendix B. The card is 1.6 inches high by 7.9 inches wide. The CM191A is used only in the minimum configuration 3B2/300. Figure 2-28 shows the component layout of the CM191A Card.



A. Front View

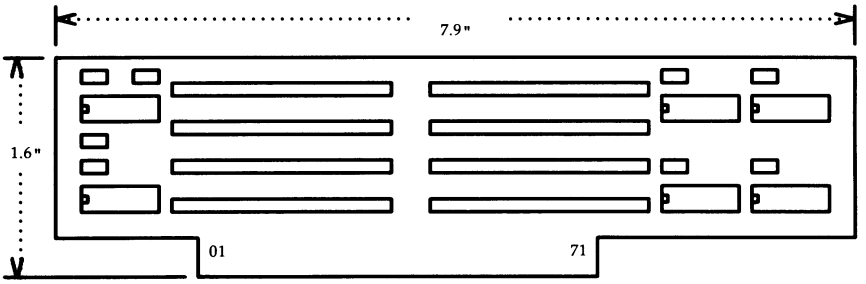


B. Rear View

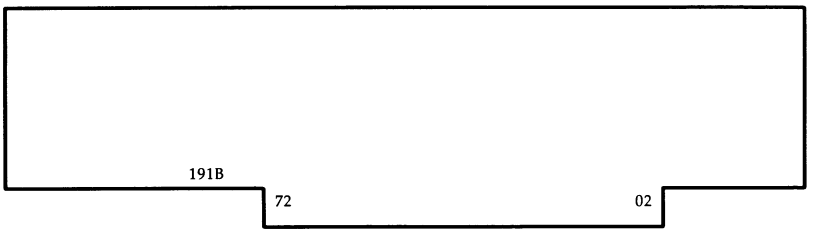
Figure 2-28: CM191A 0.25-Megabyte RAM Card Layout

CM191B 1-Megabyte RAM Card

The CM191B 1-Megabyte RAM Card is a multilayer board containing eight 256K by 4-bit DRAM SIPs (for data), four 256K by 1-bit DRAM chips (for byte parity), and two driver chips. Thirteen bypass capacitors and one resistor network are also on the board. All components are mounted on the front side of the board. Connection to the system board is via a 72-pin edge connector. Card pinout information is provided in Appendix B. The card is 1.6 inches high by 7.9 inches wide. Figure 2-29 shows the component layout of the CM191B Card.



A. Front View

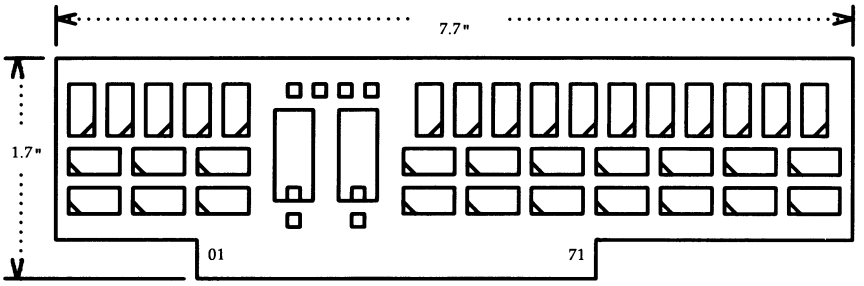


B. Rear View

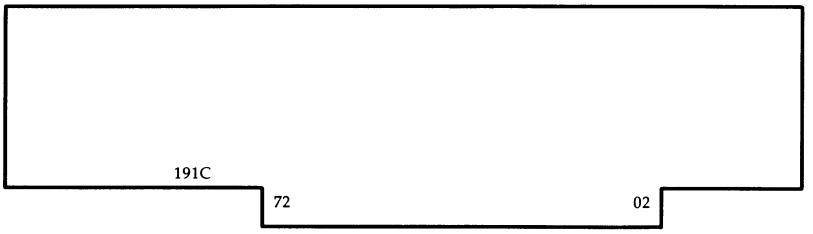
Figure 2-29: CM191B 1-Megabyte RAM Card Layout

CM191C 1-Megabyte RAM Card

The CM191C 1-Megabyte RAM Card uses surface mount technology. The card is a double-sided multilayer board containing 36 surface mounted 256K by 1-bit DRAM chips, 2 surface mount memory drivers, and 4 pull-up resistors. Thirty-eight bypass capacitors are mounted under the DRAMs and memory drivers. The CM191C Card can be used in all models of Version 2 3B2 computers. Connection to the system board is via a 72-pin edge connector. Card pinout information is provided in Appendix B. The card is 1.7 inches high by 7.7 inches wide. Figure 2-30 shows the component layout of the CM191C Card. All components are mounted on the front side of the board.



A. Front View

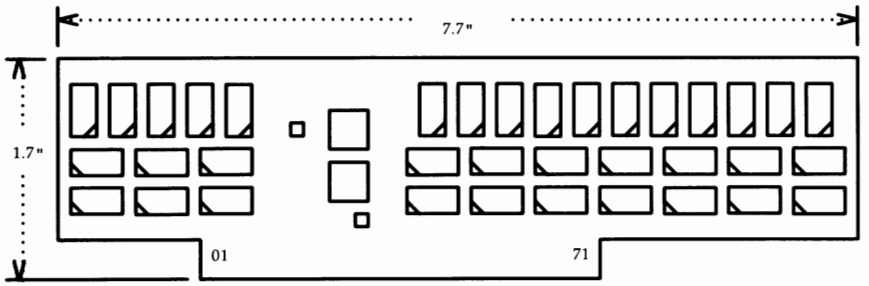


B. Rear View

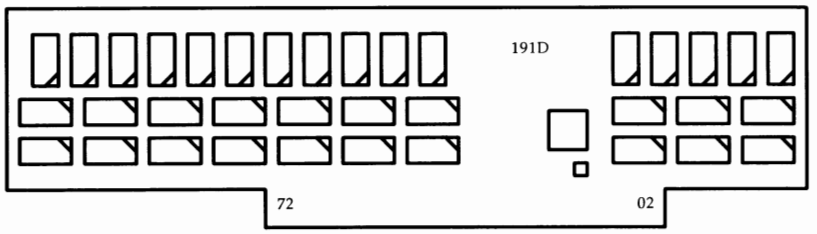
Figure 2-30: CM191C 1-Megabyte, Surface Mounted, RAM Card Layout

CM191D 2-Megabyte RAM Card

The CM191D 2-Megabyte RAM Card uses surface mount technology. The card is a double-sided multilayer board containing 72 surface mounted 256K by 1-bit DRAM chips, 3 surface mount memory drivers, and 8 pull-up resistors. Seventy-five bypass capacitors are mounted under the DRAMs and memory drivers. The CM191D Card can be used in all models of Version 2 3B2 computers. It replaces the CM192B Card used in the 3B2/400 computer. Connection to the system board is via a 72-pin edge connector. Card pinout information is provided in Appendix B. The card is 1.7 inches high by 7.7 inches wide. Figure 2-31 shows the component layout of the CM191D Card.



A. Front View

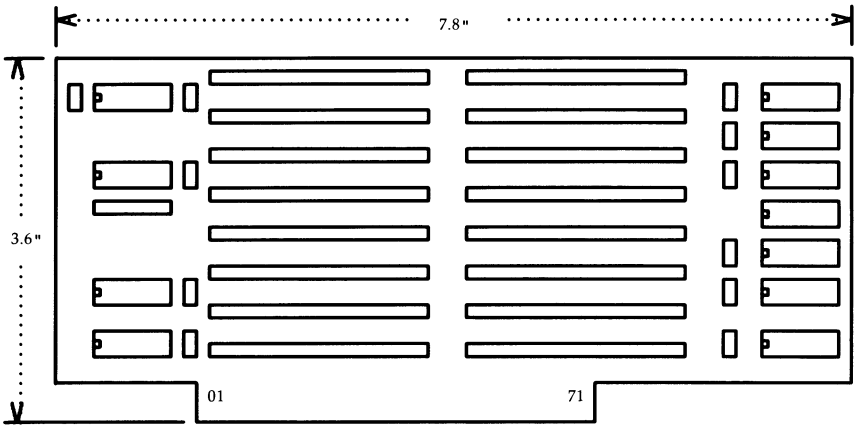


B. Rear View

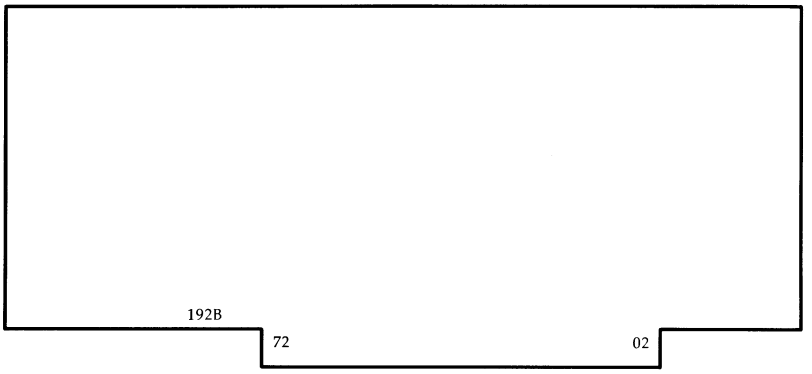
Figure 2-31: CM191D 2-Megabyte, Surface Mounted, RAM Card Layout

CM192B 2-Megabyte RAM Card

The CM191D Card has replaced the CM192B Card. The CM192B 2-Megabyte RAM Card is a multilayer board containing sixteen 256K by 4-bit DRAM chips (for data), eight 256K by 1-bit DRAM chips (for byte parity), and three driver chips. Twenty-six bypass capacitors and one resistor network are also on the board. All components are mounted on the front side of the board. Connection to the system board is via a 72-pin edge connector. Card pinout information is provided in Appendix B. The card is 3.6 inches high by 7.8 inches wide. Because of the size (height) of the card, the CM192B Card can only be used in the 3B2/400 computer. Figure 2-32 shows the component layout of the CM192B Card.



A. Front View

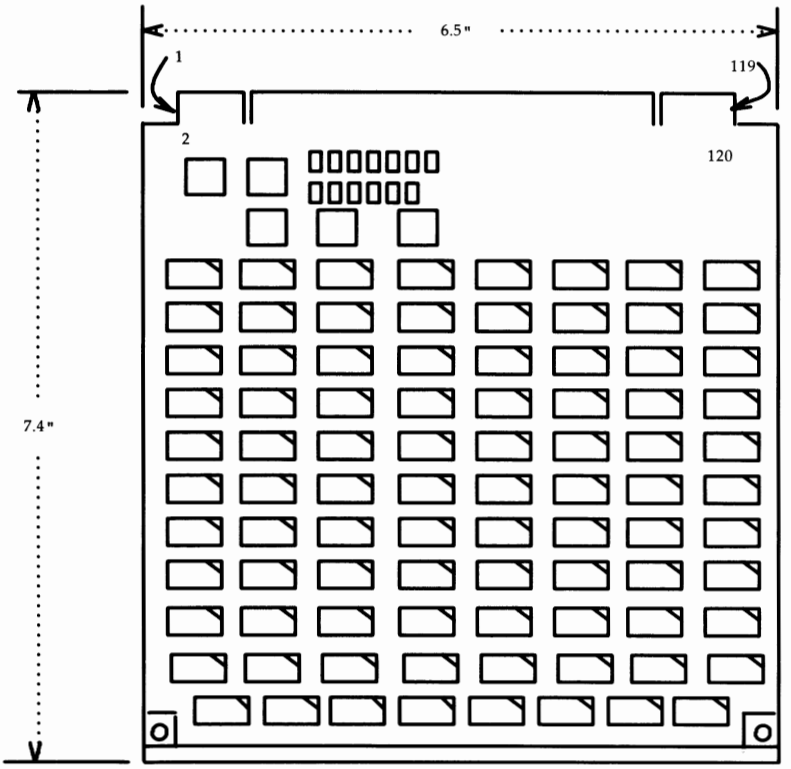


B. Rear View

Figure 2-32: CM192B 2-Megabyte RAM Card Layout

CM523A 4-Megabyte RAM Card

The CM523A 4-Megabyte RAM Card uses surface mount technology. The card is a double-sided (components on both sides) multilayer board containing 176 surface mounted 256K by 1-bit DRAM chips [including 48 chips for storing Error Correction Code (ECC) information] and 9 surface mount memory drivers. Seventy-six bypass capacitors are mounted near the DRAM and memory drivers. The CM523A Card can be used in all models of Version 3 3B2 computers. Connection to the system board is via a 120-pin connector on the backplane. Card pinout information is provided in Appendix B. The card is 6.5 inches wide by 7.4 inches deep. Figure 2-33 shows the component layout of the CM523A Card.



Conventional Component Side (Top)
(Bottom Side also has Memory Chips)

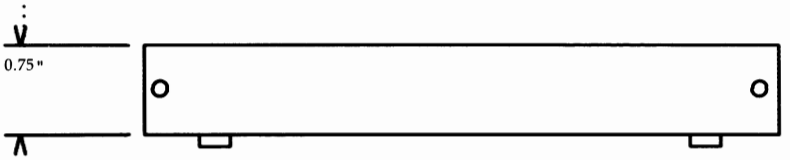
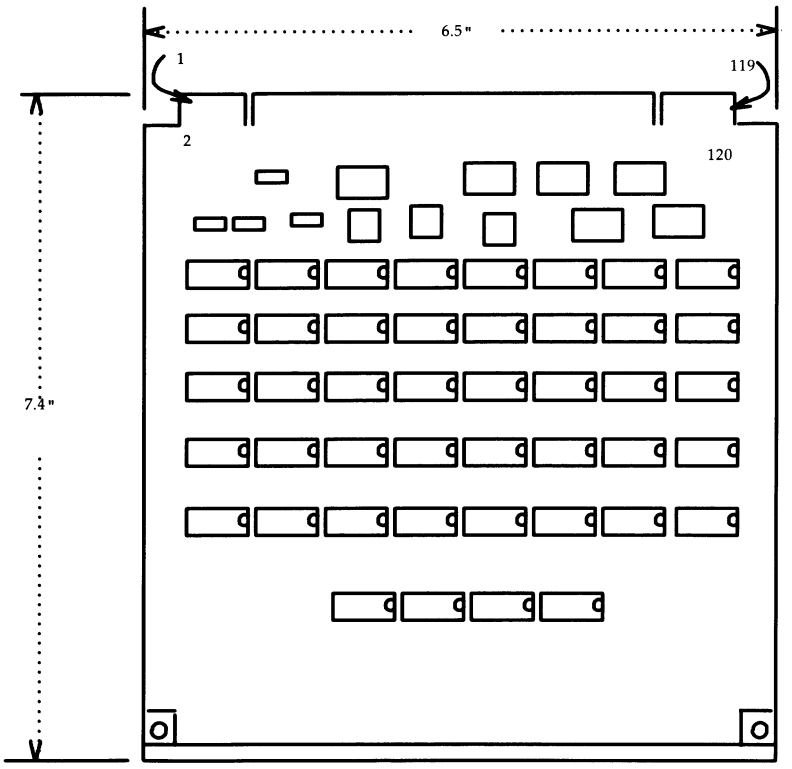


Figure 2-33: CM523A 4-Megabyte, Surface Mounted, RAM Card Layout

CM523AA 4-Megabyte RAM Card

The CM523AA 4-Megabyte RAM Card uses surface mount technology. The card is a multilayer board containing 44 surface mounted 1024K (1 M) by 1-bit DRAM chips (including 12 for storing ECC information) and 3 surface mount memory drivers. Twenty-two bypass capacitors are mounted near the DRAM and memory drivers. The CM523AA Card can be used in all models of Version 3 3B2 computers. Connection to the system board is via a 120-pin connector on the backplane. Card pinout information is provided in Appendix B. The card is 6.5 inches wide by 7.4 inches deep. Figure 2-34 shows the component layout of the CM523AA Card.



Conventional Component Side

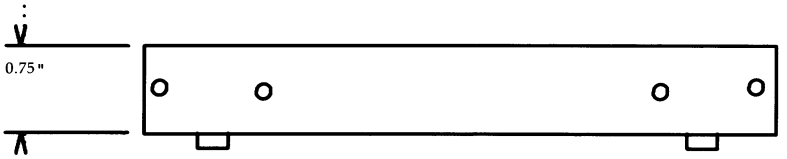
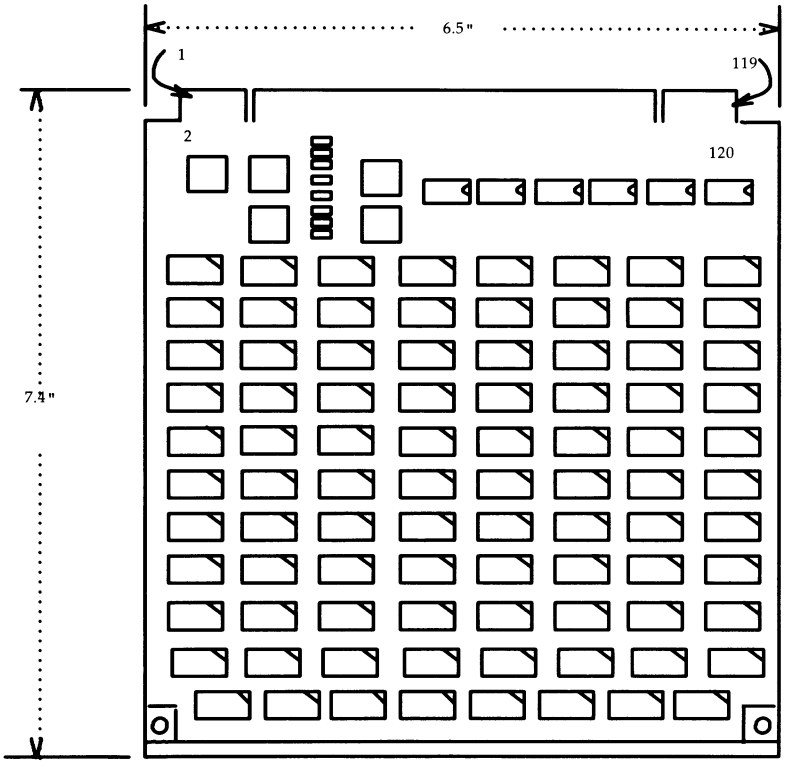


Figure 2-34: CM523AA 4-Megabyte, Surface Mounted, RAM Card Layout

CM523B 2-Megabyte RAM Card

The CM523B 2-Megabyte RAM Card uses surface mount technology. The card is a multilayer board containing 88 surface mounted 256K by 1-bit DRAM chips (which includes 24 chips for storing ECC information) and 5 surface mount memory drivers. Forty-two bypass capacitors are mounted near the DRAM and memory drivers. The CM523B Card can be used in all models of Version 3 3B2 computers. Connection to the system board is via a 120-pin connector on the backplane. Card pinout information is provided in Appendix B. The card is 6.5 inches wide by 7.4 inches deep. Figure 2-35 shows the component layout of the CM523A Card.



Conventional Component Side

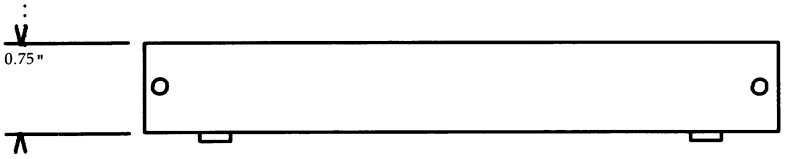
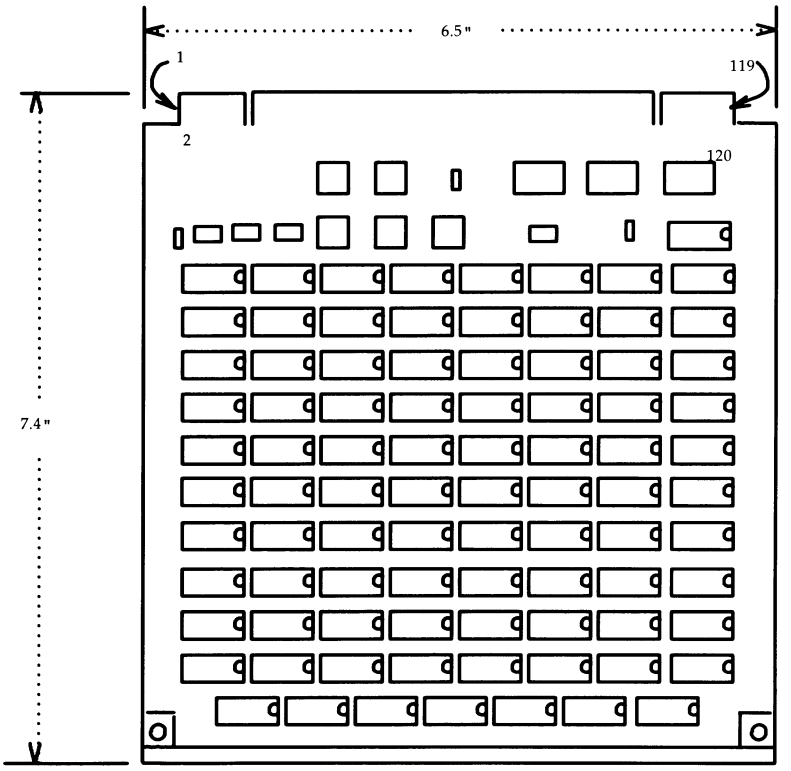


Figure 2-35: CM523B 2-Megabyte, Surface Mounted, RAM Card Layout

CM523D 16-Megabyte RAM Card

The CM523D 16-Megabyte RAM Card uses surface mount technology. The card is a double-sided multilayer board containing 176 surface mounted 1024K (1 M) by 1-bit DRAM chips including 48 for storing ECC information) and 9 surface mount memory drivers. Seventy-six bypass capacitors are mounted near the DRAM and memory drivers. The CM523D Card can be used in all models of Version 3 3B2 computers. Connection to the system board is via a 120-pin connector on the backplane. Card pinout information is provided in Appendix B. The card is 6.5 inches wide by 7.4 inches deep. Figure 2-36 shows the component layout of the CM523D Card.



Conventional Component Side (Top)
(Bottom Side also has Memory Chips)

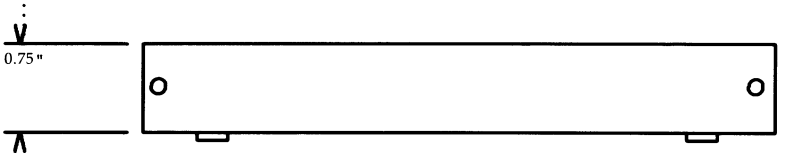


Figure 2-36: CM523D 16-Megabyte, Surface Mounted, RAM Card Layout

BACKPLANE BOARDS

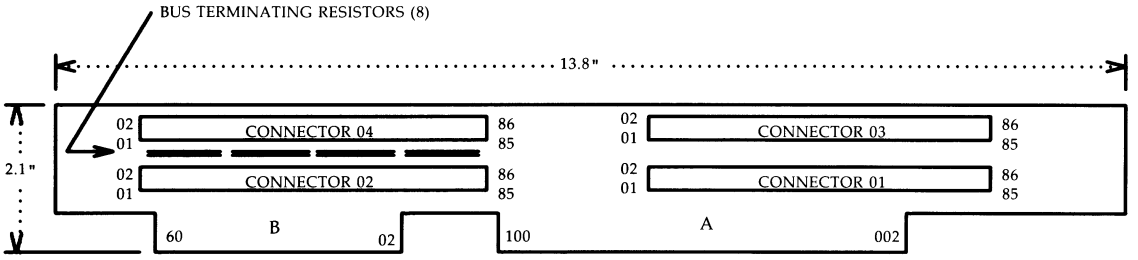
Backplane Types

The backplane board provides feature card power and signal connections. The backplane board contains resistor networks to terminate the address, data, and status signals. Because of bus termination, the backplane and the system board must always be connected for the system to be operated.

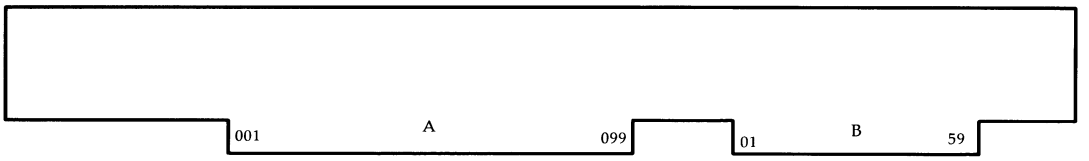
There are five types of backplane boards. Some have 4 slots (CM193A/B), some have 12 slots (CM194B and CM520A), and some have 24 slots plus the system board slot (CM519A and CM519B).

CM193A/B, 3B2/300/310 Computer Backplane Board

The CM193A/B is a 4-slot backplane board. The backplane board plugs into the 100-pin (A or J02) and 60-pin (B or J03) Input/Output (I/O) expansion connectors on the system board. A maximum of either 2 double-width or 4 single-width feature cards can be plugged into this backplane. Figure 2-37 shows the component layout of the CM193A/B Backplane. The board is a multilayer board measuring 2.1 inches high and 13.8 inches wide. Card and connector pinout information is provided in Appendix B.



A. Front View

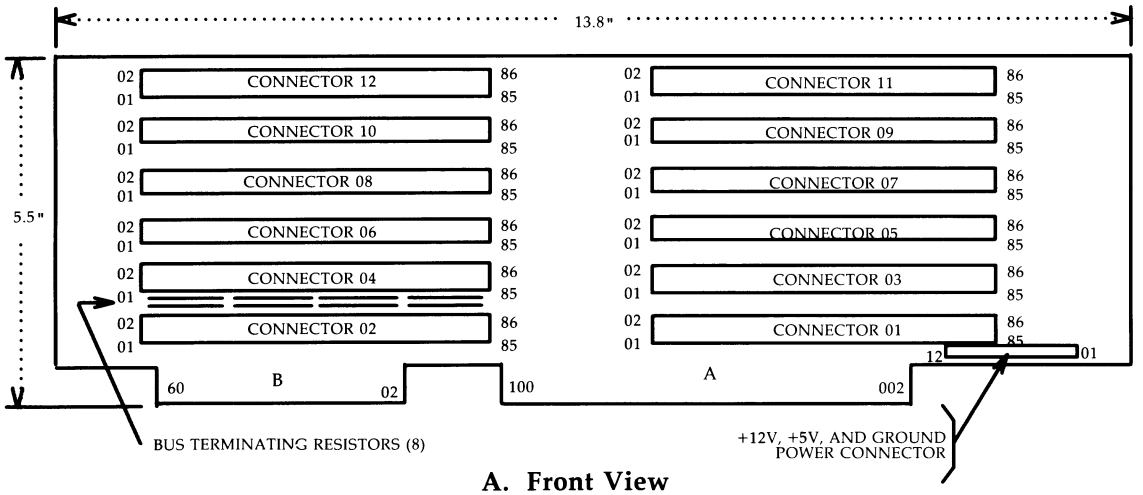


B. Rear View

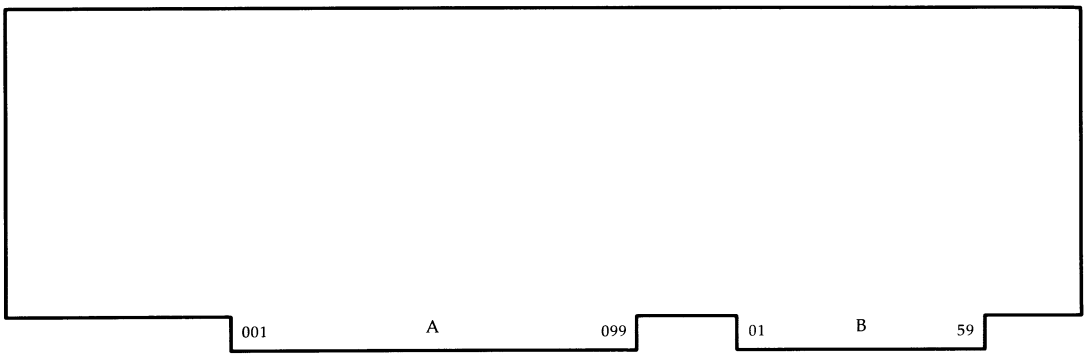
Figure 2-37: CM193A/B Backplane Board Layout

CM194B, 3B2/400 Computer Backplane Board

The CM194B is a 12-slot backplane board. The backplane board plugs into the 100-pin (A or J02) and 60-pin (B or J03) I/O expansion connectors on the system board. A maximum of either 6 double-wide or 12 single-width feature cards can be plugged into this backplane. Figure 2-38 shows the component layout of the CM194B Backplane. The board is a multilayer board measuring 5.5 inches high and 13.8 inches wide. Card and connector pinout information is provided in Appendix B.



A. Front View



B. Rear View

Figure 2-38: CM194B Backplane Board Layout

CM519A Backplane Board Layout

The CM519A is a 24-slot (plus system board slot) backplane board. The backplane board is connected to the card cage assembly. The system board plugs into the middle of the backplane board. There are 12 I/O slots above the system board to hold a maximum of either 6 double-width or 12 single-width feature cards. There are 12 performance slots underneath the system board for cards that improve the performance of the computer. Figure 2-39 shows the component layout of the CM519A Backplane. The board is a multilayer board measuring 11.3 inches high and 13.0 inches wide. Card and connector pinout information is provided in Appendix B.

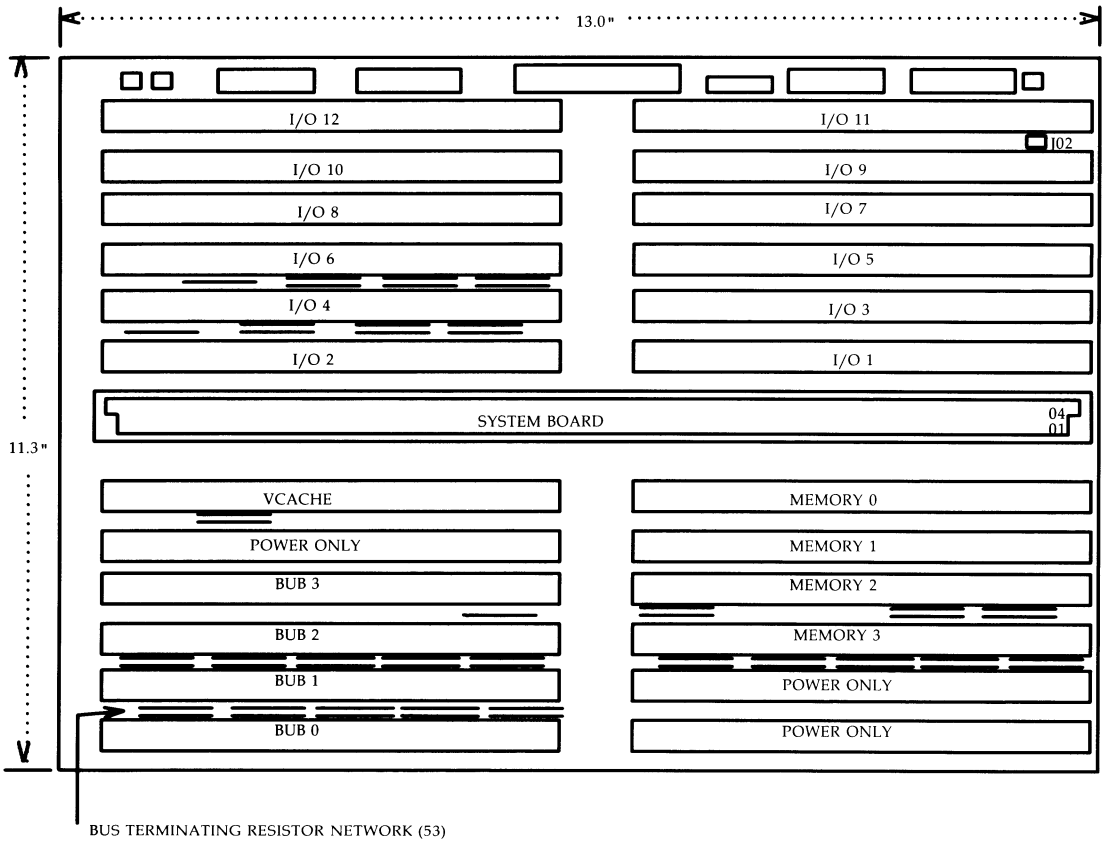


Figure 2-39: CM519A Backplane Board Layout

CM519B Backplane Board Layout

The CM519B is a 24-slot (plus system board slot) backplane board. The backplane board is connected to the card cage assembly. The system board plugs into the middle of the backplane board. There are 12 I/O slots above the system board to hold a maximum of either 6 double-width or 12 single-width feature cards. There are 12 performance slots underneath the system board for cards that improve the performance of the computer. Figure 2-40 shows the component layout of the CM519B Backplane. The board is a multilayer board measuring 11.3 inches high and 13.0 inches wide. Card and connector pinout information is provided in Appendix B.

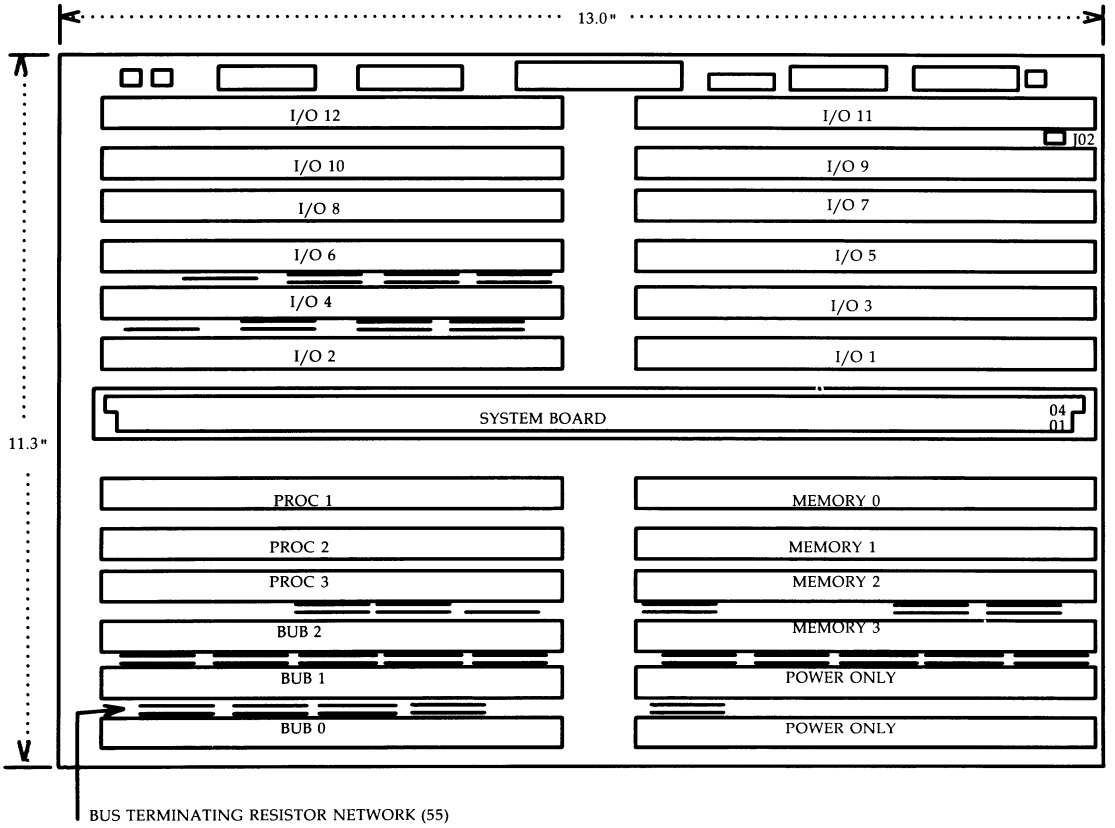


Figure 2-40: CM519B Backplane Board Layout

CM520A Backplane Board Layout

The CM520A is a 12-slot (plus system board slot) backplane board. The backplane board is connected to the card cage assembly. The system board plugs into the backplane board. A maximum of either 3 double-width or 7 single-width I/O feature cards can be plugged into this backplane. It also has five performance slots (two of which are memory card slots). Figure 2-41 shows the component layout of the CM520A Backplane. The board is a multilayer board measuring 6.5 inches high and 13.0 inches wide. Card and connector pinout information is provided in Appendix B.

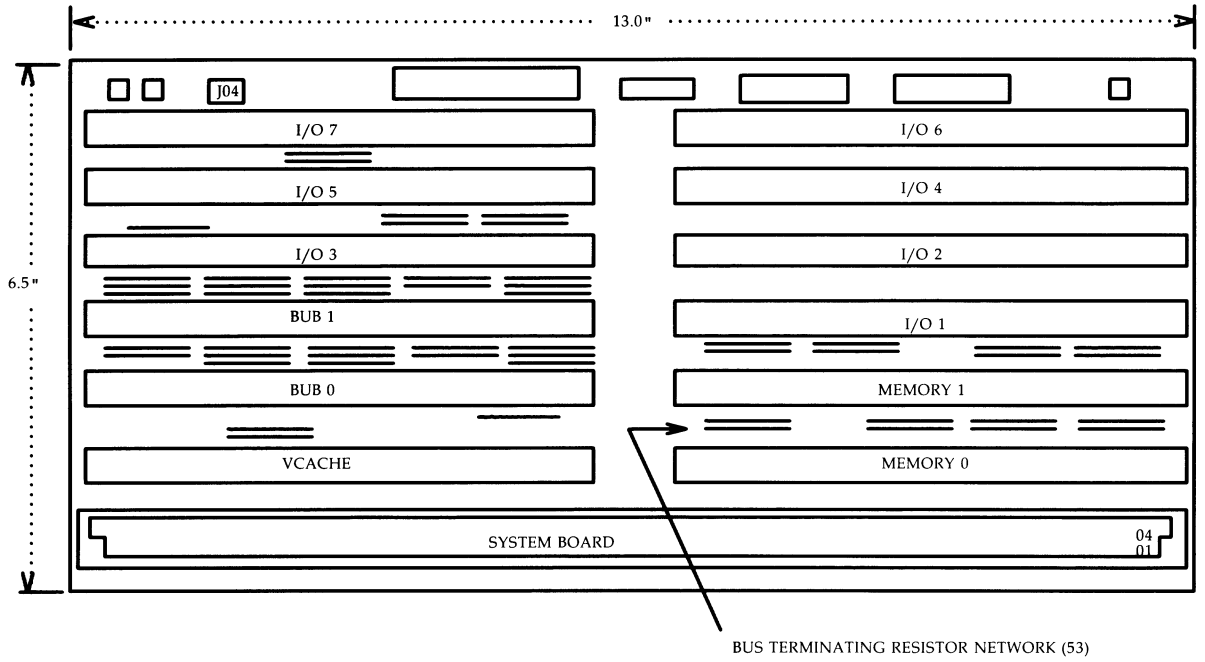


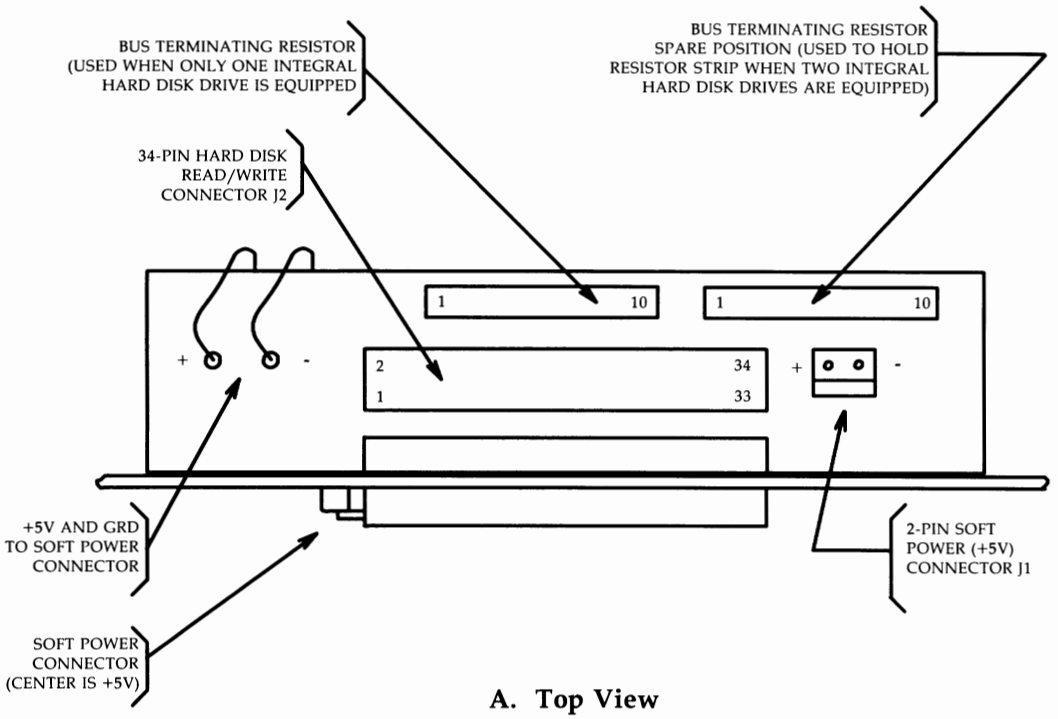
Figure 2-41: CM520A Backplane Board Layout

AUXILIARY DISK INTERFACE (ED-4C632-30)

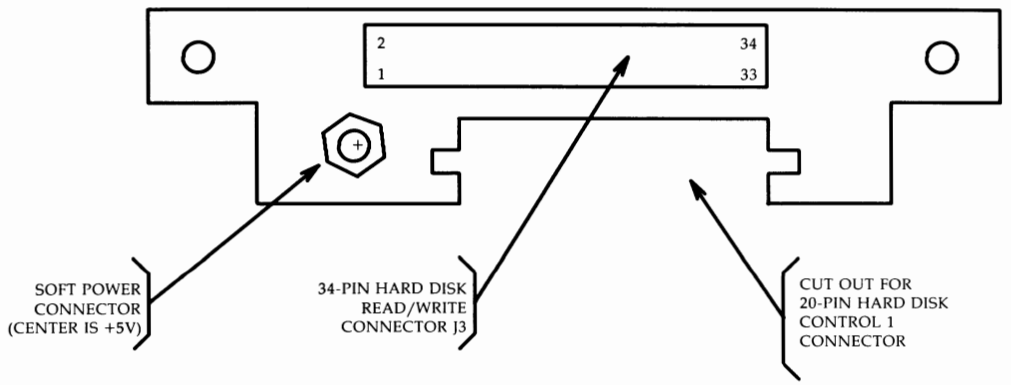
The Auxiliary Disk Interface, ED-4C632-30, is used to connect a second integral hard disk drive to a 3B2/300 or 3B2/310 computer. The second integral disk drive is equipped in an AT&T Expansion Module (AT&T/XM). The second disk drive is driven from the integral hard disk controller on the system board and is therefore called an integral hard disk drive regardless of where it is physically equipped. The Auxiliary Disk Interface also provides soft power control connections for use when an AT&T/XM is connected to the computer.

Figure 2-42 shows the layout of the Auxiliary Disk Interface. The Auxiliary Disk Interface provides connection for the 34-pin control bus cable that is multipled from connector J07 on the System Board, ED-4C637-30, to each hard disk drive. When only one hard disk drive is equipped, control bus termination is done at the Auxiliary Disk Interface. When two integral hard disk drives are equipped, the control bus terminating resistor is installed in the spare 10-pin socket on the Auxiliary Disk Interface.

The VCC (+5 V DC) used for soft power control connects to the Auxiliary Disk Interface from either the Auxiliary Disk Interface Soft Power Connector J14 when a System Board, ED-4C637-30 is used or from the hard disk drive control bus terminating resistor integrated circuit socket when a CM190A System Board is used. Connector pinout information is provided in Appendix B.



A. Top View

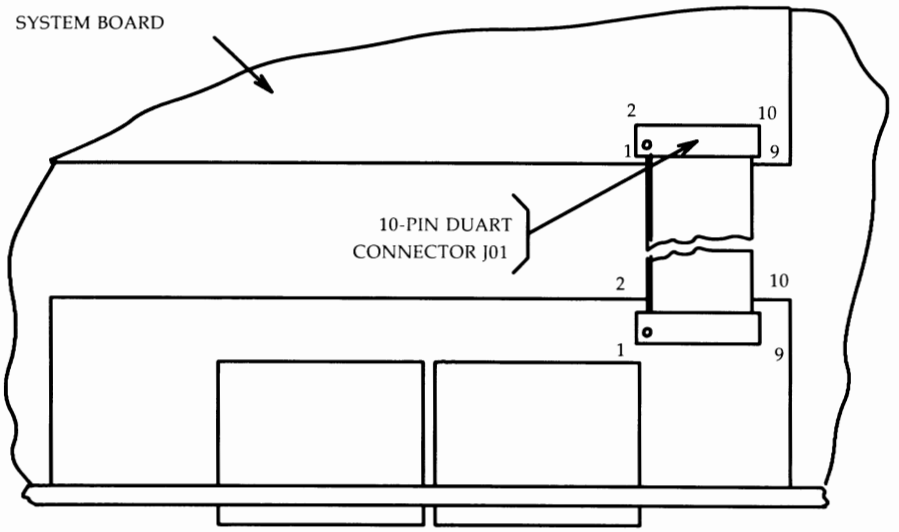


B. Front View (Back of Computer)

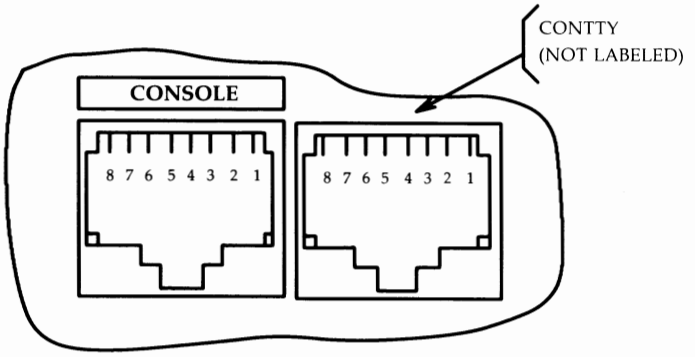
Figure 2-42: Auxiliary Disk Interface, ED-4C632-30, Layout

DUART CONNECTOR-2 INTERFACE (ED-4C492-35,G5 and ED-4C631-35,G2)

The DUART Connector-2 Interface provides the CONSOLE and CONTTY 8-pin modular jacks that connect to the 10-pin DUART system board header J01. Connector pinout information is provided in Appendix B. The 3B2/300 and 3B2/310 computers are equipped with ED-4C492-35,G5. The 3B2/400 computer is equipped with ED-4C631-35,G2. Figure 2-43 shows the DUART Connector-2 Interface layout.



A. Top View



B. Front View (Back of Computer)

Figure 2-43: DUART Connector-2 Interface, ED-4C492-30,G5 (3B2/300/310) and ED-4C631-35,G2 (3B2/400) Layout

CM195A NETWORK INTERFACE CARD

The CM195A Network Interface (NI) Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. The CM195A Card is used to connect the 3B2 computer to an AT&T 3BNET Local Area Network (3BNET LAN). Connection is via a 14-conductor drop cable to a transceiver unit in the media cable of the network. Power for the transceiver is supplied from the 3B2 computer.

The 3BNET LAN is an Ethernet compatible network operating at 10 megabits per second using the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) algorithm. Figure 2-44 shows the component layout of a typical CM195A NI Card. CM195A Card connector pinout information is provided in Appendix B. The major components of the CM195A Card are listed below:

- An INTEL* 80186 Microprocessor
- 32K bytes of Dynamic Random Access Memory (DRAM)
- 16K bytes of Read Only Memory (ROM)
- An INTEL 82586 Ethernet Controller.

* Registered trademark of Intel Corp.

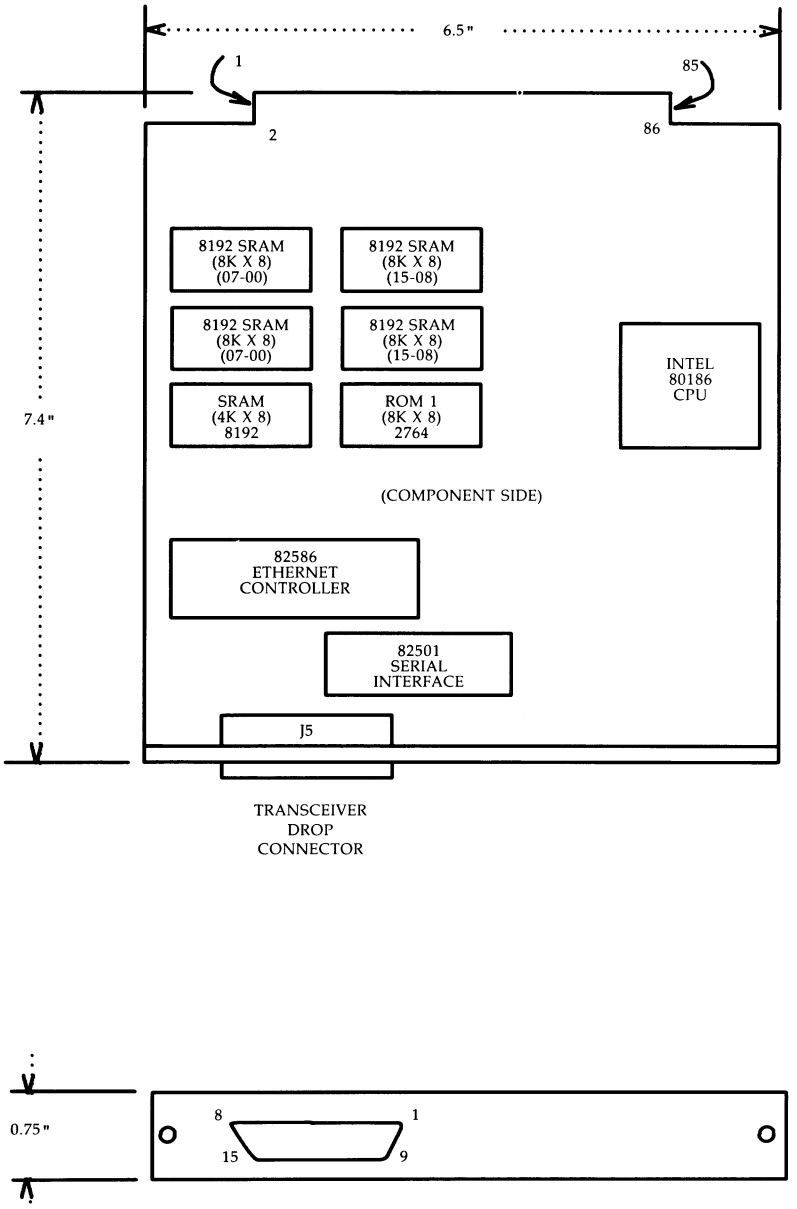


Figure 2-44: CM195A NI Card Layout

CM195AA ALARM INTERFACE CIRCUIT CARD

The CM195AA Alarm Interface Circuit (AIC) Card is part of the Remote Management Package feature for the 3B2 computer. The CM195AA Card has three 8-pin modular jacks and four 4-pin modular jacks that provide the physical connections to perform administrative and maintenance operations from a remote location.

The CM195AA Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. Figure 2-45 shows the component layout of a typical CM195AA AIC Card. CM195AA Card connector pinout information is provided in Appendix B. The major functions of the CM195AA Card are listed below:

- Add dual console capabilities
- Detect system sanity failures and generate alarms
- Provide alarm capability via interface to automatic calling units.

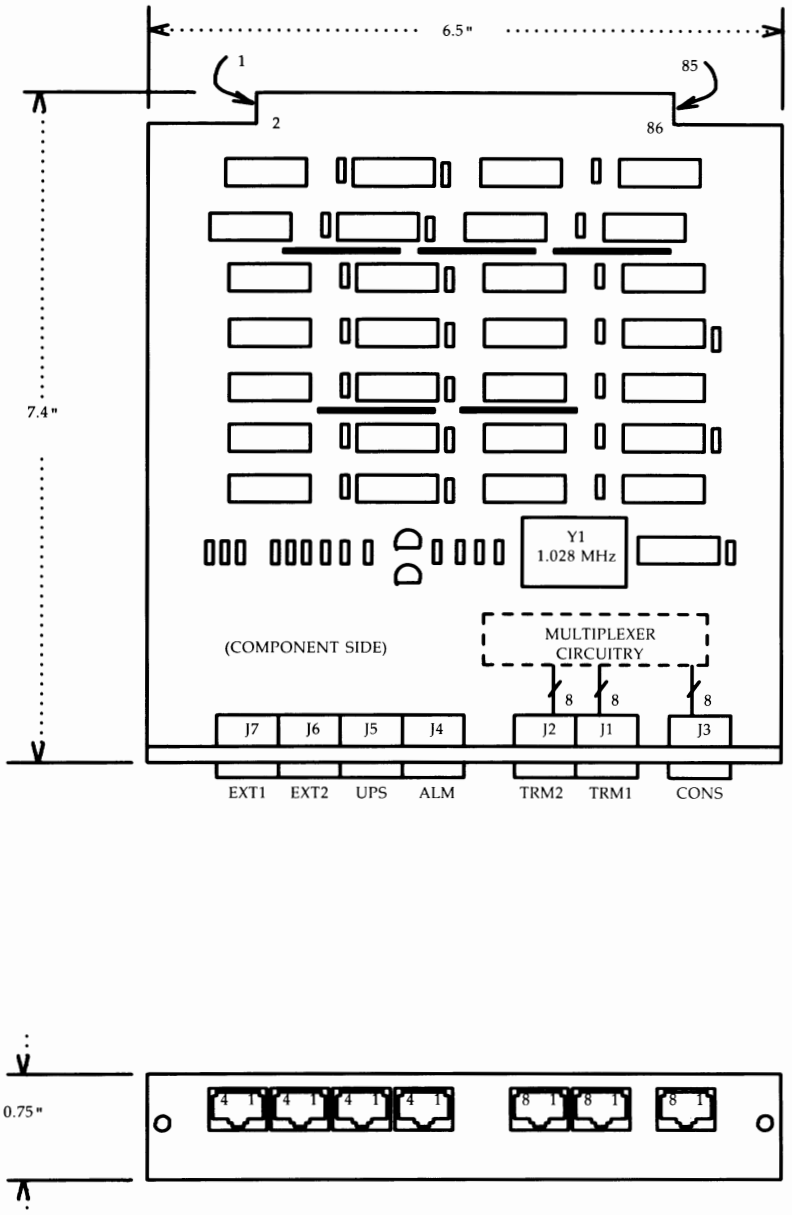


Figure 2-45: CM195AA AIC Layout

CM195AC/CM195AD "DATAKIT" VCS INTERFACE CARD

The Datakit® Virtual Circuit Switch (VCS) Interface Card consists of two piggy-backed circuit cards that plug into the backplane of the computer. The cards allow data to transmit over a fiber optic link at 230K bits per second to either a Datakit VCS or Information Systems Network (ISN) switch. When coupled with the software, this add-on provides remote login, remote execution, transfer of files and directories, and support of over 250 channels on the fiber link.

The piggy-backed circuit cards are single-width cards measuring 6.5 inches wide by 7.4 inches deep. Figure 2-46 shows the component layout of typical CM195AC and CM195AD Datakit VCS Interface Cards. The connector pinout information is provided in Appendix B. The major components of the CM195AC/CM195AD Cards are listed below:

- An INTEL 80186 Microprocessor
- 256K bytes of Static Random Access Memory (SRAM)
- Synchronous and Asynchronous Data Transfer Logic
- Timers and clock circuitry.

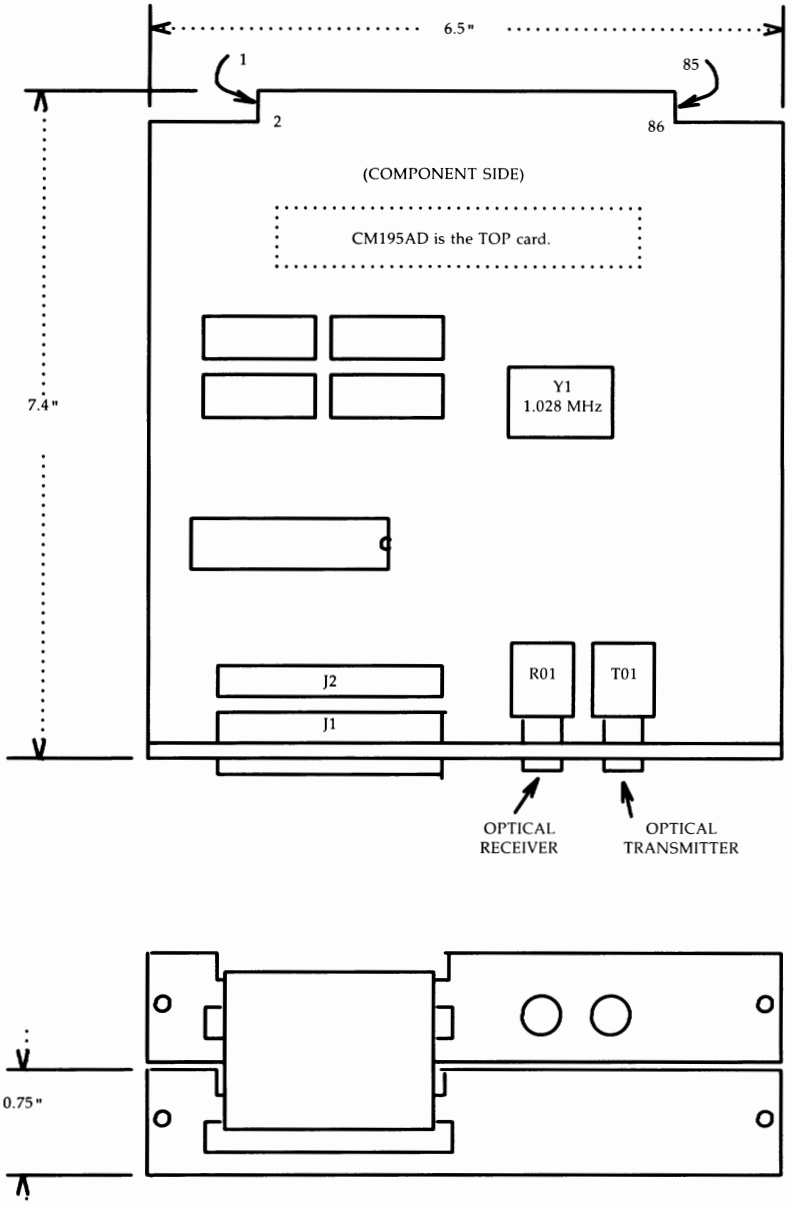


Figure 2-46: CM195AC/CM195AD Datakit VCS Interface Card Layout

CM195AE GPSC CARD PACKAGE

The CM195AE General Purpose Synchronous Controller (GPSC) Card provides two physical interfaces for synchronous data transmission. The card is capable of providing simultaneous full-duplex, full-occupancy data transmission at rates up to 64K bits per second. The connectors contain the required signals to support a variety of industry standard electrical interfaces.

Figure 2-47 shows the component layout of a typical CM195AE GPSC Card. The circuit card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. The connector pinout information is provided in Appendix B. The major components of the CM195AE Card are listed below:

- An INTEL 80186 Microprocessor
- Bus interface circuitry
- 768K bytes of Dynamic Random Access Memory (DRAM)
- Up to 32K bytes of Erasable Programmable Read Only Memory (EPROM)
- Dual Port Arbiter/Controller and Support Logic.

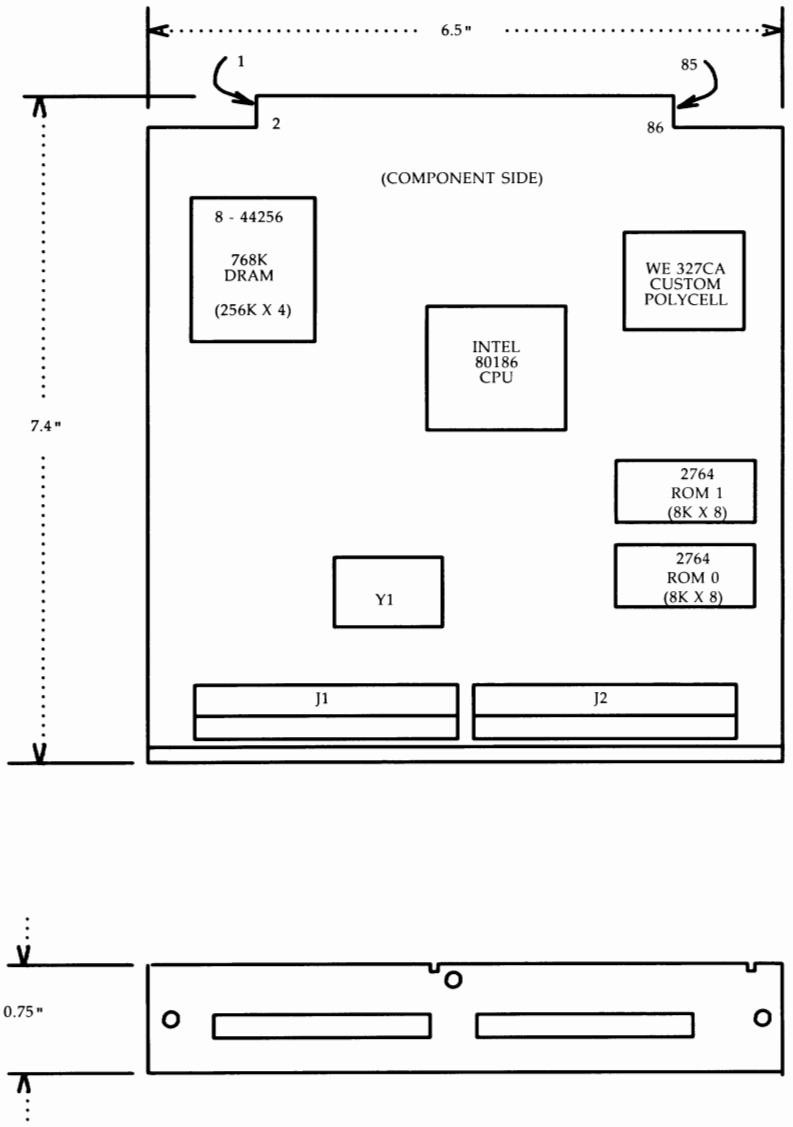


Figure 2-47: CM195AE GPSC Card Layout

CM195AY EPORTS CARD

The CM195AY Enhanced Peripheral Port Controller (EPORTS) Card provides eight separate asynchronous serial ports (RS-232C input/output interfaces). The maximum throughput of the card is 38,400 bits per second.

The high performance capability of the CM195AY EPORTS Card is available only when an accompanying EPORTS software is installed.

The CM195AY Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. The card uses surface mounted technology. Figure 2-48 shows the component layout of a typical CM195AY EPORTS Card. Connector pinout information is provided in Appendix B. The major components of the CM195AY Card are listed below:

- An INTEL 80186 Microprocessor
- 128K bytes of Dynamic Random Access Memory (DRAM)
- 16K bytes of Erasable Programmable Read Only Memory (EPROM)
- Four Dual Universal Asynchronous Receiver/Transmitter (DUART) chips.

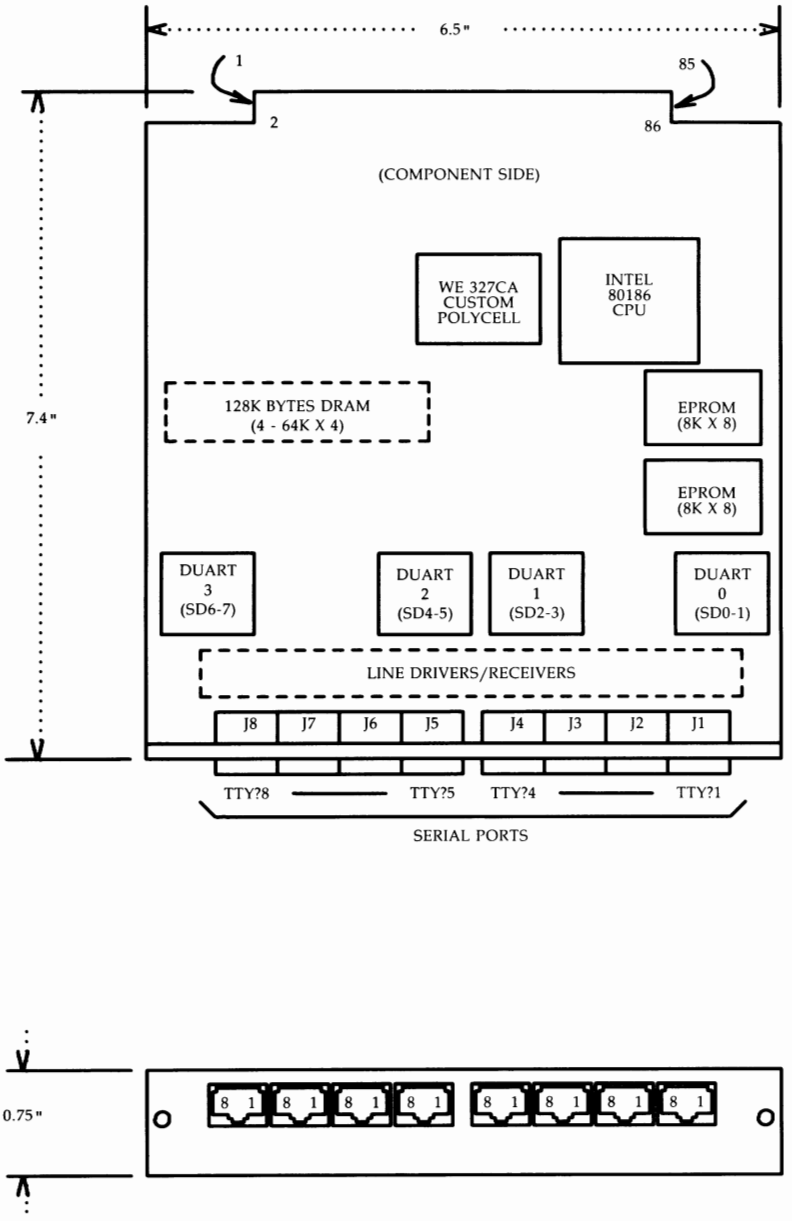


Figure 2-48: CM195AY EPORTS Card Layout

CM195B PORTS CARD

The CM195B Peripheral Port Controller (PPC) Card (also known as PORTS card) provides four separate asynchronous serial ports (RS-232C) and one parallel (CENTRONICS*) port input/output interfaces. The maximum throughput of the card is 19,200 bits per second.

A high performance version of the PORTS card (CM195B-7) is available to support certain applications. The CM195B-7 Card is stamped "HPP." The high performance capability of this card is available only when an accompanying High Performance Expanded Input/Output Utilities Package is installed. Without the accompanying software, an HPP PORTS card functions as a conventional CM195B PORTS Card.

The CM195B Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. Figure 2-49 shows the component layout of an early production CM195B PORTS Card. Figure 2-50 shows the component layout of a typical CM195B-7 PORTS Card. Connector pinout information is provided in Appendix B. The major components of the CM195B Card are listed below:

- An INTEL 80186 Microprocessor
- 32K bytes of Static Random Access Memory (SRAM)
- 16K bytes of Read Only Memory (ROM)
- Two SIGNETICS 2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) chips.

* Registered trademark of Centronics Data Computer Corp.

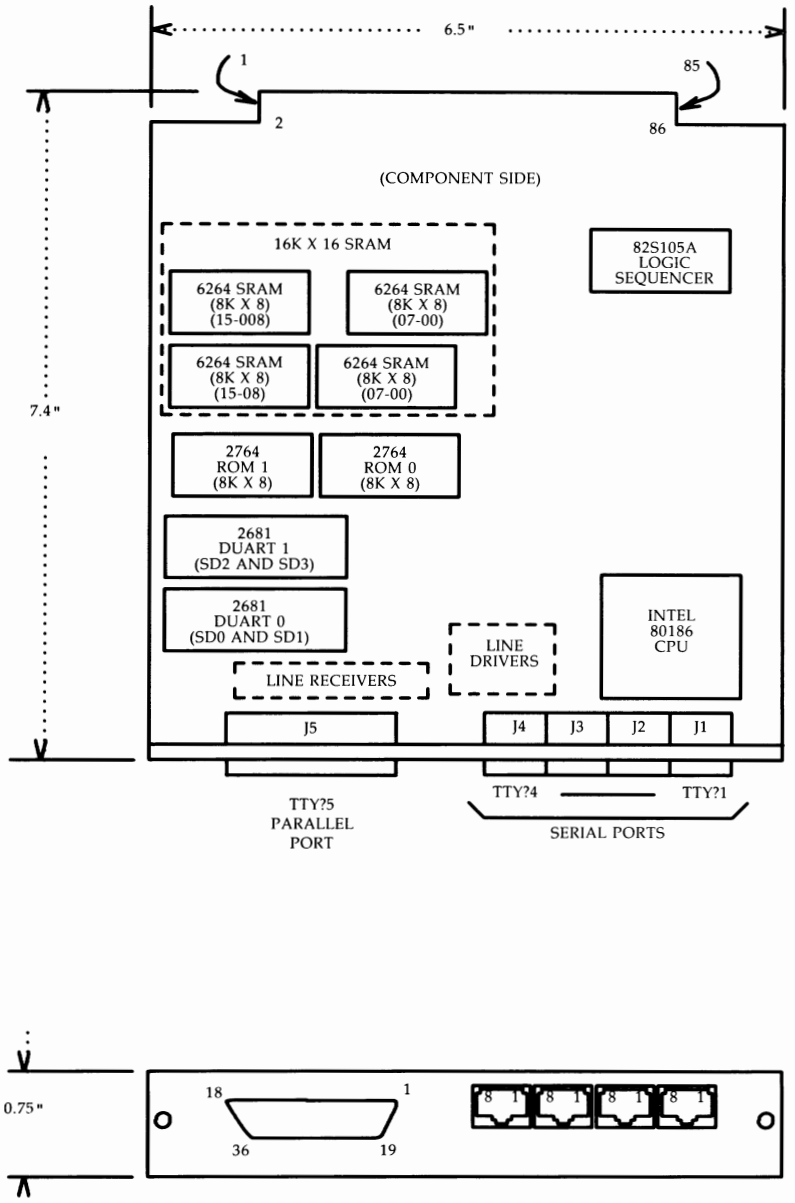


Figure 2-49: CM195B PORTS Card Layout (Early Production)

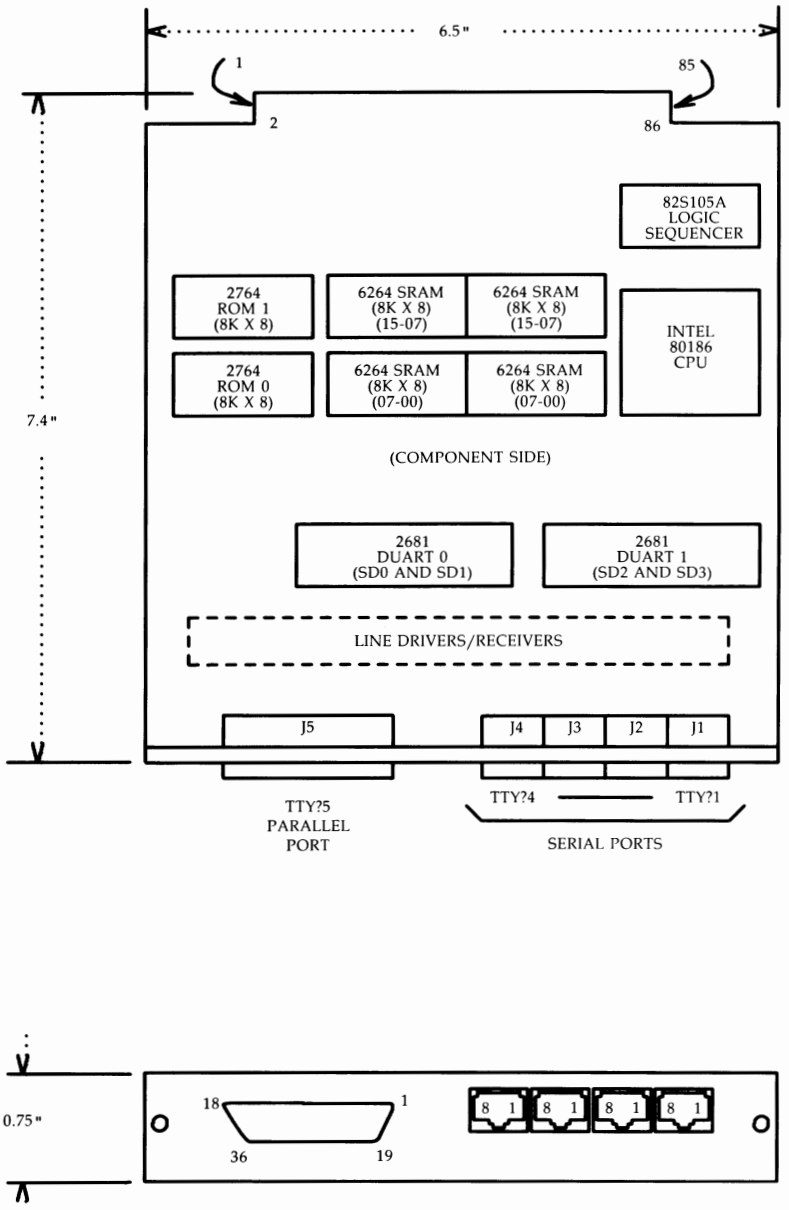


Figure 2-50: CM195B-7 PORTS Card Layout

CM195BA PORTS CARD

The CM195BA Card replaces the CM195B-7 Card. The CM195BA Peripheral Port Controller (PPC) Card (also known as PORTS card) provides four separate asynchronous serial ports (RS-232C) and one parallel (CENTRONICS) port input/output interfaces. The maximum throughput of the card is 19,200 bits per second.

The high performance capability of the CM195BA PORTS Card is available only when an accompanying High Performance Expanded Input/Output Utilities Package is installed. Without the accompanying software, the CM195BA PORTS Card functions as a CM195B PORTS Card.

The CM195BA Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. Figure 2-51 shows the component layout of a typical CM195BA PORTS Card. Connector pinout information is provided in Appendix B. The major components of the CM195BA Card are listed below:

- An INTEL 80186 Microprocessor
- 32K bytes of Static Random Access Memory (SRAM)
- 16K bytes of Read Only Memory (ROM)
- Two Dual Universal Asynchronous Receiver/Transmitter (DUART) chips.

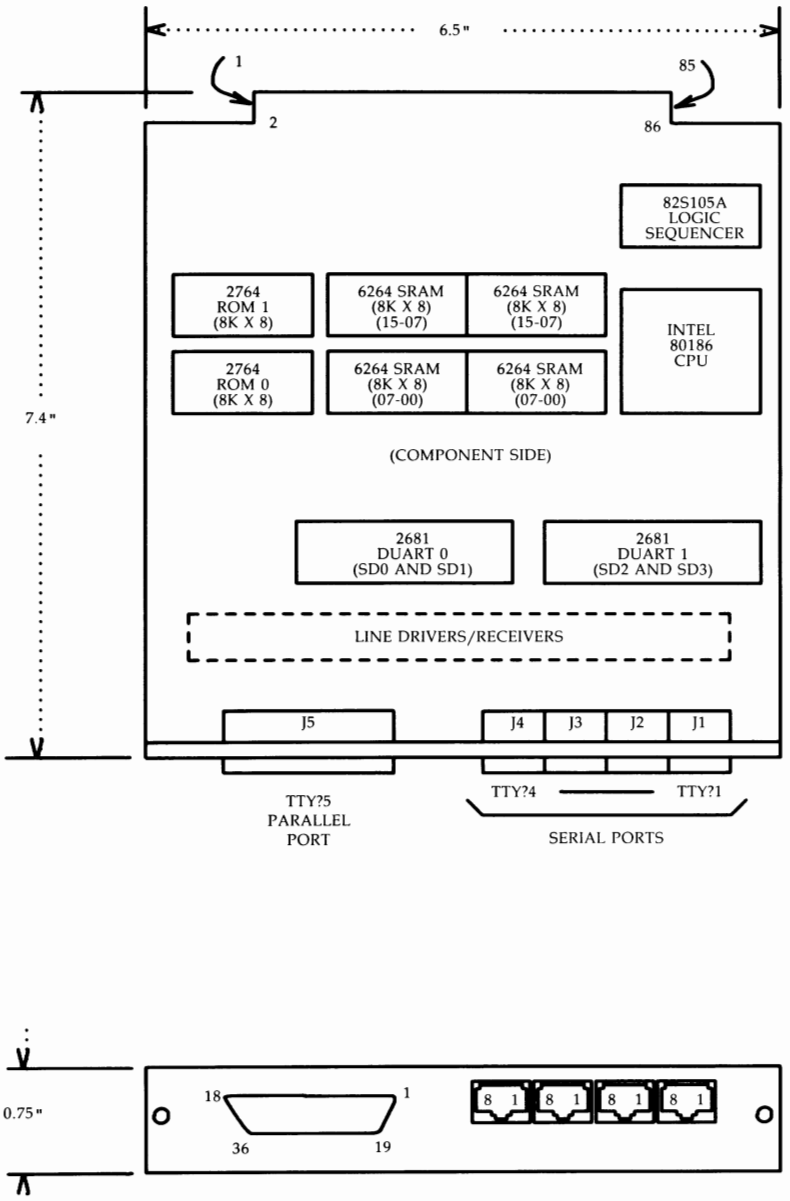


Figure 2-51: CM195BA PORTS Card Layout

CM195H CARTRIDGE TAPE CONTROLLER CARD

The CM195H Cartridge Tape Controller (CTC) Card is a single-width card used to interface one floppy disk drive and/or one cartridge tape drive to a 3B2 computer. The CTC is a single controller that serves two devices. Simultaneous device access of the two devices connected to the same CTC card is NOT possible. The CTC card is equipped in a 3B2 computer feature card slot. The external devices drives are typically equipped in an AT&T Expansion Module (AT&T/XM) cabinet. A cartridge tape drive can be mounted in an AT&T Expansion Module cabinet or by itself in a Tape Module cabinet. For a 3B2/400 computer, the first cartridge tape controller is equipped in slot 2.

The CM195H Card is a multilayer board measuring 6.5 inches wide by 7.4 inches deep. Figure 2-52 shows the component layout of a typical CM195H CTC Card. The major components of the CM195H Card are listed below:

- An INTEL 80186 Microprocessor
- 128K bytes of Dynamic Random Access Memory (DRAM)
- 16K bytes of Read Only Memory (ROM)
- A WD2793 Floppy Disk Formatter/Controller
- An AM9517A Direct Memory Access Controller (DMAC).

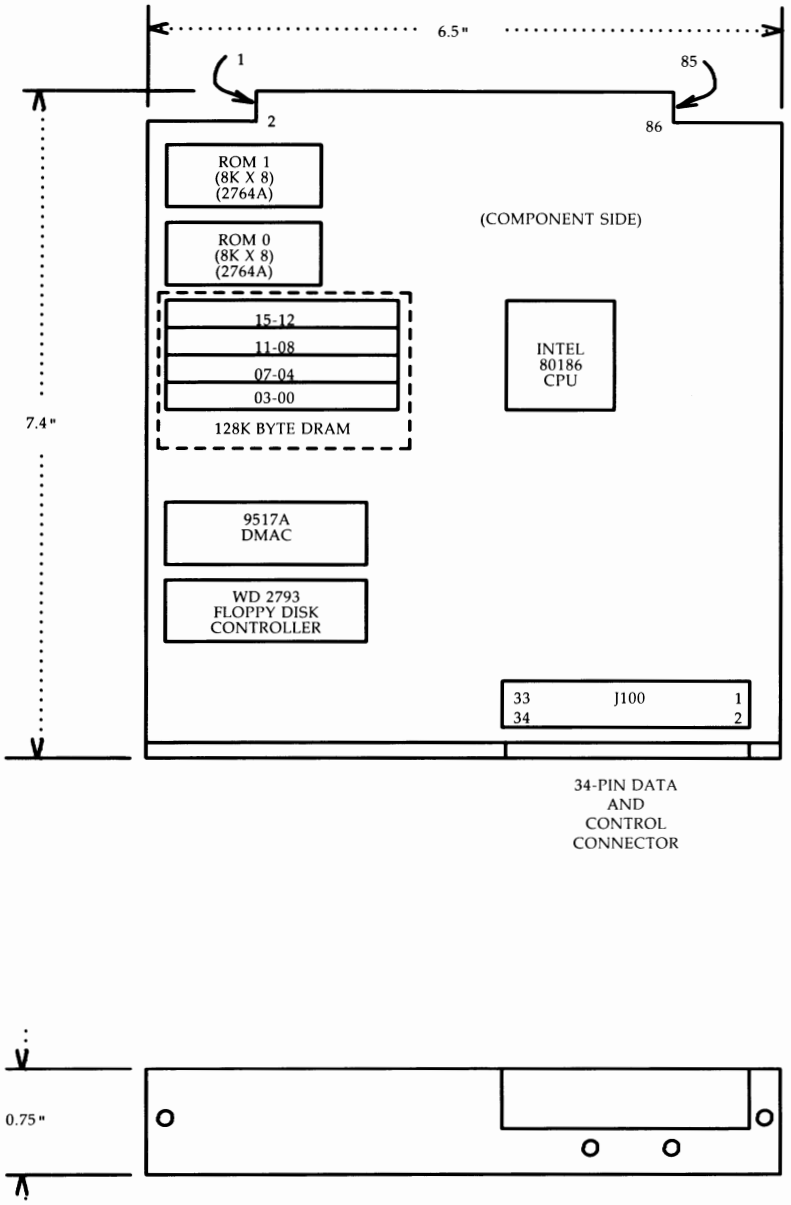


Figure 2-52: CM195H CTC Card Layout

CM195K EXPANSION DISK CONTROLLER CARD

The CM195K Expansion Disk Controller (XDC) Card is a single-width card used to interface a maximum of two external hard disk drives per card to a 3B2 computer. The hard disk interface is an ST-506 type. The XDC card is equipped in a 3B2 computer feature card slot. The external hard disk drives are equipped in an AT&T Expansion Module (AT&T/XM) cabinet. A maximum of two CM195K Cards can be equipped in the 3B2/300 and 3B2/310 computer. A maximum of four CM195K Cards can be equipped in a 3B2/400 computer. Multiple CM195K Cards are used to expand the ST-506 type hard disk storage capacity of a 3B2 computer to the following:

3B2/300 or 3B2/310	Maximum of 432 megabytes
3B2/400	Maximum of 720 megabytes

These maximum values include the integral hard disk drives.

The CM195K Card is a multilayer board measuring 6.5 inches wide and 7.4 inches deep. Connector pinout information is provided in Appendix B. Figure 2-53 shows the component layout of a typical CM195K XDC Card. The major components of the CM195AK Card are listed below:

- An INTEL 80186 Microprocessor
- 128K bytes of Dynamic Random Access Memory (DRAM)
- 16K or 32K bytes of Read Only Memory (ROM)
- An NEC 7261 Hard Disk Controller.

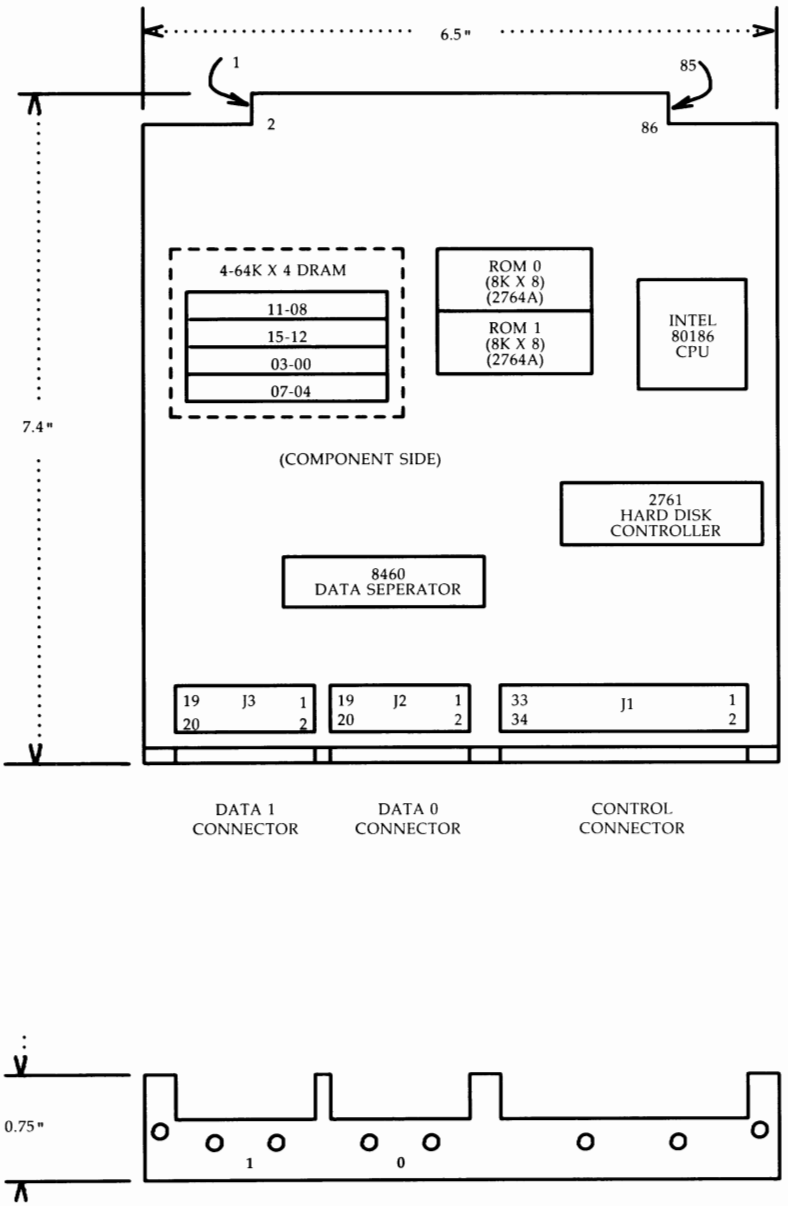


Figure 2-53: CM195K XDC Card Layout

CM195T INTELLIGENT SERIAL CONTROLLER CARD

The CM195T Intelligent Serial Controller (ISC) Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. The ISC provides for the connection of two serial ports. The CM195T Card is a general purpose, synchronous communications peripheral interface card providing a two channel, full duplex, synchronous interface. The ISC card supports both synchronous and asynchronous peripheral device operation. The ISC supports multiple applications depending on the software executing in the ISC Random Access Memory (RAM). The ISC can provide communication over synchronous channels such as Systems Network Architecture/Synchronous Data Link Control (SNA/SDLC), bi-sync, and X.25 as a function of the appropriate software being loaded on the ISC card.

The communications interface cabling provides two DB-25 male connectors. Both of these connections are RS-232C, Data Terminal Equipment (DTE) connections. Connector pinout information is provided in Appendix B. Figure 2-54 shows the component layout of a typical CM195T ISC Card. The major components of the CM195T Card are listed below:

- An INTEL 80186 Microprocessor
- 128K bytes of Dynamic Random Access Memory (DRAM)
- 16K or 32K bytes of Read Only Memory (ROM)
- An INTEL 8237 Direct Memory Access Controller (DMAC)
- An INTEL 8274 Universal Synchronous/Asynchronous Receiver/Transmitter (USART).

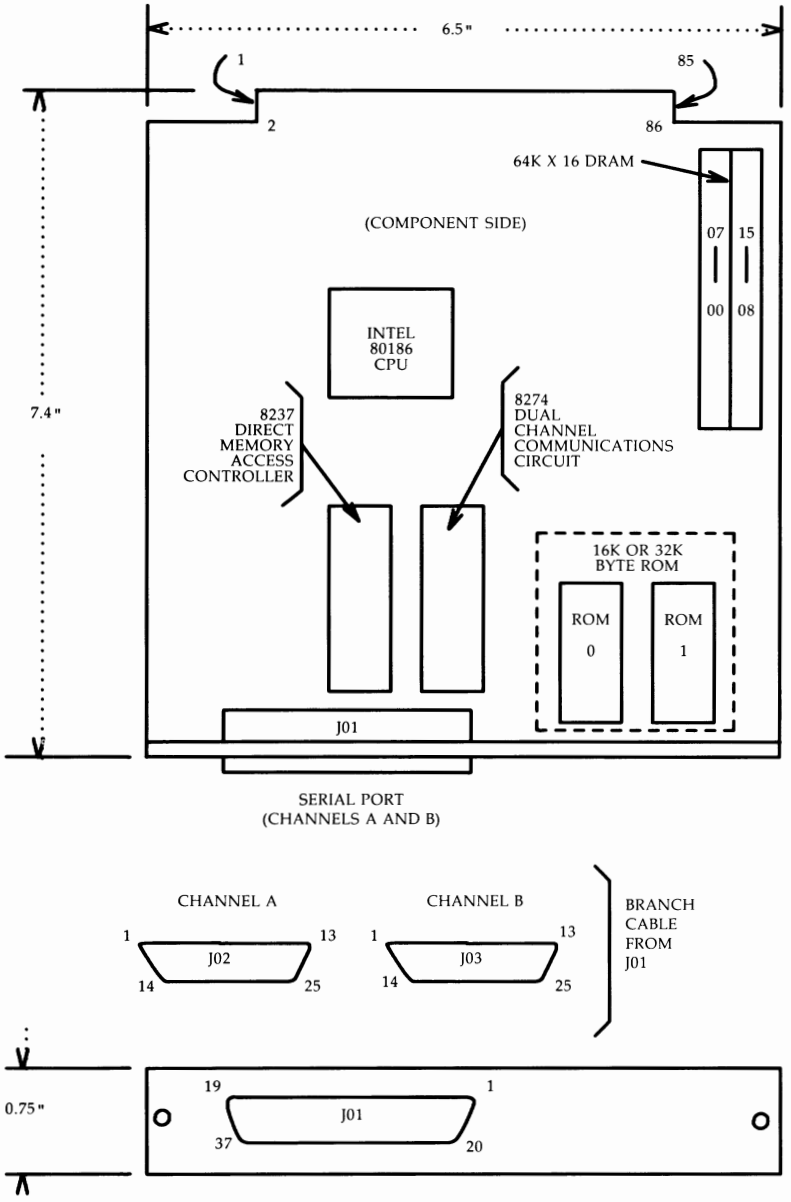


Figure 2-54: CM195T ISC Card Layout

CM195U STARLAN INTERFACE CARD

The AT&T STARLAN network is a low-cost, local area network for linking MS-DOS and UNIX system-based computers. STARLAN runs at 1 megabit per second on twisted pair wiring. The wiring is based on AT&T's Premises Distribution System (PDS). The lowest level protocols conform to the IEEE 802.3 standard for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) local area networking. The high-level protocols support applications written for Microsoft Networks.

Connection to STARLAN from a 3B2 computer is provided by a CM195U STARLAN Interface Card that plugs into a 3B2 computer feature card slot. This card is called a Network Access Unit (NAU) in terms of STARLAN.

The CM195U Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. Figure 2-55 shows the component layout of a typical CM195U STARLAN Interface Card. Connector pinout information is provided in Appendix B. The major components of the CM195U Card are listed below:

- An INTEL 80186 Microprocessor
- 16K bytes of Read Only Memory (ROM)
- 32K bytes of Static Random Access Memory (SRAM)
- An INTEL 82586 Ethernet Controller (also called a Local Area Network Coprocessor).

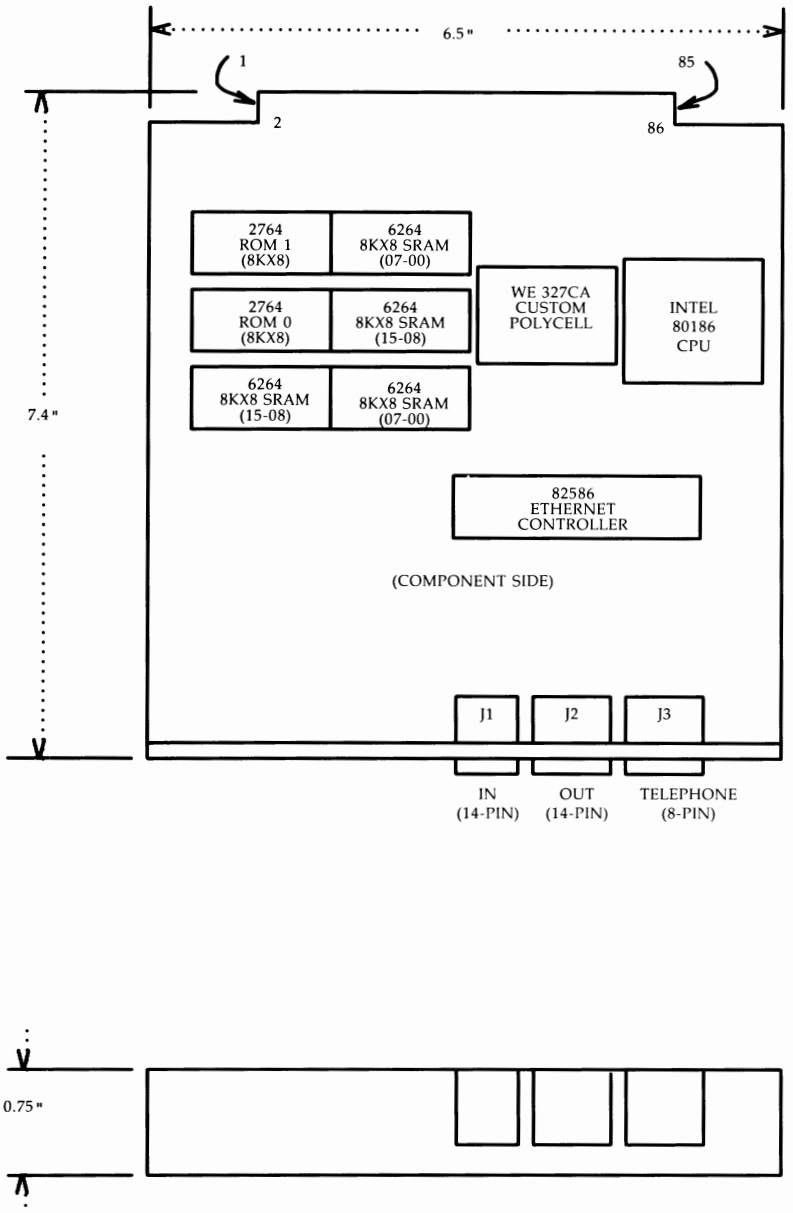


Figure 2-55: CM195U STARLAN Interface Card Layout

CM195W SCSI HOST ADAPTER CARD

The CM195W Small Computer Systems Interface (SCSI) Host Adapter Card provides connection to the industry standard SCSI bus. The SCSI bus is a 50 conductor bus that supports a wide variety of mass storage peripheral devices. The CM195W Card provides an asynchronous, single-ended interface to the SCSI bus with a peak transfer rate of 1.5 megabytes per second and with a maximum bus length of 6 meters.

The CM195W Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. Figure 2-56 shows the component layout of a typical CM195W SCSI Host Adapter Card. Connector pinout information is provided in Appendix B. The major components of the CM195W Card are listed below:

- An INTEL 80186 Microprocessor
- 128K bytes of Dynamic Random Access Memory (DRAM)
- 32K bytes of Read Only Memory (ROM)
- An NCR 5385E SCSI Protocol Controller.

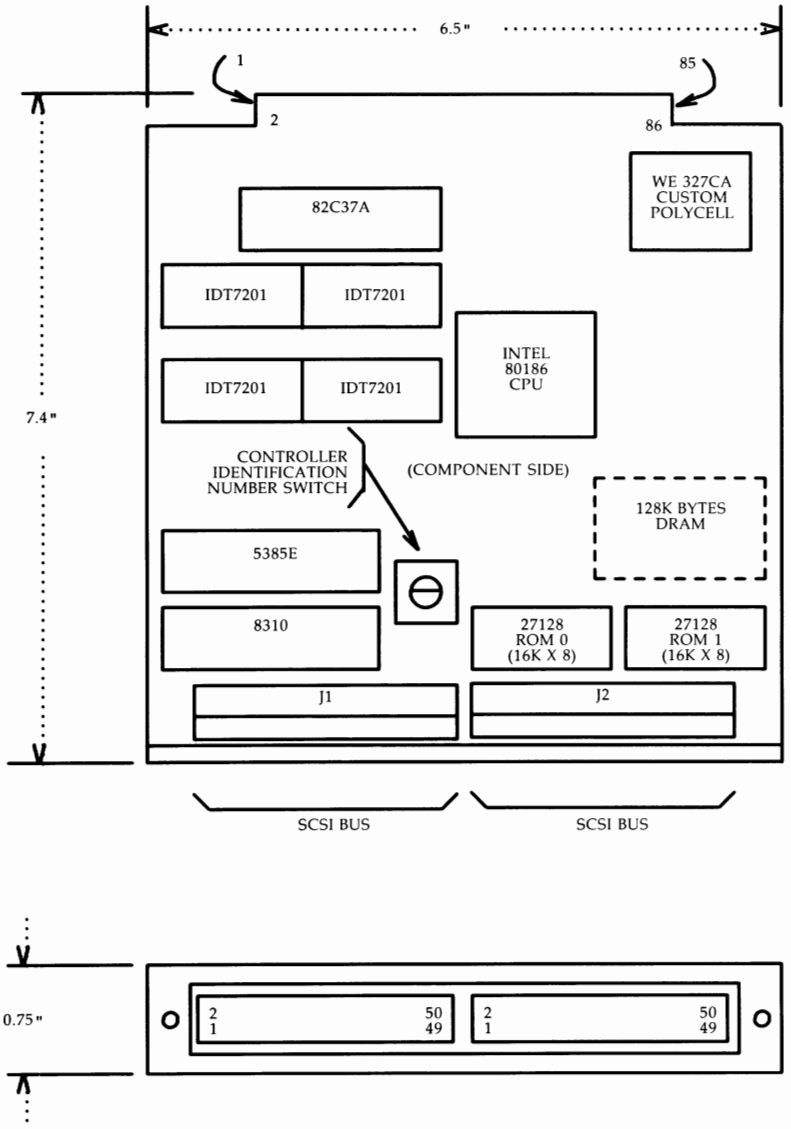


Figure 2-56: CM195W SCSI Host Adapter Card Layout

CM195Y EPORTS CARD

The CM195Y Enhanced Peripheral Port Controller (EPORTS) Card provides eight separate asynchronous serial ports (RS-232C input/output interfaces). The maximum throughput of the card is 38,400 bits per second.

The high performance capability of the CM195Y EPORTS Card is available only when an accompanying EPORTS software is installed.

The CM195Y Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. The card uses surface mounted technology. Figure 2-57 shows the component layout of a typical CM195Y EPORTS Card. Connector pinout information is provided in Appendix B. The major components of the CM195Y Card are listed below:

- An INTEL 80186 Microprocessor
- 128K bytes of Dynamic Random Access Memory (DRAM)
- 16K bytes of Read Only Memory (ROM)
- Four Dual Universal Asynchronous Receiver/Transmitter (DUART) chips.

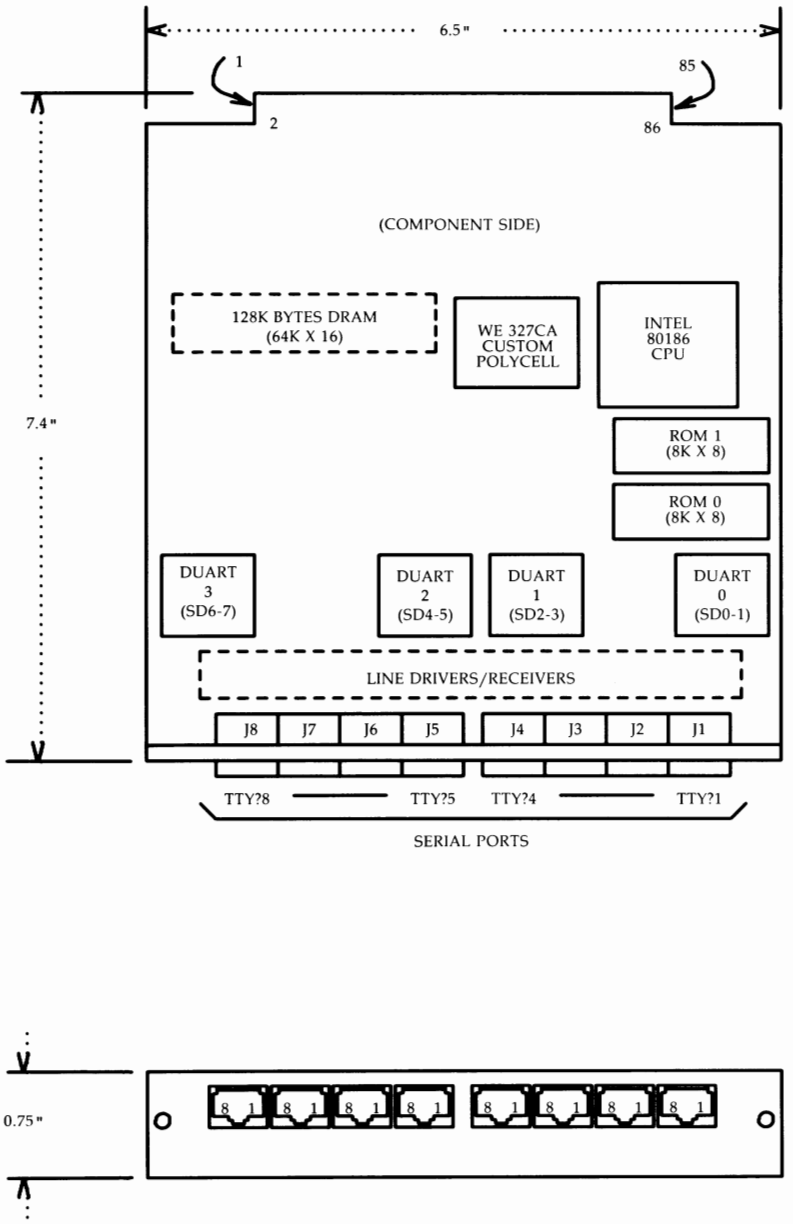


Figure 2-57: CM195Y EPORTS Card Layout

CM521A DIFFERENTIAL SCSI HOST ADAPTER CARD

The CM521A Differential Small Computer System Interface (SCSI) Host Adapter Card provides a differential connection to the industry standard SCSI bus. The SCSI bus is a 50-conductor bus that supports a wide variety of mass storage peripheral devices. The CM521A Card supports synchronous/asynchronous bus transfers and improved bandwidth across the Enhanced Input/Output (EIO) bus with a peak transfer rate of 3.0 megabytes per second and a maximum bus length of 25 meters.

The CM521A Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. Figure 2-58 shows the component layout of a typical CM521A Differential SCSI Host Adapter Card. Connector pinout information is provided in Appendix B. The major components of the CM521A Card are listed below:

- An INTEL 80186 Microprocessor
- 64K bytes of Static Random Access Memory (SRAM)
- 64K bytes of Erasable Programmable Read Only Memory (EPROM)
- A FUJITSU* MB87030 SCSI Protocol Controller operating at 8 MHz.

* Registered trademark of FUJITSU Limited, Nakahara-Ku, Kawasaki, Japan

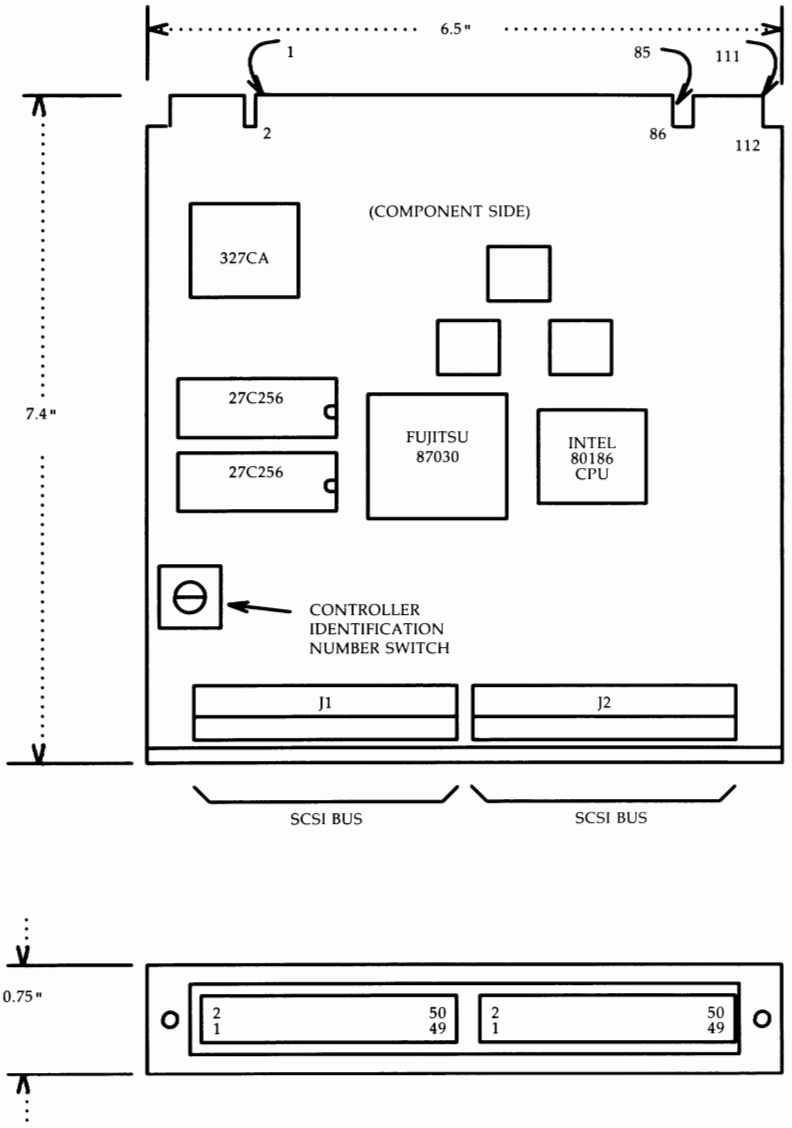


Figure 2-58: CM521A Differential SCSI Host Adapter Card Layout

CM522A VCACHE CARD

The CM522A Virtual Cache (VCACHE) Card improves system performance by storing instructions and data used by the Central Processing Unit (CPU). Electrically, the VCACHE is located between the CPU and the Memory Management Unit (MMU) and operates in parallel with the virtual-to-physical translation of the MMU. Therefore, the CPU can retrieve information from the VCACHE faster than from main memory via the MMU.

There is a software driver associated with the VCACHE feature. That driver is part of the reason the computer must be running UNIX System V Release 3.1.1 or later.

The CM522A Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. The card uses surface mounted technology. Figure 2-59 shows the component layout of a typical CM522A VCACHE Card. Connector pinout information is provided in Appendix B. The major features of the CM522A Card are listed below:

- Direct mapped operation using virtual memory addresses
- Allows the CPU access for cache hits resulting in zero CPU wait states
- Operates for frequencies up to 22 MHz
- 4K bytes of instructions and 2K bytes of data.

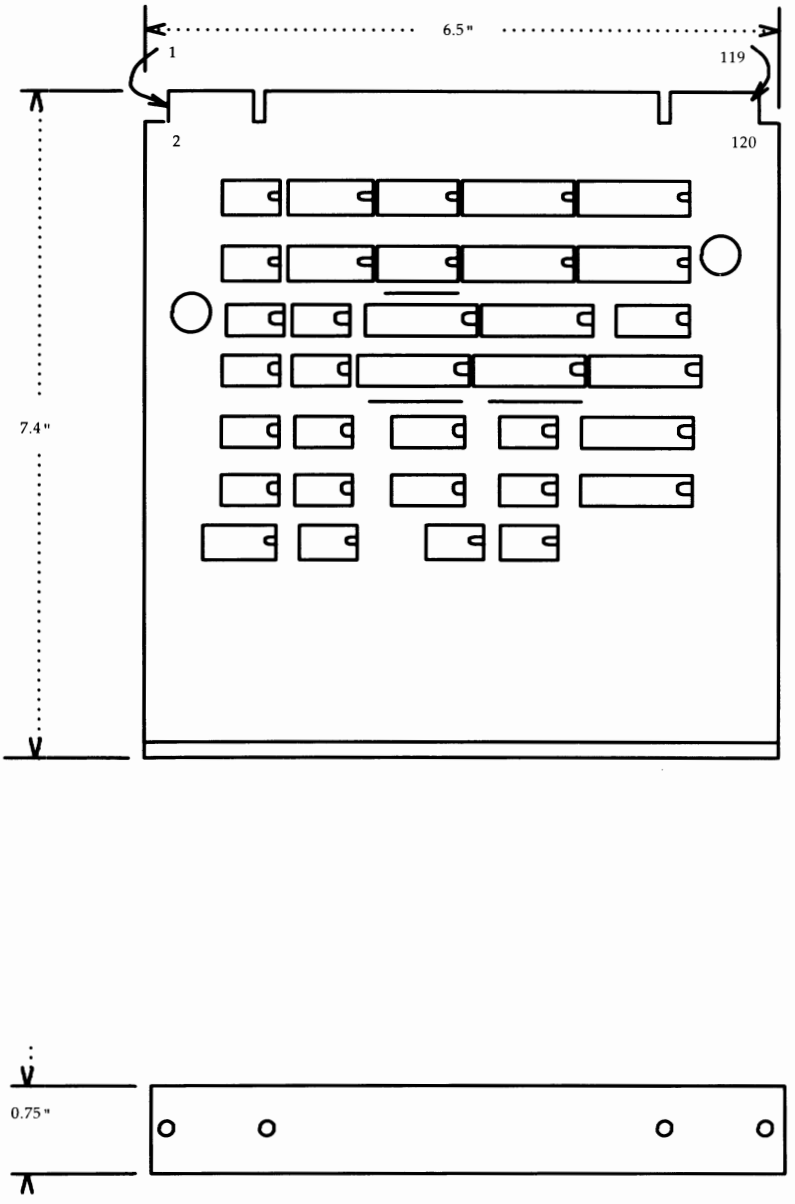


Figure 2-59: CM522A VCACHE Card Layout

CM524A PROCESSING ELEMENT CARD

The CM524A Processing Element (PE) Card improves system performance by providing another processing unit similar to that of the system board. The CM524A Card plugs into a Processor Bus (PBUS) backplane slot (labeled PROC*n*). The CM524A Card contains a Central Processing Unit (CPU), Memory Management Unit (MMU), Math Acceleration Unit (MAU), and 24-megahertz clock to form the secondary processing unit.

The Processing Element feature requires UNIX System V Release 3.2.2 or later and a CM519B Backplane. Also, the Multiprocessor Enhancement Utilities software must be installed before any system performance can be obtained.

The CM524A Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. The card uses surface mounted technology. Figure 2-60 shows the component layout of a typical CM524A PE Card. Connector pinout information is provided in Appendix B. The major components of the CM524A Card are listed below:

- A WE 32200 CPU chip
- A WE 32201 MMU chip
- A WE 32206 MAU chip
- 8K bytes of Static Random Access Memory (SRAM)
- Software controllable timer for rough time measurements and dynamic performance timing
- A 24-MHz oscillator.

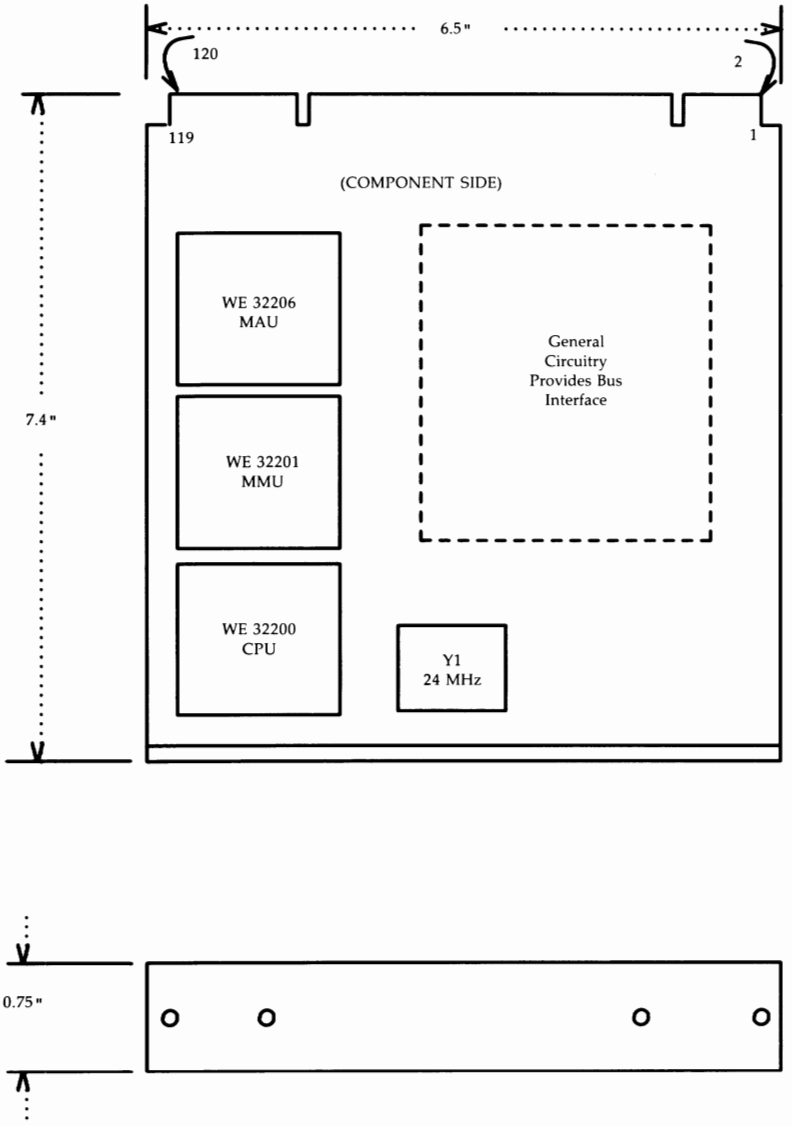


Figure 2-60: CM524A PE Card Layout

CM525B VMEbus CARD

The Versa Modula Europa bus (VMEbus) is an industry standard bus for a variety of character and networking controllers. The CM525B VMEbus Card provides the circuit interface between the 3B2 Buffered Microbus (BUB) backplane slot and the VMEbus System Controller.

The CM525B Card is a double-width card measuring 13.0 inches wide by 7.4 inches deep. Figure 2-61 shows the component layout of a CM525B VMEbus Card. Connector pinout information is provided in Appendix B. The major components of the CM525B Card are listed below:

- A 16-MHz internal clock
- An AMD29114 Interrupt Controller
- Four 8K by 8 Static Random Access Memory (SRAM).

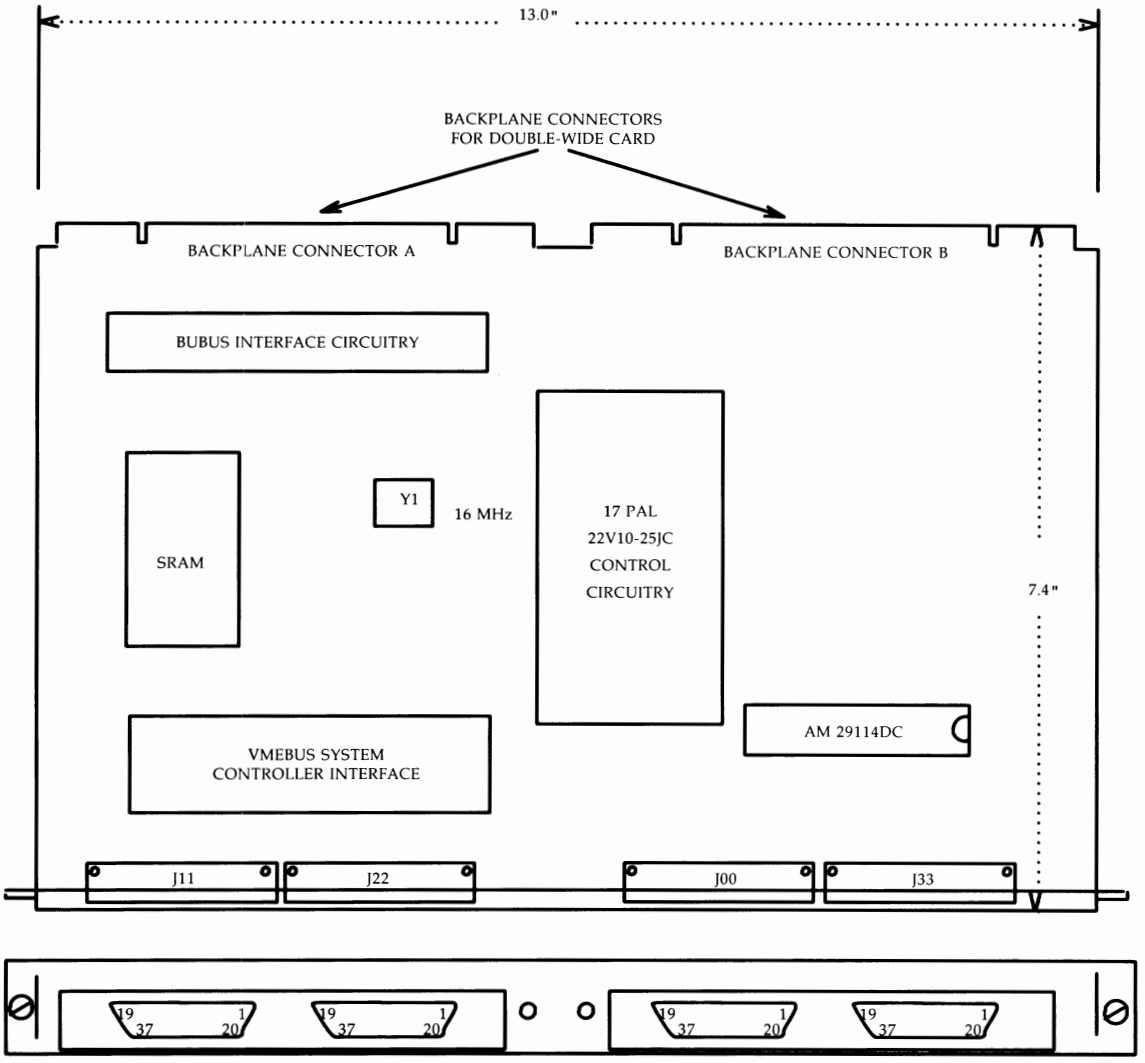


Figure 2-61: CM525B VMEbus Card Layout

CM527A MULTIPROCESSOR ENHANCEMENT CARD

The CM527A Multiprocessor Enhancement (MPE) Card plugs into a buffered microbus backplane slot (labeled BUB*n*) to improve the system performance. The CM527A Card contains a Central Processing Unit (CPU), Memory Management Unit (MMU), Math Acceleration Unit (MAU), and 18-megahertz clock to provide a secondary processing unit similar to that of the system board.

The Multiprocessor Enhancement feature requires UNIX System V Release 3.1.1 or later. Also, the Multiprocessor Enhancement Utilities software must be installed before any system performance can be obtained.

The CM527A Card is a single-width card measuring 6.5 inches wide by 7.4 inches deep. Figure 2-62 shows the component layout of a typical CM527A MPE Card. Connector pinout information is provided in Appendix B. The major components of the CM527A Card are listed below:

- A WE 32100 CPU chip
- A WE 32101 MMU chip
- A WE 32106 MAU chip
- 6K bytes onboard VCACHE circuitry
- A 18-MHz oscillator.

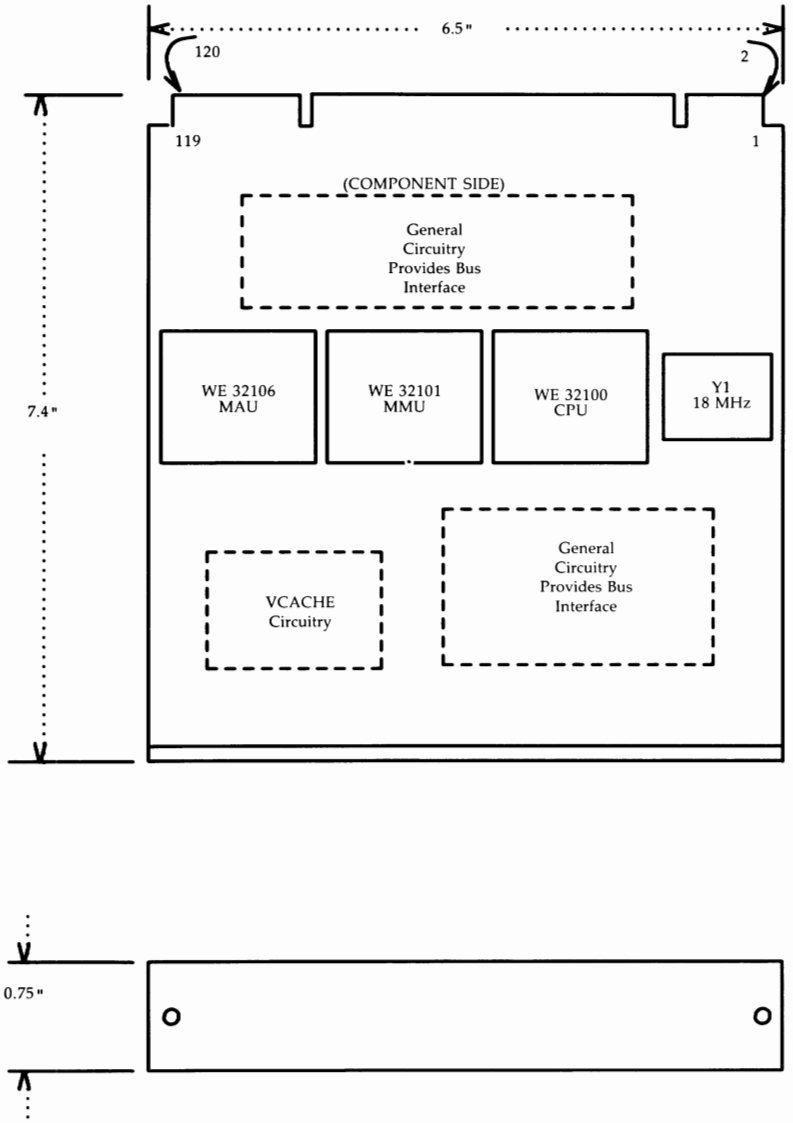


Figure 2-62: CM527A MPE Card Layout

FLOPPY DISK DRIVE (KS-23114,L4)

Floppy Disk Drive Use

One 5.25-inch, 720-kilobyte (formatted), 96 tracks-per-inch floppy disk drive is equipped for all 3B2 computer configurations. A second floppy disk drive can be equipped in an AT&T Expansion Module (AT&T/XM). Connection to the host 3B2 computer is via a CM195H Cartridge Tape Controller (CTC) Card. While it is possible to equip more than two floppy disk drives on a system, equipage of more than two floppy disk drives is not practical. Two floppy disk drives provide drive-to-drive operational capabilities that are considered to be the optimum floppy disk drive equipage.

Floppy disks can be used as file systems or as streaming devices. When used as a streaming device, data is written to and read from the floppy disk using a **cpio -o** and **cpio -i** type commands. In **cpio** form, the floppy disk provides 1422 blocks (512-byte blocks) of storage. When used as a file system, the fixed partitioning of the floppy disk provides a maximum of 1404 blocks (partition 5).

Floppy Disk Partitions

The following table defines the floppy disk partitions in terms of use, starting sector, and total number of blocks for the various controller (c), drive (d), and section (s) identifiers for the floppy disk. These identifiers are applicable to both the raw and block devices. Note that Volume Table of Contents (VTOC) partitioning is not applicable to the floppy disk drive. The raw and block device partitions for the entire floppy disk (partition 6) are linked to */dev/rSA/diskette1* and */dev/SA/diskette1*, respectively. The use of these names when specifying the entire floppy disk is preferred over the use of the controller, drive, and section identifiers to avoid accidentally writing to a different device or partition.

720-KILOBYTE FLOPPY DISK DRIVE
(18 Blocks/Cylinder, Gap=1)

FLOPPY DISK DEFAULT PARTITIONING

DISK PARTITION	USE	SECTOR START	TOTAL SECTORS*
c0d0s0	root	378 (21*18)	1044
c0d0s1	usr	452 (34*18)	810
c0d0s2	usr	810 (45*18)	612
c0d0s3	usr	1008 (56*18)	414
c0d0s4	usr	2106 (67*18)	216
c0d0s5	usr	1 (1*18)	1404
c0d0s6	entire disk	0	1422
c0d0s7	boot	0	18

* Blocks (sectors) are reported in 512-byte blocks.

Floppy Disk Drive Equipment Characteristics

Reliability.

Head Life	20,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^9 bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25 inch, double-sided, 96 tracks per inch
Rotational Speed	300 revolutions per minute
Height	1.625 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	9
Tracks/Cylinder	2
Cylinders	79 Accessible, 80 Total
Formatted Size	1422 blocks (512 bytes)

Operational.

Interface	TM100 (34 pin)
Transfer Rate	250 kilobits per second (31.25 kilobytes per second)
Latency	100 milliseconds, average
Seek Time	3 milliseconds, single track 90 milliseconds, average

23-MEGABYTE CARTRIDGE TAPE DRIVE (KS-23165,L1)

Cartridge Tape Use

One or more 23-Megabyte Cartridge Tape Drives can be added to a 3B2 computer. The drive can be mounted in an AT&T Expansion Module cabinet or by itself in a Tape Module cabinet. One 23-megabyte cartridge tape drive is standard equipage with a 3B2/400 computer. Each 23-megabyte cartridge tape drive connects to the host 3B2 computer via a CM195H Cartridge Tape Controller (CTC) Card that is installed in a 3B2 computer feature card slot. For a 3B2/400 computer, the first cartridge tape controller is equipped in slot 2. The primary use of a cartridge tape drive is as a streaming device for backing up the data stored on the hard disk drives. While the 23-megabyte cartridge tape can be configured as a file system, the intended use of a cartridge tape is as a streaming device. As a streaming device, the tape provides a capacity of 45,539 blocks (512-byte blocks). The use of a cartridge tape as a file system substantially degrades both system and tape performance.

Routine cleaning of the cartridge tape drive is required to maintain error-free operation. The CTC card keeps track of the hours of operation. Software is provided to output an advisory message warning of the need to clean the cartridge tape drive after 20 hours of operation. Depending on the environment, more frequent cleaning may be necessary to maintain error-free operation and to promote tape life. The recommended tape life in terms of pass count is 4000, when used as a streaming device. If a tape is used as a file system, the pass count (tape life) should be reduced to 2000 or less.

The 23-megabyte cartridge tape can be formatted with a pass count threshold that is less than or greater than the recommended value(s). Reformatting the cartridge tape does not reset the pass count recorded on the tape. When the pass count recorded on a tape reaches the pass count threshold, an advisory message is output to replace the tape.

Cartridge Tape Partitioning

The following table defines the partition, use, size, and number of blocks for the various controller (c), drive (d), and section (s) identifiers for the 23-megabyte cartridge tape. These identifiers are applicable to both the raw and block devices. Note that Volume Table of Contents (VTOC) partitioning is fixed for the cartridge tape by the tape formatting process. The controller number (?) depends on the slot in which the CM195H Card is equipped.

23-MEGABYTE CARTRIDGE TAPE DRIVE
(31 Blocks/Cylinder, Gap=1)

CARTRIDGE TAPE DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*
c?d0s0	root	5272	8928
c?d0s1	swap	126	5146
c?d0s2	usr	14200	31341
c?d0s3	usr	2	45539
c?d0s6	entire tape	0	45541
c?d0s7	boot	0	126

* Size is reported in 512-byte blocks.

Cartridge Tape Drive Equipment Characteristics

Physical.

Tape	DC600A cartridge tape (or equivalent)
Tracks	6
Tape Speed	78 inches per second
Recording Density	6400 bits per inch (nominal)
Formatted Size	45,541 blocks (512-byte blocks) total 45,539 blocks (512-byte blocks) accessible
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches

Operational.

Interface	SA450 (34-pin connector)
Transfer Rate	500 kilobits per second

60-MEGABYTE CARTRIDGE TAPE DRIVE (KS-23417,L2)

The 60-Megabyte Cartridge Tape Drive is used as a streaming device for mass storage of data. As the name suggests, the drive provides 60-megabytes of formatted storage capacity. Formatting of the tape is not necessary because no Volume Table of Contents (VTOC) is used.

The drive may be an internal part of the 3B2 computer cabinet or it may be a separate SCSI peripheral. Either way, connection to the 3B2 computer is via a SCSI Host Adapter card.

60-Megabyte Cartridge Tape Drive Equipment Characteristics

Physical.

Tape	DC600A cartridge tape (or equivalent)
Tracks	9
Tape Speed	90 inches per second
Recording Density	8000 bits per inch (nominal)
Formatted Size	125,604 blocks (512-byte blocks) total
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches

Operational.

Interface	SCSI (34-pin connector)
Transfer Rate	720 kilobits per second (sustained)

120-MEGABYTE CARTRIDGE TAPE DRIVE (KS-23465,L1A)

The 120-Megabyte Cartridge Tape Drive is used as a streaming device for mass storage of data. As the name suggests, the drive provides 120-megabytes of formatted storage capacity. Formatting of the tape is not necessary because no Volume Table of Contents (VTOC) is used.

The 120-Megabyte Cartridge Tape Drive is capable of reading cartridge tapes that were written by a 60-Megabyte Cartridge Tape Drive. This allows greater data interchangeability between machines. However, tapes written by 120-megabyte drives cannot be read on the 60-megabyte drive.

The drive may be an internal part of the 3B2 computer cabinet or it may be a separate SCSI peripheral. Either way, connection to the 3B2 computer is via a SCSI Host Adapter card.

120-Megabyte Cartridge Tape Drive Equipment Characteristics

Physical.

Tape	DC600A cartridge tape (or equivalent)
Tracks	15
Tape Speed	90 inches per second
Recording Density	10,000 bits per inch (nominal)
Formatted Size	266,004 blocks (512-byte blocks) total
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches

Operational.

Interface	SCSI (34-pin connector)
Transfer Rate	900 kilobits per second

HARD DISK DRIVES

Seagate 10-Megabyte Hard Disk (KS-23034,L1)

10-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 30,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3600 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	18
Tracks/Cylinder	4
Cylinders	304 Accessible, 306 Total
Formatted Size	21,888 blocks (512 bytes)

Operational.

Interface	ST-506
Transfer Rate	5.0 megabits per second (625 kilobytes per second)
Latency	8.33 milliseconds, average
Seek Time	85 milliseconds, average 205 milliseconds, maximum

Default Device Partitioning

The following table shows the default device partitioning for the Seagate 10-megabyte hard disk drive.

SEAGATE 10-MEGABYTE HARD DISK DRIVE
(72 Blocks/Cylinder, Gap=9)

SINGLE HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	3600	8928	1116
c1d0s1	swap	100	3500	----
c1d0s2	usr	12528	9360	1170
c1d0s6	entire disk	0	21888	----
c1d0s7	boot	0	100	----

DUAL HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	3600	8928	1116
c1d0s1	swap	100	3500	----
c1d0s6	entire disk	0	21888	----
c1d0s7	boot	0	100	----
c1d0s8	usr2	12528	9360	1170
c1d1s2	usr	72	21816	2727
c1d1s6	entire disk	0	21888	----
c1d1s7	boot	0	72	----

* Size is reported in 512-byte blocks.

WREN 30-Megabyte Hard Disk (KS-23054,L1)

30-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 40,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3600 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	18
Tracks/Cylinder	5
Cylinders	695 Accessible, 697 Total
Formatted Size	62,550 blocks (512 bytes)

Operational.

Interface	ST-506
Transfer Rate	5.0 megabits per second (625 kilobytes per second)
Latency	8.33 milliseconds, average
Seek Time	45 milliseconds, average 90 milliseconds, maximum

Default Device Partitioning

The following table shows the default device partitioning for the WREN 30-megabyte hard disk drive.

WREN 30-MEGABYTE HARD DISK DRIVE
(90 Blocks/Cylinder, Gap=9)

SINGLE HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	6120	12510	1552
c1d0s1	swap	100	6020	----
c1d0s2	usr	18630	43920	5490
c1d0s6	entire disk	0	62550	----
c1d0s7	boot	0	100	----

DUAL HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	6120	12510	1564
c1d0s1	swap	100	6020	----
c1d0s6	entire disk	0	62550	----
c1d0s7	boot	0	100	----
c1d0s8	usr2	18630	43920	5490
c1d1s2	usr	90	62460	7808
c1d1s6	entire disk	0	62550	----
c1d1s7	boot	0	90	----

* Size is reported in 512-byte blocks.

FUJITSU 72-Megabyte Hard Disk (KS-23054,L2)

72-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 30,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3600 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	18
Tracks/Cylinder	11
Cylinders	752 Accessible, 754 Total
Formatted Size	148,896 blocks (512 bytes)

Operational.

Interface	ST-506
Transfer Rate	5.0 megabits per second (625 kilobytes per second)
Latency	8.33 milliseconds, average
Seek Time	35 milliseconds, average 60 milliseconds, maximum

Default Device Partitioning

The following table shows the default device partitioning for the FUJITSU 72-megabyte hard disk drive.

FUJITSU 72-MEGABYTE HARD DISK DRIVE
(198 Blocks/Cylinder, Gap=9)

SINGLE HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	10296	12672	1584
c1d0s1	swap	100	10196	----
c1d0s2	usr	22968	125928	15741
c1d0s6	entire disk	0	148896	----
c1d0s7	boot	0	100	----

DUAL HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	10296	12672	1584
c1d0s1	swap	100	10196	----
c1d0s6	entire disk	0	148896	----
c1d0s7	boot	0	100	----
c1d0s8	usr2	22968	125928	15741
c1d1s2	usr	198	148698	18588
c1d1s6	entire disk	0	148896	----
c1d1s7	boot	0	198	----

* Size is reported in 512-byte blocks.

WREN II 72-Megabyte Hard Disk (KS-23054,L2)

72-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 40,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3600 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	18
Tracks/Cylinder	9
Cylinders	923 Accessible, 925 Total
Formatted Size	149,526 blocks (512 bytes)

Operational.

Interface	ST-506
Transfer Rate	5.0 megabits per second (625 kilobytes per second)
Latency	8.33 milliseconds, average
Seek Time	35 milliseconds, average 85 milliseconds, maximum

Default Device Partitioning

The following table shows the default device partitioning for the WREN II 72-megabyte hard disk drive.

WREN II 72-MEGABYTE HARD DISK DRIVE
(162 Blocks/Cylinder, Gap=9)

SINGLE HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	10206	12636	1580
c1d0s1	swap	100	10106	----
c1d0s2	usr	22842	126684	15836
c1d0s6	entire disk	0	149526	----
c1d0s7	boot	0	100	----

DUAL HARD DISK DEFAULT PARTITIONING

PARTITION	USE	SECTOR START	SIZE*	I-NODES
c1d0s0	root	10206	12636	1580
c1d0s1	swap	100	10106	----
c1d0s6	entire disk	0	149526	----
c1d0s7	boot	0	100	----
c1d0s8	usr2	22842	126684	15836
c1d1s2	usr	162	149364	18671
c1d1s6	entire disk	0	149526	----
c1d1s7	boot	0	162	----

* Size is reported in 512-byte blocks.

94-Megabyte Hard Disk (KS-23371,L7)

94-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 20,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3482 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	35
Tracks/Cylinder	7
Cylinders	821 Accessible, 823 Total
Formatted Size	201,145 blocks (512 bytes)

Operational.

Interface	ESDI
Transfer Rate	10.0 megabits per second (1250 kilobytes per second)
Latency	8.62 milliseconds, average
Seek Time	23 milliseconds, average 45 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

147-Megabyte Hard Disk (KS-23371,L17)

147-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 40,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3597 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	36
Tracks/Cylinder	9
Cylinders	967 Accessible, 969 Total
Formatted Size	313,308 blocks (512 bytes)

Operational.

Interface	ESDI
Transfer Rate	10.0 megabits per second (1250 kilobytes per second)
Latency	8.34 milliseconds, average
Seek Time	16.5 milliseconds, average 43.0 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

155-Megabyte Hard Disk (KS-23483,L25)

155-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 40,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3597 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	35
Tracks/Cylinder	9
Cylinders	964 Accessible, 966 Total
Formatted Size	303,660 blocks (512 bytes)

Operational.

Interface	SCSI (Single-ended only)
Transfer Rate	10.0 megabits per second (1250 kilobytes per second)
Latency	8.34 milliseconds, average
Seek Time	16.5 milliseconds, average 43 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

300-Megabyte Hard Disk (KS-23483,L1B or L11B)

300-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 150,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3348 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	32
Tracks/Cylinder	12
Cylinders	1640 Accessible, 1642 Total
Formatted Size	629,760 blocks (512 bytes)

Operational.

Interface	SCSI (L1B—Single-ended, L11B—Differential)
Transfer Rate	10.0 megabits per second (4 megabytes per second synchronous) (1.5 megabytes per second asynchronous)
Latency	8.96 milliseconds, average
Seek Time	17.5 milliseconds, average 32 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

300-Megabyte Hard Disk (KS-23483,L3)

300-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 150,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3597 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	43
Tracks/Cylinder	9
Cylinders	1514 Accessible, 1516 Total
Formatted Size	585,937 blocks (512 bytes)

Operational.

Interface	SCSI (Single-ended only)
Transfer Rate	12 megabits per second (1.5 megabytes per second)
Latency	8.34 milliseconds, average
Seek Time	16.5 milliseconds, average 43 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

300-Megabyte Hard Disk (KS-23371,L31)

300-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 30,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3600 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	35
Tracks/Cylinder	15
Cylinders	1215 Accessible, 1224 Total
Formatted Size	619,650 blocks (512 bytes)

Operational.

Interface	ESDI
Transfer Rate	10.0 megabits per second (1250 kilobytes per second)
Latency	8.33 milliseconds, average
Seek Time	18 milliseconds, average 40 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

600-Megabyte Hard Disk (KS-23483,L5 or L15)

600-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 15,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	3597 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	9.06 inches
Bytes/Sector	512
Sectors/Track	52
Tracks/Cylinder	15
Cylinders	1544 Accessible, 1546 Total
Formatted Size	1,204,320 blocks (512 bytes)

Operational.

Interface	SCSI (L5—Single-ended, L15—Differential)
Transfer Rate	12.0 megabits per second (1.5 megabytes per second)
Latency	8.34 milliseconds, average
Seek Time	17.5 milliseconds, average 44 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

600-Megabyte Hard Disk (KS-23483,L7 or L17)

600-Megabyte Hard Disk Equipment Characteristics

Reliability.

Life	5 years or 15,000 hours
Error Rates	Recoverable (soft) read errors occur less than 1 in 10^{10} bits transferred. Unrecoverable (hard) read errors occur less than 1 in 10^{12} bits transferred.

Physical.

Disk Type	5.25-inch, Winchester drive
Rotational Speed	4002 revolutions per minute
Height	3.25 inches
Width	5.75 inches
Depth	8.0 inches
Bytes/Sector	512
Sectors/Track	56
Tracks/Cylinder	16
Cylinders	1447 Accessible, 1457 Total
Formatted Size	1,296,512 blocks (512 bytes)

Operational.

Interface	SCSI (L7—Single-ended, L17—Differential)
Transfer Rate	12.0 megabits per second (1.5 megabytes per second)
Latency	7.47 milliseconds, average
Seek Time	16.5 milliseconds, average 32 milliseconds, maximum

Default Device Partitioning

The default device partitioning for this disk drive depends on the configuration of the computer and the release of the UNIX operating system.

POWER—EQUIPMENT DESCRIPTION

Domestic 3B2/300 and 310 Computers Power Supply, #095-10011-XX1 and #095-10060-00

Early domestic production 3B2/300 and 310 computers are equipped with a TRW #095-10011-XX1 Power Supply Unit. Current domestic production 3B2/300 and 310 computers are equipped with a TRW #095-10060-00 Power Supply Unit.

TRW #095-10011-XX1 and #095-10060-00 Equipment Characteristics

Electrical.

Voltage	115 V AC, 4 Amperes
Frequency	50/60 Hz
Total Power Consumption	350 watts (or less)

3B2/300 and 310 Computers International Power Supply, #095-10011-XX2 and #095-10061-00

Early international production 3B2/300 and 310 computers are equipped with a TRW #095-10011-XX2 Power Supply Unit. Current international production 3B2/300 and 310 computers are equipped with a TRW #095-10061-00 Power Supply Unit.

TRW #095-10011-XX2 and #095-10061-00 Equipment Characteristics

Electrical.

Voltage	220 to 240 V AC, 2 Amperes
Frequency	50/60 Hz
Total Power Consumption	350 watts (or less)

3B2/400 Computer Domestic Power Supply, #095-10035-XX1

The domestic production 3B2/400 computer is equipped with a TRW #095-10035-XX1 Power Supply Unit.

TRW #095-10035-XX1 Equipment Characteristics

Electrical.

Voltage	115 V AC, 6 Amperes
Frequency	50/60 Hz
Total Power Consumption	500 watts (or less)

3B2/400 Computer International Power Supply, #095-10035-XX2

The international production 3B2/400 computer is equipped with a TRW #095-10035-XX2 Power Supply Unit.

TRW #095-10035-XX2 Equipment Characteristics

Electrical.

Voltage	220 to 240 V AC, 3 Amperes
Frequency	50/60 Hz
Total Power Consumption	Less than 200 watts (maximum)

3B2/500 Computer Power Supply, ACS752A or CS752A

The 3B2/500 computer is equipped with either an ACS752A or a CS752A Power Supply Unit.

ACS752A and CS752A Equipment Characteristics

Electrical.

Voltage	100 to 120 V AC, 7 Amperes 200 to 240 V AC, 4 Amperes
Frequency	50/60 Hz
Power Consumption	680 watts (or less)

3B2/600, 700, and 1000 Computers Power Supply, ACS782A or CS782A

The 3B2/600, 700, and 1000 computers are equipped with either an ACS782A or a CS782A Power Supply Unit.

ACS782A and CS782A Equipment Characteristics

Electrical.

Voltage	100 to 120 V AC, 12 Amperes 200 to 240 V AC, 8.5 Amperes
Frequency	50/60 Hz
Power Consumption	1130 watts (or less)

Domestic AT&T Expansion Module Power Supply, #095-10040-XX1

The domestic production AT&T/XM is equipped with a TRW #095-10040-XX1 Power Supply Unit.

TRW #095-10040-XX1 Equipment Characteristics

Electrical.

Voltage	115 V AC, 5 Amperes
Frequency	50/60 Hz
Total Power Consumption	Less than 298 watts (maximum)

International AT&T Expansion Module Power Supply, #095-10040-XX2

The international production AT&T/XM is equipped with a TRW #095-10040-XX2 Power Supply Unit.

TRW #095-10040-XX2 Equipment Characteristics

Electrical.

Voltage	220 to 240 V AC, 2.5 Amperes
Frequency	50/60 Hz
Total Power Consumption	Less than 298 watts (maximum)

Domestic AT&T XM/405S/900S Power Supply, #095-10064-00

The domestic production AT&T XM/405S/900S is equipped with a TRW #095-10064-00 Power Supply Unit.

TRW #095-10064-00 Equipment Characteristics

Electrical.

Voltage	115 V AC, 5 Amperes
Frequency	50/60 Hz
Total Power Consumption	Less than 298 watts (maximum)

International AT&T XM/405S/900S Power Supply, #095-10073

The international production AT&T XM/405S/900S is equipped with a TRW #095-10073 Power Supply Unit.

TRW #095-10073 Equipment Characteristics

Electrical.

Voltage	220 to 240 V AC, 2.5 Amperes
Frequency	50/60 Hz
Total Power Consumption	Less than 298 watts (maximum)

AT&T SCSI Peripherals (DCM, DM, TM, and PPCU) Power Supply, #095-10065

The AT&T SCSI Peripherals (DCM, DM, TM, and PPCU) are equipped with a TRW #095-10065 Power Supply Unit.

TRW #095-10065 Equipment Characteristics

Electrical.

Voltage	100 to 120 V AC, 1.5 Amperes 200 to 240 V AC, 0.75 Amperes
Frequency	50/60 Hz
Total Power Consumption	Less than 298 watts (maximum)

3B2 Computer Backup Battery Supply

A 3.6 volt DC lithium battery is used to supply approximately 3.3 volts DC standby power for the following:

- Time-of-Day Clock
- Nonvolatile Random Access Memory (NVRAM)
- Feature Card Slots.

For the Version 2 computers, the battery connects directly to the system board via the battery connector J11. The battery assembly and the connections to the system board are shown in Figure 2-63.

The Version 3 computers provide a connector on the backplane for the battery. The battery connects to the CM520A Backplane via connector J04 and to the CM519A/B Backplanes via connector J02. The battery itself is mounted on the card cage assembly as shown in Figures 2-64 and 2-65.

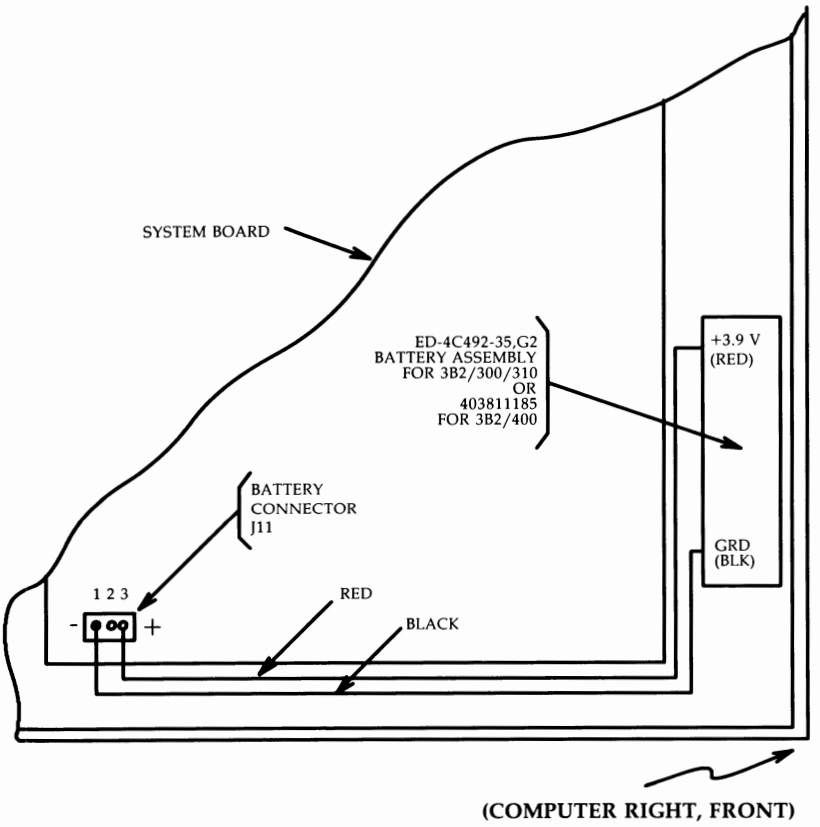


Figure 2-63: Version 2 Computer Backup Battery Supply Layout

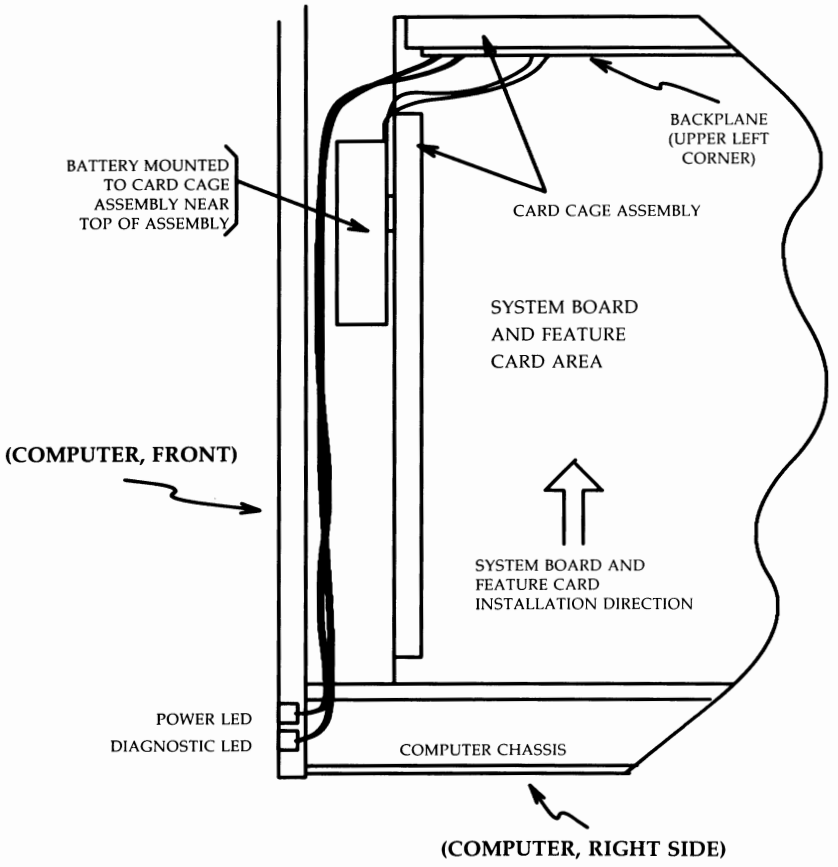


Figure 2-64: 3B2/500 Computer Backup Battery Supply Position

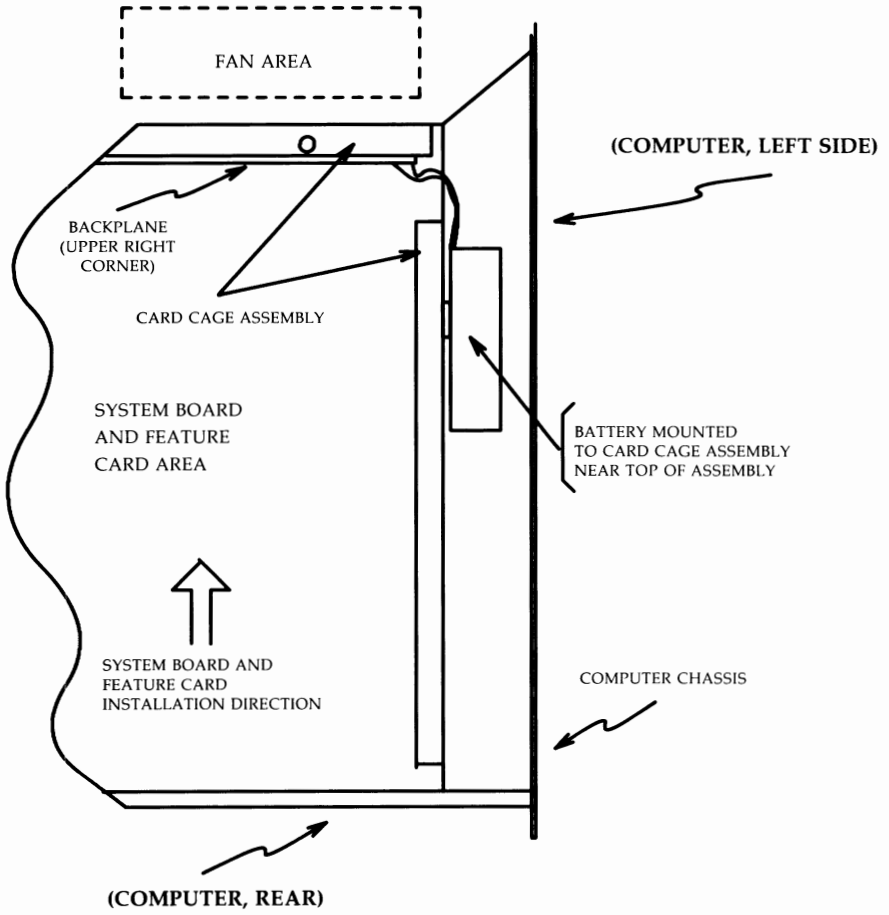


Figure 2-65: 3B2/600, 700, and 1000 Computer Backup Battery Supply Position

MISCELLANEOUS EQUIPMENT AND APPARATUS

Vertical Stands

The 3B2/300 and 310 computers and the AT&T Expansion Module (AT&T/XM) can be mounted vertically using an optional vertical stand. A vertical stand option is not applicable for the 3B2/400 computer. Refer to the *Vertical Stand Manual,* (Select Code 305-319), for complete information.

3B2 Expansion Cabinet

The 3B2 Expansion Cabinet provides a means of organizing the 3B2 computer equipment. The cabinet can house a wide variety of equipment configurations according to the mounting kits which are purchased. Refer to the *Expansion Cabinet Assembly Manual,* (Select Code 305-690), for complete information.

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FUNCTIONAL DESCRIPTION

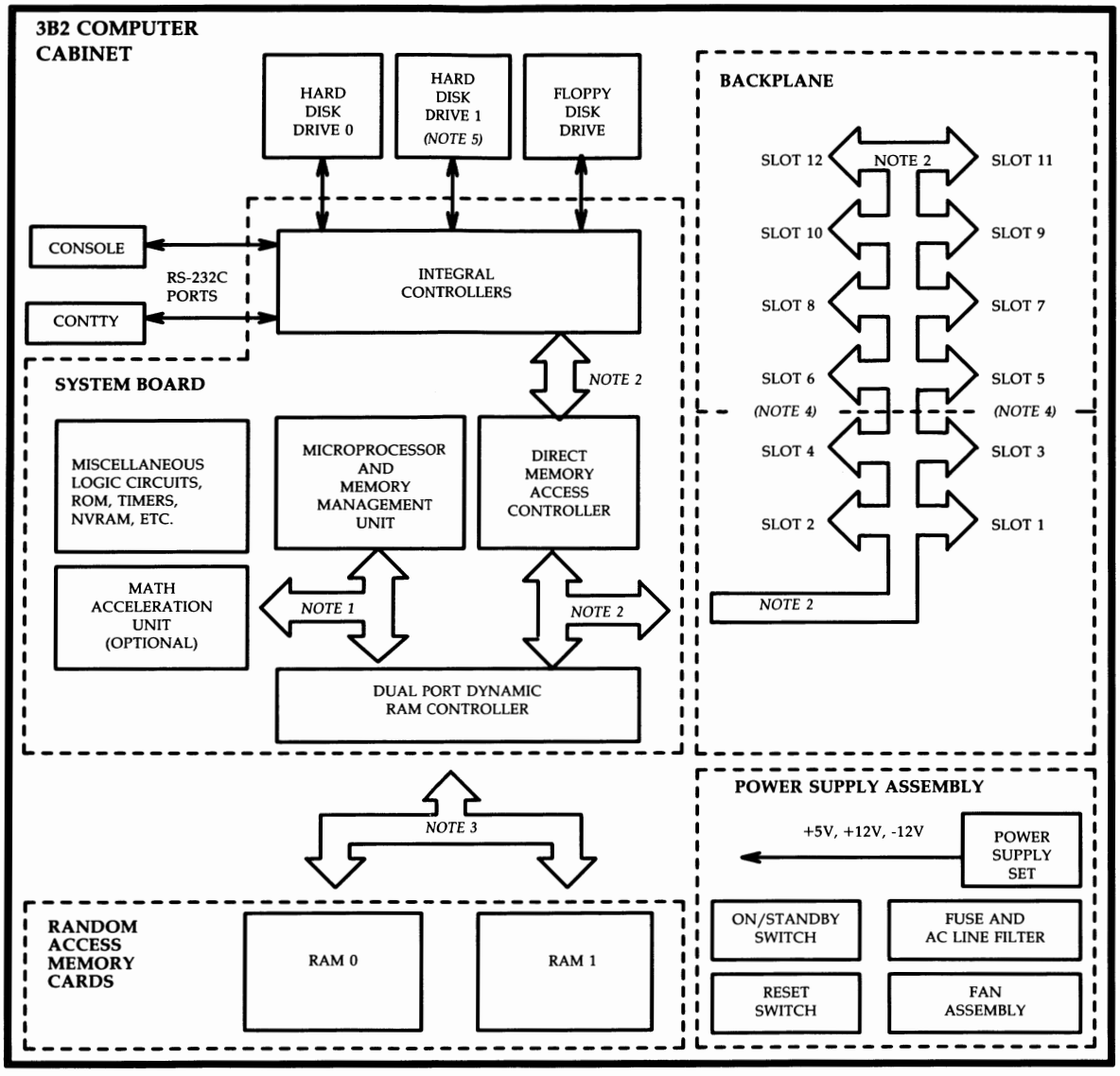
SYSTEM OVERVIEW

General

This chapter provides a high-level functional description of the 3B2 computer to a circuit card level. Signal names used in the diagrams and descriptions end with a "[0]" or "[1]" to indicate an active state of the signal. Names ending with a "0" are "active low" signals; names ending with a "1" are "active high" signals. The term "asserted" is used in the descriptions to mean that a signal is driven to its active state. The term "negated" is used in the descriptions to mean that a signal is driven to its inactive state. Hexadecimal (base 16) numbers are denoted with a **0x** prefix; for example, 0x 00A is decimal 10.

Figure 3-1 is a high-level functional block diagram of the Version 2 3B2 computers (3B2/300, 310, and 400). The following is a list of the major functional areas of Version 2 computers:

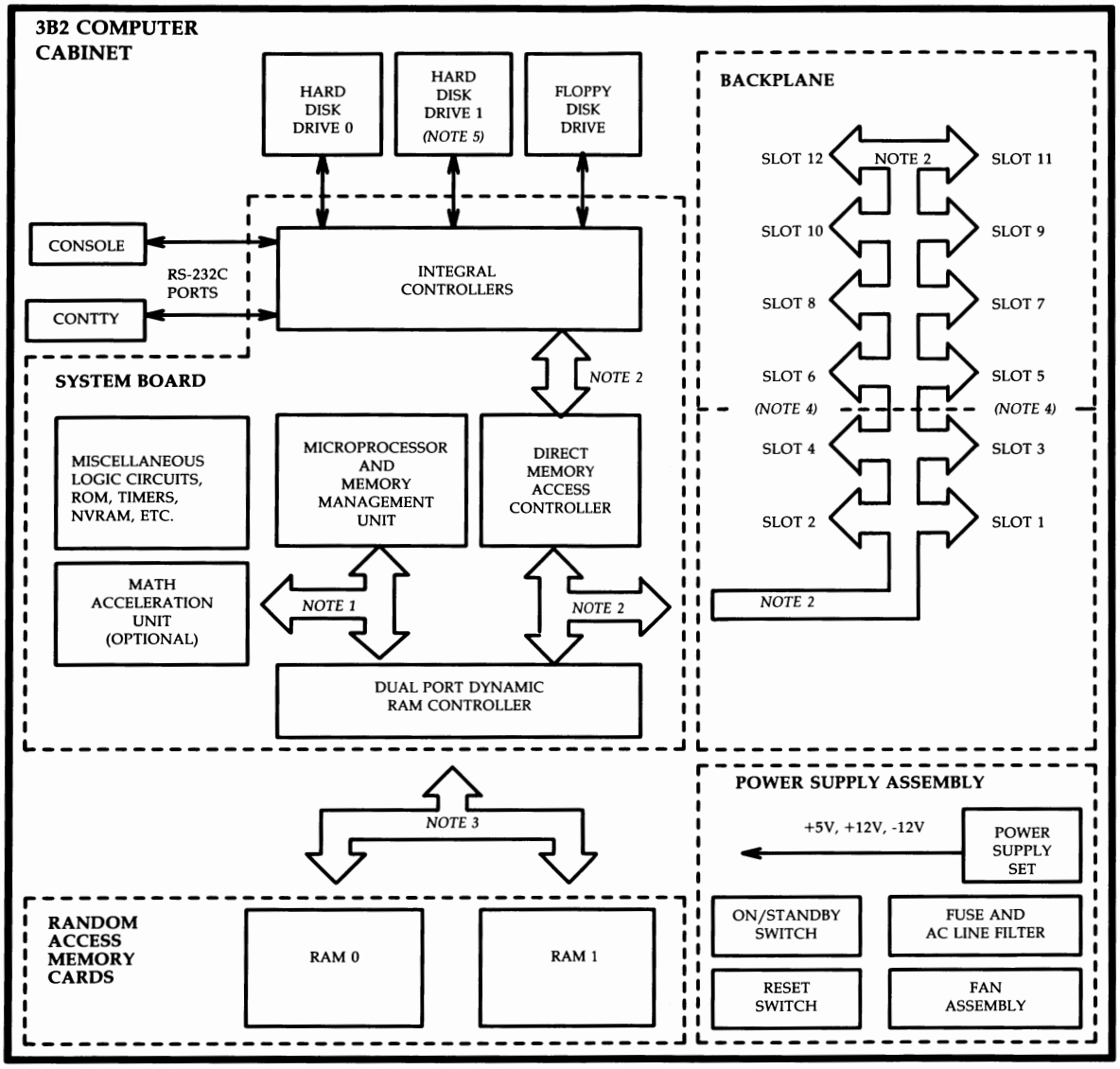
- Central Processing Unit (CPU) Microprocessor
- Memory Management Unit (MMU)
- Math Acceleration Unit (MAU) (optional)
- Dual Port Dynamic Random Access Memory (DPDRAM) Subsystem
- Direct Memory Access (DMA) Subsystem
- Input/Output (I/O) Bus
- Feature Card Connectors
- Miscellaneous Status and Control Signals
- Power and Alarm Circuits.



NOTES:

1. 32-BIT ADDRESS BUS AND 32-BIT DATA BUS.
2. 24-BIT ADDRESS BUS AND 16-BIT DATA BUS.
3. 32-BIT DATA BUS PLUS BYTE PARITY.
4. 3B2/300 AND 310 COMPUTERS HAVE 4 SLOTS. 3B2/400 COMPUTER HAS 12 SLOTS.
5. HARD DISK DRIVE 1 IS MOUNTED IN THE 3B2 COMPUTER CABINET ONLY FOR 3B2/400. FOR 3B2/300 and 310, DRIVE 1 IS MOUNTED IN AN AT&T/XM.

Figure 3-1: 3B2/300/310/400 Computer — High-Level Functional Block Diagram



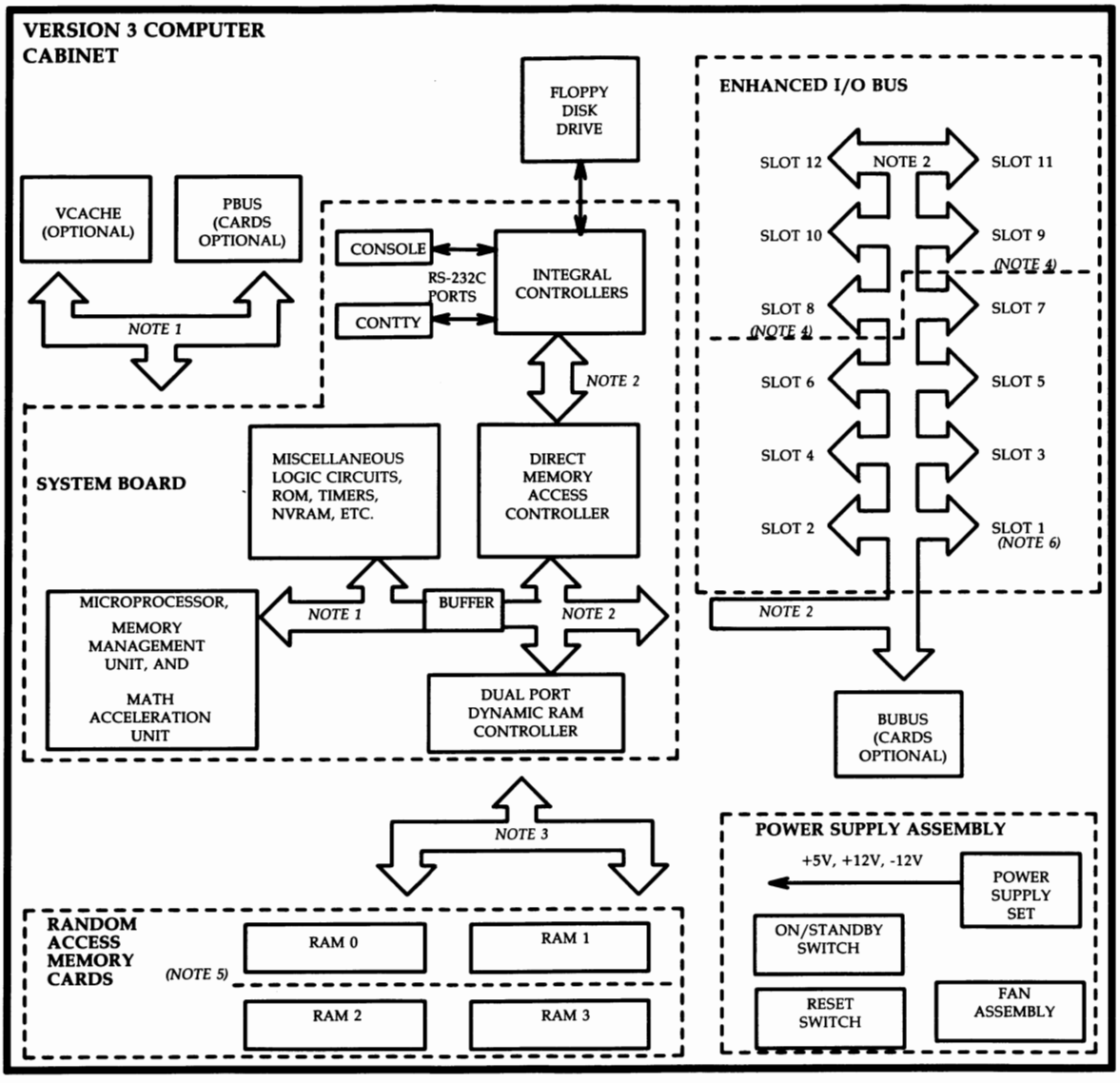
NOTES:

1. 32-BIT ADDRESS BUS AND 32-BIT DATA BUS.
2. 24-BIT ADDRESS BUS AND 16-BIT DATA BUS.
3. 32-BIT DATA BUS PLUS BYTE PARITY.
4. 3B2/300 AND 310 COMPUTERS HAVE 4 SLOTS. 3B2/400 COMPUTER HAS 12 SLOTS.
5. HARD DISK DRIVE 1 IS MOUNTED IN THE 3B2 COMPUTER CABINET ONLY FOR 3B2/400. FOR 3B2/300 and 310, DRIVE 1 IS MOUNTED IN AN AT&T/XM.

Figure 3-1: 3B2/300/310/400 Computer — High-Level Functional Block Diagram

Figure 3-2 is a high-level functional block diagram of the Version 3 3B2 computers (3B2/500, 600, 700, and 1000). The following is a list of the major functional areas of Version 3 computers:

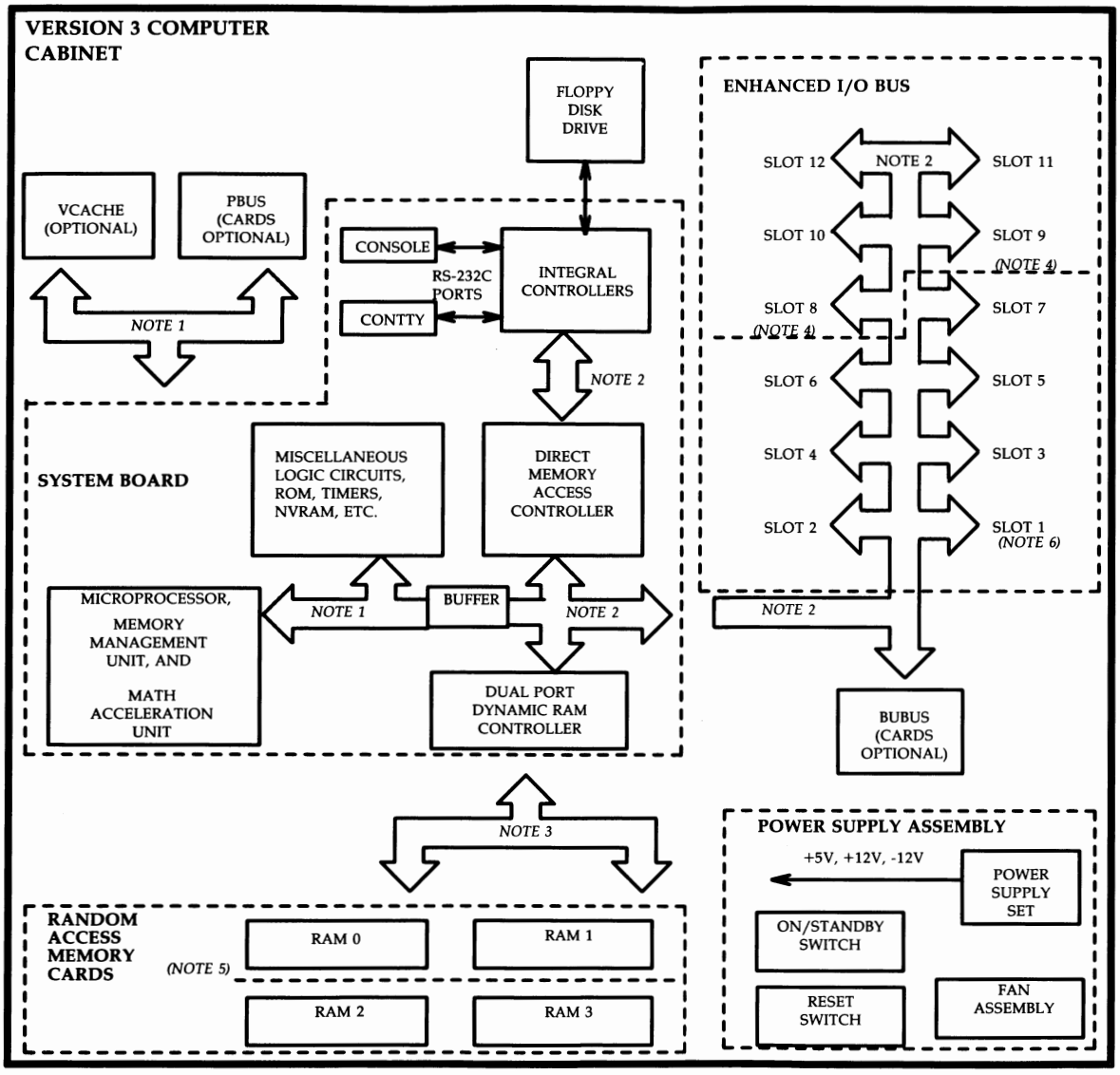
- Central Processing Unit (CPU) Microprocessor
- Memory Management Unit (MMU)
- Math Acceleration Unit (MAU)
- Dual Port Dynamic Random Access Memory (DPDRAM) Subsystem
- Direct Memory Access (DMA) Subsystem
- Enhanced Input/Output (EIO) Bus
- Feature Card Connectors
- Performance Card Connectors
- Miscellaneous Status and Control Signals
- Power and Alarm Circuits.



NOTES:

1. UNBUFFERED 32-BIT ADDRESS BUS AND 32-BIT DATA BUS.
2. BUFFERED 24-BIT ADDRESS BUS AND 16-BIT DATA BUS.
3. 32-BIT DATA BUS PLUS BYTE PARITY.
4. 3B2/500 COMPUTER HAS 7 SLOTS. OTHER VERSION 3 COMPUTERS HAVE 12 SLOTS.
5. 3B2/500 COMPUTER HAS 2 MEMORY SLOTS. OTHER VERSION 3 COMPUTERS HAVE 4 SLOTS.
6. SLOT 1 IS NORMALLY OCCUPIED BY THE SCSI HOST ADAPTER CONNECTED TO THE INTERNAL HARD DISK DRIVE(S) AND CARTRIDGE TAPE DRIVE (IF EQUIPPED).

Figure 3-2: Version 3 Computer — High-Level Functional Block Diagram



NOTES:

1. UNBUFFERED 32-BIT ADDRESS BUS AND 32-BIT DATA BUS.
2. BUFFERED 24-BIT ADDRESS BUS AND 16-BIT DATA BUS.
3. 32-BIT DATA BUS PLUS BYTE PARITY.
4. 3B2/500 COMPUTER HAS 7 SLOTS. OTHER VERSION 3 COMPUTERS HAVE 12 SLOTS.
5. 3B2/500 COMPUTER HAS 2 MEMORY SLOTS. OTHER VERSION 3 COMPUTERS HAVE 4 SLOTS.
6. SLOT 1 IS NORMALLY OCCUPIED BY THE SCSI HOST ADAPTER CONNECTED TO THE INTERNAL HARD DISK DRIVE(S) AND CARTRIDGE TAPE DRIVE (IF EQUIPPED).

Figure 3-2: Version 3 Computer — High-Level Functional Block Diagram

3B2 Computer Address Spectrum

Figures 3-3 and 3-4 show the 3B2 computer address spectrums for the Version 2 and Version 3 3B2 computers. As shown in Figure 3-3 and 3-4, the Physical Address (PA) scheme internal to the 3B2 computer uses a 27-bit address scheme (PA26—00). The most significant five bits (PA31—27) are not used. These unused bits are negated.

All input/output cards and other devices connected to the DMA Subsystem of the system board [Universal Asynchronous Receiver/Transmitters (UARTS), hard disks, DPDRAM size register, floppy disk, DMA controller] are accessed via the Byte Rotate Unit. The Byte Rotate Unit provides a hardware mechanism to transfer data to/from a 16-bit data bus from/to a 32-bit data bus while preserving byte placement within the word. Each feature card slot is assigned a unique 2-megabyte address range. Address space (2 megabytes per card) is reserved for unimplemented feature card slots 13, 14, and 15.

VERSION 2 COMPUTER ADDRESS SPECTRUM			
STARTING ADDRESS	DESCRIPTION	WIDTH	SIZE
0x 00000000	READ ONLY MEMORY (ROM)	32 BITS	64 KILOBYTES (NOTE 1)
0x 00040000	MEMORY MANAGEMENT UNIT (MMU)	—	—
0x 00041000	TIME-OF-DAY CLOCK	8 BITS	16 BYTES
0x 00042000	PROGRAMMABLE INTERVAL TIMER (8253)	8 BITS	4 BYTES
0x 00042010	CLEAR CSR BIT-6	1 BIT	1 BYTE
0x 00043000	NVRAM	4 BITS	1 KILONIBBLE
0x 00044000	CONTROL AND STATUS REGISTER (CSR)	16 BITS	2 BYTES (NOTE 2)
0x 00045000	DMA PAGE REGISTER 1 (HARD DISK)	8 BITS	1 BYTE
0x 00046000	DMA PAGE REGISTER 2 (UART A)	8 BITS	1 BYTE
0x 00047000	DMA PAGE REGISTER 3 (UART B)	8 BITS	1 BYTE
0x 00048000	INTEGRAL DMA CONTROLLER (9517)	8 BITS	16 BYTES
0x 00049000	UARTS (2681)	8 BITS	16 BYTES
0x 00049010	CLEAR UDMA INT.	8 BITS	1 BYTE
0x 0004A000	INTEGRAL HARD DISK CONTROLLER (2797)	8 BITS	2 BYTES
0x 0004B000	RESERVED	—	—
0x 0004C000	DPDRAM SIZE REGISTER	8 BITS	1 BYTE
0x 0004D000	FLOPPY DISK CONTROLLER (2797)	8 BITS	4 BYTES
0x 0004E000	DMA PAGE REGISTER 4 (FLOPPY)	8 BITS	1 BYTE
0x 0004F000	RESERVED	—	—
0x 00200000	FEATURE CARD SLOT 1	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00400000	FEATURE CARD SLOT 2	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00600000	FEATURE CARD SLOT 3	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00800000	FEATURE CARD SLOT 4	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00A00000	FEATURE CARD SLOT 5	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00C00000	FEATURE CARD SLOT 6	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00E00000	FEATURE CARD SLOT 7	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01000000	FEATURE CARD SLOT 8	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01200000	FEATURE CARD SLOT 9	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01400000	FEATURE CARD SLOT 10	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01600000	FEATURE CARD SLOT 11	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01800000	FEATURE CARD SLOT 12	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01A00000	FEATURE CARD SLOT 13	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01C00000	FEATURE CARD SLOT 14	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01E00000	FEATURE CARD SLOT 15	16 BITS	2 MEGABYTES (MAXIMUM)
0x 02000000	MAIN MEMORY (DPDRAM)	32 BITS	256 KILOBYTES TO 4 MEGABYTES (NOTE 3)

NOTES:

1. Size depends on which ROM device is used.
2. CSR requires 2 bytes to read, but is bit addressable for writing.
3. Size depends on size of memory card (256K/1 M/2 M) and the number of memory cards (1/2).

LEGEND:

CSR	Control and Status Register
DMA	Direct Memory Access
DPDRAM	Dual Port Dynamic Random Access Memory
NVRAM	Nonvolatile Random Access Memory
UARTS	Universal Asynchronous Receiver/Transmitters

Figure 3-3: Version 2 Computer Address Spectrum

VERSION 3 COMPUTER ADDRESS SPECTRUM			
STARTING ADDRESS	DESCRIPTION	WIDTH	SIZE
0x 00000000	READ ONLY MEMORY [(EP)ROM]	32 BITS	128 KILOBYTES
0x 00040000	FLOPPY CONTROL STATUS REGISTER	8 BITS	1 BYTE
0x 00041000	TIMER	—	—
0x 00042000	NVRAM	8 BITS	2 KILOBYTES
0x 00044000	CONTROL AND STATUS REGISTER (CSR)	32 BITS	4 BYTES (NOTE 1)
0x 00045000	FLOPPY DMA PAGE REGISTER	12 BITS	—
0x 00046000	UARTA DMA PAGE REGISTER	12 BITS	—
0x 00047000	UARTB DMA PAGE REGISTER	12 BITS	—
0x 00048000	DMA CONTROLLER (9517)	8 BITS	—
0x 00049000	UARTS (2681)	8 BITS	16 BYTES
0x 0004A000	FLOPPY CONTROLLER (1793)	8 BITS	2 BYTES
0x 0004B000	RESERVED (NOTE 2)	—	—
0x 0004C000	FAULT REGISTER 1	32 BITS	4 WORDS
0x 0004D000	FAULT REGISTER 2	32 BITS	1 WORD
0x 0004E000	TIME-OF-DAY CLOCK	4 BITS	—
0x 0004F000	MEMORY MANAGEMENT UNIT (MMU)	—	—
0x 00200000	FEATURE CARD SLOT 1	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00400000	FEATURE CARD SLOT 2	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00600000	FEATURE CARD SLOT 3	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00800000	FEATURE CARD SLOT 4	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00A00000	FEATURE CARD SLOT 5	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00C00000	FEATURE CARD SLOT 6	16 BITS	2 MEGABYTES (MAXIMUM)
0x 00E00000	FEATURE CARD SLOT 7	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01000000	FEATURE CARD SLOT 8	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01200000	FEATURE CARD SLOT 9	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01400000	FEATURE CARD SLOT 10	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01600000	FEATURE CARD SLOT 11	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01800000	FEATURE CARD SLOT 12	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01A00000	RESERVED	16 BITS	2 MEGABYTES (MAXIMUM)
0x 01C00000	UBUS CONNECTOR	16 BITS	2 MEGABYTES (MAXIMUM)
0x 02000000	MAIN MEMORY	32 BITS	64 MEGABYTES (NOTE 3)
0x 06000000	BUBUS CONNECTOR 1	16 BITS	64 MEGABYTES
0x 0A000000	BUBUS CONNECTOR 2	16 BITS	64 MEGABYTES
0x 0E000000	BUBUS CONNECTOR 3	16 BITS	64 MEGABYTES
0x 12000000	BUBUS CONNECTOR 4	16 BITS	64 MEGABYTES
0x C0F00000	HW, SW DEVELOPMENT SYSTEM	—	1 MEGABYTE
0x C1000000	RESERVED FOR DIAGNOSTICS	—	1 MEGABYTE

NOTES:

1. All the bits are settable and clearable by software.
2. Accessing this address returns neither DTACK nor SRDY signals.
3. 64 megabytes maximum. Actual size depends on size of memory card (2 M/4 M/16 M) and the number of memory cards (1/2/3/4).

LEGEND:

BUBUS	Buffered Microbus
CSR	Control and Status Register
DMA	Direct Memory Access
NVRAM	Nonvolatile Random Access Memory
UARTS	Universal Asynchronous Receiver/Transmitters
UBUS	Unbuffered Microbus

Figure 3-4: Version 3 Computer Address Spectrum

Input/Output Bus System

Input/Output Bus System Features

The Input/Output (I/O) bus system is an asynchronous, nonmultiplexed bus providing a flexible interface for feature cards. The system can directly address up to 16 megabytes on this bus via 24-bit address and either 8-bit or 16-bit data transfers. Other features include three interrupt priority levels and a single level of "distributed" bus arbitration.

The I/O bus system also supports a special Multiple Access Transfer Cycle in which more than one data transfer (bus access) can be made by the same feature card in a single bus cycle. After a feature card receives a bus acknowledge signal, the feature card can hold the I/O bus for no more than 4 microseconds. Multiple accesses are executed without bus arbitration and are thus a high performance consideration. A maximum of 4 data half-words can be transferred per one arbitration.

The Version 3 computers have an enhanced I/O bus. This bus supports sequential access—a subset of multiple word transfers. Up to 32 data transfers may be done simultaneously using the sequential access mode.

Peripheral Controllers

Peripheral controllers are feature cards connected to the system board via the I/O bus. There are two types of peripheral controller feature cards that connect to the I/O bus: programmed and intelligent. Feature cards requiring only power and ground connections are passive cards. Intelligent controllers can use a Bus Abort Feature (BAF) to prevent the INTEL 80186 Microprocessor from being locked up while waiting for an I/O bus request to be acknowledged. Not all intelligent controllers require the use of the BAF.

Programmed Controllers. Programmed controllers are feature cards containing programmable registers that can be written or read by the system board CPU. These feature cards have limited "on card" intelligence and operate in response to programming by the system board CPU. Programmed controllers are generally slave devices with respect to the system board CPU. After programming by the system board CPU, these types of feature cards can for example be a bus master.

Feature cards functioning as programmed controllers can provide the following:

- An 8- or 16-bit Feature Card Identification (ID) Code register. This register uniquely identifies the card and is intended to be read by the system board. The size of the register is determined by the word size of the feature card. The 8-bit feature cards use an 8-bit ID code register; 16-bit feature cards use a 16-bit ID code register.
- An optional feature card control register of up to 16 bits.
- An optional feature card status register of up to 16 bits.
- An optional 8-bit interrupt vector register. Any feature card with the capability to interrupt the system board CPU responds with a vector when the interrupt request is acknowledged.

Intelligent Controllers. Intelligent controllers are feature cards containing one or more microprocessors that are capable of autonomously executing programs stored on the cards. The use of intelligent feature cards is a major factor in achieving the high performance capabilities of a 3B2 computer. Intelligent feature cards use request and completion queues to communicate with the system board CPU. Most of the 3B2 computer feature cards are intelligent controllers. The Common Input/Output (CIO) architecture of intelligent controllers includes the following:

- Central Processing Unit (CPU)
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Onboard Random Access Memory (RAM)
- Onboard Read Only Memory (ROM)
- Miscellaneous Support Logic.

Bus Abort Feature. The Bus Abort Feature (BAF) is a defensive measure against the loss of data from a serial port. Since memory is a shared resource, the peripheral controller can be prevented from rapidly accessing the I/O bus. When a peripheral controller can not rapidly access the I/O bus, serial port data can be lost. To prevent this, intelligent controllers can abort the bus request cycle and resume autonomous processing.

Intelligent controllers use an INTEL 80186 Microprocessor. Timer 1 of the 80186 Microprocessor is used as a bus timer. This timer is reset at the start of each bus cycle. If a bus access cycle fails to complete within the programmed interval, the timer forces a ready condition to the 80186 Microprocessor. This sets the Peripheral Control and Status Register bit 6 (internal timer interrupt).

The 80186 Microprocessor bus cycle is aborted by the bus time-out; however, the bus request is still active. Therefore, the I/O bus cycle continues after the bus time-out until a bus acknowledge is received. Following the bus time-out, the 80186 Microprocessor does not use the I/O bus until the "dummy" read cycle is complete. The "dummy" read cycle is executed in response to the bus acknowledge for the pending bus request.

Input/Output Bus Structure

The system board CPU I/O bus consists of a 32-bit address bus, a 32-bit data bus, and a control bus. The I/O bus as applied to the feature card slots is an asynchronous, nonmultiplexed bus consisting of a 16-bit data, 24-bit address leads, and miscellaneous control and status leads. Figure 3-5 summarizes the I/O bus signals.

INPUT/OUTPUT BUS SIGNALS			
NAME	SIGNAL	SOURCE	TYPE
PHYSICAL ADDRESS	PPA23—00[1]	BIDIRECTIONAL	TRI-STATE
PHYSICAL ADDRESS STROBE	PPAS[0]	BIDIRECTIONAL	TRI-STATE
DATA	PD15—00[1]	BIDIRECTIONAL	TRI-STATE
DATA STROBES	PDS1—0[0]	BIDIRECTIONAL	TRI-STATE
READ/WRITE	PR[1]W[0]	BIDIRECTIONAL	TRI-STATE
DATA ACKNOWLEDGE	PDTACK[0]	BIDIRECTIONAL	OPEN COLLECTOR
DATA WIDTH	PSIZE16[0]	FEATURE CARD	OPEN COLLECTOR
FEATURE CARD FAILURE	PFAIL[0]	FEATURE CARD	OPEN COLLECTOR
BUS FAULT	PFLT[0]	BIDIRECTIONAL	OPEN COLLECTOR
BUS REQUEST	PBRQ[0]	FEATURE CARD	OPEN COLLECTOR
BUS ACKNOWLEDGE	PBACK[0]	SYSTEM BOARD	TOTEM POLE
BUS BUSY	PBUSY[0]	FEATURE CARD	TRI-STATE
INTERRUPT REQUEST	PINT2—0[0]	FEATURE CARD	OPEN COLLECTOR
INTERRUPT ACKNOWLEDGE	PIAK2—0[0]	SYSTEM BOARD	TOTEM POLE
FEATURE CARD SELECT	PCS12—01[0]	SYSTEM BOARD	TOTEM POLE
SYSTEM RESET	SYSRST[0]	SYSTEM BOARD	TOTEM POLE
SYSTEM RESET REQUEST	RQRST[0]	FEATURE CARD	OPEN COLLECTOR
+12V	V12P	SYSTEM BOARD	POWER
-12V	V12N	SYSTEM BOARD	POWER
+5V	VCC	SYSTEM BOARD	POWER
BACKUP BATTERY	VBKUP	SYSTEM BOARD	POWER
GROUND	GRD	SYSTEM BOARD	GROUND

Figure 3-5: Input/Output Bus Signals

Address Bus Signals—PPA23-00[1]. The 24 bidirectional (tri-state) address leads provide a maximum direct address capability of 16 megabytes.

Note: For Version 2 computers, the two-most significant address bus bits (bits 23 and 22) are reserved and must always be equal to logical signal zero by all peripherals. Therefore, the actual peripheral address capability used is 4 megabytes.

Data Bus Signals—PD15-00[1]. The 16 bidirectional (tri-state) data leads provide for byte or half-word data transfer.

Control Bus Signals. The Control Bus signals include status, strobes, feature card select, interrupts, error detection, and reset signals. The status signals identify the type of bus cycle (read or write) and the word width (8 or 16 bits) of a feature card. Strobes are used to control the transfer of data.

PBUSY[0] The Peripheral Bus Busy (PBUSY) signal is asserted by a feature card after receipt of a bus acknowledge (PBACKIO). PBUSY is asserted during the entire bus cycle to notify all other feature cards that the I/O bus is being used. PBUSY allows multiple accesses by the same bus master without relinquishing control of the bus between data transfers. The maximum of four transfers in one 8 microseconds I/O bus cycle is allowed.

PCS12—01[0] The Peripheral Card (Chip) Select (PCS) signals are asserted by the system board to enable (select) the feature cards. For the 3B2/400, 600, 700, and 1000 computers, 12 peripheral chip selects (PCS12—01) are used. For the 3B2/500 computer, 7 peripheral chip selects (PCS07—01) are used. For the 3B2/300 and 310 computers, only 4 peripheral chip selects (PCS04—01) are used. PCS00[0] is decoded but has no connection.

PDS1—0[0] The Peripheral Data Strobe (PDS) signals are asserted by the bus master to select which bytes of the 16-bit data bus are to be enabled. PDS0[1] enables byte 0 (data bits 15—08); PDS1[1] enables byte 1 (data bits 07—00).

PDTACK[0] The Peripheral Data Acknowledge (PDTACK) signal is asserted by the bus slave to acknowledge the receipt of valid write data or to indicate the presence of valid read data on the I/O bus. A feature card that has requested a system board CPU interrupt also asserts the PDTACK in response to the Peripheral Interrupt Acknowledge (PIAK) asserted by the system board.

PPAS[0] The Peripheral Physical Address Strobe (PPAS) is asserted by the bus master to indicate the presence of a valid physical address on the I/O bus.

PR[1]W[0] The Peripheral Read/Write (PR[1]W[0]) signal is asserted or negated by the bus master to indicate the type of access (read or write). A logic 1 indicates a read operation; a logic 0 indicates a write operation.

PSIZE16[0] The PSIZE16 signal specifies the width of the bus interface for the feature card as either 16 bits (logic 0) or 8 bits wide (logic 1). For 8-bit peripherals, data will be transferred on data bits 07—00.

RQRST[0] The Request System Reset (RQRST) signal is asserted by a feature card to request a system reset.

SYSRST[0] The System Reset (SYSRST) signal is asserted in response to a manual reset, system powerup sequence, a software request, or the RQRST[0] signal.

PBRQ[0] The Peripheral Bus Request (PBRQ) is asserted by a feature card to gain access to the I/O bus. The bus arbitration circuits on the system board handle the bus request.

PBACKI[0]/PBACKO[0]
The system board asserts a Peripheral Bus Acknowledge Output (PBACKO) signal to acknowledge a feature card bus request. This signal is daisy-chained to all

feature cards. The Peripheral Bus Acknowledge Input (PBACKI) enters a feature card. The PBACKO exits a feature card. The first feature card in the chain (feature card slot 1 to n) wanting bus access inhibits the propagation of the acknowledge signal and asserts a PBUSY[0] signal.

PINT2—0[0] Three peripheral interrupt signals are logically OR'ed from all input/output bus devices (PINT2—0[0]). A feature card connects to only one of these three interrupts. PINT2 is the highest priority of the three interrupts. A feature card asserts the appropriate PINT signal to request an interruption of the system board CPU (request for service). PINT2 is reserved for use by AT&T designs.

PIAKI2—0[0]/PIAKO2—0[0]
The system board CPU asserts the appropriate Peripheral Interrupt Acknowledge (PIAK2—0[0]) signal to respond to the receipt of a Peripheral Interrupt (PINT) request. The acknowledge signals are daisy-chained through all feature cards. The Peripheral Interrupt Acknowledge Input (PIAKI) signal enters a feature card. The Peripheral Interrupt Acknowledge Output (PIAKO) signal exits a feature card. A feature card requesting an interrupt of the system board CPU inhibits the propagation of the interrupt acknowledge signal and asserts a Peripheral Data Acknowledge (PDTACK[0]) signal during the normal bus protocol operation.

PFAIL[0] The Peripheral Fail (PFAIL) signal is asserted by a feature card to report a failure on the card.

PFLT[0] The Peripheral Fault (PFLT) signal is asserted by the bus slave to report the detection of an erroneous condition during an I/O bus cycle (for example, bus time-out).

MOS Data Bus. The ED-4C637-30 system board buffers the lower 8 bits of the I/O data bus (D07—00[1]) to create an MOS Data Bus. The MOS Data Bus serves the low power devices that cannot drive the TTL inputs over the entire data bus. The MOS Data Bus serves the following:

- Read Only Memory (ROM)
- Timers
- Time-of-Day (TOD) Clock
- Nonvolatile Random Access Memory (NVRAM).

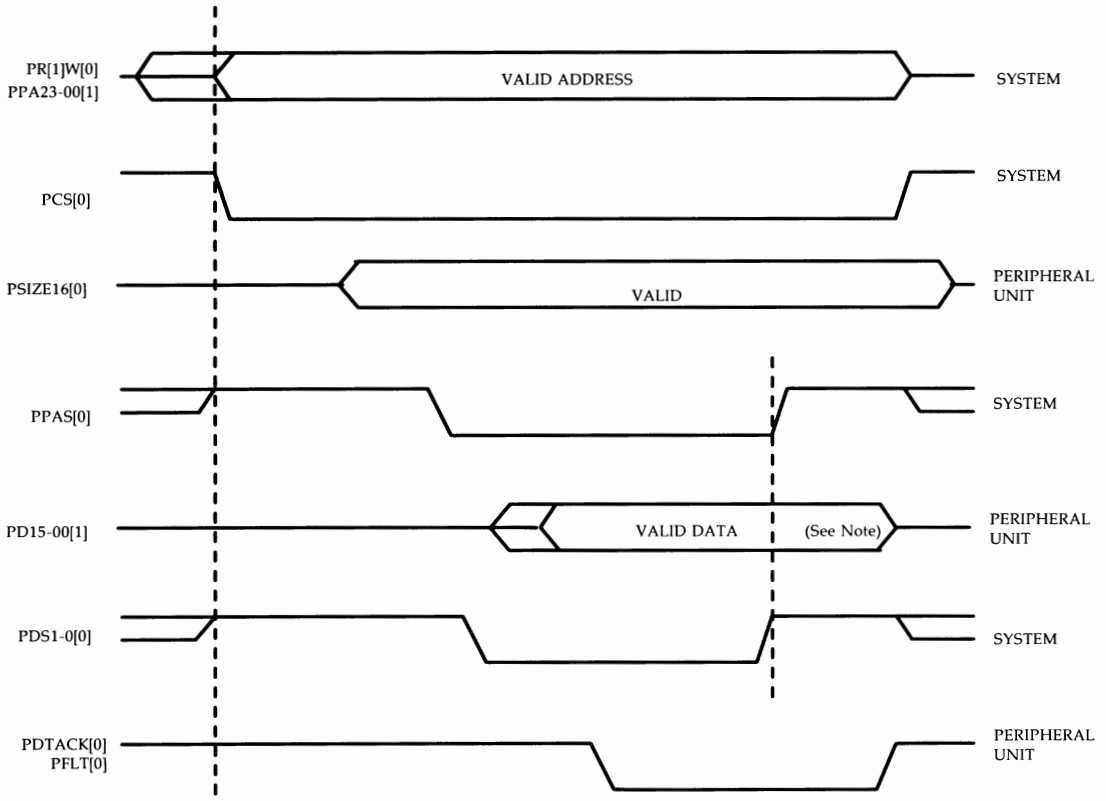
The ROM is an exception to the other devices connected to the MOS Data Bus. The ROM also connects to the data bus bits 31—08; however, only data bus bits 07—00 are connected via the MOS Data Bus (buffered).

Data Transfers

Data transfers can be categorized into the following operations:

- Main memory read operation by a feature card
- Main memory write operation by a feature card
- Feature card read operation by the system board
- Feature card write operation by the system board.

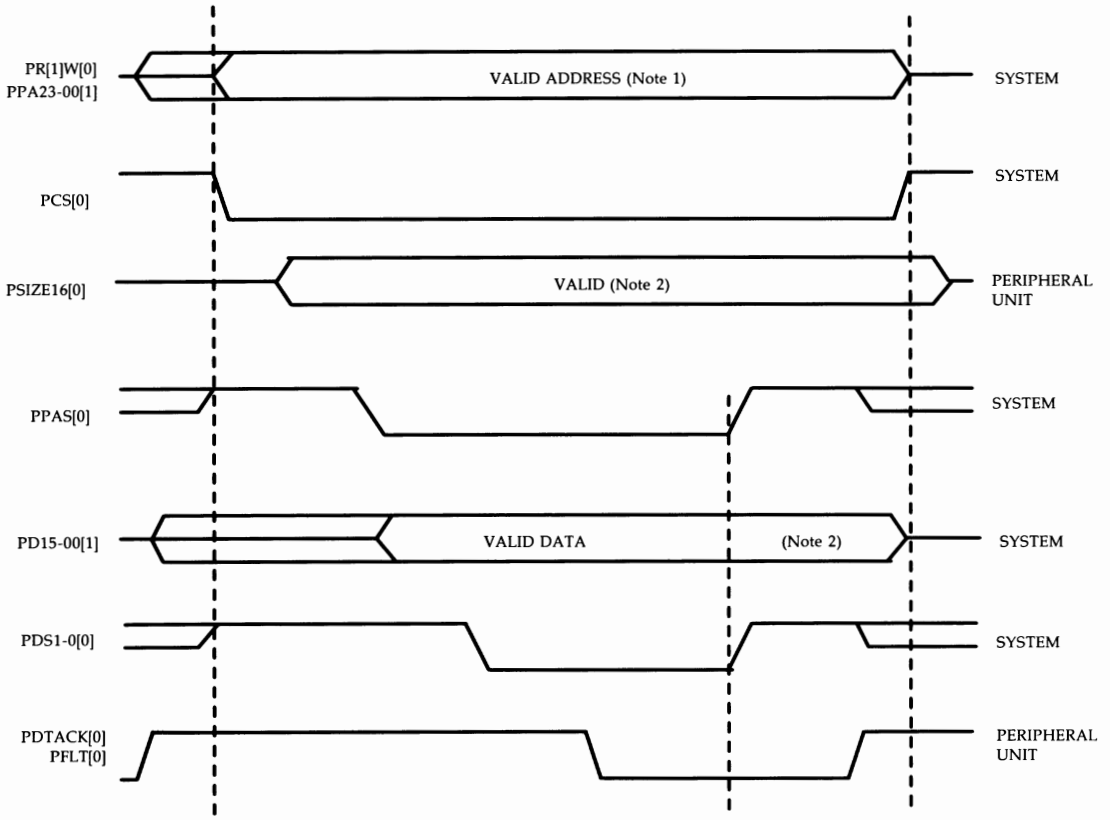
System Board Peripheral Controller Read Operation. Figure 3-6 shows the system board peripheral controller read operation. A system board CPU read operation of a peripheral controller (feature card) starts with the Peripheral Read/Write signal (PR1W0) (Read=1), Peripheral Physical Address signals (PPA23-00[1]), and the Peripheral Card (Chip) Select signal (PCS) occurring simultaneously. The selected feature card sends the PSIZE16[0] signal to define its data width (8 bits=1, 16 bits=0) in response to the PCS[0] signal. The system board CPU sends the Physical Address Strobe (PPAS[0]) to the feature card when the address lines (PPA23-00[1]) are stable. The Peripheral Data Strobes (PDS01-00[0]) are sent to the feature card to select the data byte(s) to be returned during the data bus transaction. The feature card sends the data via the Peripheral Data bus (PD15-00[1] for 16-bit peripherals or PD07-00[1] for 8-bit peripherals) and sends the Peripheral Data Transfer Acknowledge (PDTACK[0]) signal after a minimum data setup time. The system board relinquishes the bus by driving the address and data strobes inactive (high=1) and then tri-stating all of its I/O bus signals. The feature card relinquishes the bus when it sees the inactive address and data strobes.



Note: Data is valid at system board for at least 20 nanoseconds before PDTACK[0].

Figure 3-6: System Board Peripheral Controller Read Operation

System Board Peripheral Controller Write Operation. Figure 3-7 shows the system board peripheral controller write operation. A system board CPU write operation of a peripheral controller (feature card) starts with the Peripheral Read/Write signal (PR1W0) (Write=0), Peripheral Physical Address signals (PPA23-00[1]), and the Peripheral Card (Chip) Select signal (PCS[0]) occurring simultaneously. The selected feature card sends the PSIZE16[0] signal to define its data width (8 bits=1, 16 bits=0) in response to the PCS[0] signal. The system board CPU sends the Physical Address Strobe (PPAS[0]) to the feature card when the address lines (PPA23-00[1]) are stable. The system board CPU puts the data to be written to the feature card on the Peripheral Data bus (PD15-00[1]). The Peripheral Data Strobes (PDS01-00[0]) are sent to the feature card to indicate which data byte(s) were placed on the 16-bit data bus. The feature card sends the Peripheral Data Transfer Acknowledge (PDTACK[0]) signal after getting the write data from the data bus. As with a read operation, the system board releases the bus after receiving the PDTACK[0] signal by driving the strobes inactive and tri-stating the bus. The feature card relinquishes the bus when it sees the inactive (high=1) strobes.



Note 1: PSIZE16[0] must be valid at system board for at least 20 nanoseconds before PDS1-0[0].

Note 2: Data and address are valid for at least 10 nanoseconds after PDS1-0[0] and PPAS[0] raising edge, respectively.

Figure 3-7: System Board Peripheral Controller Write Operation

Peripheral Controller Main Memory Read Operation. Figure 3-8 shows the peripheral controller main memory read operation. A main memory read by a peripheral controller (feature card) starts with the feature card asserting an I/O bus access request (PBRQ[0]). When the feature card receives the Peripheral Bus Acknowledge (PBACK[0]), the feature card asserts the Peripheral Bus Busy (PBUSY[0]) signal. The feature card gates the following signals onto the I/O bus to start the data transfer:

- Physical Address (PA23—00[1])
- Peripheral Read/Write (PR[1]W[0]) (1 for read operation)
- Peripheral Size (PSIZE16[0]).

When the address and control signals are stable, the Peripheral Physical Address Strobe (PPAS[0]) and Peripheral Data Strobes (PDS1—0[0]) are asserted. The PBRQ is negated after the data transfer operation has started (following assertion of the PPAS and negation of PBACK). The assertion of the Peripheral Data Strobes causes the main memory to gate the read data onto the I/O bus. When the read data is stable, the main memory asserts the Peripheral Data Acknowledge (PDTACK[0]) signal and the feature card latches the data. The feature card negates the address, strobes, and bus busy signals and then tri-states the I/O bus. The main memory control negates the PDTACK signal and the data when the data strobes are removed.

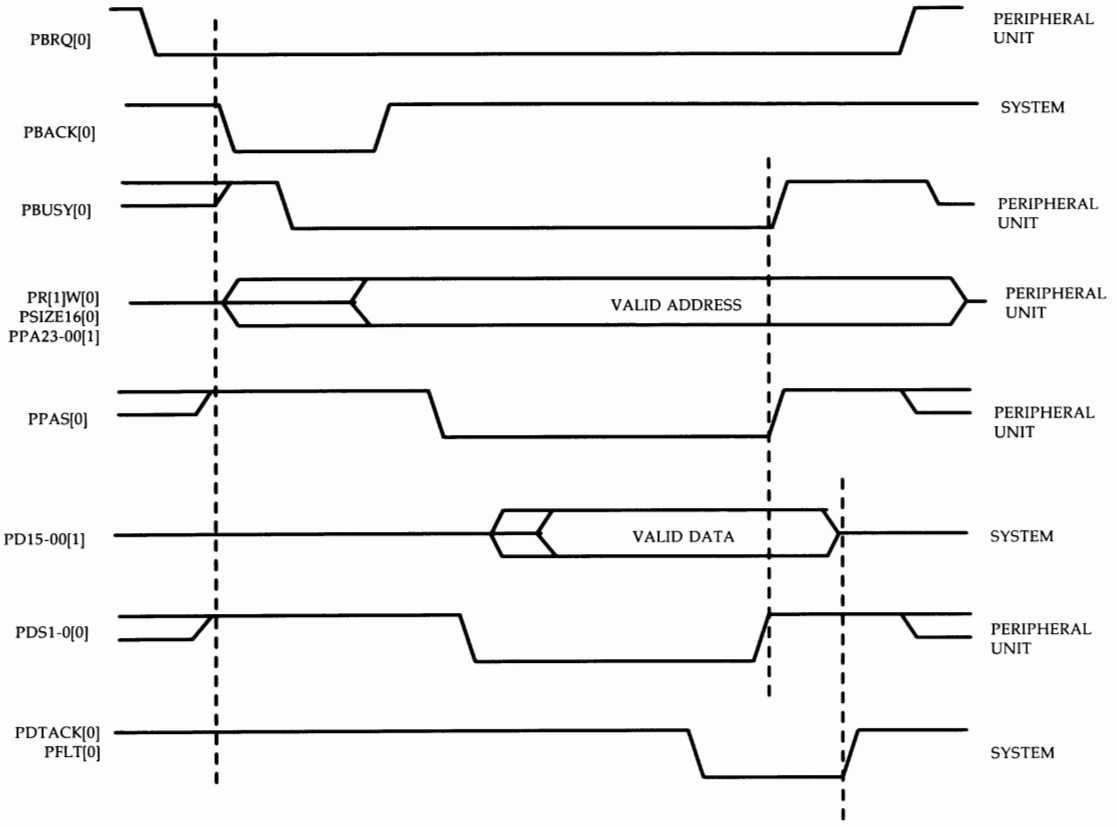


Figure 3-8: Peripheral Controller Main Memory Read Operation

Peripheral Controller Main Memory Write Operation. Figure 3-9 shows the peripheral controller main memory write operation. A main memory write by a peripheral controller (feature card) starts with the feature card asserting an I/O bus access request (PBRQ[0]). When the feature card receives the Peripheral Bus Acknowledge (PBACK[0]), the feature card asserts the Peripheral Bus Busy (PBUSY[0]) signal. The feature card gates the following signals onto the I/O bus to start the data transfer:

- Physical Address (PA23—00[1])
- Peripheral Read/Write (PR[1]W[0]) (0 for write operation)
- Peripheral Size (PSIZE16[0]).

When the address and control signals are stable, the Peripheral Physical Address Strobe (PPAS[0]) and Peripheral Data Strobes (PDS1—0[0]) are asserted. The PBRQ is negated after the data transfer operation has started (following assertion of the PPAS and negation of PBACK). The peripheral controller gates the write data onto the I/O bus Peripheral Data lines (PD15-00[1]). When the data is stable, the peripheral controller asserts the appropriate Peripheral Data Strobe(s). Then, the main memory latches the data and asserts the Peripheral Data Acknowledge (PDTACK[0]) signal. The feature card negates the strobes and bus busy signals and then tri-states the I/O bus. The main memory control negates the PDTACK signal when the data strobes are removed.

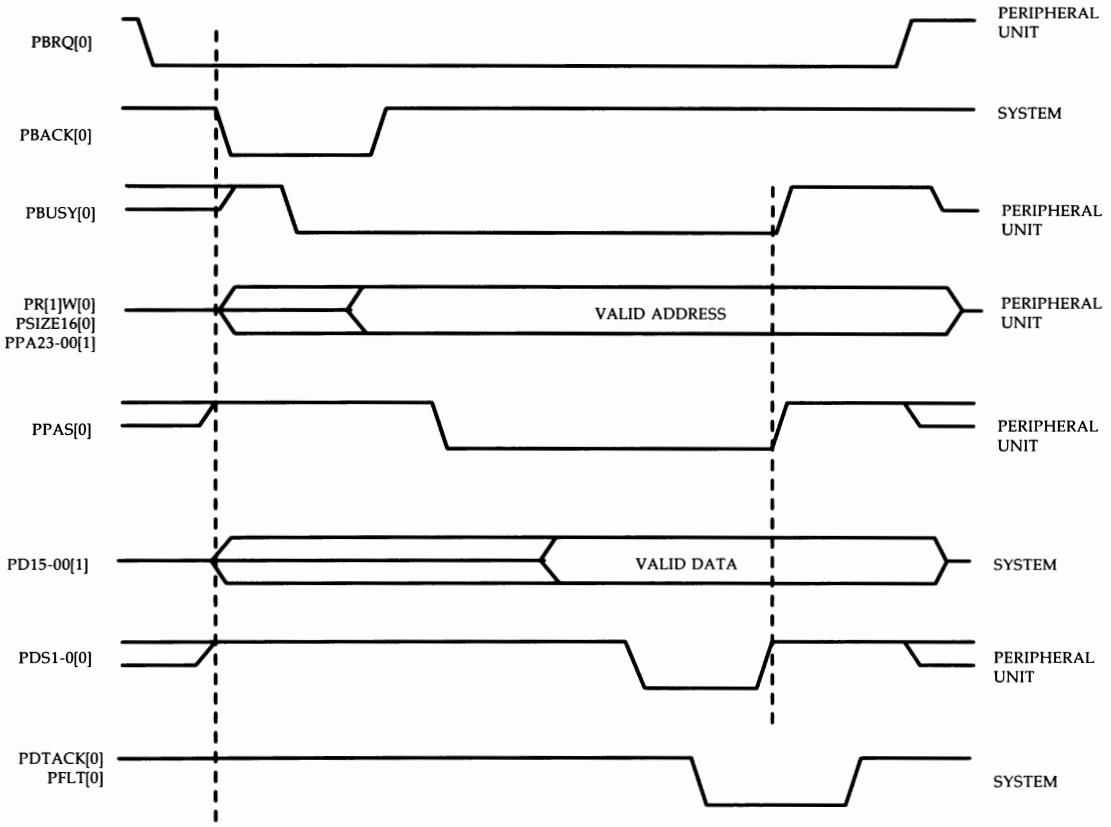


Figure 3-9: Peripheral Controller Main Memory Write Operation

Bus Arbitration

The main memory has two ports on the system board. One port is reserved for the system board (main) CPU. The other port is for the I/O bus. Access to the main memory is controlled by arbitration logic on the system board. This logic also handles the periodic refresh of the Dynamic Random Access Memory (DRAM). The arbitration logic prioritizes bus requests depending on the request source. The bus arbitration priorities are listed below:

- Memory refresh operation (highest priority)
- CPU to main memory interlock requests
- Integral floppy to main memory requests
- CPU to buffered microbus requests (includes CPU to memory)
- Buffered microbus to memory requests and feature card to memory requests (equal, rotating priority).

Any feature card can be the I/O bus master. Feature cards can only request access to the I/O bus for reading or writing main memory. A feature card requests other types of service (other than bus resources) from the system board CPU via an interrupt request. A typical scenario of how the feature card gains I/O bus access is as follows:

A feature card requests I/O bus access by asserting the Peripheral Bus Request (PBRQ[0]) signal. The PBRQ signal can only be asserted by a feature card if PBRQ is first inactive for a minimum of 80 nanoseconds. This delay provides a window sufficient for all feature cards to detect an inactive PBRQ. Similarly, the arbiter delays the assertion of the Peripheral Bus Acknowledge (PBACK[0]) signal for approximately 200 nanoseconds to provide enough time for all interested feature cards to request bus access and inhibit the Peripheral Bus Acknowledge (PBACK[0]) signal propagation. The PBACK[0] is daisy-chained through all feature cards. PBACKI[0] refers to the input acknowledge signal to a feature card. PBACKO[0] refers to the output acknowledge signal from a feature card. A feature card requesting bus access has 200 nanoseconds to block the PBACKI[0] from propagating to PBACKO[0] if the feature card wants to access the I/O bus. The feature card also asserts the Peripheral Bus Busy (PBUSY[0]) for the duration of the bus cycle. The PBACK signal is negated when the system board detects the PBUSY. The PBUSY signal notifies other feature cards that the I/O bus is in use.

When multiple feature cards request I/O bus access, the feature card physically closest to the system board has the first access. The feature card bus access priority is determined by the feature card location on the bus. Feature card slot 1 has the first access; feature card slot 12 has the last access. Bus access is shared in this sequence. Once a feature card slot has accessed the bus, it cannot regain bus access until all other slots requesting service have been accessed in sequence from 1 through 12.

For Version 3 computers, the buffered microbus slots have equal, rotating priority with the I/O bus slots. That is, if buffered microbus slot 0 has the bus now, I/O bus would have it next, followed by buffered microbus slot 1, I/O bus, buffered microbus slot 2, etc.

Multiple Input/Output Bus Accesses

More than one data transfer (bus access) can be done by the same feature card in one bus cycle. Multiple bus accesses are done without the need for additional bus arbitration. This feature is only applicable to feature cards; the system board cannot do multiple accesses on the I/O bus.

The Peripheral Bus Busy (PBUSY[0]) signal asserted by the feature card enables the feature card to maintain control of the I/O bus. The feature card can perform a maximum of four transfers without negating the PBUSY signal.

Input/Output Bus Interrupts

Three Peripheral Interrupt signals are logically OR'ed from all I/O bus devices (PINT2—0[0]). Three Peripheral Interrupt Acknowledge (PIAK) signals are daisy-chained through all I/O bus devices. PIAKI02—0[0] refers to the input acknowledge signal to a feature card. PIAKO02—0[0] refers to the output acknowledge signal from a feature card.

A feature card connects to only one of these three interrupt levels. PINT2[0] is the highest priority interrupt of these three interrupts. Peripheral controllers (feature cards) request service from the system board CPU by asserting a Peripheral Interrupt. The system board CPU acknowledges the request for service by sending a Peripheral Interrupt Acknowledge Input (PIAK) signal corresponding to the level of the peripheral interrupt being serviced.

The feature card requesting the interrupt responds to the PIAK by returning a vector and preventing the acknowledge signal from propagating further down the chain by holding PIAKO inactive. The acknowledged feature card then asserts a Peripheral Data Acknowledge (PDTACK[0]) signal to indicate a valid read of the I/O bus. The System Board CPU negates the PIAK in response to the PDTACK.

Error Detection

Two I/O bus signals are used for fault detection: Peripheral Fail (PFAIL[0]) and Peripheral Fault (PFLT[0]).

The PFAIL[0] signal is common to all feature cards. The signal is sent to report a card failure of any kind to the system.

The PFLT[0] signal is sent during a bus transaction by the slave when an erroneous condition, such as a bus time-out, is detected.

Self-Configuration

The self-configuration feature automatically rebuilds the operating system following changes in the Equipped Device Table (EDT) when the system is powered up or rebooted. Figure 3-10 shows the powerup sequence involving self-configuration. Figure 3-11 shows the manual boot sequence involving self-configuration.

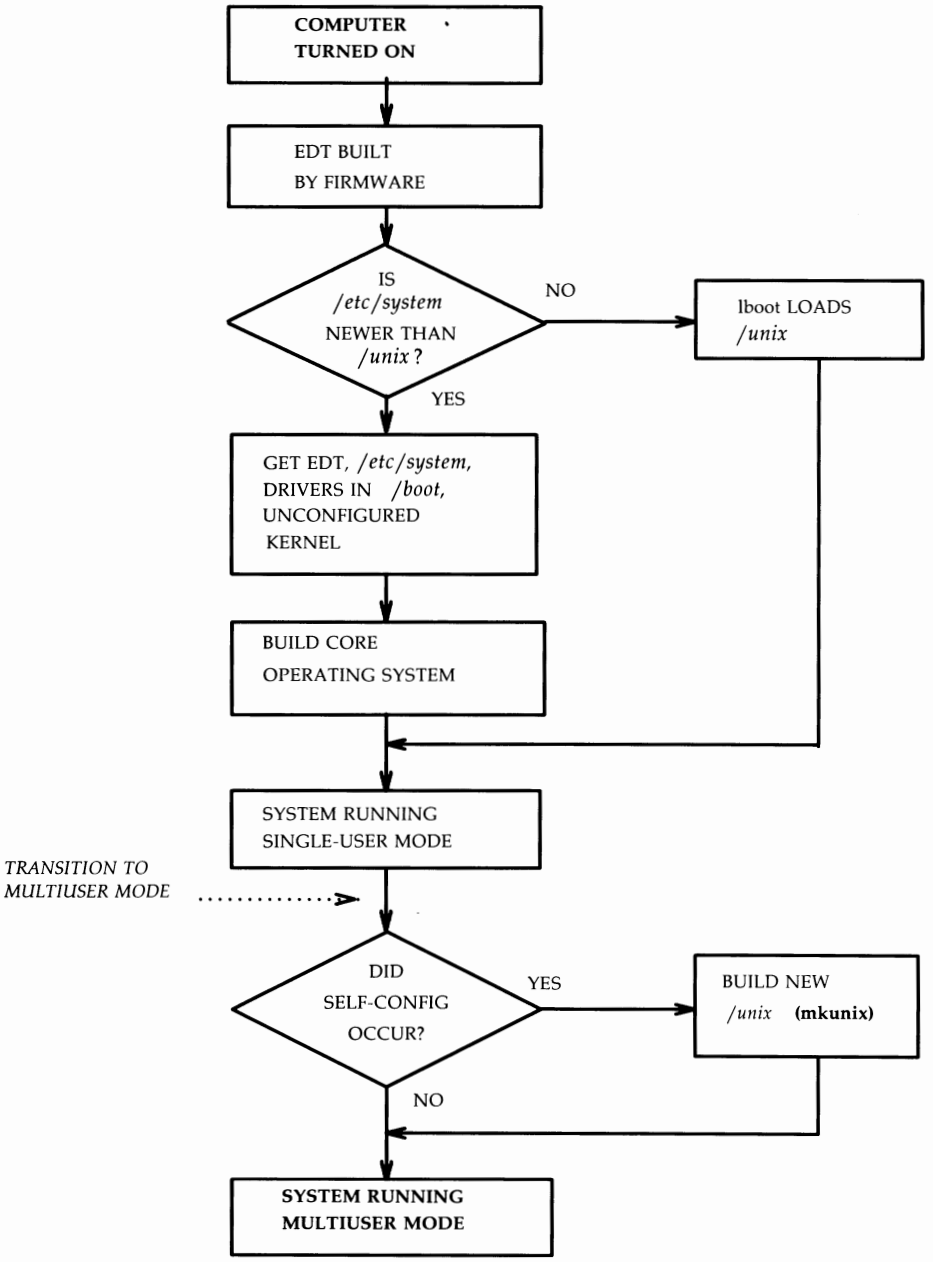


Figure 3-10: Self-Configuration — Powerup Sequence

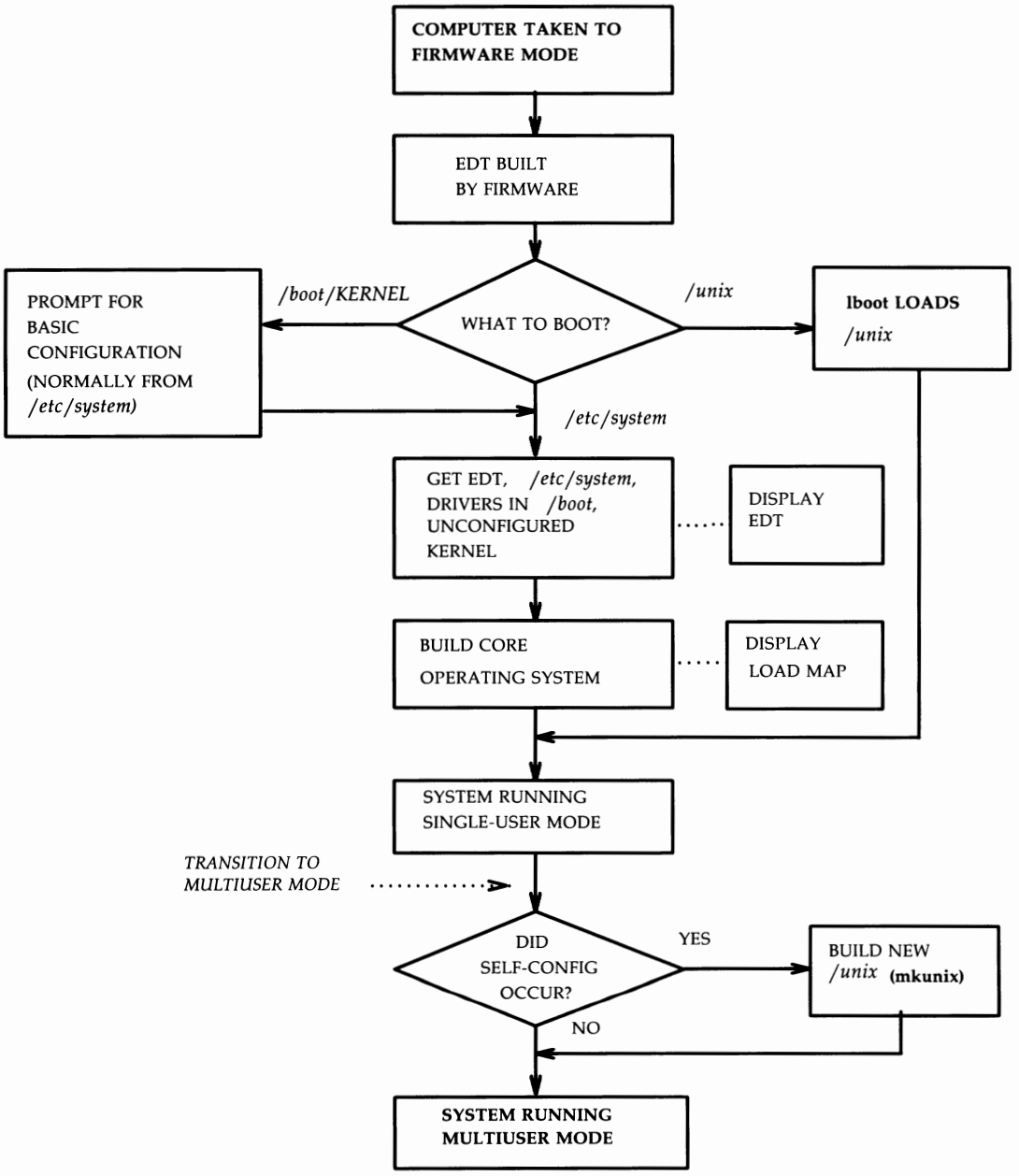


Figure 3-11: Self-Configuration — Manual Boot Sequence

Self-configuration is done by a combination of hardware, firmware, and software supplied functions. Figure 3-12 shows the self-configuration process. This process is also called auto-configuration. The self-configuration process begins with firmware examining the hardware and constructing an EDT in memory. The EDT contains information about the equipped devices. The firmware loads the **mboot** program from the boot block of the designated device into memory and executes the program. The **mboot** loads the **lboot** program from the boot device into memory and starts it running.

/unix	No reconfiguration is done if the date on */unix* is newer than the date on */etc/system*. A preconfigured kernel is loaded into memory and executed. This boot is faster than the self-configuration process.
/etc/system	The kernel is reconfigured when the system description file is booted.
/boot/KERNEL	Booting the */boot/KERNEL* file is similar to booting */etc/system* except no drivers are configured and the process is interactive. During the boot process you are asked to supply (input) information normally provided by the */etc/system* file.

Once the **lboot** program has examined the EDT and */etc/system* file, the proper drivers in the */boot* directory are included into the kernel. The load map of the new kernel is displayed when */etc/system* is booted. When the fully configured kernel is built in memory, the **lboot** program jumps to the starting address of the kernel.

When the operating system transitions to multiuser mode, a check is made to see if the system auto-configured. This check is done by the **/etc/ckauto** command in the */etc/rc.d/autoconfig* file. The core (memory) image of */unix* is copied to */unix* by **/etc/mkunix** when self-configuration occurs. The device nodes are automatically modified to match the hardware configuration as a function of each device driver.

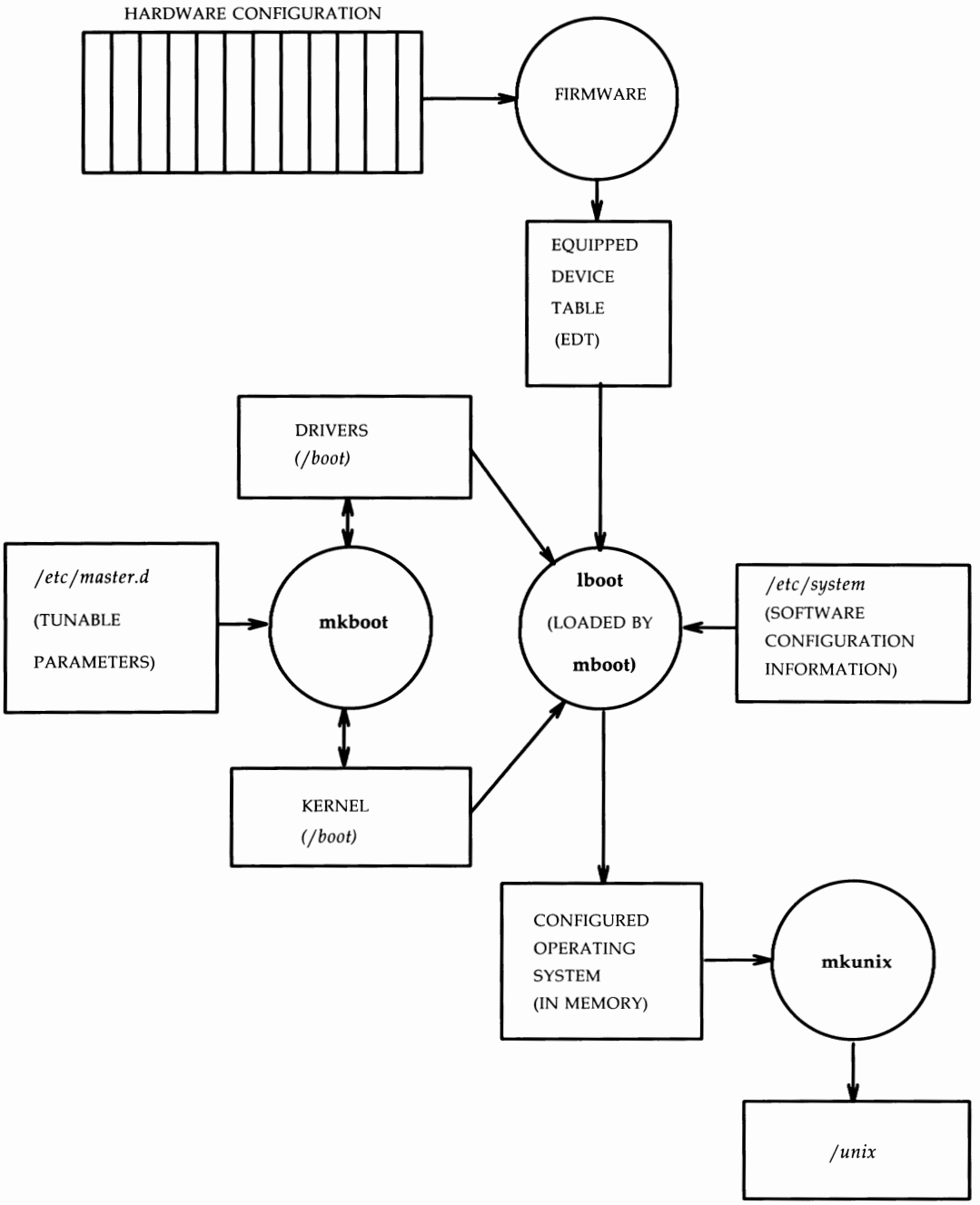


Figure 3-12: Self-Configuration Process

SYSTEM BOARDS

The Version 2 3B2 computers have a CM190A/ED-4C637-30 System Board. The Version 3 computers have a CM518A/B/C System Board. The two styles of system boards are discussed in the following sections.

CM190A/ED-4C637-30 System Board

Figure 3-13 is a functional block diagram of the Version 2 system board. The system board functional description is based primarily on the System Board, ED-4C637-30. Collectively, the 3B2 computer system board features are listed below:

- Central Processing Unit (CPU)
- Memory Management Unit (MMU)
- Math Acceleration Unit (MAU) (not supported on CM190A, optional on ED-4C637-30)
- Address decoding for 15 input/output card chip selects
- Time-of-Day (TOD), periodic, sanity, and bus timers
- 16-bit Control and Status Register (CSR)
- Eight interrupt levels (three levels for feature cards)
- Two RS-232C serial ports with data set control
- Direct Memory Access Controller (DMAC) for integral hard disk, integral floppy disk, and Universal Asynchronous Receiver/Transmitters (UARTs)
- 256 kilobytes to 4 megabytes of Dual Port Dynamic Random Access Memory (DPDRAM) with hardware refresh and per-byte parity
- Supports 8- and 16-bit feature cards
- Power reset of system board and feature cards
- "Soft power" control
- 1K by 4-bit Nonvolatile Random Access Memory (NVRAM)
- 3.6 volt DC lithium battery for NVRAM, TOD clock, and feature cards
- Supports dumb, programmed, and intelligent controller (feature) cards
- Supports feature card access of DPDRAM via daisy-chained Direct Memory Access (DMA) arbitration
- Supports programmed to control feature card access
- No option straps required for feature card addresses or interrupt vectors.

Early versions of the system board differ in the physical configuration of the CPU and MMU; however, except for the MAU capability and the system clock rate, the CM190A System Board is functionally equivalent to the System Board, ED-4C637-30. Refer to Chapter 2, Equipment Description, for information on the physical configuration of the CM190A System Board and System Board, ED-4C637-30.

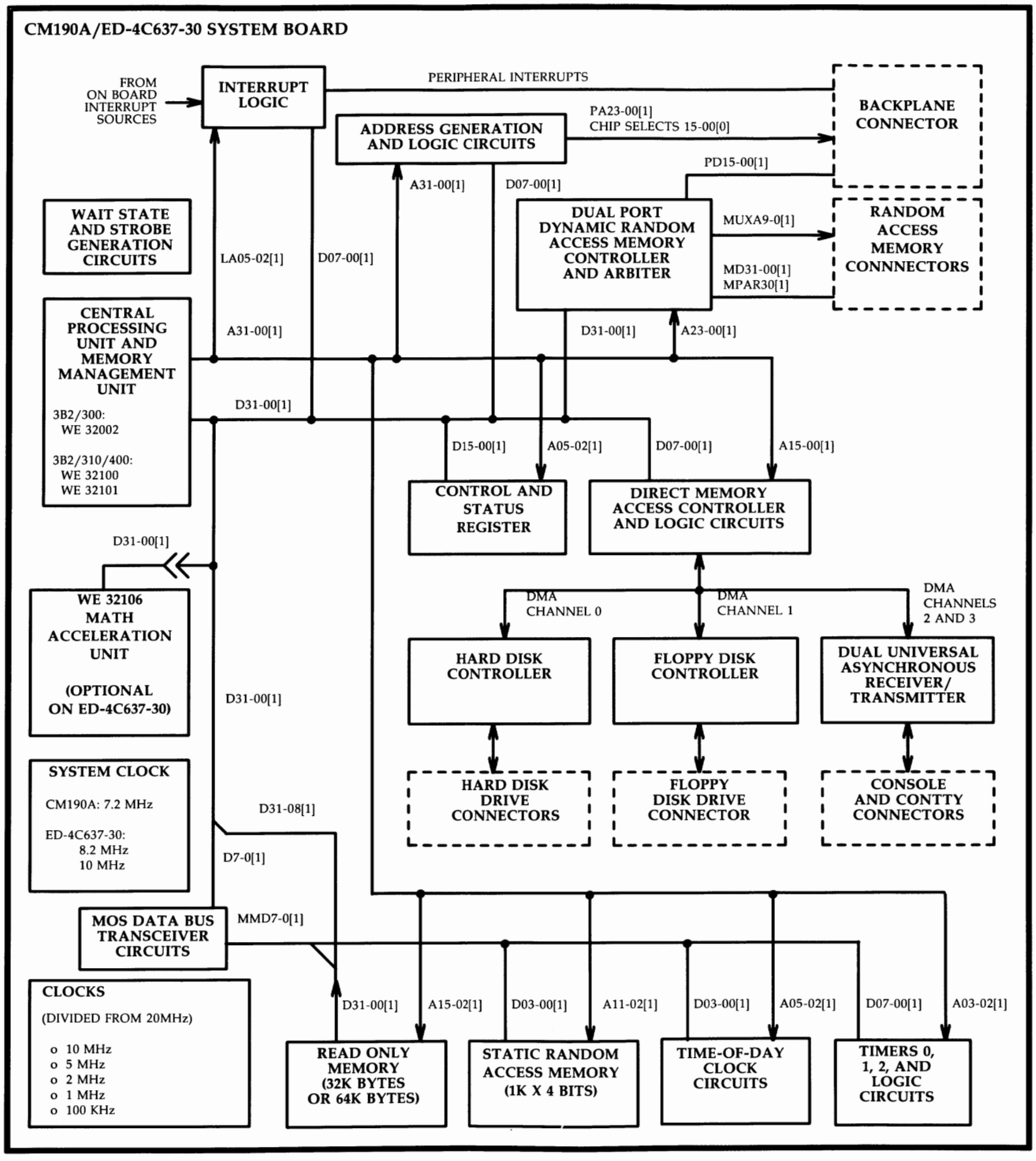


Figure 3-13: Version 2 3B2 Computer System Board — Functional Block Diagram

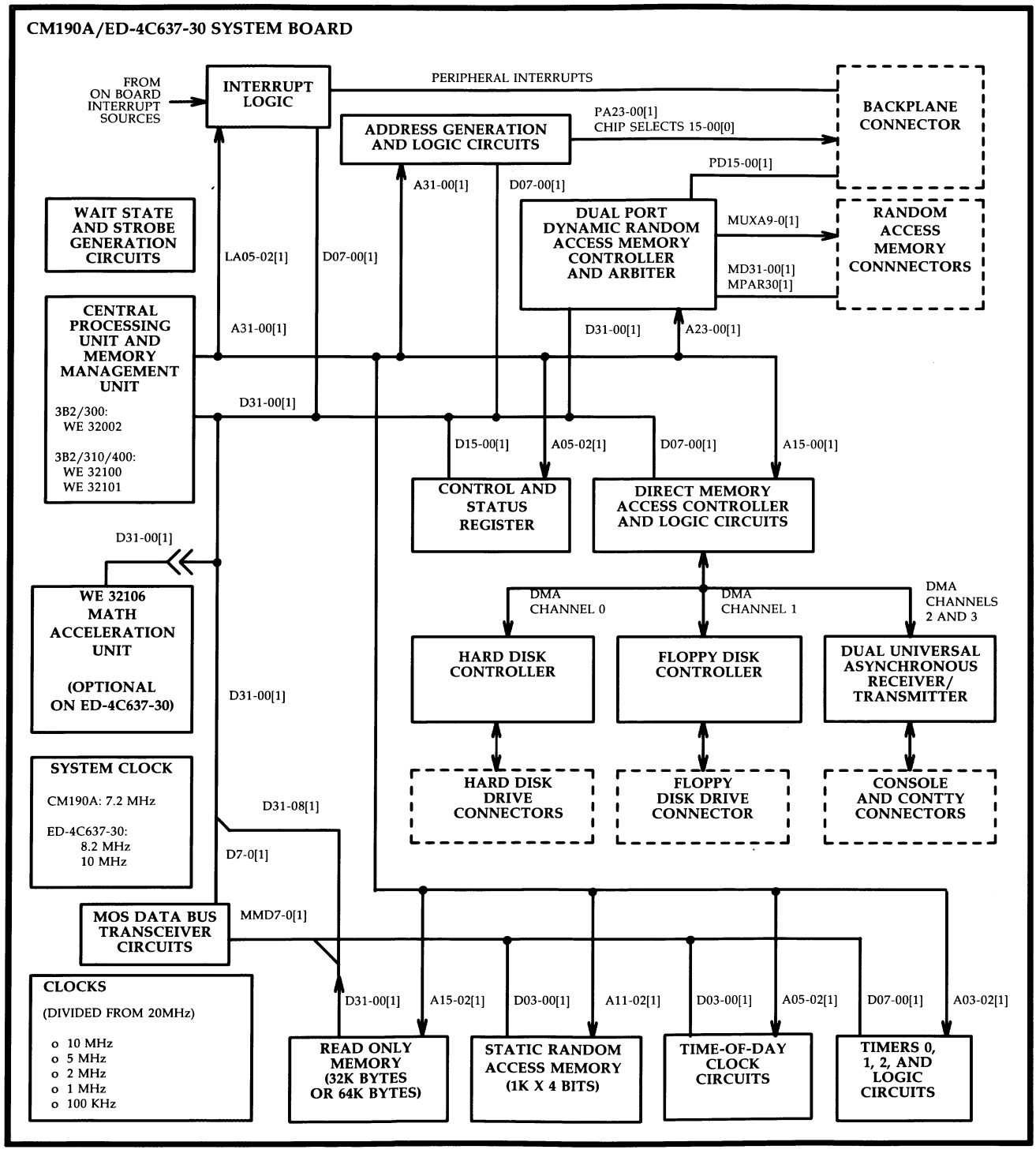


Figure 3-13: Version 2 3B2 Computer System Board — Functional Block Diagram

Central Processing Unit

The Central Processing Unit (CPU) on System Board, ED-4C637-30 is a WE 32100 Microprocessor. The CPU on a CM190A System Board is a WE 32002 Processor Module with Memory Management Unit. The CPU provides separate 32-bit address and data buses. The 32-bit address bus is used to address memory or peripherals mapped into the system memory space using physical or virtual addresses. Data is read to or written from the CPU over the 32-bit, bidirectional, data bus in either word (32-bit), half-word (16-bit) or byte (8-bit) widths. The CPU automatically expands bytes and half-words to words (32 bits) for processing. Zeros fill the high-order bits for unsigned operations. For signed operations, the sign bit (bit 7 for bytes, bit 15 for half-words) fills the high-order bits.

Instruction execution speed is enhanced by an internal instruction queue and an internal instruction cache. The instruction queue is an 8-byte, First-In-First-Out (FIFO) queue that stores prefetched instructions. The instruction cache is a 64-word cache used to increase the CPU performance by reducing the external memory reads for instruction fetches. When an instruction fetch from memory occurs, the instruction data is placed in both the instruction queue and the instruction cache. If the instruction data is needed again, it is read from the cache rather than from external memory.

Functionally, the system board CPU consists of bus interface control, main controller, fetch unit, and the execute unit circuits. Figure 3-14 shows a functional block diagram of the system board CPU.

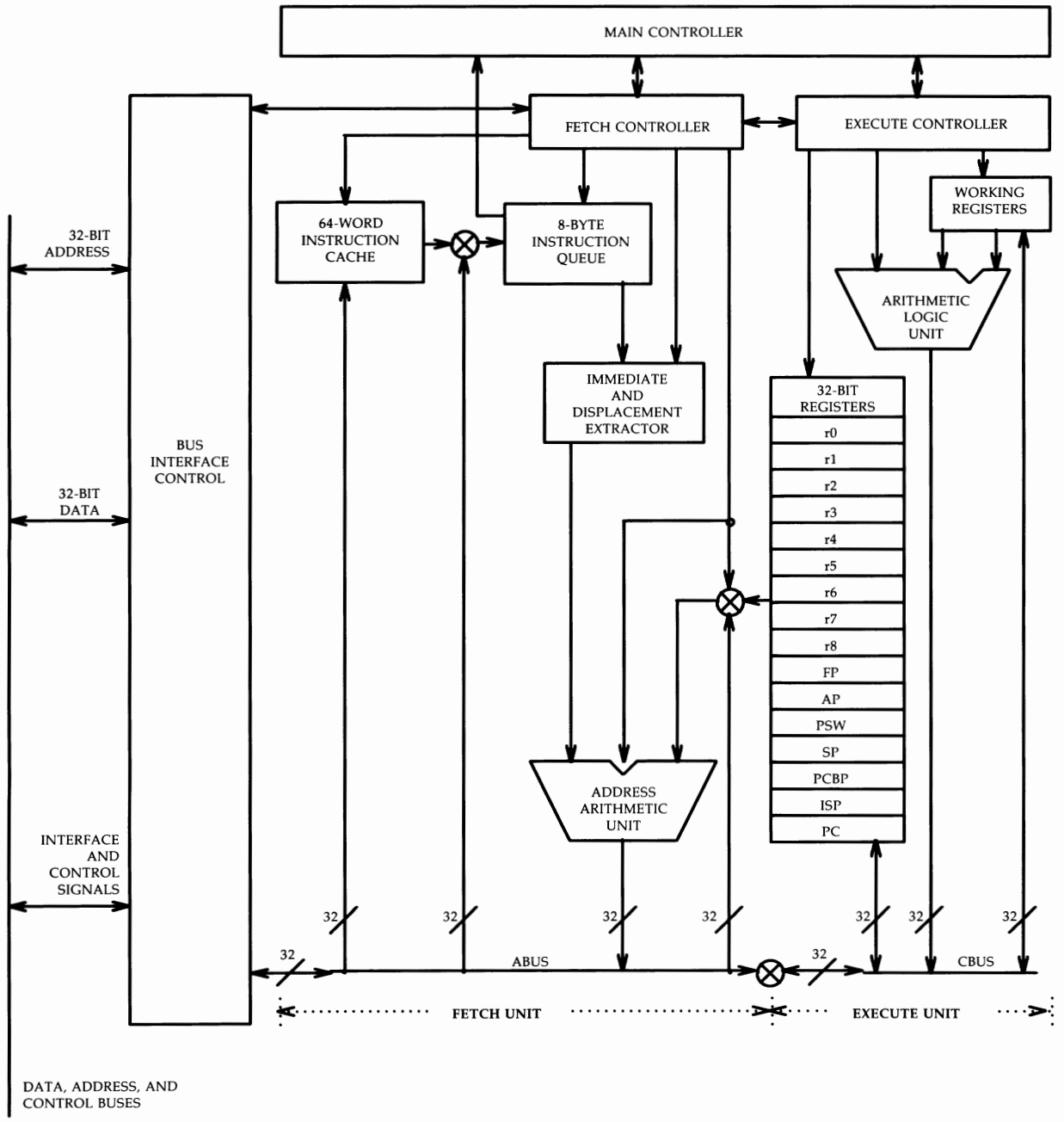


Figure 3-14: System Board CPU — Functional Block Diagram

Bus Interface Control. The bus interface control provides all strobes and control signals necessary to interface with peripherals.

Main Controller. The main controller is responsible for acquiring and decoding instruction opcodes and directing the action of the fetch and execute controllers as the specified instruction is executed. The main controller also responds to and directs the handling of interrupts and exceptions.

Fetch Unit. The fetch unit handles the instruction stream and does memory-based operand accesses. The unit consists of a fetch controller, an instruction cache, and instruction queue, an immediate and displacement extractor, and an Address Arithmetic Unit (AAU).

Execute Unit. The execute unit does all arithmetic and logical operations, all shift and rotate operations, and computes condition flags. It consists of an execute controller, sixteen 32-bit registers, working registers, and a 33-bit wide Arithmetic Logic Unit (ALU). The sixteen 32-bit registers are user-accessible. These registers include nine general-purpose registers (r8—r0) and seven dedicated registers (r15—9). All registers except the program counter (r15) can be referenced in all addressing modes. The processor status word (r11), process control block pointer (r13), and the interrupt stack pointer (r14) are privileged registers that can be read at any time, but these registers can only be written when the CPU is in the kernel (highest) execution level. The working registers are used exclusively by the CPU and are not user-accessible. The sixteen 32-bit CPU registers are further defined in the following paragraphs.

General Purpose Registers (r8—r0)

Nine general-purpose registers are used for accumulation, addressing, and for temporary data storage. They can be used in any addressing mode by any program (privileged or nonprivileged). Registers r2, r1, and r0 are also implicitly used by certain other data transfer instructions and by certain operating system instructions. Registers r2, r1, and r0 are also used by the CPU as a scratch pad. The contents of registers r8—r3 are part of the error report output by the **/etc/errdump** command.

Frame Pointer Register (r9)

The Frame Pointer (FP) register (r9) contents point to the beginning address (location) in the stack of a function's local variables. The contents of register r9 are part of the error report output by the **/etc/errdump** command.

Argument Pointer Register (r10)

The Argument Pointer (AP) register (r10) contents point to the starting address (location) in the stack where a set of arguments for a function have been pushed. The contents of register r10 are part of the error report output by the **/etc/errdump** command. This register is identified as "oap" in the error report.

Processor Status Word Register (r11)

The Processor Status Word (PSW) register (r11) contains information that determines the current execution state of the CPU. The PSW register is kernel level privileged. The contents of PSW register (r11) are part of the error report output by the **/etc/errdump** command. This register is identified as "psw" in the error report. The format of the PSW register is as follows.

	PROCESSOR STATUS WORD REGISTER														
BITS	31 — 26	25	24	23	22	21 — 18	17	16 — 13	12 — 11	10 — 09	08	07	06 — 03	02	01 — 00
FIELD	UNUSED	CFD	QIE	CD	OE	NZVC	TE	IPL	CM	PM	R	I	ISC	TM	ET

The PSW register fields are defined in the following paragraphs.

UNUSED Bits 31—26 are not used and are always cleared [0].

CFD Bit 25 is the Cache Flush Disable (CFD) bit. When set [1], instruction cache flushing is disabled when a new process is loaded. When clear [0], the contents of the cache are flushed when a new process is loaded.

QIE Bit 24 is the Quick Interrupt Enable (QIE) bit. When set [1], the quick interrupt handling facility is enabled. When clear [0], an interrupt causes a process switch to a full interrupt processing sequence.

CD Bit 23 is the Cache Disable (CD) bit. When set [1], the instruction cache is not used. When clear [0], the instruction cache is used to store and read text. Normally this bit is clear [0].

OE Bit 22 is the Enable Overflow Trap (OE) bit. When set [1], overflow traps are enabled. This bit is cleared when an overflow trap is detected and processed.

NZVC Bits 21—18 are used to represent four condition codes that reflect the status of the most recent instruction execution. The codes are tested using conditional branching instructions and indicate the following when set.

Bit 21[1] — Negative (N)

Bit 20[1] — Zero (Z)

Bit 19[1] — Overflow (V)

Bit 18[1] — Carry (C)

TE Bit 17 is the Trace Enable (TE) bit. When set [1], the trace function is enabled, causing a trace trap to occur after execution of the next instruction. Debugging and analysis software use the trace facility for single-stepping a program.

IPL Bits 16—13 are the Interrupt Priority Level (IPL) bits. Bit 13 is the least significant bit. Fifteen interrupt levels are available. An interrupt, unless it is a nonmaskable interrupt, must have a higher priority than the current registered IPL bits in order for the interrupt to be acknowledged. Level 0000 indicated that any of the fifteen interrupt priority levels (0001 through 1111) can interrupt the CPU. A registered IPL of 1111 indicates that no interrupts (except a nonmaskable interrupt) can interrupt the CPU.

CM Bits 12 and 11 are the Current Execution Mode (CM) bits. The code for bits 12 and 11 are as follows.

BIT 12	BIT 11	DESCRIPTION
0	0	KERNEL LEVEL
0	1	EXECUTIVE LEVEL
1	0	SUPERVISOR LEVEL
1	1	USER LEVEL

PM Bits 10 and 09 are the Previous Execution Mode (PM) bits. The code for bits 10 and 09 are as follows.

BIT 10	BIT 09	DESCRIPTION
0	0	KERNEL LEVEL
0	1	EXECUTIVE LEVEL
1	0	SUPERVISOR LEVEL
1	1	USER LEVEL

R-I Bits 08 and 07 are the Register-Initial Context (R-I) bits. These bits control the CPU context switching strategy. The I bit (bit 07) determines if a process executes from initial (I=1) or intermediate saved context (I=0). The R bit (bit 08, read only) determines if the registers of a process should be saved during a process switch (R=1).

ISC

Bits 06—03 are the Internal State Code (ISC) bits. The ISC bits are used to distinguish between exceptions of the same type. This field is used with the Exception Type (ET) field to determine when exception occurred. Traps, exceptions, and faults are equivalent with respect to ISC. Normal exceptions are decoded on a priority scheme if more than one occurs in a particular cycle. Exceptional conditions that reset the PSW flags are indicated by an asterisk (*) in the following data.

EXCEPTION TYPE	EXCEPTION	ISC BITS 6 5 4 3
NORMAL EXCEPTION (ET=11)	INTEGER ZERO-DIVIDE	0 0 0 0*
	TRACE TRAP	0 0 0 1
	ILLEGAL OPCODE	0 0 1 0
	RESERVED OPCODE	0 0 1 1
	INVALID DESCRIPTOR	0 1 0 0*
	EXTERNAL MEMORY FAULT	0 1 0 1
	GATE VECTOR FAULT	0 1 1 0
	ILLEGAL LEVEL CHANGE	0 1 1 1
	RESERVED DATA TYPE	1 0 0 0*
	INTEGER OVERFLOW	1 0 0 1
	PRIVILEGED OPCODE	1 0 1 0
	BREAKPOINT TRAP	1 0 1 1
	PRIVILEGED REGISTER	1 1 1 1
STACK EXCEPTION (ET=10)	STACK BOUND	0 0 0 0
	STACK FAULT	0 0 0 1
	INTERRUPT ID FETCH	0 0 1 0
PROCESS EXCEPTION (ET=01)	OLD PCB FAULT	0 0 0 0
	GATE PCB FAULT	0 0 0 1
	NEW PCB FAULT	0 1 0 0
RESET EXCEPTION (ET=00)	OLD PCB FAULT	0 0 0 0
	SYSTEM DATA	0 0 0 1
	INTERRUPT STACK FAULT	0 0 1 0
	EXTERNAL RESET	0 0 1 1
	NEW PCB FAULT	0 1 0 0
	GATE VECTOR FAULT	0 1 1 0

TM Bit 02 is the Trace Mask (TM) bit. This read-only field masks the Trace Enable (TE) bit for the duration of one instruction to avoid a trace trap. The TM bit is set [1] at the start of every instruction. The TM bit is cleared [0] as part of every microsequence that performs a context switch, a return from gate, or when any fault/interrupt is processed.

ET Bits 01 and 00 are the Exception Type (ET) bits. The ET field is used with the Internal State Code (ISC) field (PSW06—03) to distinguish between exceptions of the same type. The code for bits 01 and 00 are as follows.

BIT 01	BIT 00	DESCRIPTION
0	0	ON RESET EXCEPTION
0	1	ON PROCESS EXCEPTION
1	0	ON STACK EXCEPTION
1	1	ON NORMAL EXCEPTION

Stack Pointer Register (r12)

The Stack Pointer (SP) register contains the current 32-bit address of the top of the execution stack. This is the memory address of the next place where an item can be stored (pushed) on the stack or the last place where an item was retrieved (popped) from the stack. The SP implements a Last-In-First-Out (LIFO) queue for efficient subroutine linkage and local variable storage. The contents of Stack Pointer register (r12) are part of the error report output by the **/etc/errdump** command. This register is identified as "osp" in the error report.

Process Control Block Pointer Register (r13)

The Process Control Block Pointer (PCBP) register contains the 32-bit address of the Process Control Block (PCB) for the current process. The PCBP register is kernel level privileged (can only be written when the CPU is in the kernel mode). The PCB contains all switchable process context collected into a compact form for ease of movement between system memory and privileged internal registers. This context consists of the initial and current contents of the processor status word, program counter, and stack pointer; the last contents of registers r0 through r10; boundaries for an execution stack; and block move specifications for the process. The contents of register r13 are part of the error report output by the **/etc/errdump** command. This register is identified as "pcbp" in the error report.

Interrupt Stack Pointer Register (r14)

The Interrupt Stack Pointer (ISP) register (r14) contains the 32-bit memory address of the top of the interrupt stack. This stack is used when an interrupt request is received. The interrupt stack is also used by the Call Process (CALLPS) and Return to Process (RETPS) instructions. The ISP register is kernel level privileged. The contents of register r14 are part of the error report output by the **/etc/errdump** command. This register is identified as "isp" in the error report.

Program Counter Register (r15)

The Program Counter (PC) register (r15) contains the 32-bit memory address of the instruction being executed or, on instruction completion, contains the starting address of the next instruction to be executed. The contents of register r15 are part of the error report output by the **/etc/errdump** command. This register is identified as "opc" in the error report.

Memory Management Unit

The Memory Management Unit (MMU) on System Board, ED-4C637-30 is a WE 32101 Memory Management Unit. The MMU on a CM190A System Board is part of the WE 32002 CPU Module. Figure 3-15 shows how the MMU connects to the system. Figure 3-16 is a block diagram of the MMU. The internal MMU address spectrum is shown in Figure 3-17. Figure 3-18 shows virtual to physical address translation for contiguous memory segments. Figure 3-19 shows virtual to physical address translation for paged segments.

The MMU manipulates the microprocessor's address space by translating the virtual microprocessor addresses into physical address information. The 32-bit address can access over 4 gigabytes (2^{32}) of system memory or peripherals. The MMU also supports demand paged and demand segmented virtual memory. This permits large programs to efficiently use physical memory space.

The MMU divides the virtual address space into four sections. Each of these four sections can be subdivided into as many as 8K segments per section. These segments can be either contiguous or paged and are mapped into the physical address space by the MMU. A contiguous segment can be as large as 128K bytes. A paged segment can contain up to sixty-four 2K byte pages. Contiguous and paged segments start at an address in physical memory that is a multiple of 32 bytes.

Virtual addresses are relative addresses of an active process. Physical addresses are addresses that the main store controller can interpret as the true physical location of the memory. The function of the MMU is to translate virtual addresses to physical addresses. The address of each byte within a 2K byte block (offset) is not translated because the smallest size data block that can be placed in the main store by the MMU is 2K bytes. Therefore, the lower 11 bits of the virtual address spectrum and the lower 11 bits of the physical address spectrum are the same. The MMU stores information describing the physical location of blocks of 2K bytes of process data. This information is called descriptors. The descriptors are stored in the MMU descriptor caches. The MMU uses two descriptor caches: Segment Descriptor Cache (SDC) and Page Descriptor Cache (PDC).

Virtual address space is further described in Appendix A.

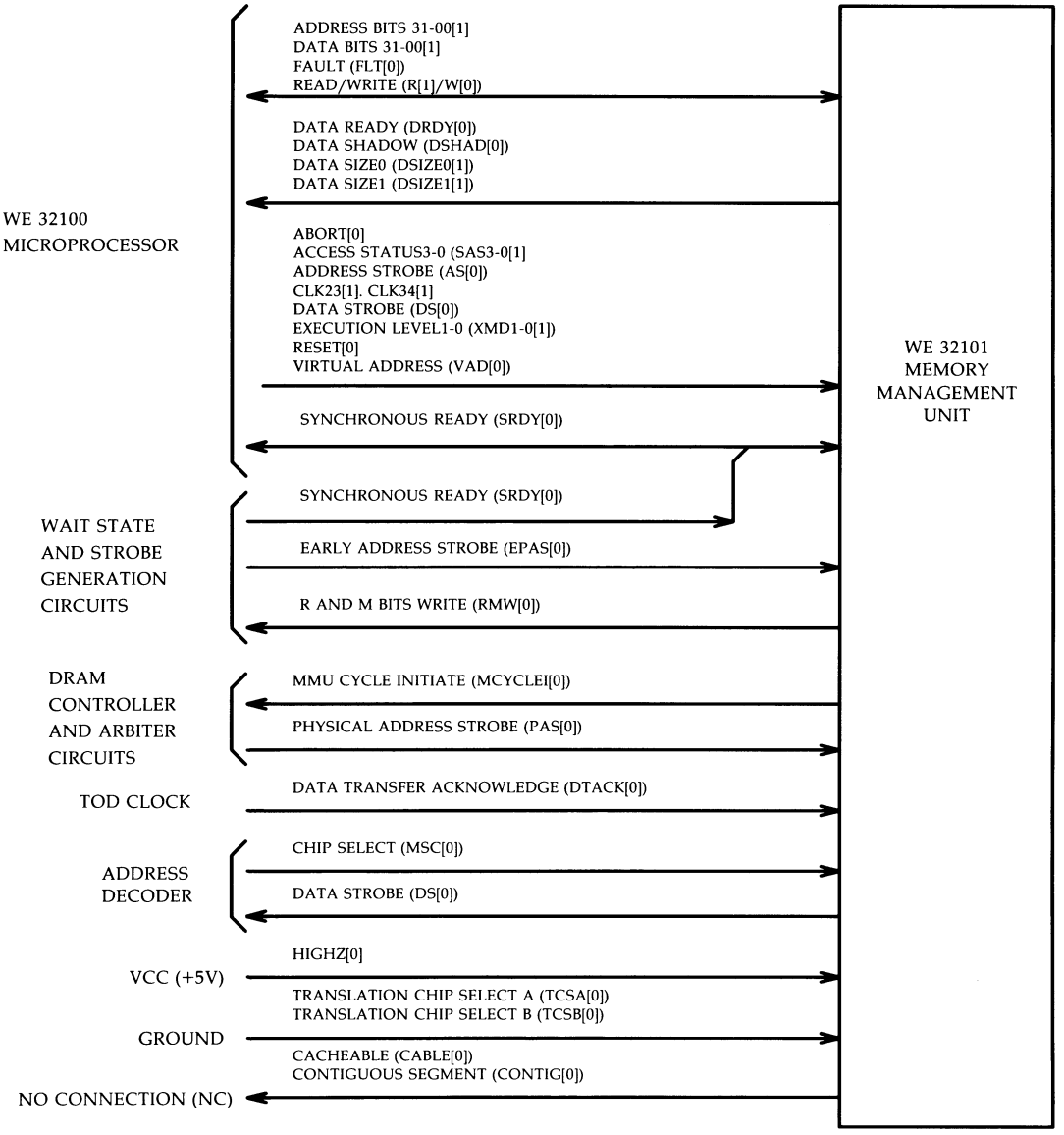


Figure 3-15: WE 32101 MMU Interconnection Diagram

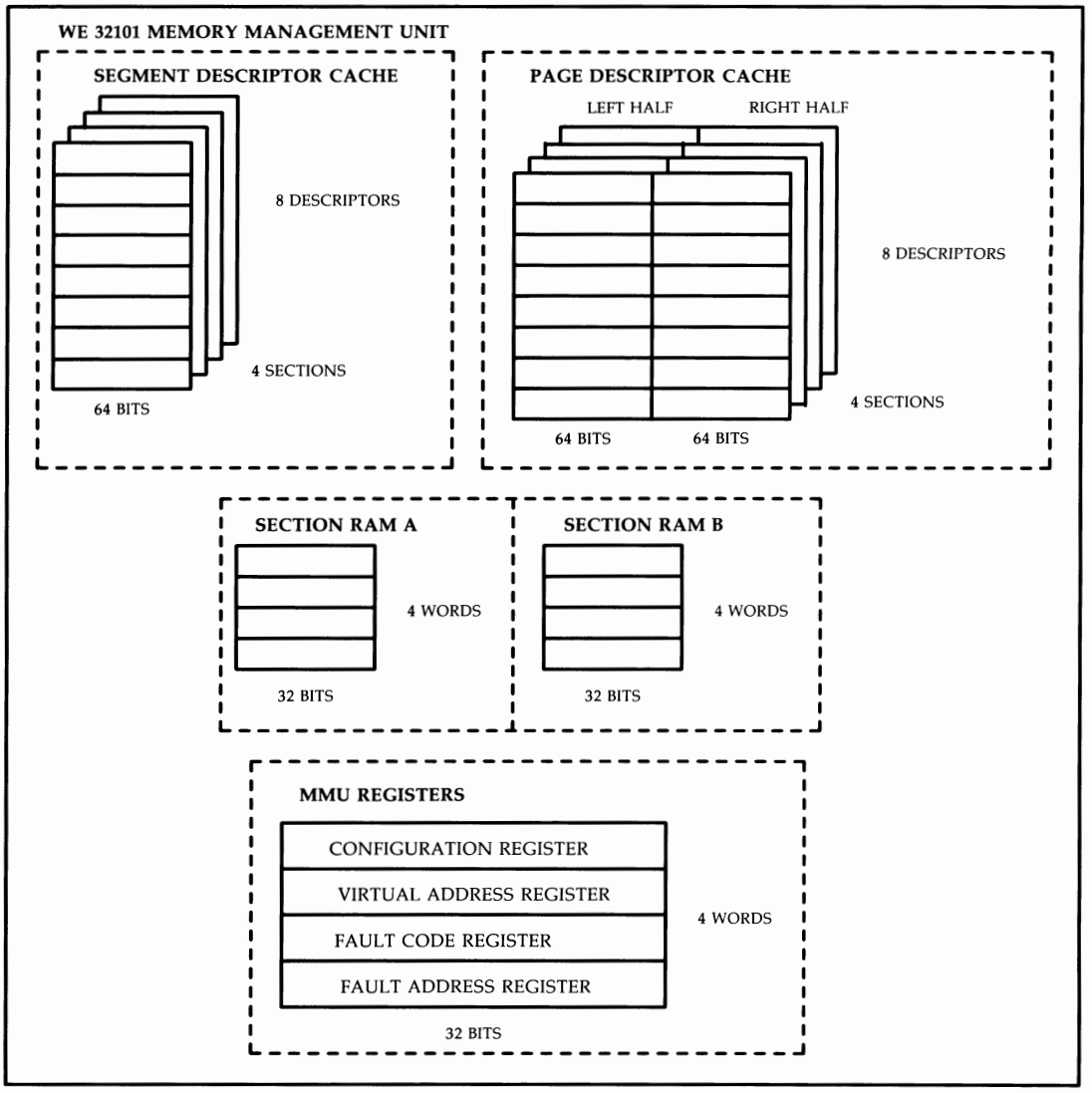


Figure 3-16: WE 32101 MMU Block Diagram

Segment Descriptor Cache. The Segment Descriptor Cache (SDC) consists of 32 descriptors. Each descriptor is 64 bits in length and is divided into four parts (sections).

Page Descriptor Cache. The Page Descriptor Cache (PDC) consists of sixty-four 64-bit descriptors organized in a 2-way set-associative configuration. The PDC is divided into four parts which correspond to the four sections of virtual memory.

Section Random Access Memories. The MMU contains two Random Access Memory (RAM) areas called Section RAM A (SRAMA) and Section RAM B (SRAMB). Each of these areas contain four 32-bit words. SRAMA bits 31—05 describes the base address of the Segment Descriptor Table (SDT) for each of the four sections of virtual memory. SRAMB bits 22—10 describes the length (number of entries) in the SDT for each of the four sections of virtual memory. The contents of SRAMA (4 words) and SRAMB (4 words) are part of the error report output by the **/etc/errdump** command. The SRAMA and SRAMB are identified as "srama" and "sramb" in the error report. The format of SRAMA and SRAMB are as follows.

	SECTION RAM A (SRAMA)	
BITS	31 — 05	04 — 00
FIELD	SDT ADDRESS	RESERVED

	SECTION RAM B (SRAMB)		
BITS	31 — 23	22 — 10	09 — 00
FIELD	RESERVED	SDT LENGTH	RESERVED

MMU Registers. The MMU contains four 32-bit registers:

- Configuration Register (CR)
- Virtual Address Register (VAR)
- Fault Code Register (FLTCR)
- Fault Address Register (FLTAR).

These registers are used to store MMU state information. The contents of FLTAR and FLTCR are part of the error report output by the **/etc/errdump** command. The FLTAR and FLTCR are identified as "fltar" and "fltcr" in the error report.

Configuration Register

The Configuration Register (CR) is used by the operating system to determine whether or not the Referenced (R) and Modified (M) bits for segment descriptors are to be updated in memory. The format of the CR is as follows.

	CONFIGURATION REGISTER			
BITS	31 — 03	02	01	00
FIELD	RESERVED	CACHEABLE	REFERENCED	MODIFIED

The CR fields are defined in the following paragraphs.

RESERVED Bits 31—03 are reserved for future use. If read, zeros are returned.

CACHEABLE Bit 02 is the Cacheable bit. The Cacheable ($) bit determines the state of $\overline{\text{CABLE}}$ during misprocessing and updating of the Referenced and Modified bits. (If $=0, then $\overline{\text{CABLE}}$ =1; if $=1, then $\overline{\text{CABLE}}$ =0.)

REFERENCED Bit 01 is the Referenced (R) bit. The R bit in the segment descriptor is set (R=1) when the segment descriptor is brought into the segment descriptor cache as a result of misprocessing. When R=0, the R bit in the segment descriptor is not updated.

MODIFIED Bit 00 is the Modified (M) bit. If M=1, the segment descriptor M bit is updated on the first write to a segment.

Virtual Address Register

The Virtual Address Register (VAR) contains the virtual address to be translated by the MMU. The VAR is overwritten each time a translation is performed or when the CPU writes to it in the peripheral mode.

Fault Code Register

The Fault Code Register (FLTCR) records the last fault and operational states in the MMU. The output of the **/etc/errdump** command includes the FLTCR. The format of the FLTCR is as follows.

	FAULT CODE REGISTER			
BITS	31 — 11	10 — 07	06 — 05	04 — 00
FIELD	RESERVED	ACCESS REQUESTED	ACCESS XLEVEL	FAULT TYPE

The FLTCR fields are defined in the following paragraphs.

RESERVED Bits 31—11 are reserved for future use. If read, zeros are returned.

ACCESS REQUESTED

Bits 10—07 are used to store the type of access the CPU requested when a fault occurred. The decode of bits 10—07 indicate the following.

BITS 10 — 07	ACCESS TYPE
0000	MOVE TRANSLATED (MT)
0001	SUPPORT PROCESSOR DATA WRITE
0011	SUPPORT PROCESSOR DATA FETCH
0111	INTERLOCKED READ
1000	ADDRESS FETCH
1001	OPERAND FETCH
1010	WRITE
1100	INSTRUCTION FETCH AFTER DISCONTINUITY
1110	INSTRUCTION FETCH

ACCESS XLEVEL

Bits 06 and 05 are used to store the execution level of the requested access when the fault occurred. The decode of bits 06 and 05 indicate the following.

BIT 06	BIT 05	DESCRIPTION
0	0	KERNEL LEVEL
0	1	EXECUTIVE LEVEL
1	0	SUPERVISOR LEVEL
1	1	USER LEVEL

FAULT TYPE

Bits 04—00 are the FAULT TYPE that occurred. The decode of bits 04—00 indicate the following. Unassigned fault type values are not included.

BITS 04—00	FAULT NAME
00000	NO FAULT
00001	MISPROCESSING MEMORY
00010	REFERENCE/MODIFIED UPDATE MEMORY
00011	SEGMENT DESCRIPTOR TABLE LENGTH
00100	PAGE WRITE
00101	PAGE DESCRIPTOR TABLE LENGTH
00110	INVALID SEGMENT DESCRIPTOR
00111	SEGMENT NOT PRESENT
01000	OBJECT TRAP
01001	PAGE DESCRIPTOR TABLE NOT PRESENT
01010	PAGE NOT PRESENT
01011	TOO MANY INDIRECTIONS
01101	ACCESS
01110	SEGMENT OFFSET
01111	ACCESS AND SEGMENT OFFSET
11111	DOUBLE PAGE HIT

Fault Address Register

The Fault Address Register (FLTAR) contains the virtual address that was being processed when the last fault that caused a write to the FLTCR and FLTAR occurred. The contents are changed when the CPU writes to it in the peripheral mode. The output of the **/etc/errdump** command includes the FLTAR.

Peripheral Mode. In the peripheral mode of MMU operation, the MMU is accessed as a memory-mapped peripheral. In this mode, internal MMU registers and logic elements are read and write accessible by the system board CPU. All peripheral mode accesses are word (32-bit) accesses. When the system board CPU asserts the MMU Chip Select (MMUCS[0]), the MMU is in the peripheral mode. The internal MMU address spectrum is shown in Figure 3-17. In the peripheral mode, physical address bits 31—00 are interpreted as follows by the MMU.

	PERIPHERAL MODE ADDRESS FIELDS				
BITS	31 — 12	11 — 08	07	06 — 02	01 — 00
FIELD	RESERVED	ENTITY	RESERVED	INDEX	RESERVED

The peripheral mode address fields are defined in the following paragraphs.

RESERVED Bits 31—12, 07, 01, and 00 are ignored by the MMU. These bits are negated (treated as zeros).

ENTITY Bits 11—08 are used to select the internal MMU circuit (entity) to be accessed. The decode of bits 11—08 is as follows.

BITS 11 — 08	SELECTED MMU DEVICE
0000	SEGMENT DESCRIPTOR CACHE BITS 31—00
0001	SEGMENT DESCRIPTOR CACHE BITS 63—32
0010	RIGHT HALF OF PAGE DESCRIPTOR CACHE BITS 31—00
0011	RIGHT HALF OF PAGE DESCRIPTOR CACHE BITS 63—32
0100	LEFT HALF OF PAGE DESCRIPTOR CACHE BITS 31—00
0101	LEFT HALF OF PAGE DESCRIPTOR CACHE BITS 63—32
0110	SECTION RAM A
0111	SECTION RAM B
1000	FAULT CODE REGISTER
1001	FAULT ADDRESS REGISTER
1010	CONFIGURATION REGISTER
1011	VIRTUAL ADDRESS REGISTER

INDEX Bits 06—02 are used to index each addressable entity. Bits 06—02 are ignored when registers are accessed. Bits 06—02 are used when segment or page descriptor caches are accessed. Bits 03 and 02 are used for section RAM accesses.

MMU INTERNAL ADDRESS SPECTRUM	
ADDRESS	**DESCRIPTION**
0x 000 ⋮ 0x 07C	SEGMENT DESCRIPTOR CACHE BITS 31—00
0x 100 ⋮ 0x 17C	SEGMENT DESCRIPTOR CACHE BITS 63—32
0x 200 ⋮ 0x 27C	RIGHT HALF OF PAGE DESCRIPTOR CACHE BITS 31—00
0x300 ⋮ 0x 37C	RIGHT HALF OF PAGE DESCRIPTOR CACHE BITS 63—32
0x 400 ⋮ 0x 47C	LEFT HALF OF PAGE DESCRIPTOR CACHE BITS 31—00
0x 500 ⋮ 0x 57C	LEFT HALF OF PAGE DESCRIPTOR CACHE BITS 63—32
0x 600 ⋮ 0x 60C	SECTION RAM A
0x 700 ⋮ 0x 70C	SECTION RAM B
0x 800	FAULT CODE REGISTER
0x 900	FAULT ADDRESS REGISTER
0x A00	CONFIGURATION REGISTER
0x B00	VIRTUAL ADDRESS REGISTER

Figure 3-17: MMU Internal Address Spectrum

Virtual to Physical Address Translation for Contiguous Segments. Figure 3-18 shows the translation of a virtual address to a physical address for a contiguous segment of physical memory. The Section Identification (SID) field is used to find the base address of the required Segment Descriptor Table (SDT). The base address of the SDT for each section is stored in the MMU. This base address and the Segment Select (SSL) field are combined to index a Segment Descriptor (SD) within the SDT. This address is added to the Segment Offset (SOT) field to form the required physical address.

Virtual to Physical Address Translation for Paged Segments. Figure 3-19 shows the translation of a virtual address to a physical address for a paged segment of physical memory. The SID field is used to find the base address of the required SDT. The base address of the SDT for each section is stored in the MMU. This base address and the SSL field are combined to index an SD within the SDT. The SD is used as the base address of a Page Descriptor Table (PDT). This PDT address is combined with the Page Select (PSL) field to index a Page Descriptor (PD). The PD contains the starting address of the paged segment that is concatenated with the Page Offset (POT) field to form the required physical address.

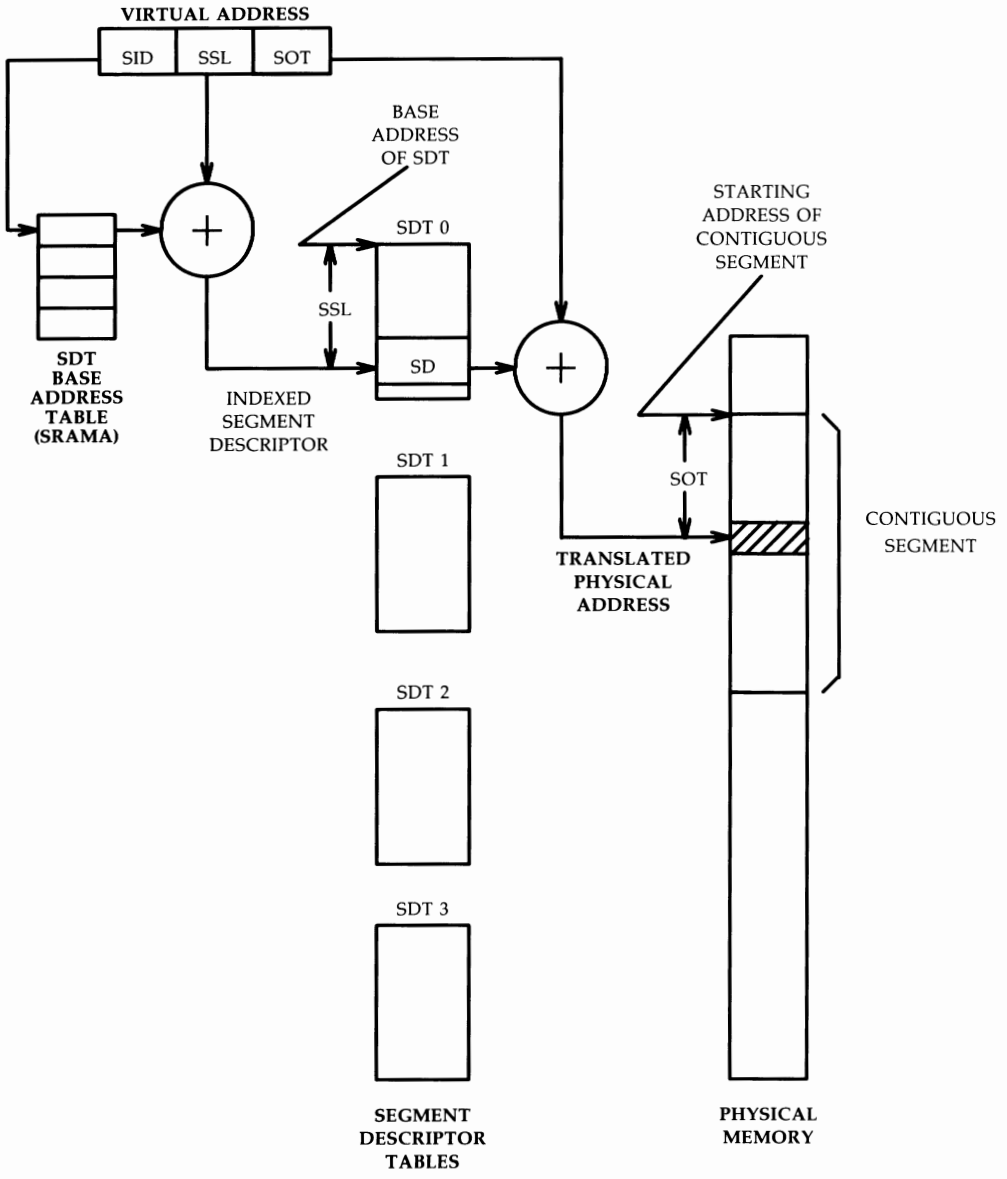


Figure 3-18: Virtual Address to Physical Address Translation for Contiguous Segments

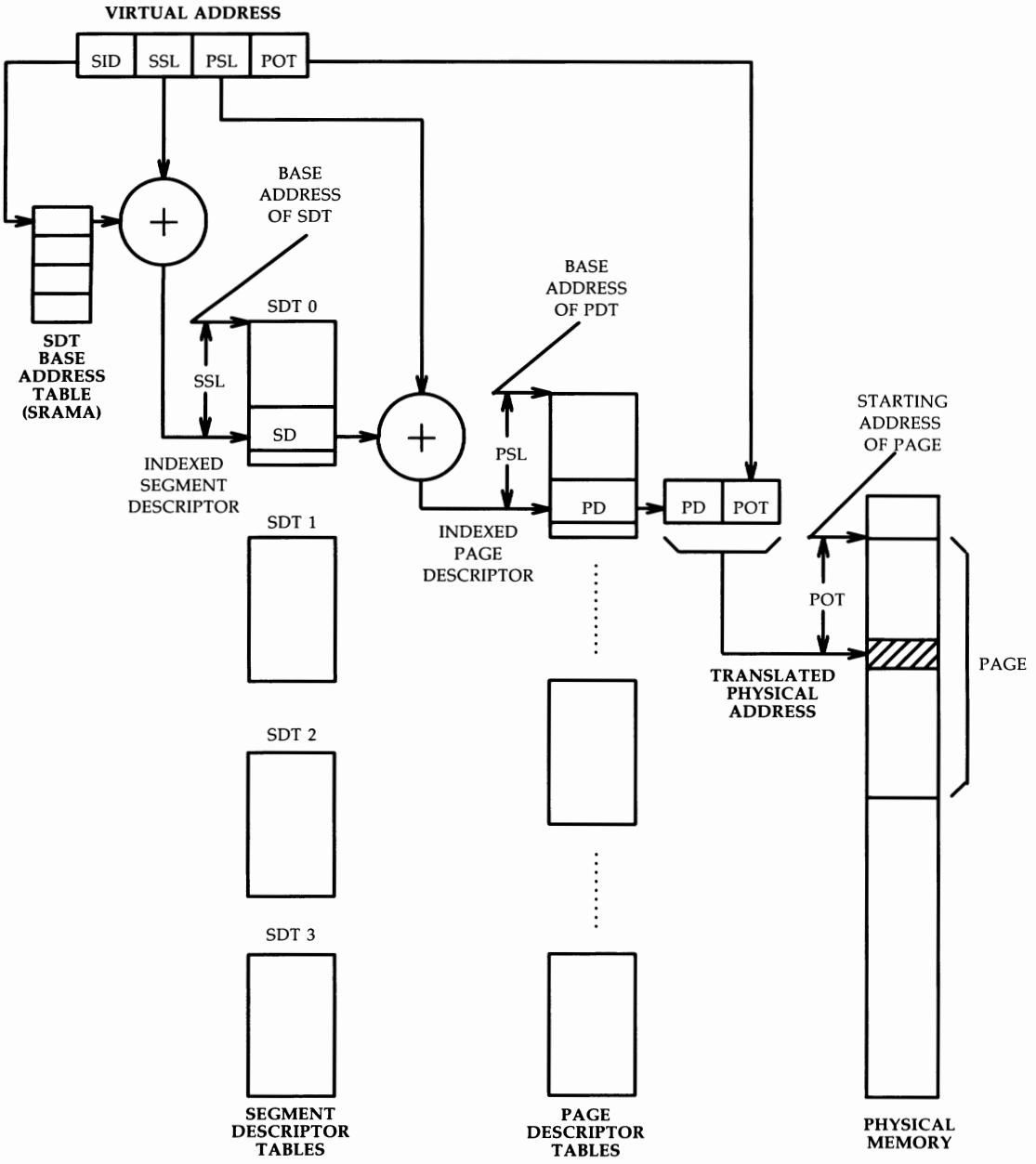


Figure 3-19: Virtual Address to Physical Address Translation for Paged Segments

Math Acceleration Unit (Optional)

The WE 32106 Math Acceleration Unit (MAU) is used in a coprocessor mode to provide hardware floating point capability for the WE 32100 Microprocessor. The MAU peripheral mode is **not** used in this application; the MAU chip select is held to a logic 1 through a pull-up resistor to VCC. The MAU provides single (32-bit), double (64-bit), and double-extended (80-bit) precision. The single precision format provides an 8-bit exponent and an exponent bias allowing the reciprocal of all normalized numbers to be represented without overflow. Double precision provides an exponent range sufficient for the product of eight 32-bit terms without overflow. Double-extended precision provides a format with a range and precision that is greater than double precision. Double-extended precision numbers lessen the chance of a result being contaminated by excessive round-off error.

The MAU supports add, subtract, multiply, divide, remainder, square root, and compare operations. The operand, result, status, and command information transfers take place over a 32-bit, bidirectional data bus with the WE 32100 Microprocessor. Figure 3-20 is a functional block diagram of the WE 32106 MAU. The WE 32106 is a 100-pin ceramic pin-array package using CMOS technology and operating at 10 MHz.

MAU Registers. The MAU contains the following four register types:

- Auxiliary Status Register
- Operand Registers
- Command Register
- Data Register.

These registers provide status, command, and control for the MAU.

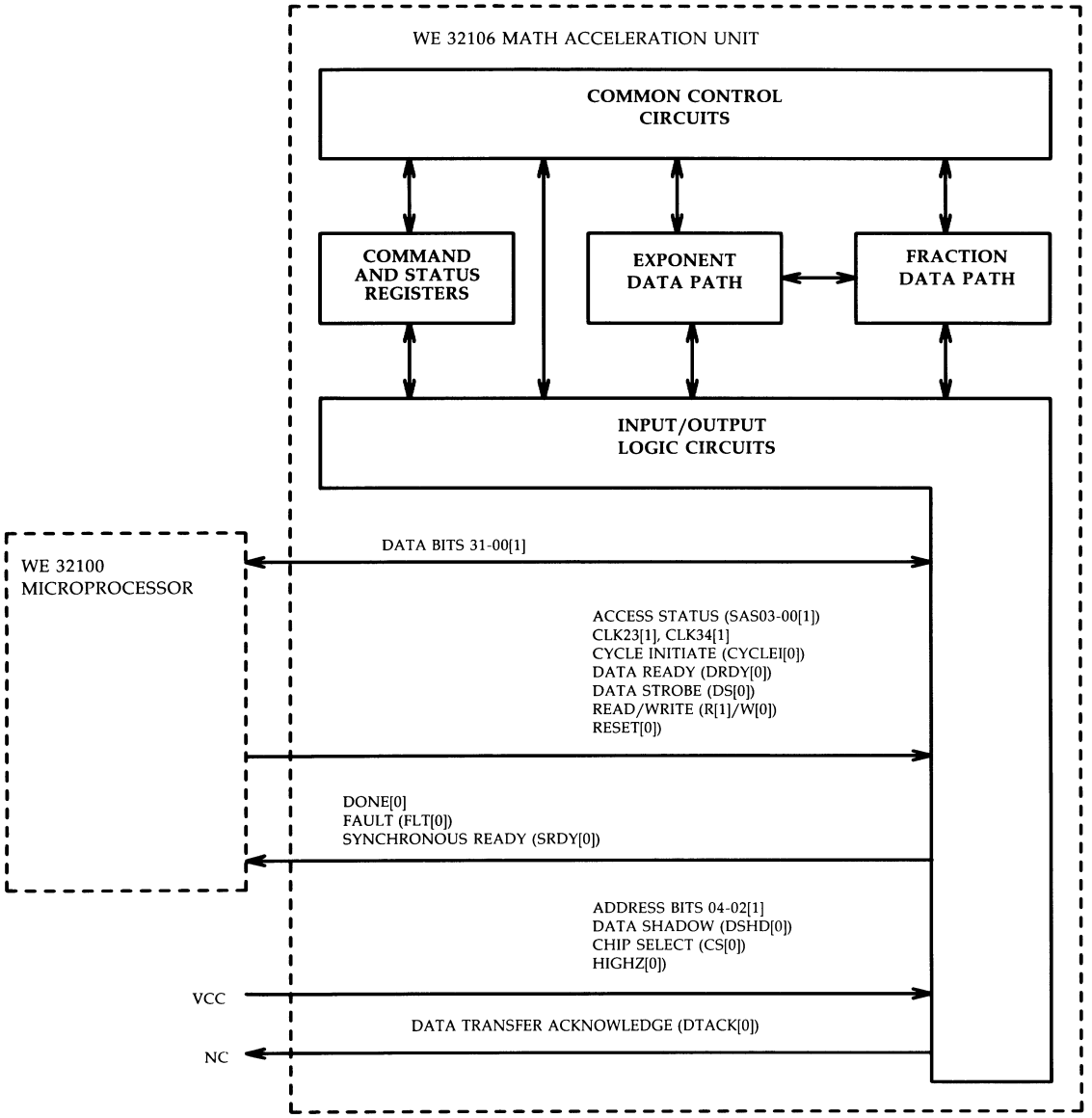


Figure 3-20: WE 32106 Math Acceleration Unit — Functional Block Diagram

Auxiliary Status Register

The Auxiliary Status Register (ASR) is used to do the following:

- Control the remainder operation (partial remainder bit)
- Signal the state of an operation (result available bit)
- Disable and record exceptions (mask and sticky bits)
- Control rounding of results (round control bits)
- Record condition codes (negative and zero bits).

The negative, zero, inexact, and integer overflow bits in the ASR match the condition codes in the PSW register of the CPU. This allows the bits to be copied into the PSW as part of the coprocessor status access and to be easily tested by the CPU. The format of the ASR is as follows.

	AUXILIARY STATUS REGISTER (31—16)										
BITS	31	30 — 26	25	24	23 — 22	21	20	19	18	17	16
FIELD	RA	UNUSED	ECP	NTNC	RC	N	Z	IO	PS	CSC	UO

	AUXILIARY STATUS REGISTER (15—00)											
BITS	15	14	13	12	11	10	09	08	07	06	05	04 — 00
FIELD	UNUSED	IM	OM	UM	QM	PM	IS	OS	US	QS	PR	UNUSED

The ASR fields are defined in the following paragraphs.

UNUSED Bits 30—26, 15, and 04—00 are not used. These bits are returned as zeros when read.

RA Bit 31 is the Result Available (RA) bit. It is cleared at the beginning of an operation and set [1] when the operation result is available. During the quiescent state, the RA bit is set.

ECP Bit 25 is the Exception Condition Present (ECP) bit. It is set [1] if any one of the floating point exception conditions except "inexact" is present. The ECP bit is cleared [0].

NTNC Bit 24 is the Nontrapping Not a Number (NAN) Control (NTNC) bit. Bit 24 is tested when an invalid operation exception occurs and bit 14 (IM) is cleared. If bit 24 is set, an exception occurs and bit 09 (IS) is set.

RC Bits 23 and 22 are the Round Control (RC) mode bits. The decode of these bits is as follows.

BIT 23	BIT 22	DESCRIPTION
0	0	ROUND TO NEAREST
0	1	ROUND TOWARDS PLUS INFINITY
1	0	ROUND TOWARDS MINUS INFINITY
1	1	ROUND TOWARDS ZERO (TRUNCATION)

N Bit 21 is the Negative (N) condition bit. Bit 21 is set [1] when result of the last operation is negative. Bit 21 is cleared when the result of the last operation is positive.

Z Bit 20 is the Zero (Z) condition bit. Bit 20 is set [1] when the result of the last operation is zero. Bit 20 is cleared when the result of the last operation is nonzero.

IO Bit 19 is the Integer Overflow (IO) bit. Bit 19 is set [1] when a convert float to integer operation causes an overflow.

PS Bit 18 is the Inexact Sticky (PS) bit. Bit 18 is set [1] when the result of an operation cannot be specified in the destination format. Bit 18 is cleared on reset.

CSC Bit 17 is the Context Switch Control (CSC) bit. Bit 17 is set [1] on every MAU instruction execution. Bit 17 is cleared on reset.

UO Bit 16 is the Unordered (UO) bit. Bit 16 is set [1] when a compare operation results in an unordered indication; otherwise this bit is cleared. Bit 16 is cleared on reset.

IM Bit 14 is the Invalid Operation Mask (IM) bit. Bit 14 is set [1] by the user to enable the generation of an exception when bit 09 (Invalid Operation Sticky bit) is set. There are no invalid operation exceptions when bit 14 is cleared.

OM Bit 13 is the Overflow Mask (OM) bit. Bit 13 is set [1] by the user to enable the generation of an exception when bit 08 (Overflow Sticky bit) is set. There are no overflow exceptions when bit 13 is cleared.

UM Bit 12 is the Underflow Mask (UM) bit. Bit 12 is set [1] by the user to enable the generation of an exception when bit 07 (Underflow Sticky bit) is set. There are no underflow exceptions when bit 12 is cleared.

QM Bit 11 is the Divide by Zero Mask (QM) bit. Bit 11 is set [1] by the user to enable the generation of an exception when bit 06 (Divide by Zero Sticky bit) is set. There are no divide by zero exceptions when bit 11 is cleared.

PM Bit 10 is the Inexact Mask (PM) bit. Bit 10 is set [1] by the user to enable the generation of an exception when bit 18 (Inexact Sticky bit) is set [1]. There are no inexact exceptions when bit 10 is cleared.

IS Bit 09 is the Invalid Operation Sticky (IS) bit. Bit 09 is set [1] when a result cannot be legally stored in a destination, or when illegal operands are given to some operation.

OS Bit 08 is the Overflow Sticky (OS) bit. Bit 08 is set [1] when an exponent of a rounded result of an arithmetic operation is too large for the exponent field of the destination format.

US Bit 07 is the Underflow Sticky (US) bit. Bit 07 is set [1] when an exponent of a rounded result of an arithmetic operation is too small to be represented in the exponent field of the destination format.

QS Bit 06 is the Divide by Zero Sticky (QS) bit. Bit 06 is set [1] when the divisor is normalized zero and the dividend is a finite nonzero number.

PR Bit 05 is the Partial Remainder (PR) bit. Bit 05 is set [1] when the result of a remainder operation is a partial remainder. Bit 05 is cleared when the result of a remainder operation is a full remainder. This bit is cleared on reset.

Operand Registers

The MAU contains four operand registers (F3—F0). Each operand register is 80 bits and contains one operand in an extended format. These registers are accessed via the Data Register in the format of three 32-bit words. In the peripheral mode, bits 95—80 are ignored during write operations. For read operations, bits 95—80 are returned as zeros. The operand registers are unchanged on reset. The contents of these registers are indeterminate on powerup. The format of each of the four operand registers is as follows.

	OPERAND REGISTERS (F3— F0)				
BITS	95 — 80	79	78 — 64	63	62 — 00
FIELD	UNUSED	SIGN	EXPONENT	J	FRACTION

The operand register fields are defined in the following paragraphs.

UNUSED Bits 95—80 are not used. These bits are returned as zeros for a read operation.

SIGN Bit 79 is the SIGN bit. When set [1] the sign is negative; cleared represents a positive value.

EXPONENT Bits 78—64 are used as the EXPONENT field. The exponent is biased by 16,383.

J Bit 63 is the Explicit (J) bit. The J bit is to the left of the binary point in the 2^0 position. In combination, the J bit and the FRACTION field can represent values in the range 0 to $2-(2^{-63})$.

FRACTION Bits 62—00 are used to represent the fractional part of a number.

Command Register

The Command Register (CR) stores command words used to initiate MAU operations. The format of this 32-bit register is as follows.

	COMMAND REGISTER					
BITS	31 — 24	23 — 15	14 — 10	09 — 07	06 — 04	03 — 00
FIELD	ID	UNUSED	OPCODE	OP1	OP2	OP3

The CR fields are defined in the following paragraphs.

ID Bits 31—24 are the Processor Identification Number of the processor that should react to the command word. The MAU is ID 0.

UNUSED Bits 23—15 are not used. These bits are returned as zeros for a read operation.

OPCODE Bits 14—10 are the Operation Code (OPCODE) field. The OPCODE field specifies the operation to be done. The OPCODES are as follows.

OPCODE	MNEMONIC	INSTRUCTION
0x 02	ADD	ADD
0x 03	SUB	SUBTRACT
0x 04	DIV	DIVIDE
0x 05	REM	REMAINDER
0x 06	MUL	MULTIPLY
0x 07	MOVE	MOVE
0x 08	RDASR	MOVE FROM ASR
0x 09	WRASR	MOVE TO ASR
0x 0A	CMP	COMPARE
0x 0B	CMPE	COMPARE WITH EXCEPTIONS
0x 0C	ABS	ABSOLUTE VALUE
0x 0D	SQRT	SQUARE ROOT
0x 0E	RTOI	ROUND TO INTEGRAL VALUE
0x 0F	FTOI	CONVERT FLOATING POINT TO INTEGER
0x 10	ITOF	CONVERT INTEGER TO FLOATING POINT
0x 11	DTOF	CONVERT DECIMAL TO FLOATING POINT
0x 12	FTOD	CONVERT FLOATING POINT TO DECIMAL
0x 13	NOP	NO OPERATION
0x 14	EROF	EXTRACT RESULT ON FAULT
0x 17	NEG	NEGATE
0x 18	LDR	LOAD DATA REGISTER
0x 1A	CMPS	COMPARE WITH FLAGS SWAPPED
0x 1B	CMPS	COMPARE WITH EXCEPTIONS AND FLAGS SWAPPED

OP1

Bits 09—07 is the Operand Specifier 1 (OP1) field. OP1 specifies whether the first source operand is a MAU register, a memory-based operand of a given size, or nonexistent (no operand). The value of this field is as follows.

BITS 09 — 07	OPERAND LOCATION
000	REGISTER F0
001	REGISTER F1
010	REGISTER F2
011	REGISTER F3
100	MEMORY-BASED SINGLE WORD
101	MEMORY-BASED DOUBLE WORD
110	MEMORY-BASED TRIPLE WORD
111	NO OPERAND

OP2

Bits 06—04 is the Operand Specifier 2 (OP2) field. OP2 specifies whether the second source operand is a MAU register, a memory-based operand of a given size, or nonexistent (no operand). The value of this field is as follows.

BITS 06 — 04	OPERAND LOCATION
000	REGISTER F0
001	REGISTER F1
010	REGISTER F2
011	REGISTER F3
100	MEMORY-BASED SINGLE WORD
101	MEMORY-BASED DOUBLE WORD
110	MEMORY-BASED TRIPLE WORD
111	NO OPERAND

OP3

Bits 03—00 are the Operand Specifier 3 (OP3) field. OP3 specifies whether the destination operand is a MAU register, a memory-based operand of a given size, or nonexistent (no operand). Even though the register destinations are specified as single, double, or double-extended, the result is stored in the registers in double-extended precision. The precision designations are used for rounding and checking for underflow and overflow. The value of this field is as follows.

BITS 03 — 00	OPERAND REGISTER	DESTINATION PRECISION
0000	F0	SINGLE
0001	F1	SINGLE
0010	F2	SINGLE
0011	F3	SINGLE
0100	F0	DOUBLE
0101	F1	DOUBLE
0110	F2	DOUBLE
0111	F3	DOUBLE
1000	F0	DOUBLE-EXTENDED
1001	F1	DOUBLE-EXTENDED
1010	F2	DOUBLE-EXTENDED
1011	F3	DOUBLE-EXTENDED
1100	DR	MEMORY-BASED SINGLE WORD
1101	DR	MEMORY-BASED DOUBLE WORD
1110	DR	MEMORY-BASED TRIPLE WORD
1111	NONE	NO OPERAND

Data Register

The system board CPU (WE 32100) uses the MAU as a coprocessor; the peripheral mode of the MAU is NOT used in this application. The Data Register (DR) is used to read and write operands (registers F3-F0) in the peripheral mode. The DR is an 82-bit register. The DR is addressed in the peripheral mode as three 32-bit registers. When exceptions occur in either the coprocessor or peripheral modes, the DR stores the data supplied by the trap handler. This exception data is read when an Extract Result on Fault (EROF) instruction (opcode) is executed. The format of the exception data stored in the DR by the trap handler is as follows.

INVALID OPERATION

If either of the source operands is a trapping Not a Number (NAN), then DR stores the NAN converted to double-extended precision (80 bits) if necessary. If both source operands are trapping NANs or infinities of different signs, then the second operand (OP2) is stored in the DR in double precision (80 bits).

OVERFLOW or UNDERFLOW

The significant (fraction) along with the 17-bit internal result exponent and the result sign are stored in the DR. The most significant bit of the 17-bit exponent is like a sign bit in 2's complement notation. An addition bit (bit 79) in the exponent ensures that no significant exponent bits are lost from an internal representation when an overflow or underflow condition occurs. The exponent is biased by 16,383. The format of the data in the DR for an overflow or underflow exception is as follows.

BITS	81	80 — 64	63	62 — 00
FIELD	SIGN	EXPONENT	J	FRACTION

DIVIDE BY ZERO

The dividend (OP2) converted to double-extended precision, if necessary, is stored in the DR for a divide by zero exception.

INEXACT The rounded result converted to double-extended precision, if necessary, is stored in the DR for and inexact exception.

MAU Coprocessor Mode. In the Coprocessor Mode, the system board CPU initiates a MAU transaction by doing a coprocessor broadcast access. This sends a 32-bit word to the MAU Command Register. The MAU checks the Identification (ID) field of the Command Register against the MAU ID (0). If an ID matches the stored ID, the 32-bit word is stored in the Command Register.

If any Operand Specifier in the command word indicates that an operand is to be obtained from main memory, the MAU waits until the proper number of coprocessor data fetch bus transactions occur.

The MAU does the operation specified and generates a result, condition codes, and possibly an exception. The MAU asserts a DONE signal and waits for the coprocessor (system board CPU) status fetch. If an exception is present, the MAU faults the access and goes to an idle state. If there is no exception, a word containing the current Auxiliary Status Register (ASR) is returned in response to the status fetch.

If the results are to be written to main memory, The MAU waits until the proper number of coprocessor data write bus transactions occur to transfer the results and then goes to an idle state.

Address Decoder

The address decoder translates physical CPU/MMU addresses into chip selects (enables) for the various memory and peripheral circuits on the system board and feature cards. The address decoder is built from Programmable Logic Arrays (PLAs) and four 3/8 decoders. The chip select signals are also used to generate Wait Select (WSEL) signals appropriate for the access time of each synchronous device. For devices on the system board, a fixed number of wait states are generated by the address decoder.

The chip selects and controls decoded from physical address bits 26—12, Physical Address Strobe (PAS[0]), Interrupt Acknowledge (IACK[0]) are summarized in Figure 3-21.

PAS[0]	IACK[0]	PHYSICAL ADDRESS BITS				SELECTED DEVICE
		27—24	23—20	19—16	15—12	
x	x	xxxx	xxxx	xxxx	0000	MEMORY MANAGEMENT UNIT (MMUCS[0])
x	x	xxxx	xxxx	xxxx	0001	TIME-OF-DAY COUNTER (TODCS[0])
x	x	xxxx	xxxx	xxxx	0010	TIMERS (TIMRCS[0])
x	x	xxxx	xxxx	xxxx	0011	NONVOLATILE RANDOM ACCESS MEMORY (NVRCS[0])
x	x	xxxx	xxxx	xxxx	0100	CONTROL AND STATUS REGISTER (CSRCS[0])
x	x	xxxx	xxxx	xxxx	0101	PAGE REGISTER 1 (PR1CS[0])
x	x	xxxx	xxxx	xxxx	0110	PAGE REGISTER 2 (PR2CS[0])
x	x	xxxx	xxxx	xxxx	0111	PAGE REGISTER 3 (PR3CS[0])
x	x	xxxx	xxxx	xxxx	1000	DIRECT MEMORY ACCESS CONTROLLER (DMACS[0])
x	x	xxxx	xxxx	xxxx	1001	DUART (UARTCS[0])
x	x	xxxx	xxxx	xxxx	1010	HARD DISK CONTROLLER (DSKCS[0])
x	x	xxxx	xxxx	xxxx	1011	NOT USED
x	x	xxxx	xxxx	xxxx	1100	MEMORY SIZE REGISTER (MSIZECS[0])
x	x	xxxx	xxxx	xxxx	1101	FLOPPY DISK CONTROLLER (FCS[0])
x	x	xxxx	xxxx	xxxx	1110	PAGE REGISTER 4 (PR4CS[0])
x	x	xxxx	xxxx	xxxx	1111	NOT USED
x	x	xxx0	000x	xxxx	xxxx	NOT USED
x	x	xxx0	001x	xxxx	xxxx	PERIPHERAL CARD 01 (PCS01[0])
x	x	xxx0	010x	xxxx	xxxx	PERIPHERAL CARD 02 (PCS02[0])
x	x	xxx0	011x	xxxx	xxxx	PERIPHERAL CARD 03 (PCS03[0])
x	x	xxx0	100x	xxxx	xxxx	PERIPHERAL CARD 04 (PCS04[0])
x	x	xxx0	101x	xxxx	xxxx	PERIPHERAL CARD 05 (PCS05[0])
x	x	xxx0	110x	xxxx	xxxx	PERIPHERAL CARD 06 (PCS06[0])
x	x	xxx0	111x	xxxx	xxxx	PERIPHERAL CARD 07 (PCS07[0])
x	x	xxx1	000x	xxxx	xxxx	PERIPHERAL CARD 08 (PCS08[0])
x	x	xxx1	001x	xxxx	xxxx	PERIPHERAL CARD 09 (PCS09[0])
x	x	xxx1	010x	xxxx	xxxx	PERIPHERAL CARD 10 (PCS10[0])
x	x	xxx1	011x	xxxx	xxxx	PERIPHERAL CARD 11 (PCS11[0])
x	x	xxx1	100x	xxxx	xxxx	PERIPHERAL CARD 12 (PCS12[0])
x	x	xxx1	101x	xxxx	xxxx	PERIPHERAL CARD 13 (PCS13[0])
x	x	xxx1	110x	xxxx	xxxx	PERIPHERAL CARD 14 (PCS14[0])
x	x	xxx1	111x	xxxx	xxxx	PERIPHERAL CARD 15 (PCS15[0])
0	1	x000	0000	000x	xxxx	READ ONLY MEMORY (ROMCS[0])
0	1	x00x	xx1x	xxxx	xxxx	INPUT/OUTPUT REQUIRED (IOREQ[0])
0	1	x00x	x1xx	xxxx	xxxx	⋮
0	1	x00x	1xxx	xxxx	xxxx	⋮
0	1	x001	xxxx	xxxx	xxxx	⋮
0	1	x000	0000	010x	1xxx	DIRECT MEMORY ACCESS SUBSYSTEM (DMASS[0])
0	1	x000	0000	010x	0xxx	MISCELLANEOUS (MISCS[0])

LEGEND:

x Don't care bit

Figure 3-21: Chip Select and Control Signals Address Decode

Input/Output Chip Selects. The address decoder enables 1 out of 15 Peripheral Chip Select (PCS) signals (PCS15—01[0]) from latched address bits 24 through 21 (LPA24[1] through LPA21[1]). For the 3B2/400 computer, only 12 peripheral chip selects (PCS12—01) are used. For the 3B2/300 and 310 computers, only 4 peripheral chip selects (PCS04—01) are used. The PCS15 through PCS13 signals are reserved for future enhancements. PCS00[0] is decoded but has no connection.

A composite input/output chip select signal (CREQ[0]) is sent to the Dual Port Dynamic RAM (DPDRAM) Controller and Arbiter Circuits to request the "Bypass Mode" to access the input/output connectors (feature card slots). The Bypass Sequencer returns a Bypass Mode Acknowledge (LCPUIO[0]) signal to enable the individual input/output card chip selects to be passed to the input/output connectors. All inputs to the Address Decoder from off-board and DMA Subsystem devices are latched under the control of the arbiter (LCPUIO signal).

Other Chip Selects. Other chip selects are used to enable various devices on and off the system board. The onboard devices chip selects decoded from physical address bits 15 through 12 are listed below:

- Memory Management Unit Chip Select (MMUCS[0])
- Time-of-Day Chip Select (TODCS[0])
- Timer Chip Select (TIMRCS[0])
- Nonvolatile RAM Chip Select (NVRCS[0])
- Control and Status Register Chip Select (CSRCS[0])
- Page Register 1 Chip Select (PR1CS[0])
- Page Register 2 Chip Select (PR2CS[0])
- Page Register 3 Chip Select (PR3CS[0])
- Page Register 4 Chip Select (PR4CS[0])
- Direct Memory Access Chip Select (DMACS[0])
- DUART Chip Select (UARTCS[0])
- Hard Disk Controller Chip Select (DSKCS[0])
- Memory Size Chip Select (MSIZECS[0])
- Floppy Disk Controller Chip Select (FCS[0]).

Physical address bits 26—17 and 15, Physical Address Strobe (PAS[0]), and Interrupt Acknowledge (IACK[0]) are combined to generate the following chip select and control signals:

- Read Only Memory Chip Select (ROMCS[0])
- Direct Memory Access Subsystem (DMASS[0])
- Miscellaneous Chip Select (MISCS[0])
- Input/Output Required (IOREQ[0]).

Read Only Memory

The Read Only Memory (ROM) is equipped as either a 32K byte or a 64K byte ROM. Systems equipped with the DEbug MONitor (DEMON) firmware use the 64K byte ROM. Four 16K by 8 read only memory integrated circuits (27128's) form a 64K byte ROM. Four 8K by 8 read only memory integrated circuits (2764's) form a 32K byte ROM. The starting address of ROM is 0x 00000000.

Timers

The timers include the following:

- Time of day (MM58174)
- Periodic (INTEL 8253)
- Sanity (INTEL 8253)
- Bus (INTEL 8253).

The periodic, sanity, and bus timers are an INTEL 8253 Programmable Interval Timer (PIT) package. The PIT package contains three independent 16-bit counters.

Clock/Calendar Timer. The Clock/Calendar Timer (MM58174) calculates current date to tenths of a second. The timer is controlled by a 32.768-kHz oscillator. The timer features automatic leap year calculation, protection for read access when changing data, and low standby current (2.2 volt, 10 microamperes). The accuracy is determined by the 32.768-kHz crystal with a 0.003 percent tolerance ($\pm$1.3 minutes per month).

Periodic Timer. The Periodic Timer (Timer 1) is a self-restarting count down timer. The time base is 100 kHz (CLKTA[1]). Each time Timer 1 reaches zero, the Periodic Interrupt bit (bit 6) is set in the CSR and a level 15 interrupt is sent to the Interrupt Decoder. The Periodic Interrupt is latched in the CSR and the level 15 interrupt asserted until CSR bit 6 is cleared by writing to address 0x 00042010.

Sanity Timer. The Sanity Timer (Timer 0) is a count down timer that is normally reset by software before it reaches zero. The time base is 100 kHz (CLKTB[1]). When the Sanity Timer reaches zero, an error signal turns on the **Diagnostic** indicator, a level 15 interrupt is sent to the Interrupt Decoder, and the Error Timer Time-out bit (bit 15) is set in the CSR. The CSR bit 15 is cleared by writing to address 0x 00044000. This count down timer is started when the power switch is pressed to OFF. System software must read the 8253 package to determine whether Sanity Timer (Timer 0) or the Bus Timer (Timer 2) timed out.

Bus Timer. The Bus Timer (Timer 2) is a count down timer that controls time-outs on the address bus. The time base is 2 MHz (CLK02[1]). Timer 2 is used to generate a fault for addresses that do not respond (send an acknowledge signal). The Bus Timer is reset when the arbiter's acknowledge is inactive. When the Bus Timer reaches zero, a bus time-out signal is sent to the DRAM and Arbiter Circuits, an error signal turns on the **Diagnostic** indicator, a level 15 interrupt is sent to the Interrupt Decoder, and the Error Timer Time-out bit (bit 15) is set in the CSR. The CSR bit 15 is cleared by writing to address 0x 00044000. System software must read the 8253 package to determine whether Sanity Timer (Timer 0) or the Bus Timer (Timer 2) timed out.

Control and Status Register

The Control and Status Register (CSR) is a 16-bit register. It provides low-level access to the system board logic circuits. The CSR controls and monitors various system functions. Certain bits are written (cleared or set) under software control. Other bits are controlled exclusively by hardware logic. CSR bits 03 through 00 reflect the state of system board peripheral devices. All CSR bits are readable by software using either a full or half-word read operation. During a read operation the CSR data is latched so that it remains constant throughout the read cycle. The CSR is NOT cleared by a hardware reset. The CSR is bit-addressable for writing. During a software write of the CSR, only one bit at a time is accessed. The state of the CSR bit after the CSR write operation is dependent only on the address; the data written is a "don't care" bit. The contents of the CSR are part of the error report output by the **/etc/errdump** command. The CSR is identified as "csr" in the error report. The CSR bit assignments and access information are shown in Figure 3-22.

VERSION 2—SYSTEM BOARD CONTROL AND STATUS REGISTER BIT ASSIGNMENTS								
BIT	DESCRIPTION	WRITE ADDRESS	FUNCTION	CONTROL				
15	ERROR TIMER TIMEOUT	0x 00044000	CLEAR		HS	PC		
14	MEMORY PARITY ERROR	0x 00044004	CLEAR		HS	PC		
13	SYSTEM RESET REQUEST	0x 00044008	SET	CR			PS	
12	ALIGNMENT FAULT	0x 0004400C	CLEAR		HS	PC		
11	DIAGNOSTIC INDICATOR ON	0x 00044010 0x 00044014	SET CLEAR			PC PC	PS PS	SR SR
10	FLOPPY MOTOR ON	0x 00044018 0x 0004401C	SET CLEAR			PC PC	PS PS	
09	RESERVED							
08	INHIBIT TIMERS	0x 00044020 0x 00044024	SET CLEAR			PC PC	PS PS	
07	INHIBIT FAULTS	0x 00044028 0x 0004402C	SET CLEAR			PC PC	PS PS	SR SR
06	PERIODIC INTERRUPT	0x 00042010	CLEAR		HS	PC		
05	PIR (LEVEL 8 INTERRUPT)	0x 00044038 0x 0004403C	SET CLEAR			PC PC	PS PS	
04	PIR (LEVEL 9 INTERRUPT)	0x 00044030 0x 00044034	SET CLEAR			PC PC	PS PS	
03	UART INTERRUPT	—	—	BO				
02	FLOPPY DISK INTERRUPT	—	—	BO				
01	DMA INTERRUPT	—	—	BO				
00	INPUT/OUTPUT BOARD FAIL	—	—	BO				

LEGEND:

BO	Signal originates elsewhere and is only buffered in the CSR
CR	Cleared by "system reset" signal
DMA	Direct Memory Access
HS	Set by hardware
PC	Cleared by programmed control
PIR	Programmed Interrupt Request
PS	Set by programmed control
SR	Set by "system reset" signal

Figure 3-22: Version 2 System Board CSR Bit Assignments

Interrupts

Interrupt Mechanism. When an external device requests an interrupt (request for service to the microprocessor), the microprocessor temporarily stops its current execution and jumps to code that services the interrupt. This code is called an interrupt handler. On completion of the interrupt handler code, execution resumes at the point where the interrupt occurred. An interrupt mechanism performs the process execution switch.

There are three functions of the interrupt mechanism, as follows:

1. The interrupt mechanism determines whether or not there will be an interrupt generated in response to an interrupt request. An interrupt is generated if the priority level requested is greater than the priority level in the Interrupt Priority Level (IPL) field of the Processor Status Word (PSW) register of the CPU. If the IPL field equals 0x F, no interrupts are acknowledged except for a nonmaskable interrupt.
2. The interrupt mechanism determines how an interrupt request will be acknowledged and the interrupt identification value. Interrupts are acknowledged as full or quick interrupts. A full interrupt starts an interrupt-handler process by means of a full context/process switch. A quick interrupt causes the interrupt handler to store the current Program Counter (PC) register and PSW register values on the execution stack and set the IPL field of the PSW to 0x F (like a subroutine call). Only a nonmaskable interrupt can interrupt the quick-interrupt handler. A nonmaskable interrupt causes the interrupt handler to store the current PC and PSW values on the execution stack just like a quick interrupt. An interrupted interrupt handler's execution is resumed as a function of popping saved states off the execution stack.
3. The interrupt mechanism saves the interrupted process context and brings in a new process context (process switching). Interrupt-vector tables are provided for full and quick interrupts. The interrupt-vector tables point to the memory locations (addresses) where interrupt PCBPs and PC/PSW pairs are stored.

Interrupt Logic. Eight hardware interrupts are provided. Three of these levels (PINT2—0[0]) are connected to the Input/Output Expansion connector for use by the feature cards that supply their own interrupt vectors. Two interrupt levels are used as Programmed Interrupt Requests (PIRs) and are accessible via the CSR. The three remaining interrupt levels are used by the system board for peripheral devices.

To acknowledge three off-board requests, the interrupt hardware requests the DPDRAM controller to enter the "bypass" mode. When the controller responds with a "bypass mode" acknowledge, the interrupt acknowledge cycle proceeds and the vector is read from the interrupting off-board device.

Interrupt levels are encoded by an 8/3 encoder and applied to the CPU interrupt request inputs as level 15 through 8 interrupts. When interrupts are acknowledged, the CPU uses the address bus bits 05 through 02 to identify the acknowledged level. In the virtual mode (VAD[0]=0), a latched version of address bits 05 through 02 are used by the interrupt circuitry. When bit 2 is low and either bit 3 or bit 4 is high, an off-board interrupt is assumed and an arbiter request is made. When the bus arbiter permits access, the proper off-board interrupt acknowledge signal is sent. Other combinations of address bits 05 through 02 are assumed to be onboard interrupts and a vector is supplied by looping the latched address bits 05 through 02 back to the data bus via a buffer. A unique vector is provided for each onboard interrupt source that is equal to the interrupt level. When an onboard interrupt is decoded, the interrupt circuit sends a wait select (WSEL1[0]).

Interrupt Assignments. Figure 3-23 defines the interrupt levels for the various interrupt sources. Interrupt 11 (INT11[0]) can be caused by either an integral floppy disk or an integral hard disk. Bit 02 of the Control and Status Register (CSR02[1]) is used to determine the interrupt source for a INT11. CSR02[1] is set for a floppy disk interrupt, and is clear for a hard disk interrupt.

VERSION 2 SYSTEM BOARD INTERRUPT ASSIGNMENTS		
LEVEL	**VECTOR**	**SOURCE**
15	15	SYSTEM ERROR AND PERIODIC TIMER (NOTE 1)
14	(NOTE 2)	INPUT/OUTPUT BOARDS (PINT20)
13	13	UARTS AND DMA COMPLETE
12	(NOTE 2)	INPUT/OUTPUT BOARDS (PINT10)
11	11	INTEGRAL DISKS (FLOPPY OR HARD DISK)
10	(NOTE 2)	INPUT/OUTPUT BOARDS (PINT00)
9	9	PIR-9 (FROM CSR)
8	8	PIR-8 (FROM CSR)

NOTES:

1. System error can be a bus time-out, parity error, or input/output card failure.
2. An 8-bit vector is supplied by the input/output card.

LEGEND:

CSR	Control and Status Register
DMA	Direct Memory Access
PIR	Programmed Interrupt Request
UARTS	Universal Asynchronous Receiver/Transmitters

Figure 3-23: System Board Interrupt Assignments

Nonvolatile Random Access Memory

The Nonvolatile Random Access Memory (NVRAM) is a single chip providing 1024 by 4 bits (1024 nibbles) of memory for the storage of system configuration parameters. Parameters include console terminal settings, system error log, and the firmware password. NVRAM is maintained by a backup battery in the absence of VCC. When power is removed from the system, NVRAM enable (chip select) is inhibited to prevent an accidental write operation from destroying the NVRAM data. NVRAM is read and written in nibbles using MOS Data Bus bits 03—00 and address bits 11—02. The following table further defines the contents of NVRAM.

NVRAM CONTENTS		
CATEGORY	**DESCRIPTION**	**NUMBER OF BYTES**
FIRMWARE (59 OF 128 BYTES USED)	FIRMWARE PASSWORD (passwd)	9
	CONSOLE SLOT AND PORT NUMBERS (cons_def)	1
	DOWNLOAD LINK BAUD RATE (link)	2
	DEFAULT BOOT DEVICE (b_dev)	1
	DEFAULT BOOT PATH NAME (b_name)	45
	FLAG TO CHECK FOR SECONTD DISK (dsk_chk)	1
	TOTAL FIRMWARE	59
UNIX OPERATING SYSTEM (66 OF 128 BYTES USED)	CONSOLE FLAGS (cflags)	2
	SAVED MONTH (nv_month)	1
	SAVED YEAR (nv_year)	1
	START OF PHYSICAL MEMORY (spmem)	4
	SYSTEM NAME (sys_name)	9
	ROOT DEVICE (rotdev)	1
	GENERAL STORAGE FOR I/O DRIVERS (ioslotinfo)	48
	TOTAL OPERATING SYSTEM	66
PANIC ERROR INFORMATION	NVRAM SANITY (nvsanity)	4
	COMMAND AND STATUS REGISTER (csr)	2
	PROCESSOR STATUS WORD (psw)	4
	GENERAL PURPOSE REGISTER 3 (r3)	4
	GENERAL PURPOSE REGISTER 4 (r4)	4
	GENERAL PURPOSE REGISTER 5 (r5)	4
	GENERAL PURPOSE REGISTER 6 (r6)	4
	GENERAL PURPOSE REGISTER 7 (r7)	4
	GENERAL PURPOSE REGISTER 8 (r8)	4
	ADDRESS POINTER (oap)	4
	PROGRAM COUNTER (opc)	4
	STACK POINTER (osp)	4
	FRAME POINTER REGISTER (ofp)	4
	INTERRUPT STACK POINTER (isp)	4
	PROCESS CONTROL BLOCK POINTER REGISTER (pcbp)	4
	FAULT CODE REGISTER (mmufltcr)	4
	FAULT ADDRESS REGISTER (mmufltar)	4
	MMU SECTION RAM A (mmusrama)	16
	MMU SECTION RAM B (mmusramb)	16
	LOCAL FRAME POINTER (lfp)	4
	MESSAGE (message)	16
	PARAMETER 1 (param1)	16
	PARAMETER 2 (param2)	16
	TIME (time)	16
	TOTAL SAVED PANIC DATA	166
AND		
FIRMWARE ERROR INFORMATION (186 OF 254 BYTES USED)	GOOD ERROR (gooderror)	4
	ERROR NUMBER (errno)	4
	PROCESSOR STATUS WORD (psw)	4
	PROGRAM COUNTER (pc)	4
	MISCELLANEOUS (misc)	4
	TOTAL UNEXPECTED INTERRUPT AND EXCEPTION DATA	20
CHECKSUM (2 BYTES)	NVRAM CHECKSUM	2
TOTAL (512 BYTES)	TOTAL BYTES USED	313

Dual Port Dynamic Random Access Memory Controller

General. The system main memory is a Dual Port Dynamic Random Access Memory (DPDRAM). The system board CPU uses one port and the other memory port is shared by the feature cards and integral Direct Memory Access Controller (DMAC). The DPDRAM Controller provides the system board CPU direct access to the I/O bus without passing through the RAM. The Dynamic Random Access Memory (DRAM) Controller handles the exchange of data and address information between the I/O bus and the system board CPU when operating in the "bypass mode."

Figure 3-24 is a functional block diagram of the DPDRAM Controller. The DRAM Controller for the DPDRAM is divided into the following functional areas:

- Address Generation Logic (address multiplexer)
- Request Generator
- Arbitration Logic
- Memory Refresh Logic
- Sequencer
- Bypass Logic
- Data Byte Rotate Unit Logic
- Parity Generation and Checking Logic.

Each of these functional areas is briefly described in the following paragraphs.

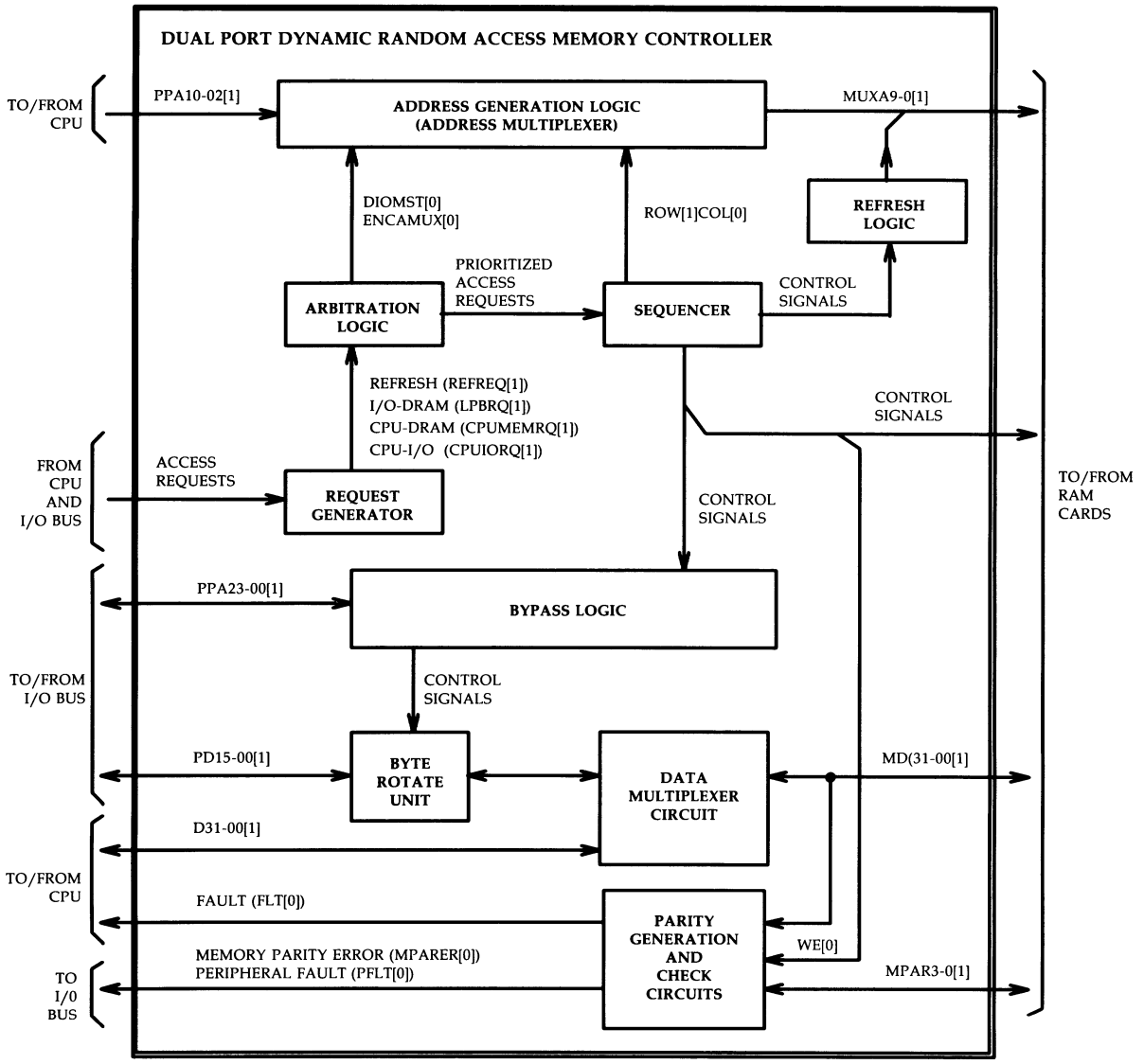


Figure 3-24: Dual Port Dynamic Random Access Memory Controller — Functional Block Diagram

Address Generation Logic. The Address Generation Logic latches the stable virtual address during virtual to physical address translation. Since the 11 least significant bits of a virtual address and a physical address are identical, CPU—memory read accesses are started when the CPU presents a stable virtual address. The early start using the 11 least significant address bits enhances system performance.

Request Generator. The Request Generator synchronizes the bus requests with the system clock and passes the synchronized data requests to the Arbitration Logic. The Request Generator passes four types of requests to the Arbitration Logic. These requests are listed below:

Memory Refresh (REFREQ[1])
The memory refresh request is automatically generated every 16 microseconds.

Input/Output—DRAM (LPBRQ[1])
The input/output—memory request can originate from a feature card (PBRQ[0]) or from the Direct Memory Access Controller (XPBRQ[0]). The request is passed to the Arbitration Logic as LPBRQ[1].

CPU—DRAM (CPUMEMRQ[1])
The CPU—memory read or write operation requests are sent to the Arbitration Logic as CPUMEMRQ[1].

CPU—Input/Output (CPUIORQ[1])
The CPU—input/output exchange request is asserted by the Address Decoder (CREQ[0]) and is sent to the Arbitration Logic as CPUIORQ[1].

Arbitration Logic. The Arbitration Logic determines which requests for memory access are to be acknowledged. These access requests from highest to lowest priority follow:

- Memory Refresh (highest priority)
- Input/Output—DRAM
- CPU—DRAM
- CPU—Input/Output (lowest priority).

Memory Refresh Logic. The refresh of the DRAM is done one row at a time every 16 microseconds. The Request Generator is a counter and request flip-flop. Refresh requests are derived from the 1-MHz clock and occur every 16 microseconds. The refresh request increments the refresh address counter.

A memory refresh operation can occur between input/output to DRAM block transfers or between the read and write halves of a CPU/MMU interlocked operation. Refresh operations continue during reset sequences to retain any data which existed before the reset.

Sequencer. The Sequencer generates the control signals (strobes) for the access operations enabled by the Arbitration logic. The Sequencer is a Field Programmable Logic Array (FPLA) and flip-flop network that combine to generate a variety of memory control signals.

Data Byte Rotate Unit. The Data Byte Rotate Unit is a collection of buffers used to multiplex the 32-bit data bus to/from the main memory to an 8- or 16-bit data bus for the I/O bus. This accommodates the input/output cards and system board devices in the Direct Memory Access Subsystem that do not have a 32 bit capability. The byte rotate unit provides data alignment and packing for 8- and 16-bit peripherals when they access the 32-bit main memory and for system board CPU when the CPU communicates directly with the input/output (feature) cards. The system board devices that use the Data Byte Rotate Unit are listed below:

- Direct Memory Access Controller
- Dual Universal Asynchronous Receiver/Transmitter
- Integral Floppy Disk Controller
- Integral Hard Disk Controller.

The Byte Rotate Unit is controlled by the Sequencer logic. The PSIZE16[0] determines whether a peripheral is capable of transferring 8 or 16 bits at a time. Address bits 01 and 00 are used to select the data bus bytes. PSIZE16 is a 0 for 16-bit transfers; PSIZE16 is a 1 for 8-bit transfers. The PSIZE16[0] signal is sent by the peripheral (feature card) in response to a chip select signal. When a peripheral is a 16-bit device, 8-bit accesses are done by asserting the appropriate data strobe (PDS1—0[0]). Devices having 8-bit data interfaces require four passes to transfer a complete 32-bit word. Devices having 16-bit data interface require two passes to transfer a complete 32-bit word.

Byte 0 (bits 31—24) is the least significant byte. Byte 1 is bits 23—16. Byte 2 is bits 15—08. Byte 3 (bits 07—00) is the most significant byte. Address bits 01 and 00 are decoded (binary) to select the data bus bytes 3—0 as applicable. For 8-bit operations both address bits 01 and 00 are used to select the data bus bytes. For 16-bit operations only address bit 01 is used to select the data bus bytes (address bit 00 is not used in 16-bit operations). For 16-bit operations either data bus bytes 1 and 0 or bytes 3 and 2 are selected by only address bit 01. When address bit 01 is high [1], data bus bytes 2 and 3 are selected (bits 15—00). When address bit 01 is negated, data bus bytes 0 and 1 are selected (bits 31—16). The data strobes (PDS0[0] and PDS1[0]) are used to select which byte or bytes to access within the main memory. Figure 3-25 summarizes the decoding of the PSIZE16, PPA01, PPA00, PDS0, and PDS1 for the selection of data bytes for the 16-bit peripheral input/output bus and for the 32-bit main memory accesses.

SIZE BIT	ADDRESS BITS		DATA STROBES		VALID DATA BYTES	
PSIZE16[0]	PPA01[1]	PPA00[1]	PDS0[0]	PDS1[0]	32-BIT MAIN MEMORY	16-BIT INPUT/OUTPUT BUS
16 BIT						
0	0	x	0	0	0 AND 1	0 AND 1
0	0	x	0	1	0	0
0	0	x	1	0	1	1
0	0	x	1	1	ILLEGAL	—
0	1	x	0	0	2 AND 3	0 AND 1
0	1	x	0	1	0 OR 2	0
0	1	x	1	0	1 OR 3	1
0	1	x	1	1	ILLEGAL	—
8 BIT						
1	0	0	x	0	0	1
1	0	1	x	0	1	1
1	1	0	x	0	2	1
1	1	1	x	0	3	1

LEGEND:
x Don't care bit

Figure 3-25: Data Byte Selection Summary

Parity Generation and Checking. Four parity bits (MPAR3—0[1]) are generated for each of the four data bytes. Parity is checked only as part of read operations. If bad parity is detected, the Peripheral Fault (PFLT[0]) and Memory Parity Error (MPARER[0]) signals are asserted to the system board CPU or peripheral controllers (feature cards) depending on the type of access.

Bypass Logic. The Bypass Logic is used to establish direct communication between the system board CPU and feature cards without having to go through the main memory. Hence the term "bypass" is used to mean that main memory is bypassed for system board—feature card direct communication. The Bypass Logic passes the low order 24 bits of the Address Bus and the lower order 16 bits of the data bus directly to the I/O bus during direct communication between CPU and feature cards.

The system board requests the "bypass" mode by asserting the composite Input/Output Chip Select signal (CREQ[0]).

Direct Memory Access Subsystem

Subsystem Structure. Figure 3-26 is a high-level functional block diagram of the Direct Memory Access (DMA) Subsystem. The DMA Subsystem includes the following:

- Direct Memory Access Controller
- Dual Universal Asynchronous Receiver/Transmitter
- Integral Hard Disk Controller
- Integral Floppy Disk Controller.

Each of these functional areas is described in the following paragraphs.

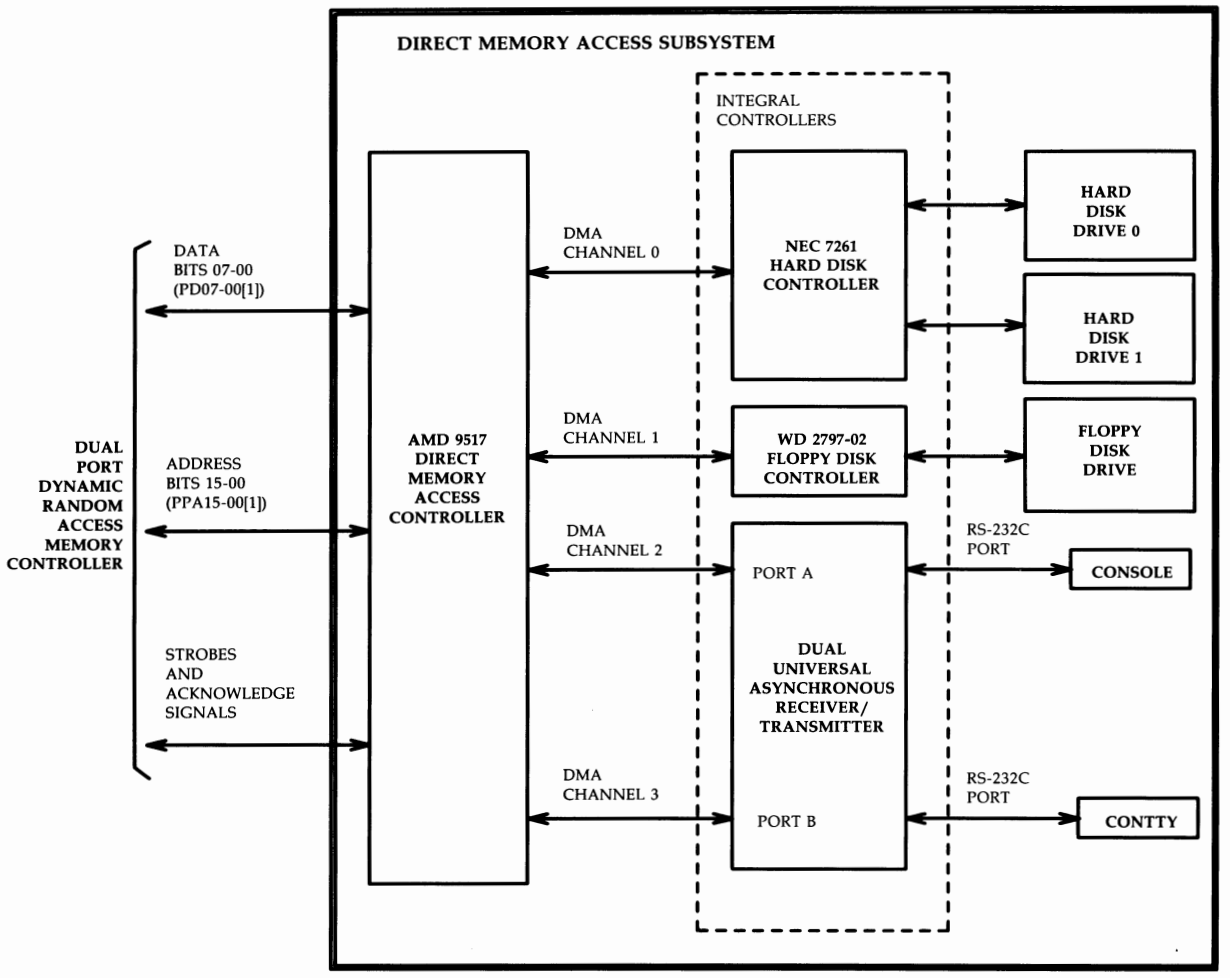


Figure 3-26: Direct Memory Access Subsystem — Functional Block Diagram

Direct Memory Access Controller. The integral Direct Memory Access Controller (DMAC) serves the Dual Universal Asynchronous Receiver/Transmitter (DUART), integral Hard Disk Controller, and the integral Floppy Disk Controller. The DMAC has four independent DMA channels. Each channel has separate registers for mode control, current address, base address, current word count, and base word count.

The DMAC generates a 16-bit address. An additional 8-bit Page Register is used for each of the four DMA channels to provide DMA accessibility to the 22-bit DPDRAM. The most significant bit of each Page Register is the read/write bit.

Dual Universal Asynchronous Receiver/Transmitter. The CONSOLE (UART 0) and CONTTY (UART 1) are driven by a Signetics 2681-40 DUART. Each channel (0 and 1) provides the following signals:

- Transmit data (TXD)
- Receive data (RXD)
- Data Carrier Detect (DCD)
- Data Terminal Ready (DTR).

Electrically, the DUART is on the peripheral bus with five other devices in the DMA Subsystem.

The UART has three output ports that are used for non-UART functions. These functions are listed below:

- Control of off-board AC power relay via output port 2 (OP2) (PWRON[0]). The signal is high during normal operations.
- Control of the Power indicator under certain operational conditions via output port 3 (OP3) (GLEDON[1]).
- Output port 4 (OP4) (UFEJCT[0]) is buffered and is sent to the floppy disk interface connector for feature application.
- Output port 5 (OP5) (UFDSEL[0]) is buffered and sent to J10 as the Floppy Drive Select (FDSEL[0]).

Integral Hard Disk Controller. The integral Hard Disk Controller provides data and access control for two Winchester disks. The interface is a ST-506 or "floppy disk type" interface at a data rate of 5 MHz. Data transfers are DMA controlled. All data lines are differential RS-422. The receiving end of all data pairs is terminated by 100-ohm resistors. All control lines are open-collector. The receiving end of all control lines are terminated by a resistor network of 220 ohms to VCC and 330 ohms to ground.

The controller connects to data bus bits 07—00[1]. The chip enable is DSKCS[0]. The controller is an NEC 7261 providing the following:

- Programmable track format
- Control two disk drives
- Parallel seek capability
- Multitrack and multisector capability
- Error checking and handling.

Integral Floppy Disk Controller. The integral Floppy Disk Controller provides data and access control for a single floppy disk drive. The controller is a WD 2797-02 and provides the following:

- Integrated data separation
- Integrated write precompensation
- Single Frequency Modulation (FM) and Modified Frequency Modulation (MFM) density
- Automatic seek with verify
- Soft sector compatibility.

The controller connects to data bus bits 07—00[1]. The chip is enabled by the FCS[0] signal. All floppy disk interface signals are terminated at the receiving end by a resistor network of 150 ohms to VCC.

System Board Firmware

The system board firmware is programmed instructions stored in Read Only Memory (ROM) which form the basic operating system when the system is not running the UNIX operating system. The purpose of this firmware is to initialize the system and provide the means to load and run other programs such as the UNIX operating system, **filledt**, and **dgmon**. The firmware level built-in programs are listed below:

baud	Change the firmware baud rate. Valid firmware baud rates are 50, 75, 110, 134, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, and 38400. The default baud rate is 9600.
edt	Display the Equipped Device Table (EDT) data.
error info	Display expanded firmware error message information. This capability is provided with firmware PF3 and later versions. (Command is intentionally omitted from firmware command menu.)
newkey	Make a new floppy key.
passwd	Change the firmware password.
sysdump	Copy the system image (RAM) to floppy disks.
version	Display firmware version information.

When the system is RESET or first powered on, the system board firmware controls the initialization of the system. The sequence of events follows:

- Test processor sanity.
- Check ROM.
- Check NVRAM.
- Check RAM.
- Check DUART.
- Check Disk Sanity.
- Self-configuration (build the EDT).
- Run normal diagnostics on all equipped boards/cards listed in the EDT.
- Boot the UNIX operating system.

System Board EDT Data

The following table shows the EDT data for a system board. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI).

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0001
DEVICE NAME (dev_name)	SBD
REQUEST QUEUE SIZE (rq_size)	0x 00
COMPLETION QUEUE SIZE (cq_size)	0x 00
BOOT DEVICE (boot_dev)	1
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	1
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	1
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM518A/B/C System Boards

Figure 3-27 is a functional block diagram of the Version 3 system board. The Version 3 3B2 computer system board features are listed below:

- Central Processing Unit (CPU)
- Memory Management Unit (MMU) (two MMUs on CM518C)
- Math Acceleration Unit (MAU)
- Time-of-Day (TOD), interval, system sanity, and unbuffered bus timers
- 32-bit Control, Status, and Error Register (CSER)
- Nine interrupt levels including nonmaskable interrupts
- Two RS-232C serial ports with data set control
- Floppy controller with digital data separator (no adjustments)
- Direct Memory Access Controller (DMAC) for integral floppy disk and Universal Asynchronous Receiver/Transmitters (UARTs)
- 2 megabytes to 64 megabytes of Dynamic Random Access Memory (DRAM) with hardware refresh and Error Correction Code (ECC)
- Supports 8- and 16-bit feature cards
- Power reset of system board and feature cards
- "Soft power" control
- 2K by 8-bit Nonvolatile Random Access Memory (NVRAM)
- 3.6 volt DC lithium battery for NVRAM, TOD clock, and feature cards
- Synchronous memory controller up to 24 MHz
- Supports a 12-slot Enhanced Input/Output (EIO) bus with sequential access capability
- Supports both buffered and unbuffered microbus slots.

Functionally, the CM518 System Boards are very similar. Physically, the CM518A uses a WE 32100 chipset while the CM518B/C System Boards use the WE 32200 chipset. The CM518C System Board also has two MMUs (WE 32201). Refer to Chapter 2, Equipment Description, for information on the physical configuration of the CM518 System Boards.

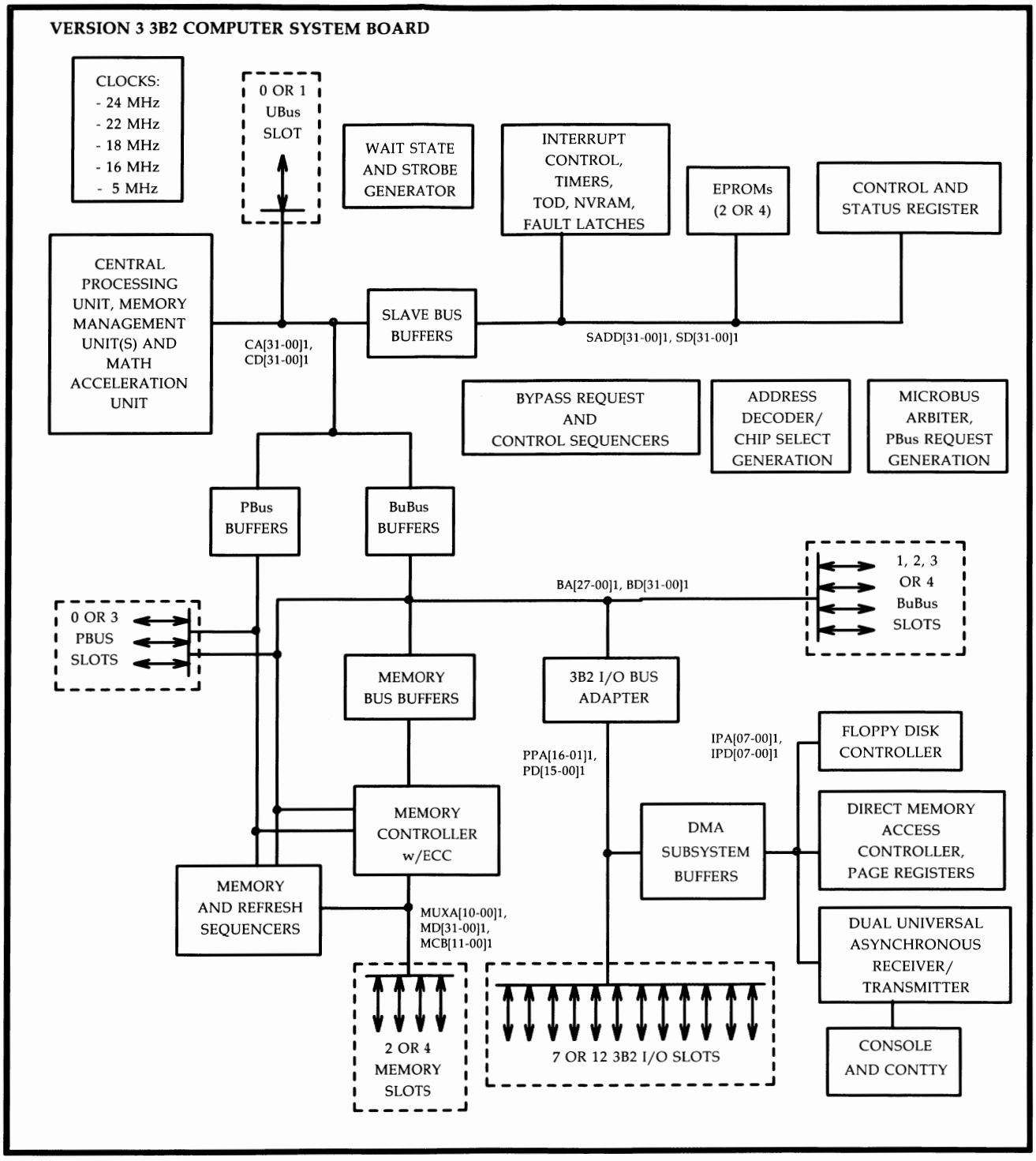


Figure 3-27: Version 3 3B2 Computer System Board — Functional Block Diagram

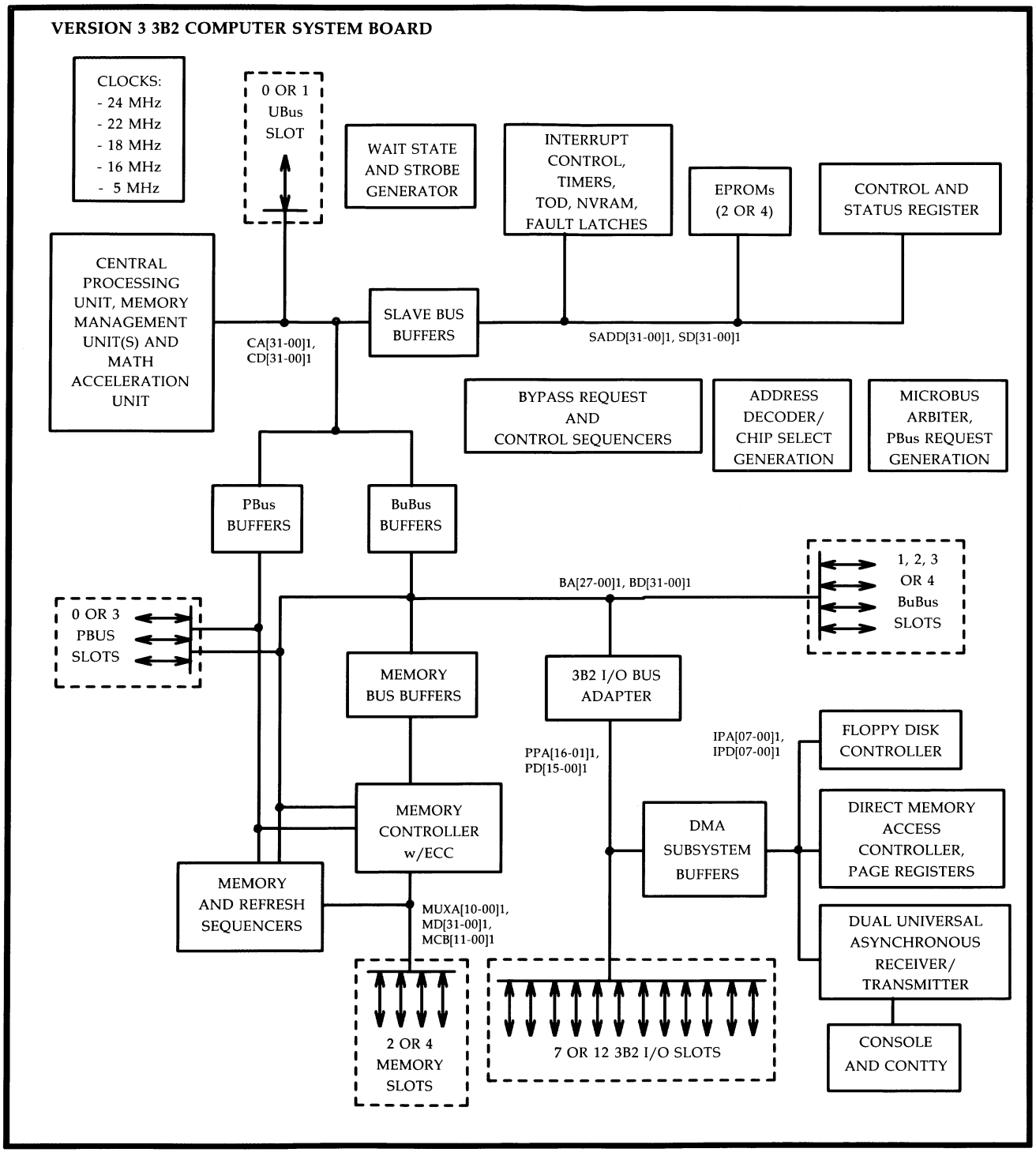


Figure 3-27: Version 3 3B2 Computer System Board — Functional Block Diagram

Central Processing Unit

The Central Processing Unit (CPU) on a CM518A System Board is a WE 32100 Microprocessor. The CPU on a CM518B/C System Board is WE 32200 Microprocessor. The WE 32100 chipset is covered in the "CM190A/ED-4C637-30 System Board" section of this chapter for Version 2 system boards. Refer to that section for detailed information on the CPU/MMU/MAU chips of the CM518A System Board. The remainder of this section will pertain to the WE 32200 chipset used on the CM518B/C System Boards.

The CPU provides separate 32-bit address and data busses. The 32-bit address bus is used to address memory or peripherals mapped into the system memory space using physical or virtual addresses. Data is read to or written from the CPU over the 32-bit, bidirectional, data bus in either word (32-bit), half-word (16-bit) or byte (8-bit) widths. The CPU automatically expands bytes and half-words to words (32 bits) for processing. Zeros fill the high-order bits for unsigned operations. For signed operations, the sign bit (bit 7 for bytes, bit 15 for half-words) fills the high-order bits.

Instruction execution speed is enhanced by an internal instruction queue and an internal instruction cache. The instruction queue is an 8-byte, First-In-First-Out (FIFO) queue that stores prefetched instructions. The instruction cache is a 64-word cache used to increase the CPU performance by reducing the external memory reads for instruction fetches. When an instruction fetch from memory occurs, the instruction data is placed in both the instruction queue and the instruction cache. If the instruction data is needed again, it is read from the cache rather than from external memory.

Functionally, the system board CPU consists of bus interface control, main controller, fetch unit, and the execute unit circuits. Figure 3-28 shows a functional block diagram of the CM518B/C System Board CPU.

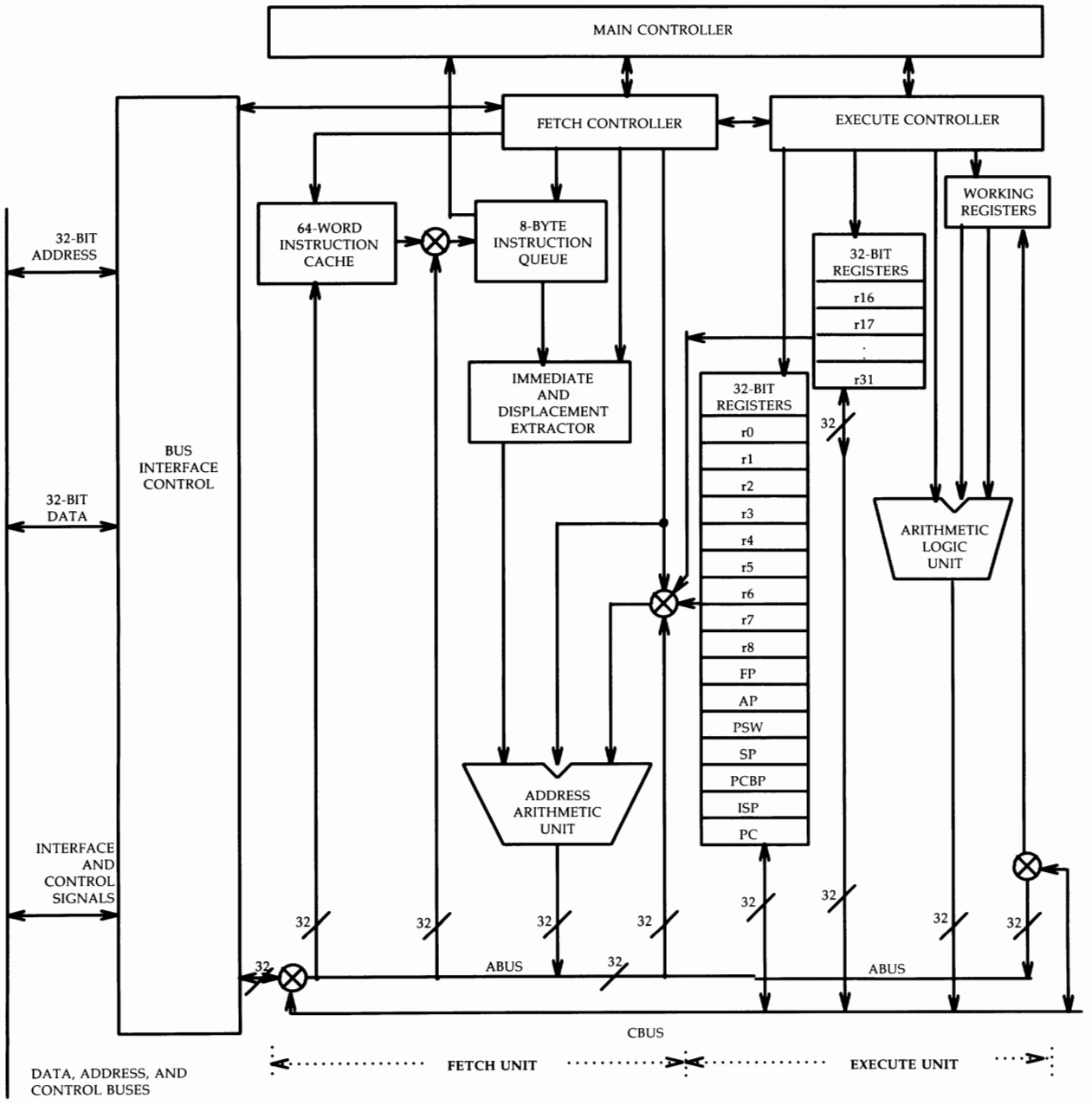


Figure 3-28: CM518B/C System Board CPU — Functional Block Diagram

Bus Interface Control. The bus interface control provides all strobes and control signals necessary to interface with peripherals.

Main Controller. The main controller is responsible for acquiring and decoding instruction opcodes and directing the action of the fetch and execute controllers as the specified instruction is executed. The main controller also responds to and directs the handling of interrupts and exceptions.

Fetch Unit. The fetch unit handles the instruction stream and does memory-based operand accesses. The unit consists of a fetch controller, an instruction cache, and instruction queue, an immediate and displacement extractor, and an Address Arithmetic Unit (AAU).

Execute Unit. The execute unit does all arithmetic, binary coded decimal, logical operations, all shift and rotate operations, and computes condition flags. It consists of an execute controller, thirty-two 32-bit registers, working registers, and a 33-bit wide Arithmetic Logic Unit (ALU). The thirty-two 32-bit registers are user-accessible. These registers include 17 general-purpose registers (r23—r16, r8—r0), 8 general-purpose kernel registers (r31—r24), and 7 dedicated registers (r15—r9). All registers except the program counter (r15) and the process status word (r11) can be referenced in all addressing modes. The general-purpose kernel registers (r31—r24), processor status word (r11), process control block pointer (r13), and the interrupt stack pointer (r14) are privileged registers that can be read at any time, but these registers can only be written when the CPU is in the kernel (highest) execution level. The working registers are used exclusively by the CPU and are not user-accessible. The thirty-two 32-bit CPU registers are further defined in the following paragraphs.

General Purpose Registers (r23—r16, r8—r0)

Seventeen general-purpose registers are used for accumulation, addressing, and for temporary data storage. They can be used in any addressing mode by any program (privileged or nonprivileged). Registers r2, r1, and r0 are also implicitly used by certain other data transfer instructions and by certain operating system instructions. Registers r2, r1, and r0 are also used by the CPU as a scratch pad. The contents of registers r8—r3 are part of the error report output by the **/etc/errdump** command.

Frame Pointer Register (r9)

The Frame Pointer (FP) register (r9) contents point to the beginning address (location) in the stack of a function's local variables. The contents of register r9 are part of the error report output by the **/etc/errdump** command.

Argument Pointer Register (r10)

The Argument Pointer (AP) register (r10) contents point to the starting address (location) in the stack where a set of arguments for a function have been pushed. The contents of register r10 are part of the error report output by the **/etc/errdump** command. This register is identified as "oap" in the error report.

Processor Status Word Register (r11)

The Processor Status Word (PSW) register (r11) contains information that determines the current execution state of the CPU. The PSW register is kernel level privileged. The contents of PSW register (r11) are part of the error report output by the **/etc/errdump** command. This register is identified as "psw" in the error report. The format of the PSW register is as follows.

	PROCESSOR STATUS WORD REGISTER																		
BITS	31—30	29	28	27	26	25	24	23	22	21—18	17	16—13	12—11	10—09	08	07	06—03	02	01—00
FIELD	UNUSED	EA	EX/UC	AR	X	CFD	QIE	CD	OE	NZVC	TE	IPL	CM	PM	R	I	ISC	TM	ET

The PSW register fields are defined in the following paragraphs.

UNUSED Bits 31—30 are not used and are always cleared [0].

EA Bit 29 is the Arbitrary Byte Alignment Enable (EA) bit. When set [1], the arbitrary byte alignment is enabled allowing the CPU to read or write word and half-word data from any byte boundary. When clear [0], arbitrary byte alignment is disabled and the alignment fault detection is enabled. The bit is cleared on external reset.

EX/UC Bit 28 is the Normal Exception and User Call (EX/UC) option bit. When set [1], normal exception procedures are identical to process switches and user-initiated process switches are enabled. The bit is cleared on external reset.

AR Bit 27 is the Additional Register Save (AR) bit. When set [1], this bit enables the additional 8 registers (r23—r16) to be saved during a process switch if no block moves are being executed. The bit is cleared on external reset.

X Bit 26 is the Extend Carry/Borrow (X) bit. This bit represents the condition code for the binary coded decimal operations. The bitcan only be set if there is a carry or borrow from a binary coded decimal arithmetic operation. The bit is reset if there is no carry or borrow.

CFD Bit 25 is the Cache Flush Disable (CFD) bit. When set [1], instruction cache flushing is disabled when a new process is loaded. When clear [0], the contents of the cache are flushed when a new process is loaded.

QIE Bit 24 is the Quick Interrupt Enable (QIE) bit. When set [1], the quick interrupt handling facility is enabled. When clear [0], an interrupt causes a process switch to a full interrupt processing sequence.

CD Bit 23 is the Cache Disable (CD) bit. When set [1], the instruction cache is not used. When clear [0], the instruction cache is used to store and read text. Normally this bit is clear [0].

OE Bit 22 is the Enable Overflow Trap (OE) bit. When set [1], overflow traps are enabled. This bit is cleared when an overflow trap is detected and processed.

NZVC Bits 21—18 are used to represent four condition codes that reflect the status of the most recent instruction execution. The codes are tested using conditional branching instructions and indicate the following when set.

Bit 21[1] — Negative (N)
Bit 20[1] — Zero (Z)
Bit 19[1] — Overflow (V)
Bit 18[1] — Carry (C)

TE Bit 17 is the Trace Enable (TE) bit. When set [1], the trace function is enabled, causing a trace trap to occur after execution of the next instruction. Debugging and analysis software use the trace facility for single-stepping a program.

IPL Bits 16—13 are the Interrupt Priority Level (IPL) bits. Bit 13 is the least significant bit. Fifteen interrupt levels are available. An interrupt, unless it is a nonmaskable interrupt, must have a higher priority than the current registered IPL bits in order for the interrupt to be acknowledged. Level 0000 indicated that any of the fifteen interrupt priority levels (0001 through 1111) can interrupt the CPU. A registered IPL of 1111 indicates that no interrupts (except a nonmaskable interrupt) can interrupt the CPU.

CM Bits 12 and 11 are the Current Execution Mode (CM) bits. The code for bits 12 and 11 are as follows.

BIT 12	BIT 11	DESCRIPTION
0	0	KERNEL LEVEL
0	1	EXECUTIVE LEVEL
1	0	SUPERVISOR LEVEL
1	1	USER LEVEL

PM Bits 10 and 09 are the Previous Execution Mode (PM) bits. The code for bits 10 and 09 are as follows.

BIT 10	BIT 09	DESCRIPTION
0	0	KERNEL LEVEL
0	1	EXECUTIVE LEVEL
1	0	SUPERVISOR LEVEL
1	1	USER LEVEL

R-I Bits 08 and 07 are the Register-Initial Context (R-I) bits. These bits control the CPU context switching strategy. The I bit (bit 07) determines if a process executes from initial (I=1) or intermediate saved context (I=0). The R bit (bit 08, read only) determines if the registers of a process should be saved during a process switch (R=1).

ISC Bits 06—03 are the Internal State Code (ISC) bits. The ISC bits are used to distinguish between exceptions of the same type. This field is used with the Exception Type (ET) field to determine when exception occurred. Traps, exceptions, and faults are equivalent with respect to ISC. Normal exceptions are decoded on a priority scheme if more than one occurs in a particular cycle. Exceptional conditions that reset the PSW flags are indicated by an asterisk (*) in the following data.

EXCEPTION TYPE	EXCEPTION	ISC BITS 6 5 4 3
NORMAL EXCEPTION (ET=11)	INTEGER ZERO-DIVIDE	0 0 0 0*
	TRACE TRAP	0 0 0 1
	ILLEGAL OPCODE	0 0 1 0
	RESERVED OPCODE	0 0 1 1
	INVALID DESCRIPTOR	0 1 0 0*
	EXTERNAL MEMORY FAULT	0 1 0 1
	GATE VECTOR FAULT	0 1 1 0
	ILLEGAL LEVEL CHANGE	0 1 1 1
	RESERVED DATA TYPE	1 0 0 0*
	INTEGER OVERFLOW	1 0 0 1
	PRIVILEGED OPCODE	1 0 1 0
	BREAKPOINT TRAP	1 0 1 1
	PRIVILEGED REGISTER	1 1 1 1
STACK EXCEPTION (ET=10)	STACK BOUND	0 0 0 0
	STACK FAULT	0 0 0 1
	INTERRUPT ID FETCH	0 0 1 0
PROCESS EXCEPTION (ET=01)	OLD PCB FAULT	0 0 0 0
	GATE PCB FAULT	0 0 0 1
	NEW PCB FAULT	0 1 0 0
RESET EXCEPTION (ET=00)	OLD PCB FAULT	0 0 0 0
	SYSTEM DATA	0 0 0 1
	INTERRUPT STACK FAULT	0 0 1 0
	EXTERNAL RESET	0 0 1 1
	NEW PCB FAULT	0 1 0 0
	GATE VECTOR FAULT	0 1 1 0

TM Bit 02 is the Trace Mask (TM) bit. This read-only field masks the Trace Enable (TE) bit for the duration of one instruction to avoid a trace trap. The TM bit is set [1] at the start of every instruction. The TM bit is cleared [0] as part of every microsequence that performs a context switch, a return from gate, or when any fault/interrupt is processed.

ET Bits 01 and 00 are the Exception Type (ET) bits. The ET field is used with the Internal State Code (ISC) field (PSW06—03) to distinguish between exceptions of the same type. The code for bits 01 and 00 are as follows.

BIT 01	BIT 00	DESCRIPTION
0	0	ON RESET EXCEPTION
0	1	ON PROCESS EXCEPTION
1	0	ON STACK EXCEPTION
1	1	ON NORMAL EXCEPTION

Stack Pointer Register (r12)

The Stack Pointer (SP) register contains the current 32-bit address of the top of the execution stack. This is the memory address of the next place where an item can be stored (pushed) on the stack or the last place where an item was retrieved (popped) from the stack. The SP implements a Last-In-First-Out (LIFO) queue for efficient subroutine linkage and local variable storage. The contents of Stack Pointer register (r12) are part of the error report output by the **/etc/errdump** command. This register is identified as "osp" in the error report.

Process Control Block Pointer Register (r13)

The Process Control Block Pointer (PCBP) register contains the 32-bit address of the Process Control Block (PCB) for the current process. The PCBP register is kernel level privileged (can only be written when the CPU is in the kernel mode). The PCB contains all switchable process context collected into a compact form for ease of movement between system memory and privileged internal registers. This context consists of the initial and current contents of the processor status word, program counter, and stack pointer; the last contents of registers r0 through r10; boundaries for an execution stack; and block move specifications for the process. The contents of register r13 are part of the error report output by the **/etc/errdump** command. This register is identified as "pcbp" in the error report.

Interrupt Stack Pointer Register (r14)

The Interrupt Stack Pointer (ISP) register (r14) contains the 32-bit memory address of the top of the interrupt stack. This stack is used when an interrupt request is received. The interrupt stack is also used by the Call Process (CALLPS) and Return To Process (RETPS) instructions. The ISP register is kernel level privileged. The contents of register r14 are part of the error report output by the **/etc/errdump** command. This register is identified as "isp" in the error report.

Program Counter Register (r15)

The Program Counter (PC) register (r15) contains the 32-bit memory address of the instruction being executed or, on instruction completion, contains the starting address of the next instruction to be executed. The contents of register r15 are part of the error report output by the **/etc/errdump** command. This register is identified as "opc" in the error report.

General-Purpose Kernel Registers (r31—r24)

These eight registers can be used for accumulation, addressing, or temporary storage. They are kernel-level privileged and can be used in any addressing mode by any privileged program.

Memory Management Unit

The Memory Management Unit (MMU) on the CM518A System Board is a WE 32101 Memory Management Unit.

Note: The WE 32100 chipset is covered in the "CM190A/ED-4C637-30 System Board" section for Version 2 system boards. Refer to that section for detailed information on the CPU/MMU/MAU chips of the CM518A System Board.

The MMU on a CM518B/C System Board is a WE 32201 Memory Management Unit. Figure 3-29 shows how the MMU connects to the system. The internal MMU address spectrum is shown in Figure 3-30. Figure 2-31 shows the virtual to physical address translation for paged segments.

The MMU manipulates the microprocessor's address space by translating the virtual microprocessor addresses into physical address information. The 32-bit address can access over 4 gigabytes (2^{32}) of system memory or peripherals. The MMU also supports demand paged and demand segmented virtual memory. This permits large programs to efficiently use physical memory space. The WE 32201 MMU comes with an on-chip 4K byte, 2-way, set-associative instruction/data cache that returns data with zero wait states on CPU virtual to physical memory accesses.

The MMU divides the virtual address space into four sections. Each of these four sections can be subdivided into as many as 8K segments per section. These segments are paged and are mapped into the physical address space by the MMU. A paged segment can contain up to sixty-four 2K byte pages. Since segments are a multiple of pages, they always start on page boundaries.

Virtual addresses are relative addresses of an active process. Physical addresses are addresses that the main store controller can interpret as the true physical location of the memory. The function of the MMU is to translate virtual addresses to physical addresses. The address of each byte within a 2K byte block (offset) is not translated because the smallest size data block that can be placed in the main store by the MMU is 2K bytes. Therefore, the lower 11 bits of the virtual address spectrum and the lower 11 bits of the physical address spectrum are the same. The MMU stores information describing the physical location of blocks of 2K bytes of process data. The description locations are stored in the MMU caches. The MMU uses four caches: ID Number Cache (IDNC), Current ID Number Registers (CIDNR), Segment Descriptor Cache (SDC) and Page Descriptor Cache (PDC).

Virtual address space is further described in Appendix A.

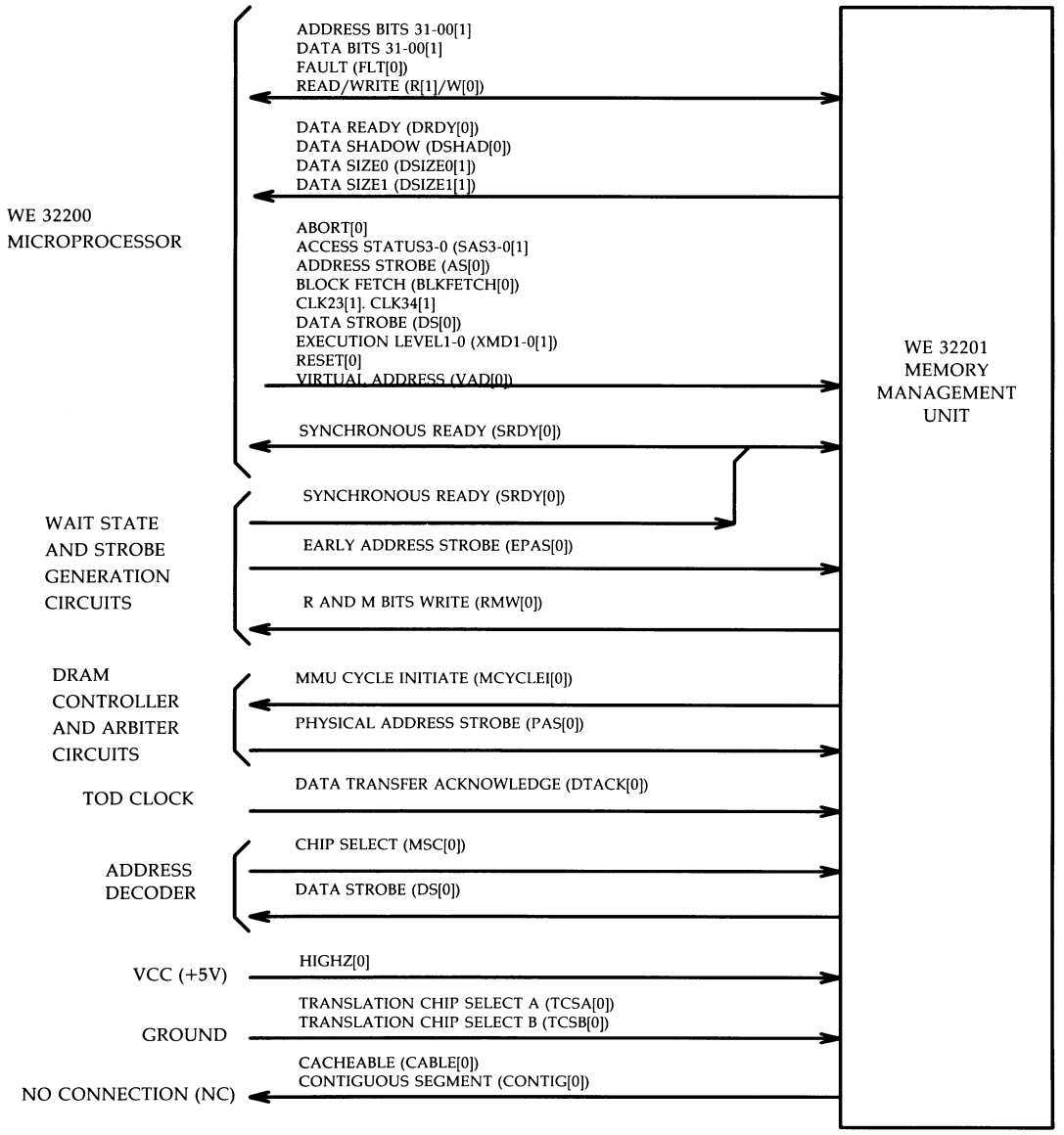


Figure 3-29: WE 32201 MMU Interconnection Diagram

ID Number Cache. The ID Number Cache (IDNC) is used to transparently assign ID numbers to each section of the MMU. The cache is organized in a 16-entry, fully associative configuration. Each entry is 32 bits in length divided into "tag" bits and data bits.

Current ID Number Registers. The Current ID Number Registers (CIDNR) contain the four current ID numbers (consisting of 4 bits each). The CIDNR is used during translation to select the ID number to be used in the page descriptor cache tag lookup.

Segment Descriptor Cache. The Segment Descriptor Cache (SDC) consists of eight entries in a directly mapped configuration. Each entry is 64 bits in length.

Page Descriptor Cache. The Page Descriptor Cache (PDC) consists of sixty-four 64-bit entries organized in a fully associative configuration.

Section Random Access Memories. The MMU contains two Random Access Memory (RAM) areas called Section RAM A (SRAMA) and Section RAM B (SRAMB). Each of these areas contain four 32-bit words. SRAMA bits 31—03 describes the base address of the Segment Descriptor Table (SDT) for each of the four sections of virtual memory. SRAMB bits 22—10 describes the length (number of entries) in the SDT for each of the four sections of virtual memory. The contents of SRAMA (4 words) and SRAMB (4 words) are part of the error report output by the **/etc/errdump** command. The SRAMA and SRAMB are identified as "srama" and "sramb" in the error report. The format of SRAMA and SRAMB are as follows.

	SECTION RAM A (SRAMA)	
BITS	31 — 03	02 — 00
FIELD	SDT ADDRESS	RESERVED

	SECTION RAM B (SRAMB)		
BITS	31 — 23	22 — 10	09 — 00
FIELD	RESERVED	SDT LENGTH	RESERVED

MMU Registers. The MMU contains five 32-bit registers:

- Fault Code Register (FLTCR)
- Fault Address Register (FLTAR)
- Virtual Address Register (VAR)
- Configuration Register (CR)
- Flush ID Number Register (FIDNR).

These registers are used to store MMU state information. The contents of FLTAR and FLTCR are part of the error report output by the **/etc/errdump** command. The FLTAR and FLTCR are identified as "fltar" and "fltcr" in the error report.

Fault Code Register

The Fault Code Register (FLTCR) is loaded whenever a fault occurs during an MMU operation. The contents are changed to the default state when the CPU writes to it in the peripheral mode. Reading the FLTCR does not change the contents. The output of the **/etc/errdump** command includes the FLTCR. The format of the FLTCR is as follows.

	FAULT CODE REGISTER			
BITS	31 — 11	10 — 07	06 — 05	04 — 00
FIELD	RESERVED	ACCESS REQUESTED	ACCESS XLEVEL	FAULT TYPE

The FLTCR fields are defined in the following paragraphs.

RESERVED Bits 31—11 are reserved for future use. If read, zeros are returned.

ACCESS REQUESTED

Bits 10—07 are used to store the type of access the CPU requested when a fault occurred. The decode of bits 10—07 indicate the following.

BITS 10 — 07	ACCESS TYPE
0000	MOVE TRANSLATED (MT)
0001	SUPPORT PROCESSOR DATA WRITE
0011	SUPPORT PROCESSOR DATA FETCH
0111	INTERLOCKED READ
1000	ADDRESS FETCH
1001	OPERAND FETCH
1010	WRITE
1100	INSTRUCTION FETCH AFTER DISCONTINUITY
1101	INSTRUCTION PREFETCH
1110	INSTRUCTION FETCH

ACCESS XLEVEL

Bits 06 and 05 are used to store the execution level of the requested access when the fault occurred. The decode of bits 06 and 05 indicate the following.

BIT 06	BIT 05	DESCRIPTION
0	0	KERNEL LEVEL
0	1	EXECUTIVE LEVEL
1	0	SUPERVISOR LEVEL
1	1	USER LEVEL

FAULT TYPE

Bits 04—00 are the FAULT TYPE that occurred. The decode of bits 04—00 indicate the following. Unassigned fault type values are not included.

BITS 04—00	FAULT NAME
00000	NO FAULT
00001	MISPROCESSING MEMORY
00010	REFERENCED/MODIFIED UPDATE MEMORY
00011	SEGMENT DESCRIPTOR TABLE LENGTH
00100	PAGE WRITE
00101	PAGE DESCRIPTOR TABLE LENGTH
00110	INVALID SEGMENT DESCRIPTOR
00111	SEGMENT NOT PRESENT
01000	RESERVED
01001	PAGE DESCRIPTOR TABLE NOT PRESENT
01010	PAGE NOT PRESENT
01011	TOO MANY INDIRECTIONS
01101	ACCESS
01110	ACCESS OFFSET
01111	RESERVED

Fault Address Register

The Fault Address Register (FLTAR) contains the virtual address that was being processed when the last fault that caused a write to the FLTCR occurred. The output of the **/etc/errdump** command includes the FLTAR.

Virtual Address Register

The Virtual Address Register (VAR) contains the virtual address to be translated by the MMU. The VAR is overwritten each time a translation is performed. Writing to the VAR causes the corresponding page descriptor and segment descriptor to be flushed. If the segment descriptor is contiguous, then all page descriptors are flushed.

Configuration Register

The Configuration Register (CR) is used to enable or disable certain options of the MMU. Upon reset, all bits are cleared. The format of the CR is as follows.

	CONFIGURATION REGISTER						
BITS	31 — 07	06	05	04 — 03	02	01	00
FIELD	RESERVED	DCE	MCE	PS	CACHEABLE	REFERENCED	MODIFIED

The CR fields are defined in the following paragraphs.

RESERVED Bits 31—07 are reserved for future use. If read, zeros are returned.

DCE Bit 06 is the Data Cache Enable (DCE) bit. This bit must be set to enable data cache. For parts without data cache, this bit must contain a zero.

MCE Bit 05 is the Multiple Context Enable (MCE) bit. When set [1], the multiple context feature is enabled. When cleared[0], the MMU operates is single context mode.

PS Bits 04—03 are the Page Size (PS) bits. These bits determine the page size for the MMU operations as follows:

BIT 04	BIT 03	PAGE SIZE
0	0	2 Kilobytes
0	1	4 Kilobytes
1	0	8 Kilobytes
1	1	RESERVED

CACHEABLE

Bit 02 is the Cacheable bit. The Cacheable ($) bit determines the state of $\overline{\text{CABLE}}$ during misprocessing and updating of the Referenced and Modified bits. (If $=0, then $\overline{\text{CABLE}}$ =1; if $=1, then $\overline{\text{CABLE}}$ =0.)

REFERENCED

Bit 01 is the Referenced (R) bit. The R bit in the segment descriptor is set (R=1) when the segment descriptor is brought into the segment descriptor cache as a result of misprocessing. When R=0, the R bit in the segment descriptor is not updated.

MODIFIED Bit 00 is the Modified (M) bit. If M=1, the segment descriptor M bit is updated on the first write to a segment.

Flush ID Number Register

The Flush ID Number Register (FIDNR) is used in multiple context only. Writing the address of the SDT to the FIDNR causes all page descriptor cache entries associated with the flushed ID to be flushed from the PDC and SDC. The format of the FIDNR is as follows.

	FLUSH ID NUMBER REGISTER	
BITS	31 — 03	02 — 00
FIELD	SDT ADDRESS	RESERVED

Peripheral Mode. In the peripheral mode of MMU operation, the MMU is accessed as a memory-mapped peripheral. In this mode, internal MMU registers and logic elements are read and write accessible by the system board CPU. All peripheral mode accesses are word (32-bit) accesses. When the system board CPU asserts the MMU Chip Select (MMUCS[0]), the MMU is in the peripheral mode. The internal MMU address spectrum is shown in Figure 3-30. In the peripheral mode, physical address bits 31—00 are interpreted as follows by the MMU.

	PERIPHERAL MODE ADDRESS FIELDS			
BITS	31 — 12	11 — 08	07 — 02	01 — 00
FIELD	RESERVED	ENTITY	INDEX	RESERVED

The peripheral mode address fields are defined in the following paragraphs.

RESERVED Bits 31—12, 01, and 00 are ignored by the MMU. These bits are negated (treated as zeros).

ENTITY Bits 11—08 are used to select the internal MMU circuit (entity) to be accessed. The decode of bits 11—08 is as follows.

BITS 11 — 08	SELECTED MMU DEVICE
0000	SEGMENT DESCRIPTOR CACHE BITS 31—00
0001	SEGMENT DESCRIPTOR CACHE BITS 63—32
0010	PAGE DESCRIPTOR CACHE BITS 31—00
0011	PAGE DESCRIPTOR CACHE BITS 63—32
0100	FLUSH DATA CACHE REGISTER
0101	RESERVED
0110	SECTION RAM A
0111	SECTION RAM B
1000	FAULT CODE REGISTER
1001	FAULT ADDRESS REGISTER
1010	CONFIGURATION REGISTER
1011	VIRTUAL ADDRESS REGISTER
1100	ID NUMBER CACHE
1101	CURRENT ID NUMBER REGISTER
1110	FLUSH ID NUMBER REGISTER
1111	VERSION REGISTER

INDEX Bits 07—02 are used to index each addressable entity. Bits 07—02 are ignored when register are accessed. Bits 07—02 are used when segment or page descriptor caches are accessed. Bits 03 and 02 are used for section RAM accesses.

MEMORY MANAGEMENT UNIT INTERNAL ADDRESS SPECTRUM	
ADDRESS	**DESCRIPTION**
0x 000 ⋮ 0x 07C	SEGMENT DESCRIPTOR CACHE BITS 31—00
0x 100 ⋮ 0x 17C	SEGMENT DESCRIPTOR CACHE BITS 63—32
0x 200 ⋮ 0x 27C	PAGE DESCRIPTOR CACHE BITS 31—00
0x300 ⋮ 0x 37C	PAGE DESCRIPTOR CACHE BITS 63—32
0x 400	FLUSH DATA CACHE REGISTER
0x 500	RESERVED
0x 600 ⋮ 0x 60C	SECTION RAM A
0x 700 ⋮ 0x 70C	SECTION RAM B
0x 800	FAULT CODE REGISTER
0x 900	FAULT ADDRESS REGISTER
0x A00	CONFIGURATION REGISTER
0x B00	VIRTUAL ADDRESS REGISTER
0x C00 ⋮ 0xCFC	ID NUMBER CACHE
0x D00 ⋮ 0x D0C	CURRENT ID NUMBER REGISTER
0x E00	FLUSH ID NUMBER REGISTER
0x F00	VERSION REGISTER

Figure 3-30: MMU Internal Address Spectrum

Virtual to Physical Address Translation for Paged Segments. Figure 3-31 shows the translation of a virtual address to a physical address for a paged segment of physical memory. The Section Identification (SID) field is used to find the base address of the required Segment Descriptor Table (SDT). The base address of the SDT for each section is stored in the MMU. This base address and the Segment Select (SSL) field are combined to index a Segment Descriptor (SD) within the SDT. The SD is used as the base address of a Page Descriptor Table (PDT). This PDT address is combined with the Page Select (PSL) field to index a Page Descriptor (PD). The PD contains the starting address of the paged segment that is concatenated with the Page Offset (POT) field to form the required physical address.

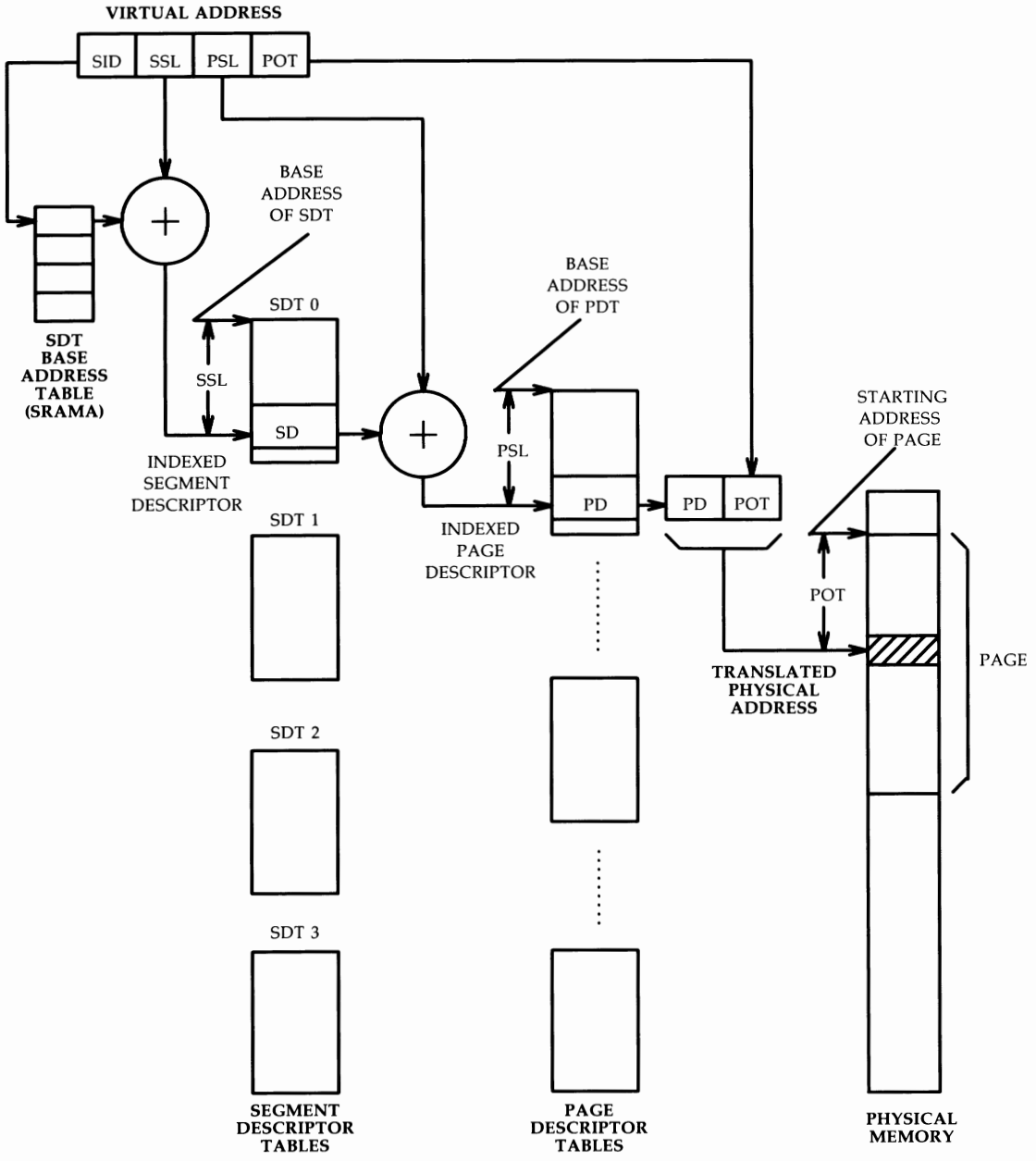


Figure 3-31: Virtual Address to Physical Address Translation for Paged Segments

Math Acceleration Unit

The WE 32106 Math Acceleration Unit (MAU) is used on the CM518A System Board.

Note: The WE 32100 chipset is covered in the "CM190A/ED-4C637-30 System Board" section for Version 2 system boards. Refer to that section for detailed information on the CPU/MMU/MAU chips of the CM518A System Board.

The CM518B/C System Boards use the WE 32206 MAU. The MAU is used in a coprocessor mode to provide hardware floating point capability for the WE 32200 Microprocessor. The MAU peripheral mode is **not** used in this application; the MAU chip select is held to a logic 1 through a pull up resistor to VCC. The MAU provides single (32-bit), double (64-bit), and double-extended (80-bit) precision. The single precision format provides an 8-bit exponent and an exponent bias allowing the reciprocal of all normalized numbers to be represented without overflow. Double precision provides an exponent range sufficient for the product of eight 32-bit terms without overflow. Double-extended precision provides a format with a range and precision that is greater than double precision. Double-extended precision numbers lessen the chance of a result being contaminated by excessive roundoff error.

The MAU supports add, subtract, multiply, divide, remainder, square root, and compare operations. The operand, result, status, and command information transfers take place over a 32-bit, bidirectional data bus with the WE 32200 Microprocessor. Figure 3-32 is a functional block diagram of the WE 32206 MAU. The WE 32206 is a 125-pin ceramic pin-array package using CMOS technology and operating at 24 MHz.

MAU Registers. The MAU contains four register types:

- Auxiliary Status Register
- Operand Registers
- Command Register
- Data Register.

These registers provide status, command, and control for the MAU.

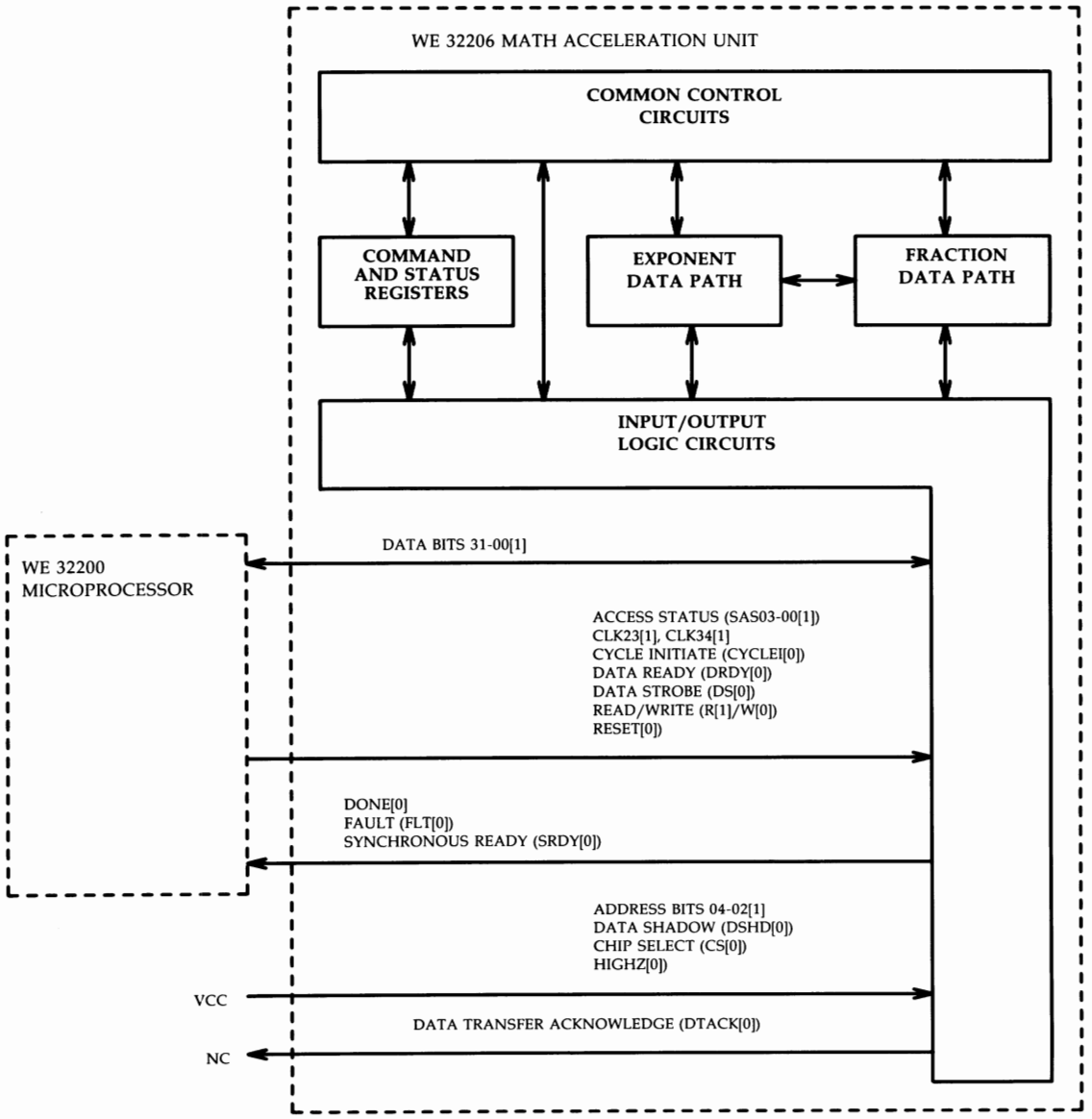


Figure 3-32: WE 32206 Math Acceleration Unit — Functional Block Diagram

Auxiliary Status Register

The Auxiliary Status Register (ASR) is used to do the following:

- Control the remainder operation (partial remainder bit)
- Signal the state of an operation (result available bit)
- Disable and record exceptions (mask and sticky bits)
- Control rounding of results (round control bits)
- Record condition codes (negative and zero bits).

The negative, zero, inexact, and integer overflow bits in the ASR match the condition codes in the PSW register of the CPU. This allows the bits to be copied into the PSW as part of the coprocessor status access and to be easily tested by the CPU. The format of the ASR is as follows.

	AUXILIARY STATUS REGISTER (31—16)										
BITS	31	30 — 26	25	24	23 — 22	21	20	19	18	17	16
FIELD	RA	UNUSED	ECP	NTNC	RC	N	Z	IO	PS	CSC	UO

	AUXILIARY STATUS REGISTER (15—00)													
BITS	15	14	13	12	11	10	09	08	07	06	05	04	03—01	00
FIELD	WF	IM	OM	UM	QM	PM	IS	OS	US	QS	PR	UW	VER	FE

The ASR fields are defined in the following paragraphs.

UNUSED Bits 30—26 are not used. These bits are returned as zeros when read.

RA Bit 31 is the Result Available (RA) bit. It is cleared at the beginning of an operation and set [1] when the operation result is available. During the quiescent state, the RA bit is set.

ECP Bit 25 is the Exception Condition Present (ECP) bit. It is set [1] if any one of the floating point exception conditions except "inexact" is present. The ECP bit is cleared [0].

NTNC Bit 24 is the Nontrapping Not a Number (NAN) Control (NTNC) bit. Bit 24 is tested when an invalid operation exception occurs and bit 14 (IM) is cleared. If bit 24 is set, an exception occurs and bit 09 (IS) is set.

RC Bits 23 and 22 are the Round Control (RC) mode bits. The decode of these bits is as follows.

BIT 23	BIT 22	DESCRIPTION
0	0	ROUND TO NEAREST
0	1	ROUND TOWARDS PLUS INFINITY
1	0	ROUND TOWARDS MINUS INFINITY
1	1	ROUND TOWARDS ZERO (TRUNCATION)

N Bit 21 is the Negative (N) condition bit. Bit 21 is set [1] when result of the last operation is negative. Bit 21 is cleared when the result of the last operation is positive.

Z Bit 20 is the Zero (Z) condition bit. Bit 20 is set [1] when the result of the last operation is zero. Bit 20 is cleared when the result of the last operation is nonzero.

IO Bit 19 is the Integer Overflow (IO) bit. Bit 19 is set [1] when a convert float to integer operation causes an overflow.

PS Bit 18 is the Inexact Sticky (PS) bit. Bit 18 is set [1] when the result of an operation cannot be specified in the destination format. Bit 18 is cleared on reset.

CSC Bit 17 is the Context Switch Control (CSC) bit. Bit 17 is set [1] on every MAU instruction execution. Bit 17 is cleared on reset.

UO Bit 16 is the Unordered (UO) bit. Bit 16 is set [1] when a compare operation results in an unordered indication; otherwise this bit is cleared. Bit 16 is cleared on reset.

WF Bit 15 is the Write Fault (WF) indicator bit. If enabled (bit 0), this bit is set [1] when a fault condition occurs during the writing of any result to memory. When this bit is set, the MAU will not reexecute the operation upon a restart from the CPU. Instead, it returns a DONE signal and stores the result of the previously faulted operation in memory.

IM Bit 14 is the Invalid Operation Mask (IM) bit. Bit 14 is set [1] by the user to enable the generation of an exception when bit 09 (Invalid Operation Sticky bit) is set. There are no invalid operation exceptions when bit 14 is cleared.

OM Bit 13 is the Overflow Mask (OM) bit. Bit 13 is set [1] by the user to enable the generation of an exception when bit 08 (Overflow Sticky bit) is set. There are no overflow exceptions when bit 13 is cleared.

UM Bit 12 is the Underflow Mask (UM) bit. Bit 12 is set [1] by the user to enable the generation of an exception when bit 07 (Underflow Sticky bit) is set. There are no underflow exceptions when bit 12 is cleared.

QM Bit 11 is the Divide by Zero Mask (QM) bit. Bit 11 is set [1] by the user to enable the generation of an exception when bit 06 (Divide by Zero Sticky bit) is set. There are no divide by zero exceptions when bit 11 is cleared.

PM Bit 10 is the Inexact Mask (PM) bit. Bit 10 is set [1] by the user to enable the generation of an exception when bit 18 (Inexact Sticky bit) is set [1]. There are no inexact exceptions when bit 10 is cleared.

IS Bit 09 is the Invalid Operation Sticky (IS) bit. Bit 09 is set [1] when a result cannot be legally stored in a destination, or when illegal operands are given to some operation.

OS Bit 08 is the Overflow Sticky (OS) bit. Bit 08 is set [1] when an exponent of a rounded result of an arithmetic operation is too large for the exponent field of the destination format.

US Bit 07 is the Underflow Sticky (US) bit. Bit 07 is set [1] when an exponent of a rounded result of an arithmetic operation is too small to be represented in the exponent field of the destination format.

QS Bit 06 is the Divide by Zero Sticky (QS) bit. Bit 06 is set [1] when the divisor is normalized zero and the dividend is a finite nonzero number.

PR Bit 05 is the Partial Remainder (PR) bit. Bit 05 is set [1] when the result of a remainder operation is a partial remainder. Bit 05 is cleared when the result of a remainder operation is a full remainder. This bit is cleared on reset.

UW Bit 04 is the Unaligned Word (UW) bit. If enabled (bit 0), this bit is set [1] when a fault condition occurs due to an unaligned word being received.

VER Bits 03—01 are used to determine which MAU is being used: 001 indicates a WE 32206 MAU, 000 indicates a WE 32106 MAU.

FE Bit 00 is the Feature Enable (FE) bit. When set [1], the Write Fault (WF) and Unaligned Word (UW) features of the MAU are enabled.

Operand Registers

The MAU contains eight operand registers (F7—F0). Each operand register is 80 bits and contains one operand in an extended format. These registers are accessed via the Data Register in the format of three 32-bit words. In the peripheral mode, bits 95—80 are ignored during write operations. For read operations, bits 95—80 are returned as zeros. The operand registers are unchanged on reset. The contents of these registers are indeterminate on powerup. The format of each of the eight operand registers is as follows.

	OPERAND REGISTERS (F3— F0)				
BITS	95 — 80	79	78 — 64	63	62 — 00
FIELD	UNUSED	SIGN	EXPONENT	J	FRACTION

The operand register fields are defined in the following paragraphs.

UNUSED Bits 95—80 are not used. These bits are returned as zeros for a read operation.

SIGN Bit 79 is the SIGN bit. When set [1] the sign is negative; cleared represents a positive value.

EXPONENT Bits 78—64 are used as the EXPONENT field. The exponent is biased by 16,383.

J Bit 63 is the Explicit (J) bit. The J bit is to the left of the binary point in the 2^0 position. In combination, the J bit and the FRACTION field can represent values in the range 0 to $2-(2^{-63})$.

FRACTION Bits 62—00 are used to represent the fractional part of a number.

Command Register

The Command Register (CR) stores command words used to initiate MAU operations. The format of this 32-bit register is as follows.

	COMMAND REGISTER										
BITS	31—24	23—21	20	19	18	17	16—15	14—10	09—07	06—04	03—00
FIELD	ID	UNUSED	RB1	RB2	RB3	RCS	RC	OPCODE	OP1	OP2	OP3

The CR fields are defined in the following paragraphs.

ID Bits 31—24 are the Processor Identification Number of the processor that should react to the command word. The MAU is ID 0.

UNUSED Bits 23—21 are not used. These bits are returned as zeros for a read operation.

RB(1-3) Bits 20—18 are the Register Bank (RB1—RB3) bits. A "0" specifies registers F0 through F3 and a "1" specifies registers F4 through F7.

RCS Bit 17 is the Round Control Selection (RCS) bit. When clear [0], round control is determined by the RC bits in the Auxiliary Status Register. When set [1], round control is determined by the RC bits in the Control Register.

RC Bits 16 and 15 make up the Round Control (RC) bits. They determine the method of rounding as follows.

BIT 16	BIT 15	DESCRIPTION
0	0	ROUND TO NEAREST
0	1	ROUND TOWARDS PLUS INFINITY
1	0	ROUND TOWARDS MINUS INFINITY
1	1	ROUND TOWARDS ZERO (TRUNCATION)

OPCODE Bits 14—10 are the Operation Code (OPCODE) field. The OPCODE field specifies the operation to be done. The OPCODES are as follows.

OPCODE	MNEMONIC	INSTRUCTION
0x 02	ADD	ADD
0x 03	SUB	SUBTRACT
0x 04	DIV	DIVIDE
0x 05	REM	REMAINDER
0x 06	MUL	MULTIPLY
0x 07	MOVE	MOVE
0x 08	RDASR	MOVE FROM ASR
0x 09	WRASR	MOVE TO ASR
0x 0A	CMP	COMPARE
0x 0B	CMPE	COMPARE WITH EXCEPTIONS
0x 0C	ABS	ABSOLUTE VALUE
0x 0D	SQRT	SQUARE ROOT
0x 0E	RTOI	ROUND TO INTEGRAL VALUE
0x 0F	FTOI	CONVERT FLOATING POINT TO INTEGER
0x 10	ITOF	CONVERT INTEGER TO FLOATING POINT
0x 11	DTOF	CONVERT DECIMAL TO FLOATING POINT
0x 12	FTOD	CONVERT FLOATING POINT TO DECIMAL
0x 13	NOP	NO OPERATION
0x 14	EROF	EXTRACT RESULT ON FAULT
0x 17	NEG	NEGATE
0x 18	LDR	LOAD DATA REGISTER
0x 1A	CMPS	COMPARE WITH FLAGS SWAPPED
0x 1B	CMPS	COMPARE WITH EXCEPTIONS AND FLAGS SWAPPED

OP1 Bits 09—07 is the Operand Specifier 1 (OP1) field. OP1 specifies whether the first source operand is a MAU register, a memory-based operand of a given size, or nonexistent (no operand). The value of this field is as follows.

BITS 09 — 07	OPERAND LOCATION
000	REGISTER F0 OR F4 (DEPENDING ON RB1)
001	REGISTER F1 OR F5 (DEPENDING ON RB1)
010	REGISTER F2 OR F6 (DEPENDING ON RB1)
011	REGISTER F3 OR F7 (DEPENDING ON RB1)
100	MEMORY-BASED SINGLE WORD
101	MEMORY-BASED DOUBLE WORD
110	MEMORY-BASED TRIPLE WORD
111	NO OPERAND

OP2

Bits 06—04 is the Operand Specifier 2 (OP2) field. OP2 specifies whether the second source operand is a MAU register, a memory-based operand of a given size, or nonexistent (no operand). The value of this field is as follows.

BITS 06 — 04	OPERAND LOCATION
000	REGISTER F0 OR F4 (DEPENDING ON RB2)
001	REGISTER F1 OR F5 (DEPENDING ON RB2)
010	REGISTER F2 OR F6 (DEPENDING ON RB2)
011	REGISTER F3 OR F7 (DEPENDING ON RB2)
100	MEMORY-BASED SINGLE WORD
101	MEMORY-BASED DOUBLE WORD
110	MEMORY-BASED TRIPLE WORD
111	NO OPERAND

OP3

Bits 03—00 are the Operand Specifier 3 (OP3) field. OP3 specifies whether the destination operand is a MAU register, a memory-based operand of a given size, or nonexistent (no operand). Even though the register destinations are specified as single, double, or double-extended, the result is stored in the registers in double-extended precision. The precision designations are used for rounding and checking for underflow and overflow. The value of this field is as follows.

BITS 03 — 00	OPERAND REGISTER	DESTINATION PRECISION
0000	F0 OR F4	SINGLE
0001	F1 OR F5	SINGLE
0010	F2 OR F6	SINGLE
0011	F3 OR F7	SINGLE
0100	F0 OR F4	DOUBLE
0101	F1 OR F5	DOUBLE
0110	F2 OR F6	DOUBLE
0111	F3 OR F7	DOUBLE
1000	F0 OR F4	DOUBLE-EXTENDED
1001	F1 OR F5	DOUBLE-EXTENDED
1010	F2 OR F6	DOUBLE-EXTENDED
1011	F3 OR F7	DOUBLE-EXTENDED
1100	—	MEMORY-BASED SINGLE WORD
1101	—	MEMORY-BASED DOUBLE WORD
1110	—	MEMORY-BASED TRIPLE WORD
1111	—	NO OPERAND

Data Register

The system board CPU (WE 32200) uses the MAU as a coprocessor; the peripheral mode of the MAU is NOT used in this application. The Data Register (DR) is used to read and write operands (registers F3-F0) in the peripheral mode. The DR is an 96-bit register. The DR is addressed in the peripheral mode as three 32-bit registers. When exceptions occur in either the coprocessor or peripheral modes, the DR stores the data supplied by the trap handler. This exception data is read when an Extract Result on Fault (EROF) instruction (opcode) is executed. The format of the exception data stored in the DR by the Trap Handler is as follows.

INVALID OPERATION

If either of the source operands is a trapping Not a Number (NAN), then DR stores the NAN converted to double-extended precision (80 bits) if necessary. If both source operands are trapping NANs or infinities of different signs, then the second operand (OP2) is stored in the DR in double precision (80 bits).

OVERFLOW or UNDERFLOW

The significant (fraction) along with the 17-bit internal result exponent and the result sign are stored in the DR. The most significant bit of the 17-bit exponent is like a sign bit in 2's complement notation. An addition bit (bit 79) in the exponent ensures that no significant exponent bits are lost from an internal representation when an overflow or underflow conditions occurs. The exponent is biased by 16,383. The least significant bit (L), the guard (G) bit, round bit (R), and sticky bit (S) of the unrounded result are stored in the DR. The format of the data in the DR for an overflow or underflow exception is as follows.

BITS	95	94	93	92	91—82	81	80—64	63	62—00
FIELD	L	G	R	S	UNUSED	SIGN	EXPONENT	J	FRACTION

DIVIDE BY ZERO

The dividend (OP2) converted to double-extended precision, if necessary, is stored in the DR for a divide by zero exception. The L, G, R, and S bits are also stored.

INEXACT

The rounded result converted to double-extended precision, if necessary, is stored in the DR for and inexact exception. The L, G, R, and S bits are also stored.

MAU Coprocessor Mode. In the Coprocessor Mode, the system board CPU initiates a MAU transaction by doing a coprocessor broadcast access. This sends a 32-bit word to the MAU Command Register. The MAU checks the Identification (ID) field of the Command Register against the MAU ID (0). If an ID matches the stored ID, the 32-bit word is stored in the Command Register.

If any Operand Specifier in the command word indicates that an operand is to be obtained from main memory, the MAU waits until the proper number of coprocessor data fetch bus transactions occur.

The MAU does the operation specified and generates a result, condition codes, and possibly an exception. The MAU asserts a DONE signal and waits for the coprocessor (system board CPU) status fetch. If an exception is present, the MAU faults the access and goes to an idle state. If there is no exception, a word containing the current Auxiliary Status Register (ASR) is returned in response to the status fetch.

If the results are to be written to main memory, the MAU waits until the proper number of coprocessor data write bus transactions occur to transfer the results and then goes to an idle state.

Address Decoder

The address decoder translates physical CPU/MMU addresses into chip selects (enables) for the various memory and peripheral circuits on the system board and feature cards. The address decoder is built from Programmable Logic Arrays (PLAs) and four 3/8 decoders. The chip select signals are also used to generate Wait Select (WSEL) signals appropriate for the access time of each synchronous device. For devices on the system board, a fixed number of wait states are generated by the address decoder.

The chip selects and controls decoded from physical address bits 26—12, Physical Address Strobe (PAS[0]), Interrupt Acknowledge (IACK[0]) are summarized in Figure 3-33.

PAS[0]	IACK[0]	PHYSICAL ADDRESS BITS				SELECTED DEVICE
		27—24	23—20	19—16	15—12	
x	x	xxxx	xxxx	xxxx	0000	MEMORY MANAGEMENT UNIT (MMUCS[0])
x	x	xxxx	xxxx	xxxx	0001	TIME-OF-DAY COUNTER (TODCS[0])
x	x	xxxx	xxxx	xxxx	0010	TIMERS (TIMRCS[0])
x	x	xxxx	xxxx	xxxx	0011	NONVOLATILE RANDOM ACCESS MEMORY (NVRCS[0])
x	x	xxxx	xxxx	xxxx	0100	CONTROL AND STATUS REGISTER (CSRCS[0])
x	x	xxxx	xxxx	xxxx	0101	PAGE REGISTER 1 (PR1CS[0])
x	x	xxxx	xxxx	xxxx	0110	PAGE REGISTER 2 (PR2CS[0])
x	x	xxxx	xxxx	xxxx	0111	PAGE REGISTER 3 (PR3CS[0])
x	x	xxxx	xxxx	xxxx	1000	DIRECT MEMORY ACCESS CONTROLLER (DMACS[0])
x	x	xxxx	xxxx	xxxx	1001	DUART (UARTCS[0])
x	x	xxxx	xxxx	xxxx	1010	HARD DISK CONTROLLER (DSKCS[0])
x	x	xxxx	xxxx	xxxx	1011	NOT USED
x	x	xxxx	xxxx	xxxx	1100	MEMORY SIZE REGISTER (MSIZECS[0])
x	x	xxxx	xxxx	xxxx	1101	FLOPPY DISK CONTROLLER (FCS[0])
x	x	xxxx	xxxx	xxxx	1110	PAGE REGISTER 4 (PR4CS[0])
x	x	xxxx	xxxx	xxxx	1111	NOT USED
x	x	xxx0	000x	xxxx	xxxx	NOT USED
x	x	xxx0	001x	xxxx	xxxx	PERIPHERAL CARD 01 (PCS01[0])
x	x	xxx0	010x	xxxx	xxxx	PERIPHERAL CARD 02 (PCS02[0])
x	x	xxx0	011x	xxxx	xxxx	PERIPHERAL CARD 03 (PCS03[0])
x	x	xxx0	100x	xxxx	xxxx	PERIPHERAL CARD 04 (PCS04[0])
x	x	xxx0	101x	xxxx	xxxx	PERIPHERAL CARD 05 (PCS05[0])
x	x	xxx0	110x	xxxx	xxxx	PERIPHERAL CARD 06 (PCS06[0])
x	x	xxx0	111x	xxxx	xxxx	PERIPHERAL CARD 07 (PCS07[0])
x	x	xxx1	000x	xxxx	xxxx	PERIPHERAL CARD 08 (PCS08[0])
x	x	xxx1	001x	xxxx	xxxx	PERIPHERAL CARD 09 (PCS09[0])
x	x	xxx1	010x	xxxx	xxxx	PERIPHERAL CARD 10 (PCS10[0])
x	x	xxx1	011x	xxxx	xxxx	PERIPHERAL CARD 11 (PCS11[0])
x	x	xxx1	100x	xxxx	xxxx	PERIPHERAL CARD 12 (PCS12[0])
x	x	xxx1	101x	xxxx	xxxx	PERIPHERAL CARD 13 (PCS13[0])
x	x	xxx1	110x	xxxx	xxxx	PERIPHERAL CARD 14 (PCS14[0])
x	x	xxx1	111x	xxxx	xxxx	PERIPHERAL CARD 15 (PCS15[0])
0	1	x000	0000	000x	xxxx	READ ONLY MEMORY (ROMCS[0])
0	1	x00x	xx1x	xxxx	xxxx	INPUT/OUTPUT REQUIRED (IOREQ[0])
0	1	x00x	x1xx	xxxx	xxxx	¦
0	1	x00x	1xxx	xxxx	xxxx	¦
0	1	x001	xxxx	xxxx	xxxx	¦
0	1	x000	0000	010x	1xxx	DIRECT MEMORY ACCESS SUBSYSTEM (DMASS[0])
0	1	x000	0000	010x	0xxx	MISCELLANEOUS (MISCS[0])

LEGEND:

x Don't care bit

Figure 3-33: Chip Select and Control Signals Address Decode

Input/Output Chip Selects. The Address Decoder enables 1 out of 15 Peripheral Chip Select (PCS) signals (PCS15—01[0]) from latched address bits 24 through 21 (LPA24[1] through LPA21[1]). For the 3B2/400 computer, only 12 peripheral chip selects (PCS12—01) are used. For the 3B2/300/310 computer, only 4 peripheral chip selects (PCS04—01) are used. The PCS15 through PCS13 signals are reserved for future enhancements. PCS00[0] is decoded but has no connection.

A composite input/output chip select signal (CREQ[0]) is sent to the DRAM Controller and Arbiter Circuits to request the "Bypass Mode" to access the input/output connectors (feature card slots). The Bypass Sequencer returns a Bypass Mode Acknowledge (LCPUIO[0]) signal to enable the individual input/output card chip selects to be passed to the input/output connectors. All inputs to the address decoder from off-board and DMA Subsystem devices are latched under the control of the arbiter (LCPUIO signal).

Other Chip Selects. Other chip selects are used to enable various devices on and off the system board. The on-board devices chip selects decoded from physical address bits 15 through 12 are listed below:

- Memory Management Unit Chip Select (MMUCS[0])
- Time-of-Day Chip Select (TODCS[0])
- Timer Chip Select (TIMRCS[0])
- Nonvolatile RAM Chip Select (NVRCS[0])
- Control and Status Register Chip Select (CSRCS[0])
- Page Register 1 Chip Select (PR1CS[0])
- Page Register 2 Chip Select (PR2CS[0])
- Page Register 3 Chip Select (PR3CS[0])
- Page Register 4 Chip Select (PR4CS[0])
- Direct Memory Access Chip Select (DMACS[0])
- DUART Chip Select (UARTCS[0])
- Hard Disk Controller Chip Select (DSKCS[0])
- Memory Size Chip Select (MSIZECS[0])
- Floppy Disk Controller Chip Select (FCS[0]).

Physical address bits 26—17 and 15, Physical Address Strobe (PAS[0]), and Interrupt Acknowledge (IACK[0]) are combined to generate the following chip select and control signals:

- Read Only Memory Chip Select (ROMCS[0])
- Direct Memory Access Subsystem (DMASS[0])
- Miscellaneous Chip Select (MISCS[0])
- Input/Output Required (IOREQ[0]).

Read Only Memory

The Erasable Programmable Read Only Memory (EPROM) is configured to yield 128K bytes of ROM. For the CM518A/B System Boards, the ROM is formed using four 32K by 8 EPROM integrated circuits (27256's). For the CM518C System Board, the ROM is formed using two 64K by 8 EPROM integrated circuits (27512's). The starting address of ROM is 0x 00000000.

Timers

The timers include the following:

- Time of day (MM58274)
- Interval (INTEL 82C54)
- Sanity (INTEL 82C54)
- Bus (INTEL 82C54).

The interval, sanity, and bus timers are implemented in an INTEL 82C54 timer chip.

Clock/Calendar Timer. The Clock/Calendar Timer (MM58374) calculates current date to tenths of a second. The timer is controlled by a 32.768-kHz oscillator. The timer features automatic leap year calculation, protection for read access when changing data, and low standby current (2.2 volt, 10 microamperes). The accuracy is determined by the 32.768-kHz crystal with a 0.003 percent tolerance ($\pm$1.3 minutes per month).

Periodic Timer. The Interval Timer (Timer 1) has a 100 kHz (CLKTA[1]). The Inhibit UNIX Interval Timer (INHUIT) CSER bit (bit 7) inhibits operation of this timer. When the timer expires, the UNIX Interval Timer Time-out (UITT) bit (bit 0) of the CSER is set and a level 15 interrupt is sent to the Interrupt Decoder.

Sanity Timer. The Sanity Timer (Timer 0) is a count down timer that is normally reset by software before it reaches zero. The time base is 10 kHz (CLKTB[1]). The Inhibit System Sanity Timer (INHSST) CSER bit (bit 8) inhibits operation of this timer. When the Sanity Timer reaches zero, an error signal turns on the **Diagnostic** indicator, a level 15 interrupt is sent to the Interrupt Decoder, and the Sanity Timer Time-out (SANTO) bit (bit 29) is set in the CESR. The CSER bit 29 is cleared by writing to address 0x 00044000. This count down timer is started when the power switch is pressed to OFF. System software must read the 82C54 package to determine whether Sanity Timer (Timer 0) or the Bus Timer (Timer 2) timed out.

Bus Timer. The Bus Timer (Timer 2) is as the Unbuffered Bus (UBus) access timer. The time base is 500 kHz (CLK02[1]). The Inhibit UBus Timer (INHUBT) CSER bit (bit 10) inhibits operation of this timer. The UBus timer starts counting when the virtual address strobe is asserted. The UBus timer is reset when the virtual address strobe is negated. If the timer is not reset within the programmed period (1 millisecond), an error signal turns on the **Diagnostic** indicator, a level 15 interrupt is sent to the Interrupt Decoder, and the UBus Timer Time-out bit (bit 26) is set in the CSER. The CSER bit 26 is cleared by writing to address 0x 00044000. System software must read the 82C54 package to determine whether Sanity Timer (Timer 0) or the Bus Timer (Timer 2) timed out.

Control, Status, and Error Register

The Control, Status, and Error Register (CSER) is a 32-bit register. It provides low-level access to the system board logic circuits. The CSER controls and monitors various system functions. All bits are clearable or setable under software control. All CSER bits are writable by software using a full word write to the address of that bit, half-word write to the given address plus 2, or a byte write to the address plus 3.

The CSER bit assignments and access information are shown in Figure 3-34. The 32 bits are divided into four groups of 8 bits. A read operation at the address of any bit in a group places the whole group on data bits 07—00 so that it remains constant throughout the read cycle. The CSER is NOT cleared by a hardware reset. The state of the CSER after a write operation is dependent only on the address; the data written is a "don't care" bit. The contents of the CSER are part of the error report output by the **/etc/errdump** command. The CSER is identified as "cser" in the error report.

VERSION 3—CONTROL, STATUS, AND ERROR REGISTER BIT ASSIGNMENTS								
BIT	DESCRIPTION	WRITE ADDRESS	ACTIVE	PROPERTIES				
0	UNIX INTERVAL TIMER TIMEOUT	0x 00044000	SET	HS		PC		
1	POWER DOWN REQUEST	0x 00044004	SET	HS	PS	PC		
2	OPER. INTERRUPT LEVEL 15	0x 00044008	SET	HS	PS	PC		
3	DUART INTERRUPT	0x 0004400C	SET	HS		PC		
4	DUART DMA COMPLETE INTERRUPT	0x 00044010	SET	HS		PC		
5	PIR LEVEL 9	0x 00044014	SET		PS	PC		
6	PIR LEVEL 8	0x 00044018	SET		PS	PC		
7	INHIBIT UNIX INTERVAL TIMER	0x 0004401C	SET		PS	PC	SR	
8	INHIBIT SYSTEM SANITY TIMER	0x 00044020	SET		PS	PC	SR	
9	INHIBIT UBUS TIMER	0x 00044024	SET		PS	PC	SR	
10	INHIBIT FAULTS TO CPU	0x 00044028	SET		PS	PC	SR	
11	INHIBIT SINGLE BIT ERROR RPT.	0x 0004402C	SET		PS	PC		
12	INHIBIT INTEGRAL 3B2 I/O BUS	0x 00044030	SET		PS	PC		
13	INHIBIT 4 BUB SLOTS	0x 00044034	SET		PS	PC		
14	FORCE ECC SYNDROME	0x 00044038	CLEAR		PS	PC		
15	THERMAL SHUTDOWN REQUEST	0x 0004403C	SET	HS		PC		CR
16	FAILURE LED ON	0x 00044040	SET	HS	PS	PC		
17	POWER DOWN—POWER SUPPLY	0x 00044044	CLEAR		PS	PC	SR	
18	FLOPPY SPEED FAST	0x 00044048	SET		PS	PC		
19	FLOPPY SIDE 1	0x 0004404C	CLEAR		PS	PC		
20	FLOPPY MOTOR ON	0x 00044050	CLEAR		PS	PC	SR	
21	FLOPPY DENSITY	0x 00044054	SET		PS	PC		
22	FLOPPY SIZE	0x 00044058	SET		PS	PC		
23	SINGLE BIT ERROR	0x 0004405C	SET	HS		PC		
24	MULTIPLE BIT ERROR	0x 00044060	SET	HS		PC		
25	UBUS/BUB RECEIVED FAIL	0x 00044064	SET	HS		PC		
26	UBUS TIMER TIMEOUT	0x 00044068	SET	HS		PC		
27	FAULT REGISTERS FROZEN	0x 0004406C	SET	HS		PC		
28	DATA ALIGNMENT ERROR	0x 00044070	SET	HS		PC		
29	SANITY TIMER TIMEOUT	0x 00044074	SET	HS		PC		
30	ABORT SWITCH ACTIVATED	0x 00044078	SET	HS		PC		
31	SYSTEM RESET REQUEST	0x 0004407C	SET		PS			CR

LEGEND:

CR	Cleared by "system reset" signal
DMA	Direct Memory Access
HS	Set by hardware
PC	Cleared by programmed control
PIR	Programmed Interrupt Request
PS	Set by programmed control
SR	Set by "system reset" signal

Figure 3-34: Version 3 System Board CSER Bit Assignments

Interrupts

Interrupt Mechanism. When an external device requests an interrupt (request for service to the microprocessor), the microprocessor temporarily stops its current execution and begins executing code that services the interrupt. This code is called an interrupt handler. On completion of the interrupt handler code, execution resumes at the point where the interrupt occurred. An interrupt mechanism performs the process execution switch.

There are three functions of the interrupt mechanism, as follows.

1. The interrupt mechanism determines whether or not there will be an interrupt generated in response to an interrupt request. An interrupt is generated if the priority level requested is greater than the priority level in the Interrupt Priority Level (IPL) field of the Processor Status Word (PSW) register of the CPU. If the IPL field equals 0x F, no interrupts are acknowledged except for a nonmaskable interrupt.
2. The interrupt mechanism determines how an interrupt request will be acknowledged and the interrupt identification value. Interrupts are acknowledged as full or quick interrupts. A full interrupt starts an interrupt-handler process by means of a full context/process switch. A quick interrupt causes the interrupt handler to store the current Program Counter (PC) register and PSW register values on the execution stack and set the IPL field of the PSW to 0x F (like a subroutine call). Only a nonmaskable interrupt can interrupt the quick-interrupt handler. A nonmaskable interrupt causes the interrupt handler to store the current PC and PSW values on the execution stack just like a quick interrupt. An interrupted interrupt handler's execution is resumed as a function of popping saved states off the execution stack.
3. The interrupt mechanism saves the interrupted process context and brings in a new process context (process switching). Interrupt-vector tables are provided for full and quick interrupts. The interrupt-vector tables point to the memory locations (addresses) where interrupt PCBPs and PC/PSW pairs are stored.

Interrupt Logic. Eight hardware interrupts are provided. Three of these levels (PINT2—0[0]) are connected to the Input/Output Expansion connector for use by the feature cards that supply their own interrupt vectors. Two interrupt levels are used as Programmed Interrupt Requests (PIRs) and are accessible via the Control, Status, and Error Register (CSER). The three remaining interrupt levels are used by the system board for peripheral devices.

To acknowledge three off-board requests, the interrupt hardware requests the DRAM controller to enter the "bypass" mode. When the controller responds with a "bypass mode" acknowledge, the interrupt acknowledge cycle proceeds and the vector is read from the interrupting off-board device.

Interrupt levels are encoded by an 8/3 encoder and applied to the CPU interrupt request inputs as level 15 through 8 interrupts. When interrupts are acknowledged, the CPU uses the address bus bits 05 through 02 to identify the acknowledged level. In the virtual mode (VAD[0]=0), a latched version of address bits 05 through 02 are used by the interrupt circuitry. When bit 2 is low and either bit 3 or bit 4 is high, an off-board interrupt is assumed and an arbiter request is made. When the bus arbiter permits access, the proper off-board interrupt acknowledge signal is sent. Other combinations of address bits 05 through 02 are assumed to be onboard interrupts and a vector is supplied by looping the latched address bits 05 through 02 back to the data bus via a buffer. A unique vector is provided for each onboard interrupt source that is equal to the interrupt level. When an onboard interrupt is decoded, the interrupt circuit sends a wait select (WSEL1[0]).

Interrupt Assignments. Figure 3-35 defines the interrupt levels for the various interrupt sources. When a 3B2 Enhanced Input/Output (EIO) bus peripheral and a Buffered Microbus (BUB) peripheral interrupt the CPU at the same time and same level, the system board will pass the CPU interrupt acknowledge to the I/O peripheral. The 3B2 EIO bus has priority over the BUB for equal interrupts.

VERSION 3 SYSTEM BOARD INTERRUPT ASSIGNMENTS		
LEVEL	**VECTOR**	**SOURCE**
NMI	00	ABORT SWITCH ACTIVATION (NOTE 1)
NMI	00	SANITY TIMER EXPIRATION (NOTE 1)
NMI	00	THERMAL SHUTDOWN (NOTE 1)
15	15	UNIX INTERVAL TIMER TIMEOUT
15	15	POWER DOWN REQUEST
15	15	UBUS OR BUB OPERATIONAL INTERRUPT
15	15	SINGLE BIT MEMORY ERROR
15	15	MULTIPLE BIT MEMORY ERROR
15	15	UBUS, BUB, EIO BUS RECEIVED FAIL
15	15	UBUS TIMER TIMEOUT
14	(NOTE 2)	BUB (REAL TIME INTERRUPT)
13	13	DUART AND DUART DMA COMPLETE
12	(NOTE 2)	BUB (BLOCK)
11	11	FLOPPY AND FLOPPY DMA COMPLETE
10	(NOTE 2)	BUB (CHARACTER)
9	9	PIR-9 (FROM CSER)
8	8	PIR-8 (FROM CSER)

NOTES:

1. Vector 00 is provided by internal CPU operation.
2. First level interrupt vector provided by system board hardware; second level by peripheral.

LEGEND:

CSER	Control, Status, and Error Register
DMA	Direct Memory Access
NMI	Nonmaskable Interrupt
PIR	Programmed Interrupt Request
DUART	Dual Universal Asynchronous Receiver/Transmitter

Figure 3-35: Version 3 System Board Interrupt Assignments

Nonvolatile Random Access Memory

The Nonvolatile Random Access Memory (NVRAM) is a single chip providing 2K by 8 bits of memory for the storage of system configuration parameters. The chip is an 8K by 8 bit chip, but only 2K of the chip is used. Only 512 bytes of the 2K used is actually allocated. Parameters include console terminal settings, system error log, and the firmware password. NVRAM is maintained by a backup battery in the absence of VCC. When power is removed from the system, NVRAM enable (chip select) is inhibited to prevent an accidental write operation from destroying the NVRAM data. NVRAM should be read and written on full word boundaries using data bus bits 07—00. The following table further defines the contents of NVRAM.

NVRAM CONTENTS		
CATEGORY	**DESCRIPTION**	**NUMBER OF BYTES**
FIRMWARE (59 OF 128 BYTES USED)	FIRMWARE PASSWORD (passwd)	9
	CONSOLE SLOT AND PORT NUMBERS (cons_def)	1
	DOWNLOAD LINK BAUD RATE (link)	2
	DEFAULT BOOT DEVICE (b_dev)	1
	DEFAULT BOOT PATH NAME (b_name)	45
	FLAG TO CHECK FOR SECONTD DISK (dsk_chk)	1
	TOTAL FIRMWARE	59
UNIX OPERATING SYSTEM (67 OF 128 BYTES USED)	CONSOLE FLAGS (cflags)	2
	SAVED MONTH (nv_month)	1
	SAVED YEAR (nv_year)	1
	START OF PHYSICAL MEMORY (spmem)	4
	SYSTEM NAME (sys_name)	9
	ROOT DEVICE (rotdev)	1
	GENERAL STORAGE FOR I/O DRIVERS (ioslotinfo)	48
	SYSTEM BOARD ARTMASTER (artmaster)	1
	TOTAL OPERATING SYSTEM	67
PANIC ERROR INFORMATION	NVRAM SANITY (nvsanity)	4
	COMMAND AND STATUS REGISTER (csr)	2
	PROCESSOR STATUS WORD (psw)	4
	GENERAL PURPOSE REGISTER 3 (r3)	4
	GENERAL PURPOSE REGISTER 4 (r4)	4
	GENERAL PURPOSE REGISTER 5 (r5)	4
	GENERAL PURPOSE REGISTER 6 (r6)	4
	GENERAL PURPOSE REGISTER 7 (r7)	4
	GENERAL PURPOSE REGISTER 8 (r8)	4
	ADDRESS POINTER (oap)	4
	PROGRAM COUNTER (opc)	4
	STACK POINTER (osp)	4
	FRAME POINTER REGISTER (ofp)	4
	INTERRUPT STACK POINTER (isp)	4
	PROCESS CONTROL BLOCK POINTER REGISTER (pcbp)	4
	FAULT CODE REGISTER (mmufltcr)	4
	FAULT ADDRESS REGISTER (mmufltar)	4
	MMU SECTION RAM A (mmusrama)	16
	MMU SECTION RAM B (mmusramb)	16
	LOCAL FRAME POINTER (lfp)	4
	MESSAGE (message)	16
	PARAMETER 1 (param1)	16
	PARAMETER 2 (param2)	16
	TIME (time)	16
	TOTAL SAVED PANIC DATA	166
AND		
FIRMWARE ERROR INFORMATION (198 OF 254 BYTES USED)	GOOD ERROR (gooderror)	4
	ERROR NUMBER (errno)	4
	PROCESSOR STATUS WORD (psw)	4
	PROGRAM COUNTER (pc)	4
	MISCELLANEOUS (misc)	4
	STATUS CONTROL REGISTER AT FAULT (cser)	4
	FAULT LATCH REGISTER 1 (fl1)	4
	FAULT LATCH REGISTER 2 (fl2)	4
	TOTAL UNEXPECTED INTERRUPT AND EXCEPTION DATA	32
CHECKSUM (2 BYTES)	NVRAM CHECKSUM	2
TOTAL (2048 BYTES)	TOTAL BYTES USED	346

Dynamic Random Access Memory Controller

General. The system main memory is Dynamic Random Access Memory (DRAM). The DRAM Controller provides the system board CPU direct access to the I/O bus without passing through the RAM. The DRAM Controller handles the exchange of data and address information between the I/O bus and the system board CPU when operating in the "bypass mode."

Figure 3-36 is a functional block diagram of the DRAM Controller. The DRAM Controller for RAM is divided into the following functional areas:

- Address Generation Logic (address multiplexer)
- Request Generator
- Arbitration Logic
- Memory Refresh Logic
- Sequencer
- Bypass Logic
- Data Byte Rotate Unit Logic
- Parity Generation and Checking Logic.

Each of these functional areas is briefly described in the following paragraphs.

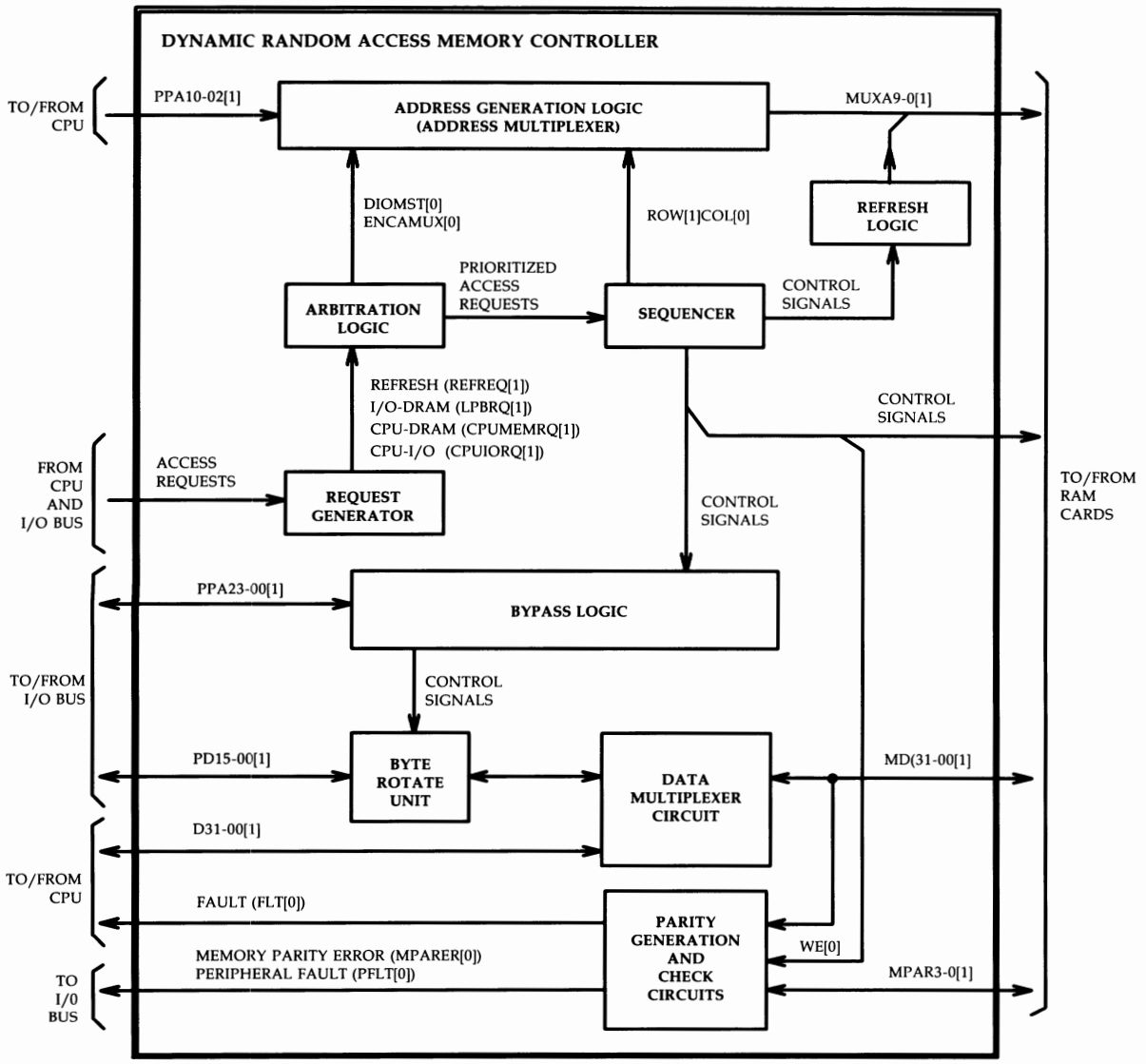


Figure 3-36: Dynamic Random Access Memory Controller — Functional Block Diagram

Address Generation Logic. The Address Generation Logic latches the stable virtual address during virtual to physical address translation. Since the 11 least significant bits of a virtual address and a physical address are identical, CPU—memory read accesses are started when the CPU presents a stable virtual address. The early start using the 11 least significant address bits enhances system performance.

Request Generator. The Request Generator synchronizes the bus requests with the system clock and passes the synchronized data requests to the Arbitration Logic. The Request Generator passes four types of requests to the Arbitration Logic. These requests are listed below:

Memory Refresh (REFREQ[1])
The memory refresh request is automatically generated every 16 microseconds.

Input/Output—DRAM (LPBRQ[1])
The input/output—memory request can originate from a feature card (PBRQ[0]) or from the Direct Memory Access Controller (XPBRQ[0]). The request is passed to the Arbitration Logic as LPBRQ[1].

CPU—DRAM (CPUMEMRQ[1])
The CPU—memory read or write operation requests are sent to the Arbitration Logic as CPUMEMRQ[1].

CPU—Input/Output (CPUIORQ[1])
The CPU—input/output exchange request is asserted by the Address Decoder (CREQ[0]) and is sent to the Arbitration Logic as CPUIORQ[1].

Arbitration Logic. The Arbitration Logic determines which requests for memory access are to be acknowledged. These access requests from highest to lowest priority are as follows:

- Memory Refresh (highest priority)
- Input/Output—DRAM
- CPU—DRAM
- CPU—Input/Output (lowest priority).

Memory Refresh Logic. The refresh of the DRAM is done one row at a time every 16 microseconds. The Request Generator is a counter and request flip-flop. Refresh requests are derived from the 1-MHz clock and occur every 16 microseconds. The refresh request increments the refresh address counter.

A memory refresh operation can occur between input/output to DRAM block transfers or between the read and write halves of a CPU/MMU interlocked operation. Refresh operations continue during reset sequences to retain any data which existed before the reset.

Sequencer. The Sequencer generates the control signals (strobes) for the access operations enabled by the arbitration logic. The Sequencer is a Field Programmable Logic Array (FPLA) and flip-flop network that combine to generate a variety of memory control signals.

Data Byte Rotate Unit. The Data Byte Rotate Unit is a collection of buffers used to multiplex the 32-bit data bus to/from the main memory to an 8- or 16-bit data bus for the I/O bus. This accommodates the input/output cards and system board devices in the DMA Subsystem that do not have a 32 bit capability. The byte rotate unit provides data alignment and packing for 8- and 16-bit peripherals when they access the 32-bit main memory and for system board CPU when the CPU communicates directly with the input/output (feature) cards. The system board devices that use the Data Byte Rotate Unit are listed below:

- Direct Memory Access Controller
- Dual Universal Asynchronous Receiver/Transmitter
- Integral Floppy Disk Controller
- Integral Hard Disk Controller.

The Byte Rotate Unit is controlled by the Sequencer logic. The PSIZE16[0] determines whether a peripheral is capable of transferring 8 or 16 bits at a time. Address bits 01 and 00 are used to select the data bus bytes. PSIZE16 is a 0 for 16-bit transfers; PSIZE16 is a 1 for 8-bit transfers. The PSIZE16[0] signal is sent by the peripheral (feature card) in response to a chip select signal. When a peripheral is a 16-bit device, 8-bit accesses are done by asserting the appropriate data strobe (PDS1—0[0]). Devices having 8-bit data interfaces require four passes to transfer a complete 32-bit word. Devices having 16-bit data interface require two passes to transfer a complete 32-bit word.

Byte 0 (bits 31—24) is the least significant byte. Byte 1 is bits 23—16. Byte 2 is bits 15—08. Byte 3 (bits 07—00) is the most significant byte. Address bits 01 and 00 are decoded (binary) to select the data bus bytes 3—0 as applicable. For 8-bit operations both address bits 01 and 00 are used to select the data bus bytes. For 16-bit operations only address bit 01 is used to select the data bus bytes (address bit 00 is not used in 16-bit operations). For 16-bit operations either data bus bytes 1 and 0 or bytes 3 and 2 are selected by only address bit 01. When address bit 01 is high [1], data bus bytes 2 and 3 are selected (bits 15—00). When address bit 01 is negated, data bus bytes 0 and 1 are selected (bits 31—16). The data strobes (PDS0[0] and PDS1[0]) are used to select which byte or bytes to access within the main memory. Figure 3-37 summarizes the decoding of the PSIZE16, PPA01, PPA00, PDS0, and PDS1 for the selection of data bytes for the 16-bit peripheral input/output bus and for the 32-bit main memory accesses.

SIZE BIT	ADDRESS BITS		DATA STROBES		VALID DATA BYTES	
PSIZE16[0]	PPA01[1]	PPA00[1]	PDS0[0]	PDS1[0]	32-BIT MAIN MEMORY	16-BIT INPUT/OUTPUT BUS
16 BIT						
0	0	x	0	0	0 AND 1	0 AND 1
0	0	x	0	1	0	0
0	0	x	1	0	1	1
0	0	x	1	1	ILLEGAL	—
0	1	x	0	0	2 AND 3	0 AND 1
0	1	x	0	1	0 OR 2	0
0	1	x	1	0	1 OR 3	1
0	1	x	1	1	ILLEGAL	—
8 BIT						
1	0	0	x	0	0	1
1	0	1	x	0	1	1
1	1	0	x	0	2	1
1	1	1	x	0	3	1

LEGEND:

x Don't care bit

Figure 3-37: Data Byte Selection Summary

Parity Generation and Checking. Twelve half-word Hamming check bits (MCB11—0[1]) accompany the 32 data bits on the data bus. Parity is checked only as part of read operations. If bad parity is detected, the Peripheral Fault (PFLT[0]) and Memory Parity Error (MPARER[0]) signals are asserted to the system board CPU or peripheral controllers (feature cards) depending on the type of access.

Bypass Logic. The Bypass Logic is used to establish direct communication between the system board CPU and feature cards without having to go through the main memory. Hence the term "bypass" is used to mean that main memory is bypassed for system board—feature card direct communication. The Bypass Logic passes the low order 24 bits of the Address Bus and the lower order 16 bits of the data bus directly to the I/O bus during direct communication between CPU and feature cards.

The system board requests the "bypass" mode by asserting the composite Input/Output Chip Select signal (CREQ[0]).

Direct Memory Access Subsystem

Subsystem Structure. Figure 3-38 is a high-level functional block diagram of the Direct Memory Access (DMA) Subsystem. The DMA Subsystem includes the following:

- Page Registers
- Floppy Control Register
- Floppy Disk Controller
- Floppy Controller Data Separator
- Direct Memory Access Controller
- Dual Universal Asynchronous Receiver/Transmitter.

Each of these functional areas is described in the following paragraphs.

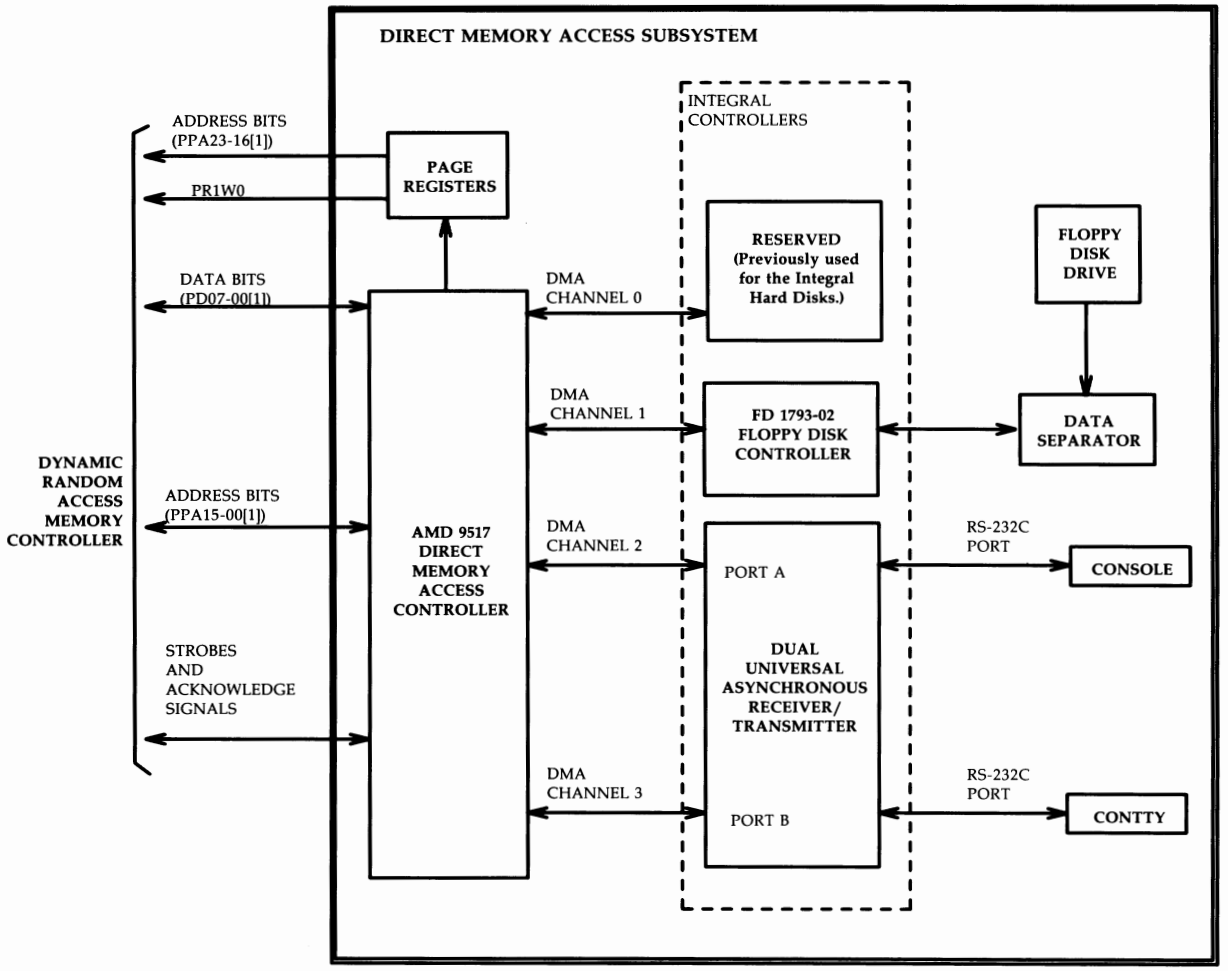


Figure 3-38: Direct Memory Access Subsystem — Functional Block Diagram

Page Registers. The Page Registers consist of three 12-bit registers. There is one register for each DMA channel used. (Channel 0 is not used.) The registers are "write only" and MUST be written as a half-word quantity, although they are only 12 bits wide. The addresses for the Page Registers are as follows.

REGISTER	ADDRESS
FLOPPY	0x 45002
UART A	0x 46002
UART B	0x 47002

The registers contain the upper portion of the address as well as the read/write (R1W0) bit. The R1W0 bit indicates the type of memory access. If the R1W0 bit is high [1], then the DMAC is going to read main memory. The Page Register address bits will allow up to 16 megabytes of addressing, but are limited to 64 kilobytes by the EIO bus. The order of the Page Register bits is as follows.

BIT	DATA BIT	FUNCTION
00	D00[1]	PA16[1]
01	D01[1]	PA17[1]
02	D02[1]	PA18[1]
03	D03[1]	PA19[1]
04	D04[1]	PA20[1]
05	D05[1]	PA21[1]
06	D06[1]	PA22[1]
07	D07[1]	PA23[1]
08	D08[1]	RESERVED
09	D09[1]	RESERVED
10	D10[1]	RESERVED
11	D11[1]	PR1W0

Floppy Control Register. The floppy control register was implemented to control some of the user programmable functions. The register is an 8-bit read/write register. The beginning address for the floppy control register is 0x 40003. The assignments for the floppy control register bits are as follows.

BIT	DATA BIT	FUNCTION
0	D00[1]	FLOPPY DRIVE SELECT 0
1	D01[1]	FLOPPY DRIVE SELECT 1
2	D02[1]	FLOPPY DRIVE SELECT 2
3	D03[1]	FLOPPY DRIVE SELECT 3
4	D04[1]	PRECOMPENSATION BIT 0
5	D05[1]	PRECOMPENSATION BIT 1
6	D06[1]	PRECOMPENSATION BIT 2
7	D07[1]	FORCE PRECOMPENSATION

Up to four floppy disk drives can be configured with this system. Bits 0—3 are used to select which floppy disk drive is used. Bits 4—6 are used by the data separator to determine the amount of precompensation used when writing the floppy.

Integral Floppy Disk Controller. The integral Floppy Disk Controller provides data and access control for a single floppy disk drive. The controller is a FD 1793-02 and provides the following:

- Single Frequency Modulation (FM) and Modified Frequency Modulation (MFM) density
- Automatic seek with verify
- Soft sector compatibility.

The controller resides on the DMA Subsystem data bus bits 07—00[1]. The chip is enabled by the FCS[0] signal or the DMA acknowledge DACK1[0]. All floppy disk interface signals are terminated at the receiving end by a resistor network of 150 ohms to VCC.

Floppy Controller Data Separator. The FDC 9229-BT data separator is used to separate the data and clock signal from the data coming in from the floppy disk drive. The data separator includes the following features:

- Digital data separator
- Separates FM and MFM encoded data
- No adjustments necessary
- Compatible for 5.25- and 8-inch floppy disks
- Variable write precompensation
- Internal oscillator circuit
- Track selectable write precompensation.

The data separator receives controls from the floppy controller and floppy controller register. The floppy controller indicates when a write occurs and if precompensation should be performed. The floppy controller register determines how much precompensation to perform.

The CSER is also involved in the data separator. Bits 21 and 22 select the density of the floppy disk drive and the size of the floppy disk drive, respectively. These signals control the internal dividers of the data separator. A 16-MHz clock signal is connected to the data separator and divided to create the proper clock for the floppy controller. The separator generates the clock for the floppy controller and the read clock for the incoming data.

Direct Memory Access Controller. The integral Direct Memory Access Controller (DMAC) serves the Dual Universal Asynchronous Receiver/Transmitter (DUART) and the integral Floppy Disk Controller. The DMAC has four independent DMA channels. Each channel has separate registers for mode control, current address, base address, current word count, and base word count.

The DMAC generates a 16-bit address. An additional 12-bit "page" register is used for three of the four DMA channels (Channel 0 is not used) to provide DMA accessibility to the 26-bit Dynamic Random Access Memory (DRAM). The most significant bit of each Page Register is the read/write bit.

Dual Universal Asynchronous Receiver/Transmitter. The CONSOLE (UART 0) and CONTTY (UART 1) are driven by a Signetics 2681-40 DUART. Each channel (0 and 1) provides the following signals:

- Transmit data (TXD)
- Receive data (RXD)
- Data Carrier Detect (DCD)
- Data Terminal Ready (DTR).

Electrically, the DUART is on the peripheral bus with five other devices in the DMA Subsystem.

The UART has three output ports that are used for non-UART functions. These functions are listed below:

- Control of off-board AC power relay via Output Port 2 (OP2) (PWRON[0]). The signal is high during normal operations.
- Control of the Power indicator under certain operational conditions via Output Port 3 (OP3) (GLEDON[1]).
- Output Port 4 (OP4) (UFEJCT[0]) is buffered and is sent to the floppy disk interface connector for feature application.
- Output Port 5 (0P5) (UFDSEL[0]) is buffered and sent to J10 as the Floppy Drive Select (FDSEL[0]).

System Board Firmware

The system board firmware is programmed instructions stored in ROM which form the basic operating system when the system is not running the UNIX operating system. The purpose of this firmware is to initialize the system and provide the means to load and run other programs such as the UNIX operating system, **filledt**, and **dgmon**. The firmware level built-in programs are listed below:

baud	Change the firmware baud rate. Valid firmware baud rates are 50, 75, 110, 134, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, and 38400. The default baud rate is 9600.
edt	Display the Equipped Device Table (EDT) data.
errorinfo	Display expanded firmware error message information. This capability is provided with firmware PF3 and later versions.
express	Enable/disable diagnostics execution during reboot.
newkey	Make a new floppy key.
passwd	Change the firmware password.
sysdump	Copy the system image (RAM) to floppy disks.
version	Display firmware version information.

When the system is RESET or first powered on, the system board firmware controls the initialization of the system. The sequence of events is as follows:

- Test processor sanity.
- Check ROM.
- Check NVRAM.
- Check RAM.
- Check DUART.
- Check Disk Sanity.
- Self-configuration (build the EDT).
- Run normal diagnostics on all equipped boards/cards listed in the EDT. (If not disabled via the **express** command.)
- Boot the UNIX operating system.

System Board EDT Data

The following table shows the EDT data for a system board. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI).

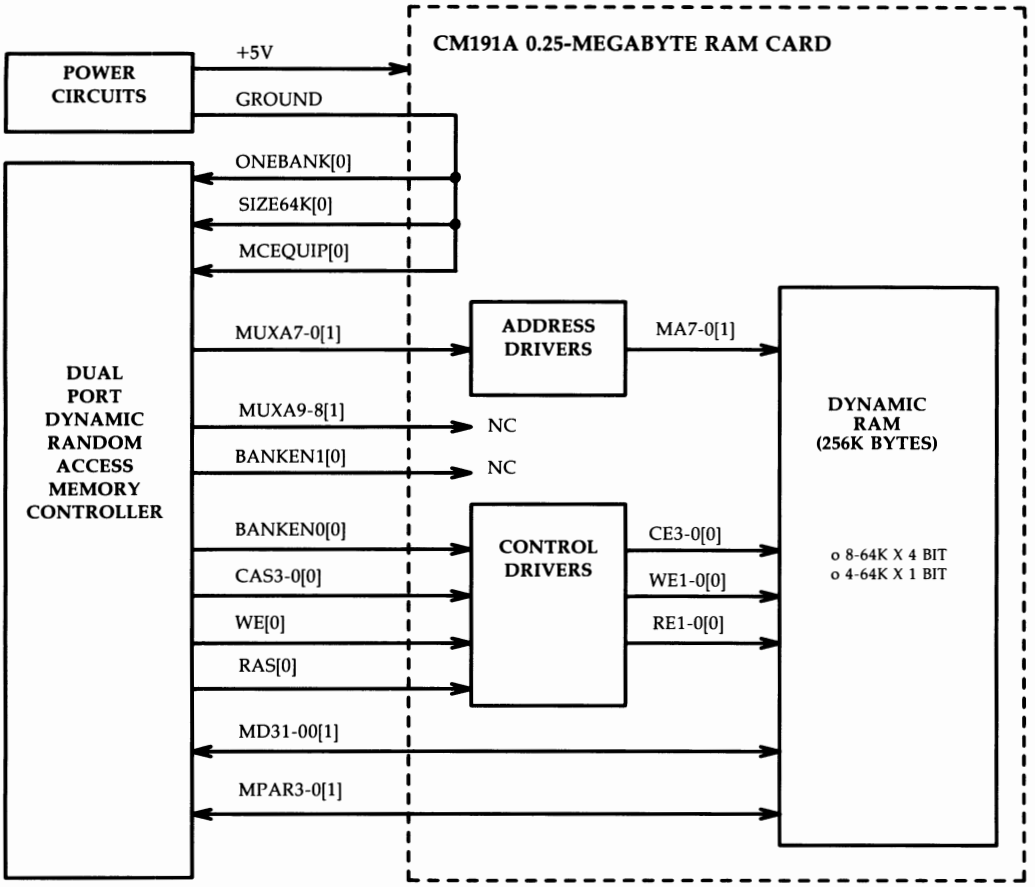
EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0001
DEVICE NAME (dev_name)	SBD
REQUEST QUEUE SIZE (rq_size)	0x 00
COMPLETION QUEUE SIZE (cq_size)	0x 00
BOOT DEVICE (boot_dev)	1
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	1
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	1
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

RANDOM ACCESS MEMORY CARDS

CM191A/B/C/D and CM192B Memory Cards

Functional block diagrams of the various Version 2 Random Access Memory (RAM) cards are provided in Figures 3-39 through 3-43. Functionally, all memory cards consist of address drivers, control drivers, and a Dynamic Random Access Memory (DRAM) circuit. The various types and sizes of cards are identified to the system during self-configuration by the state of the SIZE64K[0] and ONEBANK[0] signals. The various types of memory cards in relation to the state of the SIZE64K[0] and ONEBANK[0] signals are summarized in the following table.

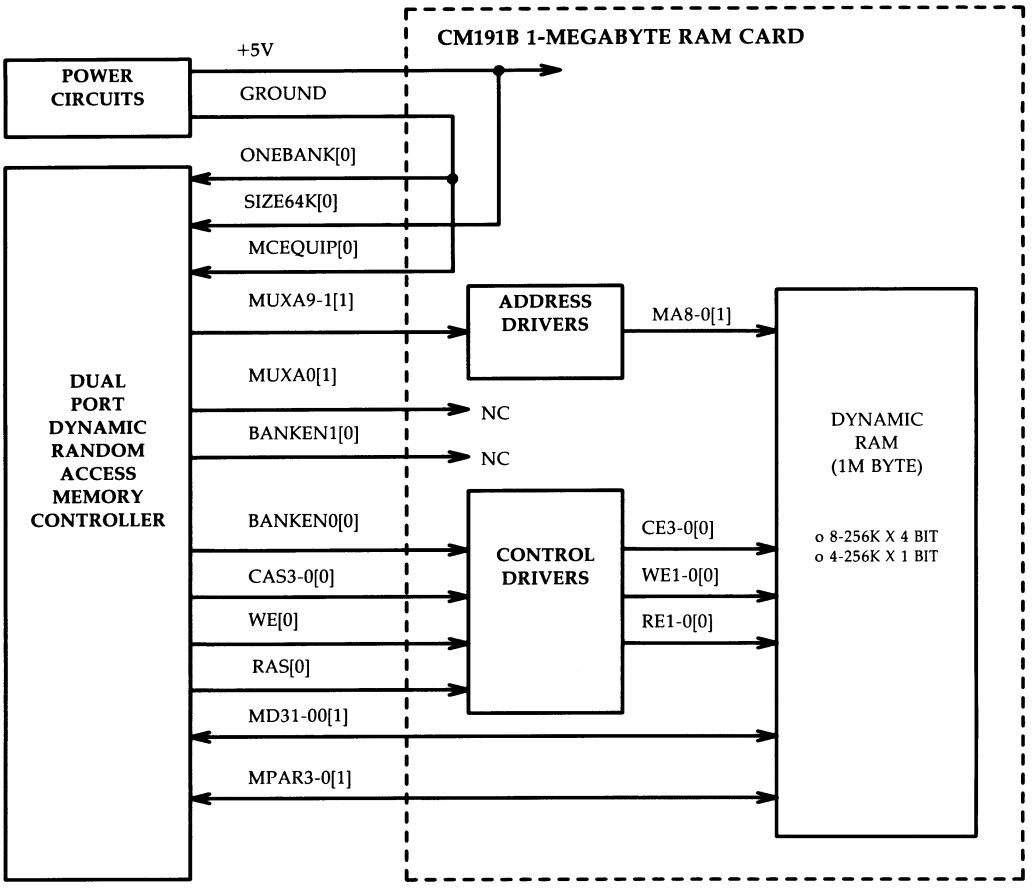
CARD TYPE	SIZE64K[0]	ONEBANK[0]
CM191A (0.25 M)	0 = 64K	0 = 1 BANK
CM191B (1.0 M)	1 = 256K	0 = 1 BANK
CM191C (1.0 M)	1 = 256K	0 = 1 BANK
CM191D (2.0 M)	1 = 256K	1 = 2 BANKS
CM192B (2.0 M)	1 = 256K	1 = 2 BANKS



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable
MA	Memory Address
MCEQUIP	Memory Card Equipped
MUXA	Multiplexed Address
NC	No Connection
RAS	Row Address Strobe
RE	RAS Enable
WE	Write Enable

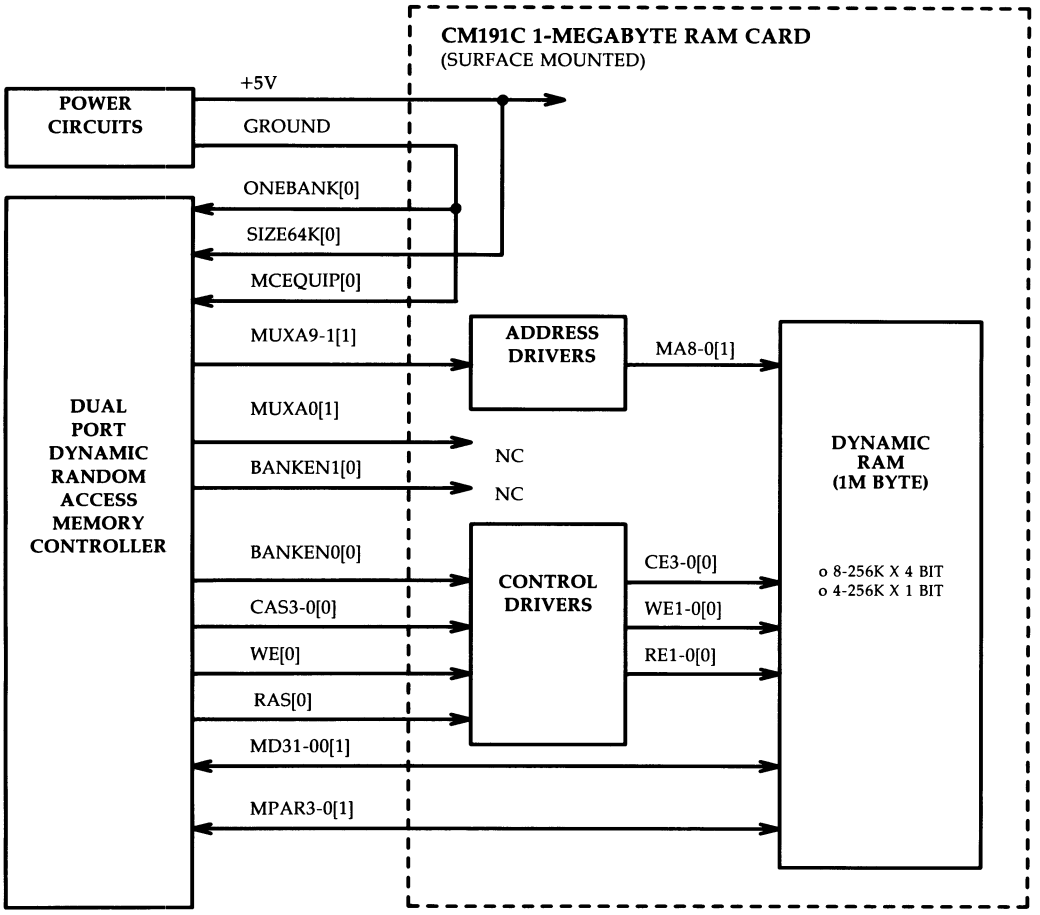
Figure 3-39: CM191A 0.25-Megabyte RAM Card — Functional Block Diagram



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable
MA	Memory Address
MCEQUIP	Memory Card Equipped
MUXA	Multiplexed Address
NC	No Connection
RAS	Row Address Strobe
RE	RAS Enable
WE	Write Enable

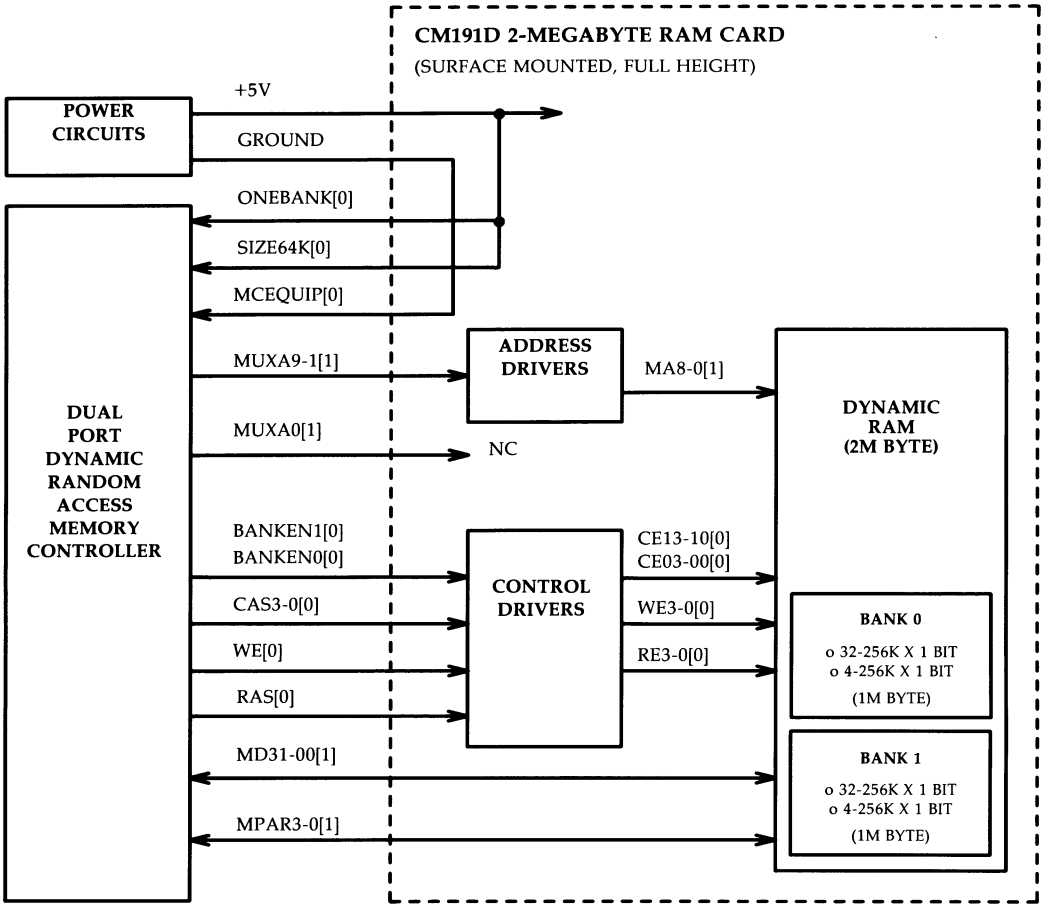
Figure 3-40: CM191B 1-Megabyte RAM Card — Functional Block Diagram



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable
MA	Memory Address
MCEQUIP	Memory Card Equipped
MUXA	Multiplexed Address
NC	No Connection
RAS	Row Address Strobe
RE	RAS Enable
WE	Write Enable

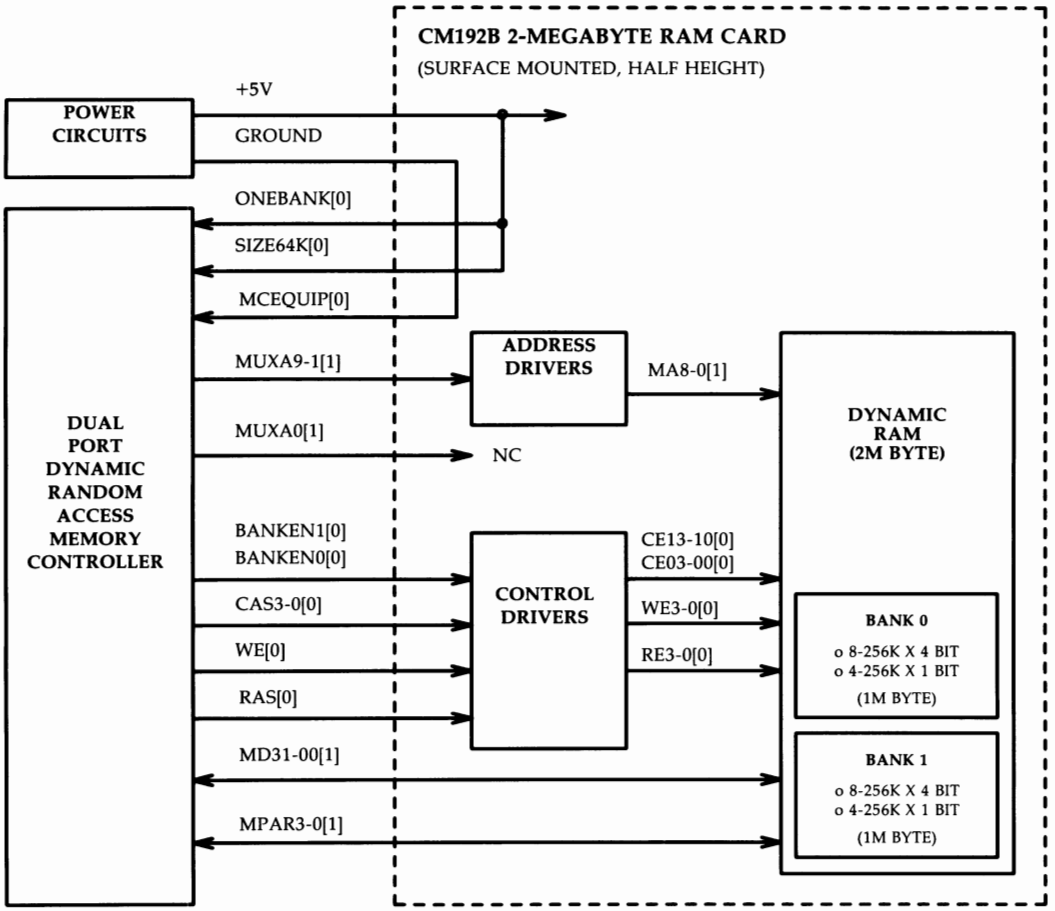
Figure 3-41: CM191C 1-Megabyte, Surface Mounted, RAM Card — Functional Block Diagram



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable
MA	Memory Address
MCEQUIP	Memory Card Equipped
MUXA	Multiplexed Address
NC	No Connection
RAS	Row Address Strobe
RE	RAS Enable
WE	Write Enable

Figure 3-42: CM191D 2-Megabyte, Surface Mounted, Full Height, RAM Card — Functional Block Diagram



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable
MA	Memory Address
MCEQUIP	Memory Card Equipped
MUXA	Multiplexed Address
NC	No Connection
RAS	Row Address Strobe
RE	RAS Enable
WE	Write Enable

Figure 3-43: CM192B 2-Megabyte, Surface Mounted, Half Height, RAM Card — Functional Block Diagram

Memory Control Signals

The memory control signals include the following:

BANKEN0[0] The "bank enable 0" signal is used to select (enable) the read or write access of memory array bank 0.

BANKEN1[0] The "bank enable 1" signal is used to select (enable) the read or write access of memory array bank 1.

CAS3—0[0] The "column address strobes" signal is used to strobe (enable) the column address.

WE[0] The "write enable" signal is used to write data to the memory.

RAS[0] The "row address strobe" signal is used to strobe (enable) the row address.

Memory Address Signals

Memory address signals are supplied from the Address Generation logic of the Dual Port Dynamic Random Access Memory Controller via a 10-bit multiplexed memory address bus. Control signals applied to the memory cards determine whether the address is used as a row or column address. The relationship between the I/O bus and the multiplexed memory address bus for row and column addresses is shown in the following table. Note that all multiplexed address bus bits are NOT used by a given RAM card.

INPUT/OUTPUT ADDRESS BUS		MULTIPLEXED MEMORY ADDRESS BUS BITS	MEMORY CARD TYPE		
ROW ADDRESS BITS	COLUMN ADDRESS BITS		CM191A	CM191B/C/D	CM192B
02	19	9	NC	x	x
10	18	8	NC	x	x
09	17	7	x	x	x
08	16	6	x	x	x
07	15	5	x	x	x
06	14	4	x	x	x
05	13	3	x	x	x
04	12	2	x	x	x
03	11	1	x	x	x
02	10	0	x	NC	NC

Data and Parity Signals

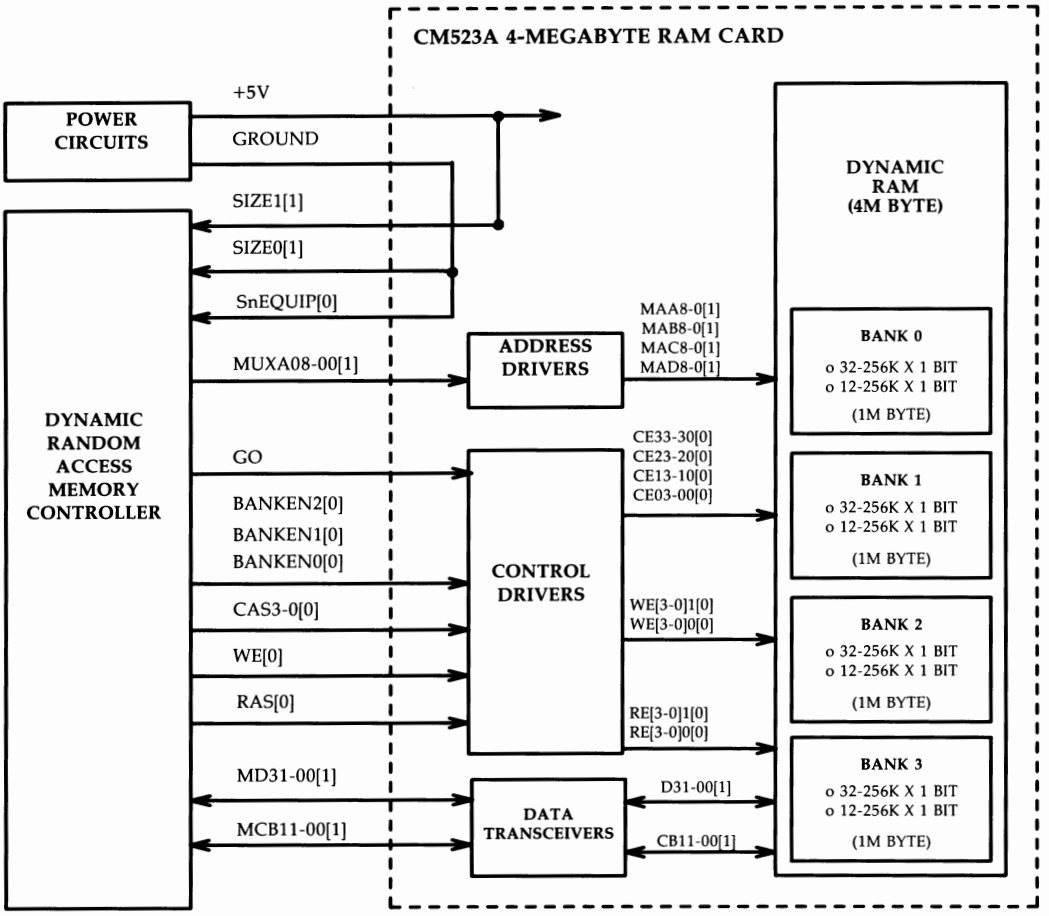
The data bus includes 32 data bits (MD31—00[1]) and 4 bits of byte parity (MPAR3—0[1]). The relationship of the parity bits to the data bytes is shown in the following table.

MPAR0	MPAR1	MPAR2	MPAR3
MD31 — 24	MD23 — 16	MD15 — 08	MD07 — 00

CM523A/AA/B/D Memory Cards

Functional block diagrams of the various Version 3 RAM cards are provided in Figures 3-44 through 3-47. Functionally, all memory cards consist of address drivers, control drivers, data transceivers, and a Dynamic Random Access Memory (DRAM) circuit. The various types and sizes of cards are identified to the system during self-configuration by the state of the SIZE0[1] and SIZE1[1] signals. The various types of memory cards in relation to the state of the SIZE0[1] and SIZE1[1] signals are summarized in the following table.

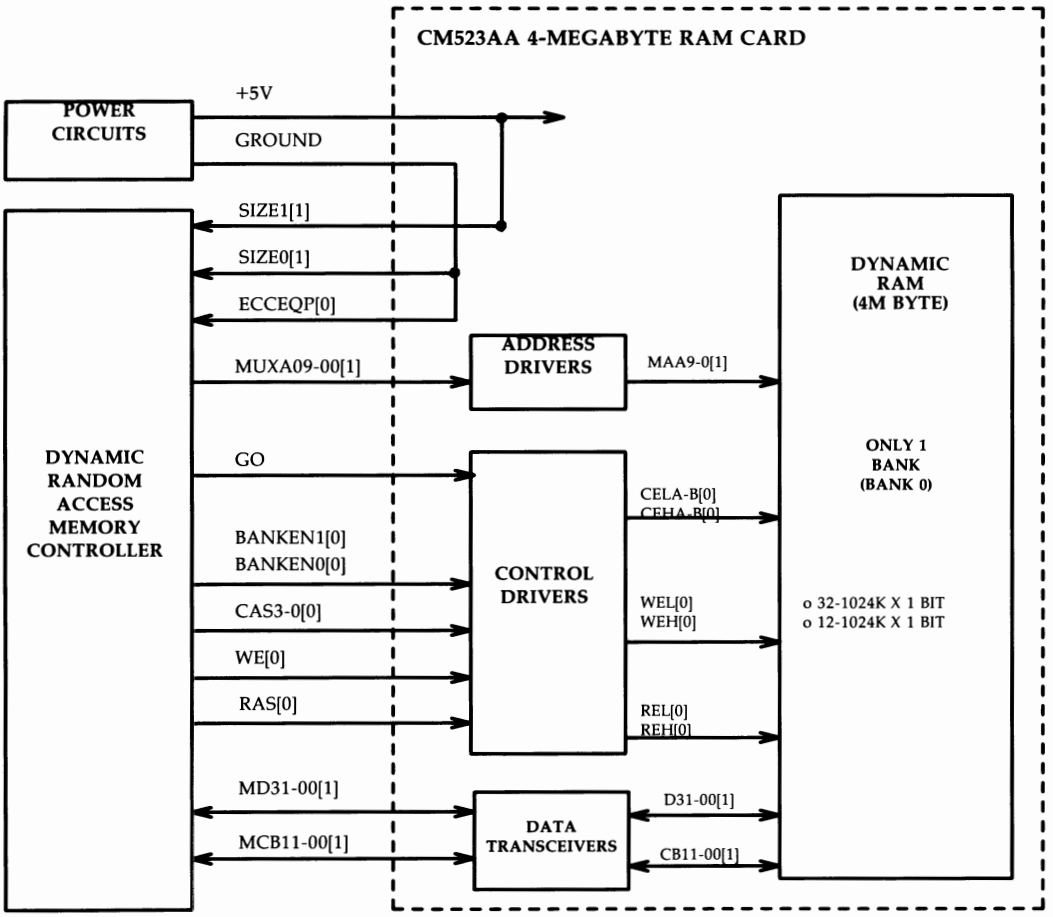
CARD TYPE	SIZE1[1]	SIZE0[1]
CM523A/AA (4.0 M)	1	0
CM523B (2.0 M)	0	0
CM523D (16.0 M)	1	1



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable
MA	Memory Address
MUXA	Multiplexed Address
RAS	Row Address Strobe
RE	RAS Enable
SnEQUIP	Slot n Equipped
WE	Write Enable

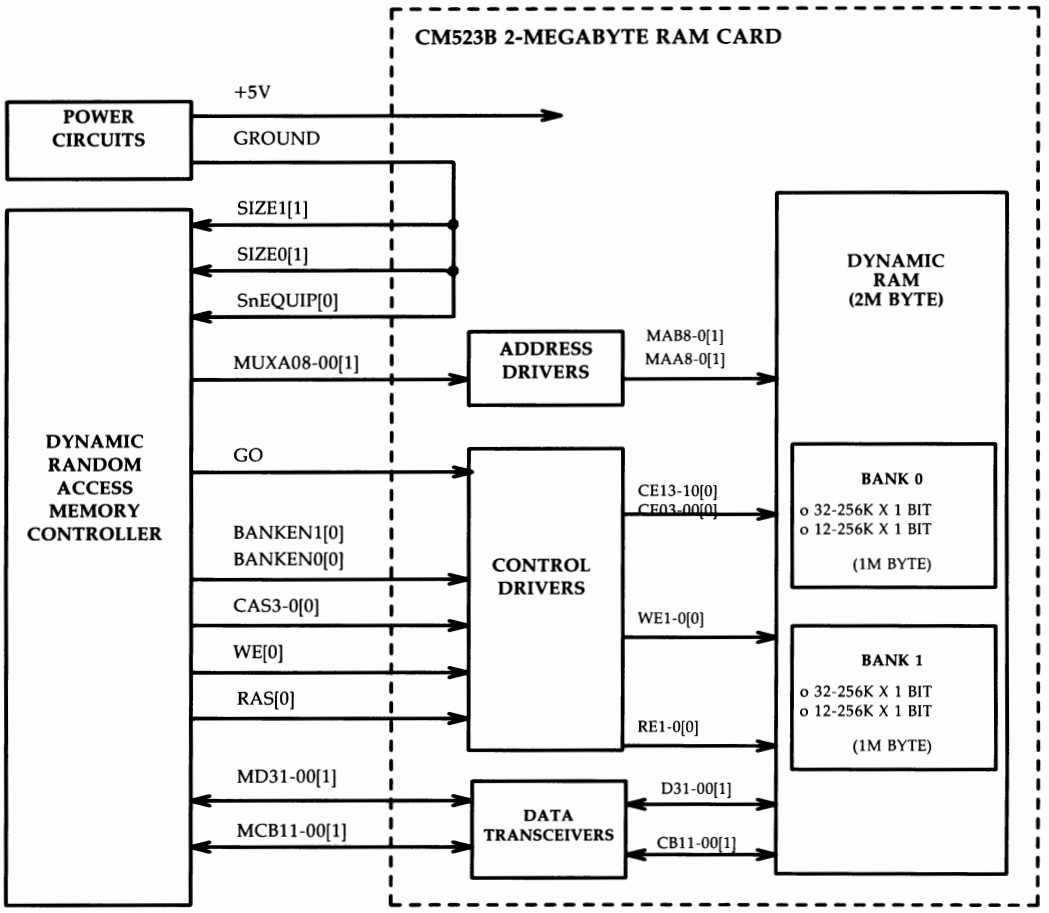
Figure 3-44: CM523A 4-Megabyte RAM Card — Functional Block Diagram



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable (Low and High)
MA	Memory Address
MUXA	Multiplexed Address
RAS	Row Address Strobe
RE	RAS Enable (Low and High)
SnEQUIP	Slot n Equipped
WE	Write Enable (Low and High)

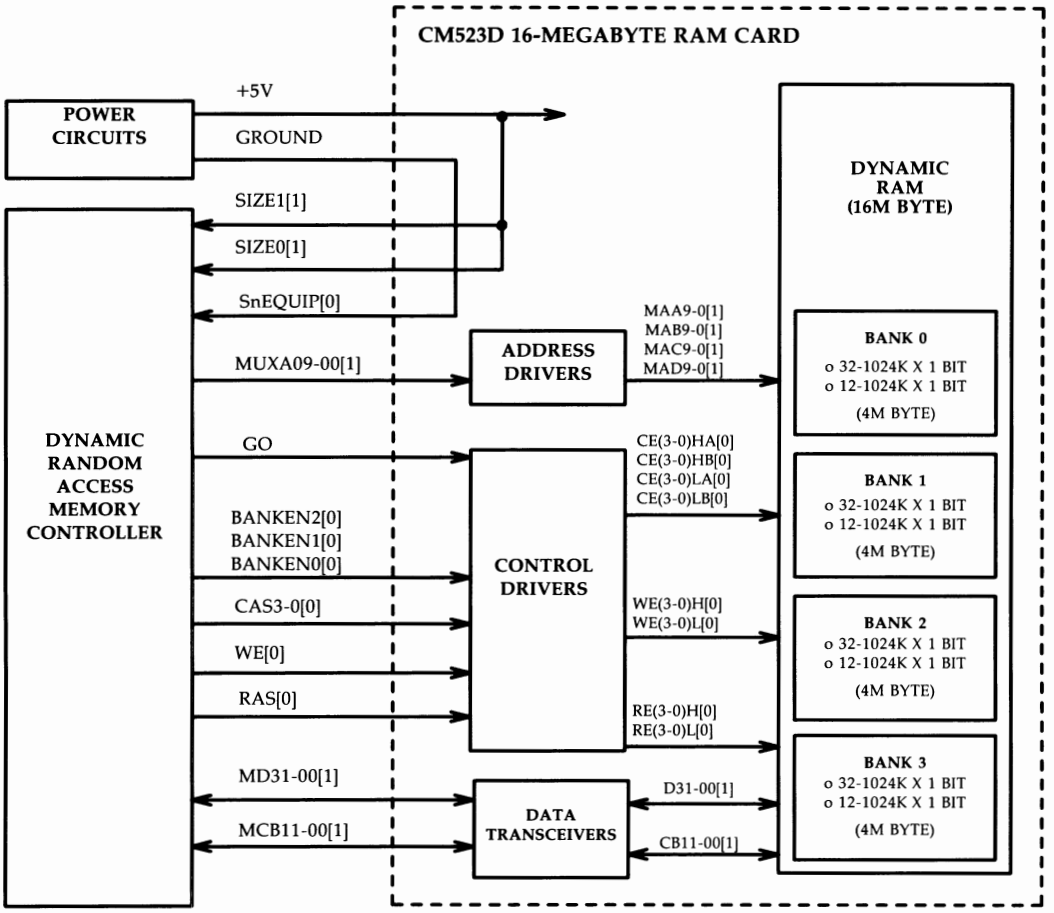
Figure 3-45: CM523AA 4-Megabyte RAM Card — Functional Block Diagram



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable
MA	Memory Address
MUXA	Multiplexed Address
RAS	Row Address Strobe
RE	RAS Enable
SnEQUIP	Slot n Equipped
WE	Write Enable

Figure 3-46: CM523B 2-Megabyte RAM Card — Functional Block Diagram



LEGEND:

CAS	Column Address Strobe
CE	CAS Enable (High and Low Half-words)
MA	Memory Address
MUXA	Multiplexed Address
RAS	Row Address Strobe
RE	RAS Enable (High and Low Half-words)
SnEQUIP	Slot n Equipped
WE	Write Enable (High and Low Half-words)

Figure 3-47: CM523D 16-Megabyte RAM Card — Functional Block Diagram

Memory Control Signals

The memory control signals include the following:

BANKEN(3-0)[0]
The "bank enable" signals are used to select (enable) the read or write access of individual memory array banks.

CAS3-0[0] The "column address strobes" signals are used to strobe (enable) the column address.

CE(3-0)[0] The "CAS enable" signals are buffered versions of CAS(3-0)[0] and are used to enable the column address into the memory chips of the designated bank (3-0).

RAS[0] The "row address strobe" signals are used to strobe (enable) the row address.

RE(3-0)[0] The "RAS enable" signals are buffered versions of RAS[0] and are used to enable the row address into the memory chips of the designated bank.

WE(3-0)[0] The "write enable" signals are used to write data to the memory.

Note: The enable signals operate on half-words, designated by "H" and "L" for "high order" or "low order."

Memory Address Signals

Memory address signals are supplied from the Address Generation logic of the Dynamic Random Access Memory Controller (DRAMC) via a 10-bit multiplexed memory address bus. Control signals applied to the memory cards determine whether the address is used as a row or column address. The relationship between the buffered microbus and the multiplexed memory address bus for row and column addresses is shown in the following table. Note that all multiplexed address bus bits are NOT necessarily used by a given RAM card.

BUFFERED MICROBUS ADDRESS		MULTIPLEXED MEMORY ADDRESS BUS BITS
ROW ADDRESS BITS	COLUMN ADDRESS BITS	
23	22	10
21	20	9
19	10	8
18	09	7
17	08	6
16	07	5
15	06	4
14	05	3
13	04	2
12	03	1
11	02	0

Data and Check Signals

The data bus includes 32 data bits (MD31—00[0]) and 12 bits of half-word modified Hamming check (MCB11—0[0]). The Hamming bits, along with the error detection and correction circuitry in the memory controller, allow double-bit error detection and single-bit error correction in each half-word of memory. The relationship of the check bits to the data bytes is shown in the following table.

MCB11—06[1]	MCB05—00[1]
MD31 — 16[1]	MD15 — 00[1]

BACKPLANES

General

The backplane provides connections for power and bus signals between the system board and other circuit cards that may be in the computer. The backplane also provides for the proper termination of all bus signals. Because of bus termination, the backplane and system board must always be connected for the computer to be operational.

The Version 2 backplanes are restricted to I/O feature cards. The 3B2/300 and 310 computers backplane (CM193A/B) provide connections for four feature cards. The 3B2/400 computers backplane (CM194B) provides connections for 12 feature cards.

The Version 3 backplanes provide a connection for the Version 3 system boards. There are also connections for I/O feature cards, performance enhancement cards, and memory cards. The CM519 series backplanes also have "power only" slots that supply power but no bus connections. The following table lists the backplane connections for the Version 3 computers.

	3B2/500 (CM520A)	3B2/600 (CM519A)	3B2/700 (CM519A)	3B2/1000 (CM519B)
I/O Slots	7	12	12	12
Performance Slots	3	5	5	6
Memory Slots	2	4	4	4
Power Only Slots	0	3	3	2

CM193A/B Backplane Board

The CM193A/B is a 4-slot backplane board. The backplane board plugs into the 100-pin (A or J02) and 60-pin (B or J03) input/output expansion connectors on the system board. A maximum of either two double-width or four single-width feature cards can be plugged into this backplane. Figure 3-48 is a functional block diagram of a CM193A/B Backplane.

All power, ground, and bus signals for the features cards are from the J02 and J03 system board connections. Certain bus signals are terminated on the backplane as shown on Figure 3-48. No connections are provided for the Card Select 15—05 (CS15—05[0]) signals by the CM193A/B Backplane.

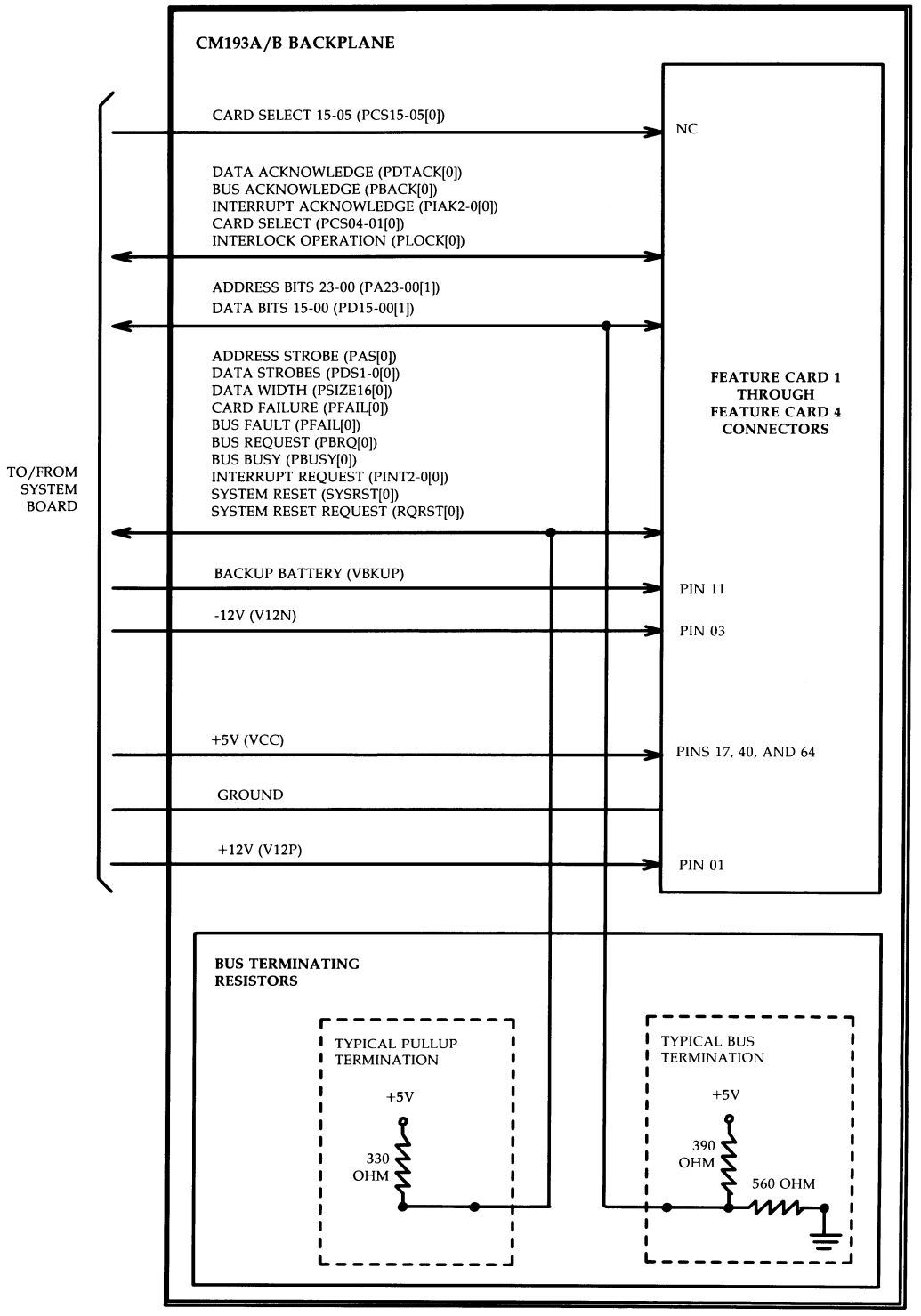


Figure 3-48: CM193A/B (3B2/300 and 310) Backplane — Functional Block Diagram

CM194B Backplane

The CM194B is a 12-slot backplane board. The backplane board plugs into the 100-pin (A or J02) and 60-pin (B or J03) input/output expansion connectors on the system board. A maximum of either 6 double-width or 12 single-width feature cards can be plugged into this backplane.

All bus signals for the features cards are from the J02 and J03 system board connections. Certain bus signals are terminated on the backplane as shown on Figure 3-49. No connections are provided for the Card Select 15—13 (CS15—13[0]) signals by the CM194B Backplane.

Power and ground for the features cards are handled differently from the CM193A/B Backplane. Because of the number of feature cards supported by the CM194B Backplane, +5 volt (VCC), +12 volt (V12P) and ground connections are directly supplied from the Power Supply via the 12-pin power connector on the backplane. Only the -12 volt (V12N) power is supplied to the backplane from the system board connector (J02).

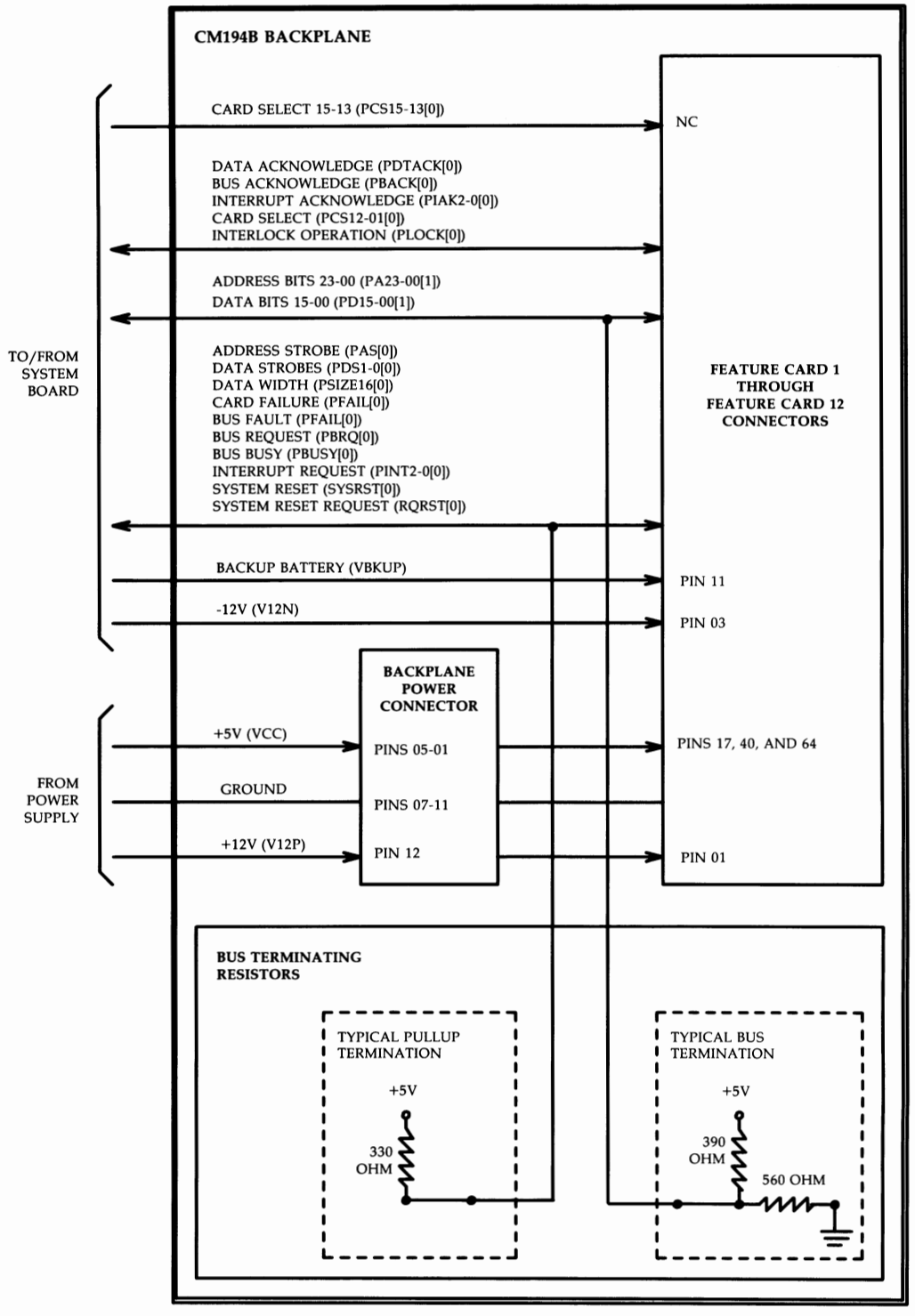


Figure 3-49: CM194B (3B2/400) Backplane — Functional Block Diagram

CM519A Backplane Board

The CM519A is a 24-slot backplane board. The system board plugs into the middle of the backplane board. There are 12 I/O slots above the system board to hold a maximum of either 6 double-wide or 12 single-width feature cards. There are 12 performance slots underneath the system board consisting of 4 memory, 4 buffered microbus (for MPE cards), 1 VCACHE, and 3 power only connectors. Figure 3-50 shows the functional diagram of the CM519A Backplane. Exact signal and pinout information is provided in Appendix B.

Power and ground (+5 volt, +12 volt, -12 volt, and GRD) for the feature cards are supplied from the power supply via connectors on the backplane. The floppy disk drive is connected directly to the backplane via a 34-pin connector. The "Power" and "Diagnostic" LEDs and NVRAM battery are also connected to the backplane.

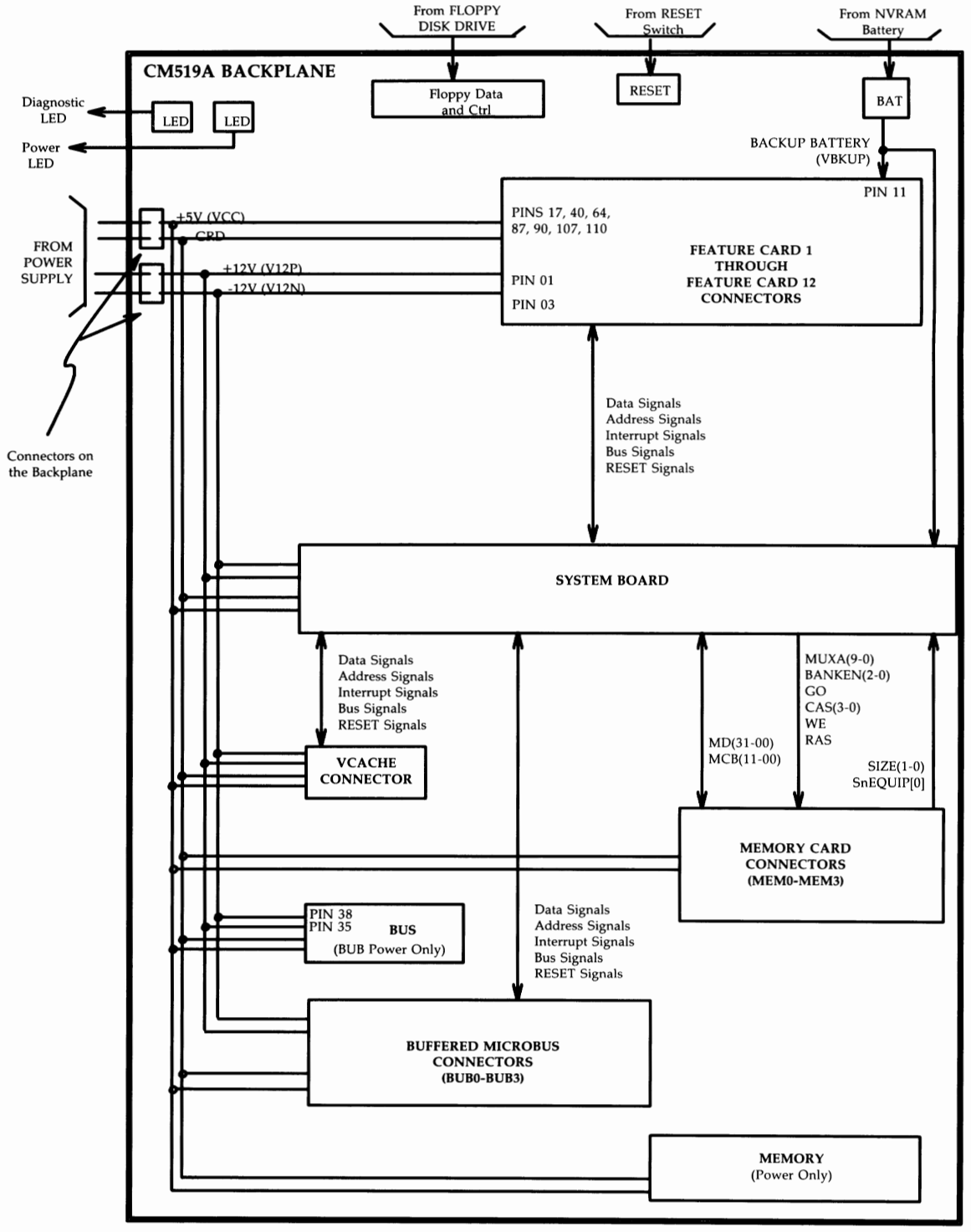


Figure 3-50: CM519A (3B2/600 and 700) Backplane — Functional Block Diagram

CM519B Backplane Board

The CM519B is a 24-slot backplane board. The system board plugs into the middle of the backplane board. There are 12 I/O slots above the system board to hold a maximum of either 6 double-wide or 12 single-width feature cards. There are 12 performance slots underneath the system board consisting of 4 memory, 3 buffered microbus (for MPE cards), 3 processor bus (for PE cards), and 2 power only connectors. Figure 3-51 shows the functional diagram of the CM519B Backplane. Exact signal and pinout information is provided in Appendix B.

Power and ground (+5 volt, +12 volt, -12 volt, and GRD) for the features cards are supplied from the power supply via connectors on the backplane. The floppy disk drive is connected directly to the backplane via a 34-pin connector. The "Power" and "Diagnostic" LEDs and NVRAM battery are also connected to the backplane.

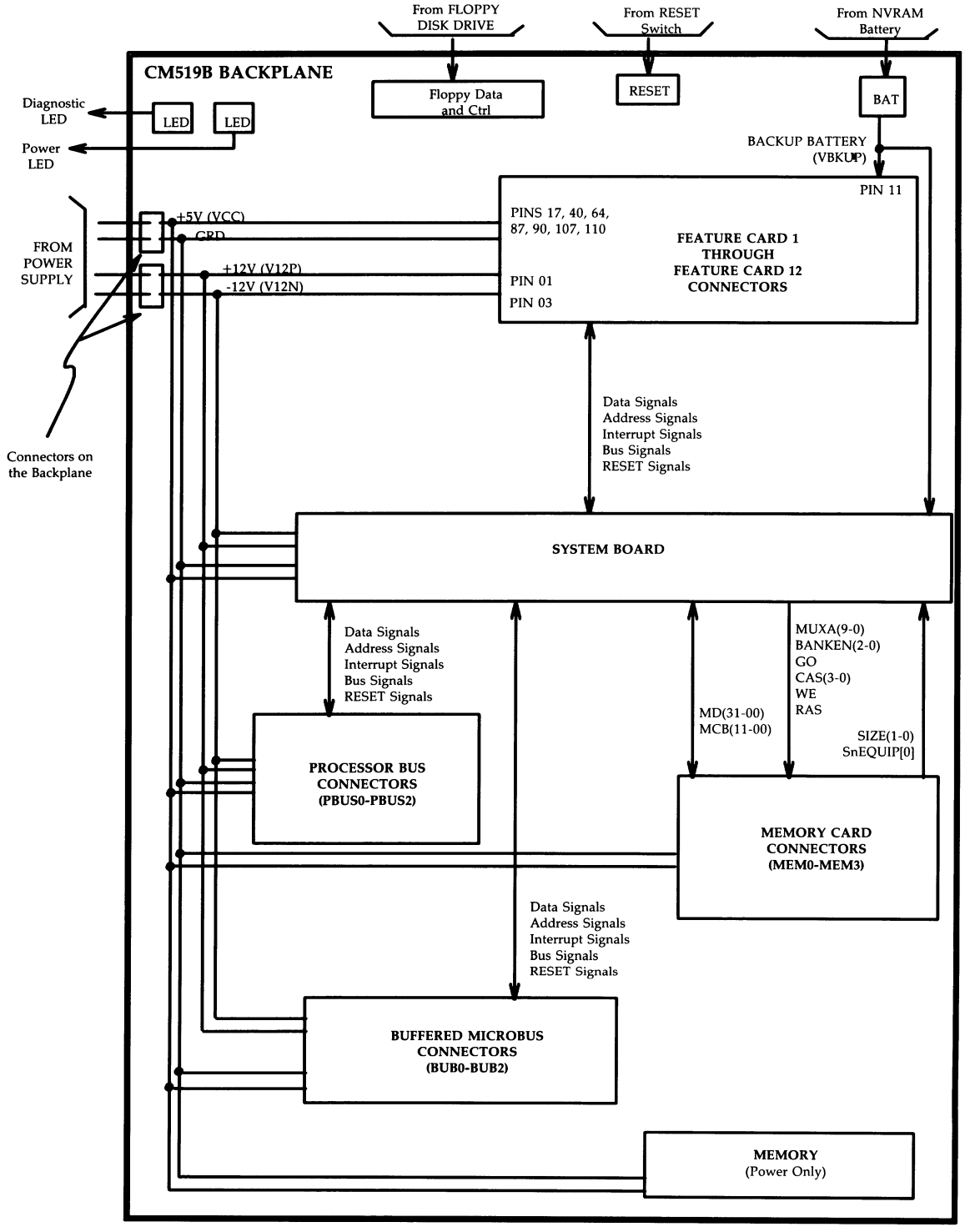


Figure 3-51: CM519B (3B2/1000) Backplane — Functional Block Diagram

CM520A Backplane Board

The CM520A is a 12-slot backplane board. The system board plugs into the bottom of the backplane board. There are 7 I/O slots to hold a maximum of either 3 double-wide or 7 single-width feature cards. There are 5 performance slots consisting of 2 memory, 2 buffered microbus (for MPE cards), and 1 VCACHE connectors. Figure 3-52 shows the functional diagram of the CM520A Backplane. Exact signal and pinout information is provided in Appendix B.

Power and ground (+5 volt, +12 volt, -12 volt, and GRD) for the features cards are supplied from the power supply via connectors on the backplane. The floppy disk drive is connected directly to the backplane via a 34-pin connector. The "Power" and "Diagnostic" LEDs and NVRAM battery are also connected to the backplane.

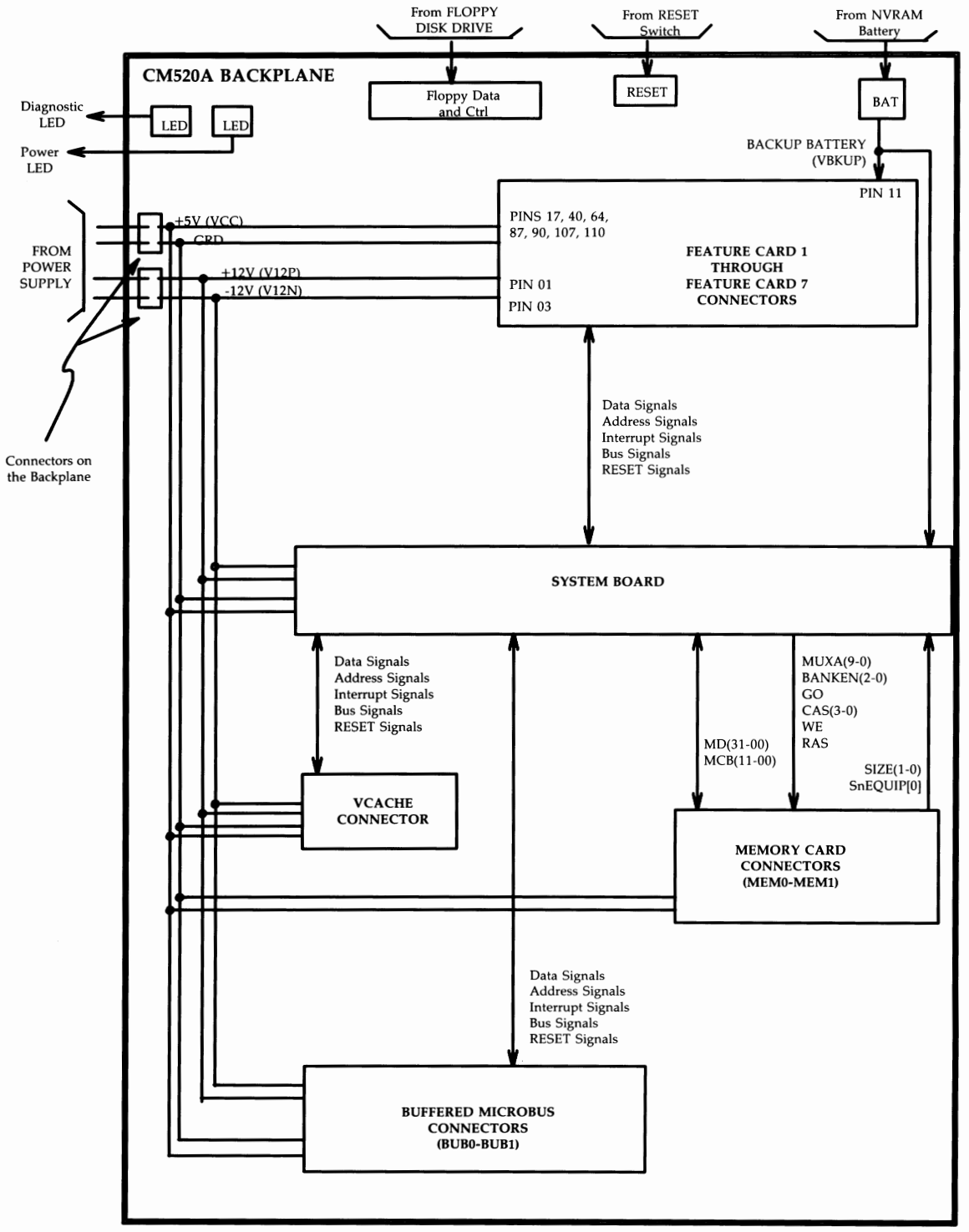


Figure 3-52: CM520A (3B2/500) Backplane — Functional Block Diagram

CM195A NETWORK INTERFACE CARD

General

The CM195A Network Interface (NI) Card is an intelligent feature card used to interface the 3B2 computer to the AT&T 3BNET Local Area Network. Figure 3-53 is a functional block diagram of the CM195A NI Card. The NI card consists of the Common Input/Output (CIO) circuits and the Network Interface circuits. The CIO circuits include the following:

- INTEL 80186 Microprocessor
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Local Random Access Memory (RAM)
- Local Read Only Memory (ROM)
- Miscellaneous circuits.

The Network Interface is an INTEL 82586 Ethernet Controller. The Network Interface circuits function as a network coprocessor.

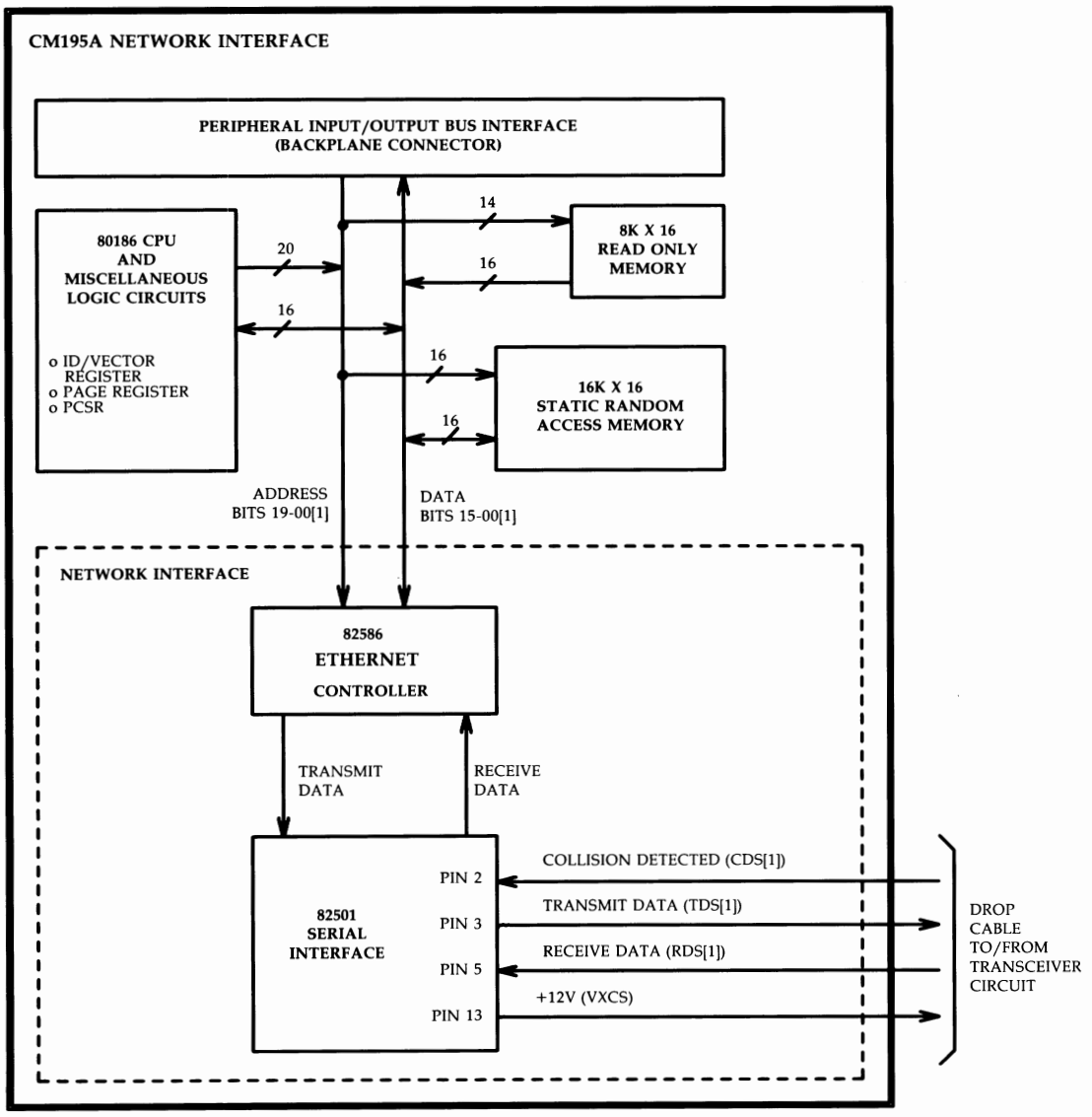


Figure 3-53: CM195A NI Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the NI card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the NI card are described in the following paragraphs. Figure 3-54 shows the NI card address map.

Input/Output Bus Control

The I/O bus control circuitry responds to I/O bus and 80186 Microprocessor control signals. Three major paths are listed below:

- 80186 Microprocessor read or write of the system board main memory
- System board CPU read or write NI card
- Interrupt Acknowledge (PIAK[0]).

The I/O bus control circuitry responds to the I/O bus and to the 80186 Microprocessor control signals by selectively enabling the appropriate I/O bus signals. In addition, the Bus Abort Feature (BAF) can be prematurely forced. Certain Peripheral Control and Status Register (PCSR) bits can also be set when the NI is accessed.

NI CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	RAM (VECTOR TABLE)	READ/WRITE	16	128
0x 00080	—	LCS	RAM (DEMON)	READ/WRITE	16	256
0x 00180	—	LCS	RAM (USER)	READ/WRITE	16	255.6K
0x 20000	—	LCS	UNUSED	—	—	128K
0x 40000	—	(NOTE 1)	UNUSED	—	—	256K
0x 80000	—	MCS	DPDRAM	READ/WRITE	16	128K/PAGE
0x A0000	—	MCS	NOT USED	—	—	128K
0x C0000	0x 0400	PS0	DEMON	—	—	128
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	1
0x C0082	0x 0484	PS1	PCSR BITS 7—0	READ	8	1
0x C0086	0x 0486	PS1	RESERVED			
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 2)	1	—
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 2)	1	—
0x C008A	0x 048A	PS1	PCSR BIT 2 (INT2)	(NOTE 2)	1	—
0x C008B	0x 048B	PS1	PCSR BIT 3 (INT3)	(NOTE 2)	1	—
0x C008C	0x 048C	PS1	PCSR BIT 4 (NOT USED)	(NOTE 3)	1	—
0x C008D	0x 048D	PS1	PCSR BIT 5 (ARDY)	(NOTE 3)	1	—
0x C008E	0x 048E	PS1	PCSR BIT 6 (BAF)	(NOTE 3)	1	—
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT1[0])	(NOTE 2)	1	—
0x C0100	0x 0500	PS2	NOT USED	—	—	128
0x C0180	0x 0580	PS3	NOT USED	—	—	128
0x C0200	0x 0600	PS4	DUART 0 AND 1	—	—	128
0x C0280	0x 0680	PS5	DUART 2 AND 3	—	—	128
0x C0300	0x 0700	PS6	PARALLEL PORT	—	—	128
0x C0400	0x FF00	80186	80186 CONTROL BLOCK	—	16	256
0x C0420	0x FF20	80186	INTERRUPT CONTROL	—	16	32
0x C0450	0x FF50	80186	TIMER 0 CONTROL	—	16	8
0x C0458	0x FF58	80186	TIMER 1 CONTROL	—	16	8
0x C0460	0x FF60	80186	TIMER 2 CONTROL	—	16	6
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL	—	16	10
0x C04C0	0x FFC0	80186	DMA 0 CONTROL	—	16	12
0x C04D0	0x FFD0	80186	DMA 1 CONTROL	—	16	12
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	—	16	2
0x F0000	—	UCS	ROM	READ	16	63.9K
(NOTE 4)	—	UCS	DEMON ROM	READ	16	128

NOTES:

1. External address decoding is required to select addresses in the 0x 40000 — 0x 7FFFF range.
2. Bit is cleared [0] (reset) by 80186 Microprocessor access.
3. Bit is cleared [0] (reset) by 80186 Microprocessor access unless "dummy" read of BAF is pending.
4. The application links ROM firmware with a DEMON function that is limited to 128 bytes.

LEGEND:

ARDY	Asynchronous Data Ready
BAF	Bus Abort Feature
DMA	Direct Memory Access
DPDRAM	Dual Port Dynamic Random Access Memory
LCS	Lower RAM Chip Select
MCS	Memory Chip Select
NRZI	Nonreturn to Zero Insertion
PCSR	Peripheral Control and Status Register
PS	Peripheral Select
UCS	Upper RAM Chip Select

Figure 3-54: CM195A NI Card Address Map

ID/Vector Register

The NI card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 8-bit NI card ID code. Later the register contains an 8-bit interrupt vector. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the NI card ID code to the ID/Vector Register and waits. The NI card ID code is 0x 02. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register are a unique 16-bit ID code of the card.

Page Register

The NI card uses a 24-bit I/O address to do system board main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

Peripheral Control and Status Register

The NI card contains an 8-bit Peripheral Control and Status Register (PCSR) which is addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access.

NI PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT1[0] and is asserted by the NI firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is used for the BAF. Bit 6 is set [1] by hardware when the 80186 Microprocessor is delayed in accessing main memory and must be cleared by firmware. During normal operation, PCSR6 is cleared by the 80186 Microprocessor addressing PCSR6 unless a "dummy" read is pending. The 80186 Microprocessor cannot access DPDRAM when PCSR6 is set [1]. Addressing PCSR6 (0x 048E) clears (negates) the bit.
5	Used to control Asynchronous Data Ready (ARDY[1]). Addressing PCSR5 asserts ELPBK[0] signal.
4	PCSR4 is reserved for future NI development. Addressing PCS4[1] (0x 48C) clears (negates) the bit.
3	PCSR3 is not used by the NI card. Addressing PCSR3 (0x 048B) clears (resets) the bit.
2	PCSR2 is not used by the NI card. Addressing PCSR3 (0x 048A) clears (resets) the bit.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the NI PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the NI firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by a system board CPU access of the NI ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the NI firmware.

Local RAM

The NI card contains 32K bytes of Static Random Access Memory (SRAM) configured as 16K by 16 bits. The DRAM is accessed via the Low Memory Chip Select (LCS0) from 80186 Microprocessor and address bits 12—00. Note that 256K bytes of RAM address space is reserved. The 32K bytes of RAM is used for intermediate data storage of the data being transmitted/received to/from the network.

Local ROM

Firmware for the 80186 Microprocessor is stored in the ROM. The NI card ROM contains 16K bytes configured as 8K by 16 bits. The ROM is accessed via the Upper Memory Chip Select (UCS[0]) and address bits 14—00.

Network Interface

The AT&T 3BNET is an Ethernet compatible, local area network. Data is transferred over the network by attaching a destination identification to the data to be transferred. The **nisend** command is used to attach a destination code and file name to the data to be transferred. The NI firmware handles the transfer of the data between the 3B2 computer main memory and the Network Interface Local RAM. The data to be transferred is divided into packets of 1024 bytes for transfer over the network. The Ethernet Controller autonomously reads the data from local RAM, converts the data to serial stream, and transmits the stream over the network. If collisions are detected, the information packet is retransmitted automatically. The receiving system acknowledges the receipt of the data.

Ethernet Controller Circuit

The Network Interface is an 82586 Ethernet Controller that manages the process of transmitting and receiving data over the network. The primary functions of the controller are as follows:

- Decode the serial data
- Check for data integrity
- Convert serial data into parallel data format
- Store parallel data in the local RAM
- Save and report networking errors for the node.

The Network Interface connects to the network via a coaxial drop cable and a transceiver circuit. The interface between the Network Interface and the transceiver circuit consists of the following signals.

Receive Pair
: A differential signal that is active when any data is received.

Transmit Pair
: A differential signal that is active when any data is transmitted.

Collision Presence Pair
: A differential signal that is active while a collision is in progress.

Power Pair
: The transceiver is powered by +12 volt DC supplied by the 3B2 computer.

CM195A Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM195A NI Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are NI software defined values. As such, the rq_size and cq_size values may differ between versions of NI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0002
DEVICE NAME (dev_name)	NI
REQUEST QUEUE SIZE (rq_size)	0x 0A
COMPLETION QUEUE SIZE (cq_size)	0x 19
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

3BNET Characteristics

Coaxial Media Cable

The maximum end-to-end length of the media cable without using repeaters is 500 meters. The data transmission rate over the media cable is 10 megabits per second.

Terminators The media cable is terminated at each end with 50-ohm resistors to prevent signal reflection.

Transceivers Transceivers provide nodal tap into the media cable and provide electrical isolation for transmitting and receiving signals. These units must be installed at designated points on the media cable to maintain standing wave specifications. Transceivers are powered by 12 volt DC supplied from the NI card via the drop cable.

Drop Cable The drop cable interconnects the transceiver and the NI card. The maximum length of this cable is 50 meters.

Ethernet Data Packet Format

The format of an Ethernet Data Packet is as follows:

FIELD	PREAMBLE	DESTINATION ADDRESS	SOURCE ADDRESS	TYPE	DATA	CRC
SIZE	64 BITS	48 BITS	48 BITS	16 BITS	46 TO 1500 BYTES	32 BITS

PREAMBLE The Preamble is a 64-bit field of alternating 1's and 0's, ending with two consecutive 1's. This field synchronizes the receiving circuits to the incoming data packet.

DESTINATION ADDRESS
The 48-bit Destination Address field is the nodal address to which the data is being transmitted.

SOURCE ADDRESS
The 48-bit Source Address field is the nodal address from which the data is being transmitted.

TYPE The 16-bit Type field is used for a high-level data protocol.

DATA The Data field is the data to be sent over the network and is from 46 to 1500 bytes in length.

CRC The 32-bit Cyclic Redundancy Check (CRC) field is calculated on all of the other fields. This field is also called the Frame Check Sequence field.

CM195AA ALARM INTERACE CIRCUIT CARD

General

The CM195AA Alarm Interface Circuit (AIC) Card is part of the Remote Management Package. The AIC card provides the following capabilities:

- Dual console
- System sanity failure detection and alarm generation
- Alarm interface to automatic calling units
- Uninterruptible Power Supply (UPS) and external input connections.

These functions are achieved via hardware resident on the I/O bus. The card contains no "intelligence" as such. Figure 3-55 is a functional block diagram of the AIC card.

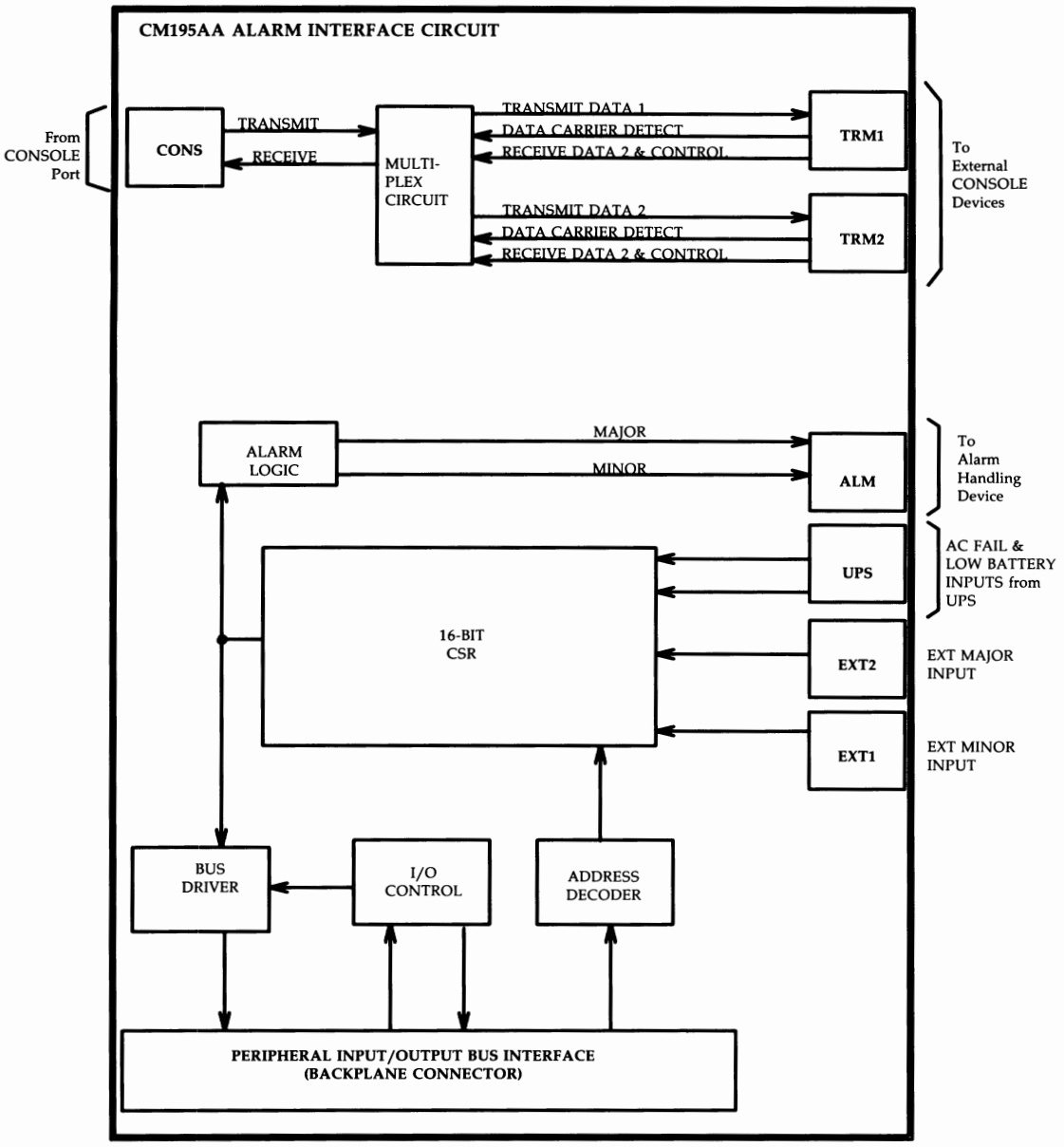


Figure 3-55: CM195AA AIC Card — Functional Block Diagram

I/O Bus Interface

The only operation supported by the AIC hardware is a "read" by the integral CPU. A read operation at a specific address will cause a specific result. The addresses and corresponding results are shown in Figure 3-56.

OFFSET	LIMIT	CSR BIT	RESULT
0X00	0X01	—	READ BOARD ID (ID=0x0101)
0X04	0X05	—	READ 16 BIT AIC STATUS REGISTER
0X20	—	00	SET SWMINOR1 TO CAUSE MINOR ALARM FROM SOFTWARE
0X21	—	00	CLEAR SWMINOR1
0X22	—	01	SET SWMAJOR1 TO CAUSE MAJOR ALARM FROM SOFTWARE
0X23	—	01	CLEAR SWMAJOR1
0X24	—	02	SET SANEN1 TO ENABLE SANITY TIMER
0X25	—	02	CLEAR SANEN1 TO DISABLE SANITY TIMER
0X26	—	03	NO FUNCTION
0X27	—	03	CLEAR SANITY TIMER (PRESENTS A LOGIC 0 ON STATUS REGISTER BIT 03 FOR 127.5 MILLISECONDS)
0X28	—	04	SET INHALRM1 TO INHIBIT ALL ALARMS
0X29	—	04	CLEAR INHALRM1 TO ENABLE ALARMS
0X2A	—	05	SET ACFAIL1 FOR DIAGNOSTIC TEST OF THIS BIT
0X2B	—	05	CLEAR ACFAIL1 TO CLEAR THIS BIT FROM CSR
0X2C	—	06	SET LOWBAT1 FOR DIAGNOSTIC TEST OF THIS BIT
0X2D	—	06	CLEAR LOWBAT1 (CLEARS LOW BATTERY STATUS FROM CSR)
0X2E	—	07	SET EXTTL21 FOR DIAGNOSTIC TEST OF THIS BIT
0X2F	—	07	CLEAR EXTTL21 (CLEARS EXTERNAL MAJOR ALARM FROM CSR)
0X30	—	08	SET EXTTL11 FOR DIAGNOSTIC TEST OF THIS BIT
0X31	—	08	CLEAR EXTTL11 (CLEARS EXTERNAL MINOR ALARM FROM CSR)
0X32	—	09	SET ISANE1 BIT 9 FOR DIAGNOSTIC TEST OF THIS BIT
0X33	—	09	CLEAR INSANE1 INDICATION OF SANITY TIMEOUT FROM CSR
0X34	—	10	SET BIT 10 TO SET TMOUT1 TO 1 AND ASSERT PINT20
0X35	—	10	CLEAR BIT 10 TO CLEAR TMOUT1 ONLY
0X36	—	—	CLEAR PENDING PINT20
0X37	—	—	CAUSE SYSTEM RESET VIA I/O BUS LEAD RQRST0
0X38	—	12	RESERVED
0X39	—	12	RESERVED
0X3A	—	13	RESERVED
0X3B	—	13	RESERVED
0X3C	—	14	RESERVED
0X3D	—	14	RESERVED
0X3E	—	15	TRM1 AND TRM2 DTRT IS CONTROLLED BY 3B2 UART
0X3F	—	15	TRM1 AND TRM2 DTR IS FORCED ACTIVE (POWER UP DEFAULT STATE)

Figure 3-56: CM195AA AIC Card Address Spectrum

ID data is supplied to the bus when the AIC card is read (addresses 0X01 and 0X02). For addresses 0X04 and 0X05, the AIC Status Register information is passed to the bus. The following table contains the AIC Status Register bit definitions.

BIT	NAME	DESCRIPTION
15	RESV151	WHEN 0, AIC FORCES DTR ACTIVE ON TRM1 & TRM2 WHEN 1, DTR IS CONTROLLED BY THE 3B2 UART
14	—	RESERVED FOR FUTURE APPLICATIONS
13	—	RESERVED FOR FUTURE APPLICATIONS
12	—	RESERVED FOR FUTURE APPLICATIONS
11	—	RESERVED FOR FUTURE APPLICATIONS
10	TMOUT1	WHEN SET, AN INTERRUPT ON FIRST TIMEOUT HAD OCCURRED
09	INSANE1	WHEN SET, INDICATES SANITY TIMER HAS FIRED SECOND TIME
08	EXTTL11	WHEN SET, INDICATES MINOR ALARM ON TTL INPUT 1
07	EXTTL21	WHEN SET, INDICATES MAJOR ALARM ON TTL INPUT 2
06	LOWBAT1	WHEN SET TO 1, INDICATES CLOSURE HAD OCCURRED ON EXTERNAL "LOW BATTERY" INPUT FROM UPS
05	ACFAIL1	WHEN SET TO 1, INDICATES CLOSURE HAD OCCURRED ON EXTERNAL "AC FAILURE" INPUT
04	INHALRM1	1 INDICATES ALL ALARM OUTPUTS INHIBITED
03	CLRTMRS0	WILL BE ACTIVE 0 FOR 127.5 MILLISECONDS FOLLOWING A CLEAR SANITY TIMER COMMAND
02	SANEN1	WHEN SET TO 1, SANITY TIMER ENABLED AND RUNNING WHEN CLEARED, THE TIMER IS DISABLED
01	SWMAJOR1	1 INDICATES SOFTWARE HAD SET MAJOR ALARM
00	SWMINOR1	1 INDICATES SOFTWARE HAD SET MINOR ALARM

Dual Console

The dual console feature is basically a straight hardware type arrangement. The CONS port on the AIC card is connected to the CONSOLE port of the computer. The leads are reversed on the CONS port to allow the use of a standard 8-pin modular phone cord between the CONSOLE and CONS port.

The Data Carrier Detect (DCD) lines go high to determine which one of the TRM ports has data flow. For example, when DCD1 is high, only data from TRM1 is allowed through the multiplexer.

The TRM1 port has priority over the TRM2 port. That is, if both are ON (DCD high), TRM1 data will flow through the multiplexer and TRM2 will only mirror data received by TRM1. The following table shows the remote console priorities based on DCD condition.

STATE OF DCD		SYSTEM BOARD ACTION			
		TRM1		TRM2	
TRM1	TRM2	TRANSMIT	RECEIVE	TRANSMIT	RECEIVE
OFF	OFF	NO	NO	NO	YES
ON	OFF	YES	YES	NO	NO
OFF	ON	NO	NO	YES	YES
ON	ON	YES	YES	YES	NO

System Failure Detection and Alarm Generation

All alarm stimuli are gated into one of the two alarm outputs from the AIC card. Ultimately, one of these alarm stimuli will induce current flow in one of the opto-coupler devices. One coupler is dedicated to providing closure for major alarms, the other is for minor alarms.

Major alarms are caused by software command, second sanity time-out, AC failure and low battery condition, or an external input which is user defined. Minor alarms are caused by software command, AC failure indication, or external input which is user defined. The following table defines the types of alarm stimuli and the resulting action.

ALARM STIMULUS	ACTION TAKEN
SW SET SWMAJOR1	Major alarm sent to autodialer and recorded in Status Register. No other machine action.
SW SET SWMINOR1	Minor alarm sent to autodialer and recorded in Status Register. No other machine action.
HW SANITY TIMEOUT1	PINT20 asserted over I/O bus and recorded separately in AIC CSR bit 10. No alarm or other machine action.
HW SANITY TIMEOUT2	Major alarm sent to autodialer, INSANE1 latched in AIC CSR, RQRST0 asserted (not latched) over I/O bus to bring system down (and back up under software option).
3B2 DC POWER FAILURE	Major alarm sent to autodialer. No other machine action. CSR invalid.
COMMERCIAL AC FAILURE AT 3B2 INPUT (NO UPS INSTALLED)	Same as 3B2 DC power failure.
COMMERCIAL AC FAILURE AT 3B2 INPUT: UPS WITH NO AC CLOSURE ABILITY INSTALLED	No AIC hardware detection of AC loss. No action taken.
COMMERCIAL AC FAILURE AT 3B2 INPUT: UPS WITH AC FAILURE DETECTION INSTALLED	ACFAIL1 latched in CSR. Minor alarm sent to autodialer.
EXTENDED AC FAILURE AT 3B2 INPUT SUCH THAT BATTERIES BECOME LOW ON A UPS WHICH HAS AC LOSS AND LOW BATTERY DETECTION AND CLOSURES	UPS provides closure on Low Battery lines which is logged in AIC CSR bit LOWBAT1. If ACFAIL1 is also set, PINT20 is asserted over the I/O bus to bring the system down and a major alarm is sent. If ACFAIL1 is not sent, only the Low Battery CSR bit is latched.
LOW BATTERY CLOSURE ONLY, FROM UPS WITH LOW BATTERY DETECTION	LOWBAT1 latched in CSR. No other machine action unless ACFAIL1 is active. (See above)

External Interface Specification

The available ports for open-ended development are the ports labeled ALM, UPS, EXT2, and EXT1.

Each of these ports is a 6-pin (4 equipped) modular, plug-type connector. The input ports are designed to support Transistor-Transistor-Logic (TTL) driven inputs or relay closure type inputs. Power should be removed from the 3B2 computer before a connection is made to any of these ports. Since the ports are sensitive to state changes, connecting cables while the power is present can cause erratic system behavior, even system panics.

The following table shows the interface specifications for the external interface ports.

		PORT LABELS			
		ALM	**UPS**	**EXT2**	**EXT1**
Direction		Output	Input	Input	Input
Current		Sink 35ma max	Source 2ma max	Source 2ma max	Source 2ma max
Voltage		VCE: 1.0v at 35ma 0.8v at 10ma 0.7v at 5ma VCE: 30v max VEC: 7.0v max	VIL = 0.8v max VIH = 2.0v min VIH = 7.0v max*	VIL = 0.8v max VIH = 2.0v min VIH = 7.0v max*	VIL = 0.8v max VIH = 2.0v min VIH = 7.0v max*
Active State		Conducts	Logic Low "0"	Logic Low "0"	Logic Low "0"
Signal Duration		127ms min	20ns min (low)	20ns min (low)	20ns min (low)
Pin† Signals	P1	Darlington Emitter‡ (MJOUT1)	Ground	Ground§	Ground¶
	P2	Darlington Collector‡ (MAJORIN1)	AC FAILURE (ACFSET0)	EXTERNAL TTL§ (EXT2IN0)	EXTERNAL TTL¶ (EXT1IN0)
	P3	Darlington Emitter** (MINOUT1)	Ground	Ground	Ground
	P4	Darlington Collector** (MININ1)	LOWBAT (LOWBSET0)	NC	NC

LEGEND: NC — No Connection.
* — Absolute maximum rating over a free-air temperature range of 0 to 70 degrees C.
† — P1 is on the right and P4 is on the left of each modular jack, referenced with the component side up and the face plate toward you.
‡ — Major alarm outputs (intended for activating an External Alarm Processing Unit).
§ — Closure across these pins results in major alarm (accepts either TTL or Closure).
¶ — Closure across these pins results in minor alarm (accepts either TTL or Closure).
** — Minor alarm outputs (intended for activating an External Alarm Processing Unit).

CM195AA Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM195AA Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0101
DEVICE NAME (dev_name)	AIC
REQUEST QUEUE SIZE (rq_size)	0x 00
COMPLETION QUEUE SIZE (cq_size)	0x 00
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	0
CONSOLE CAPABILITY (cons_cap)	1
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM195AC/CM195AD "DATAKIT" VCS INTERFACE CARD

General

The Datakit Virtual Circuit Switch (VCS) Interface card provides a high speed fiber optic connection from a 3B2 host computer to a Datakit VCS. The connection is made through a combination of the CM195AD Fiber Interface Board (FIB) and the CM195AC Datakit VCS Processing Unit Card. Both cards are standard 3B2 computer feature cards interconnected by two 40-conductor ribbon cable.

The CM195AC Card provides the interface to the 3B2 computer I/O bus and implements the Level C functions associated with Universal Fiber Trunk Interface (UFTI) protocol. The CM195AD Card implements the point-to-point link functions over the optical fiber. A block diagram of the add-on is shown in Figure 3-57.

The CM195AC Datakit VCS Processing Unit Card hardware consists of five distinct pieces:

- INTEL 80186 Microprocessor
- Input/Output (I/O) Bus Control
- Nonvolatile Memory
- Volatile Memory
- External Interface.

These components are under the control of the INTEL 80186 Microprocessor, unless another intelligent source wishes to make use of the processing unit memory by asserting a "hold" request.

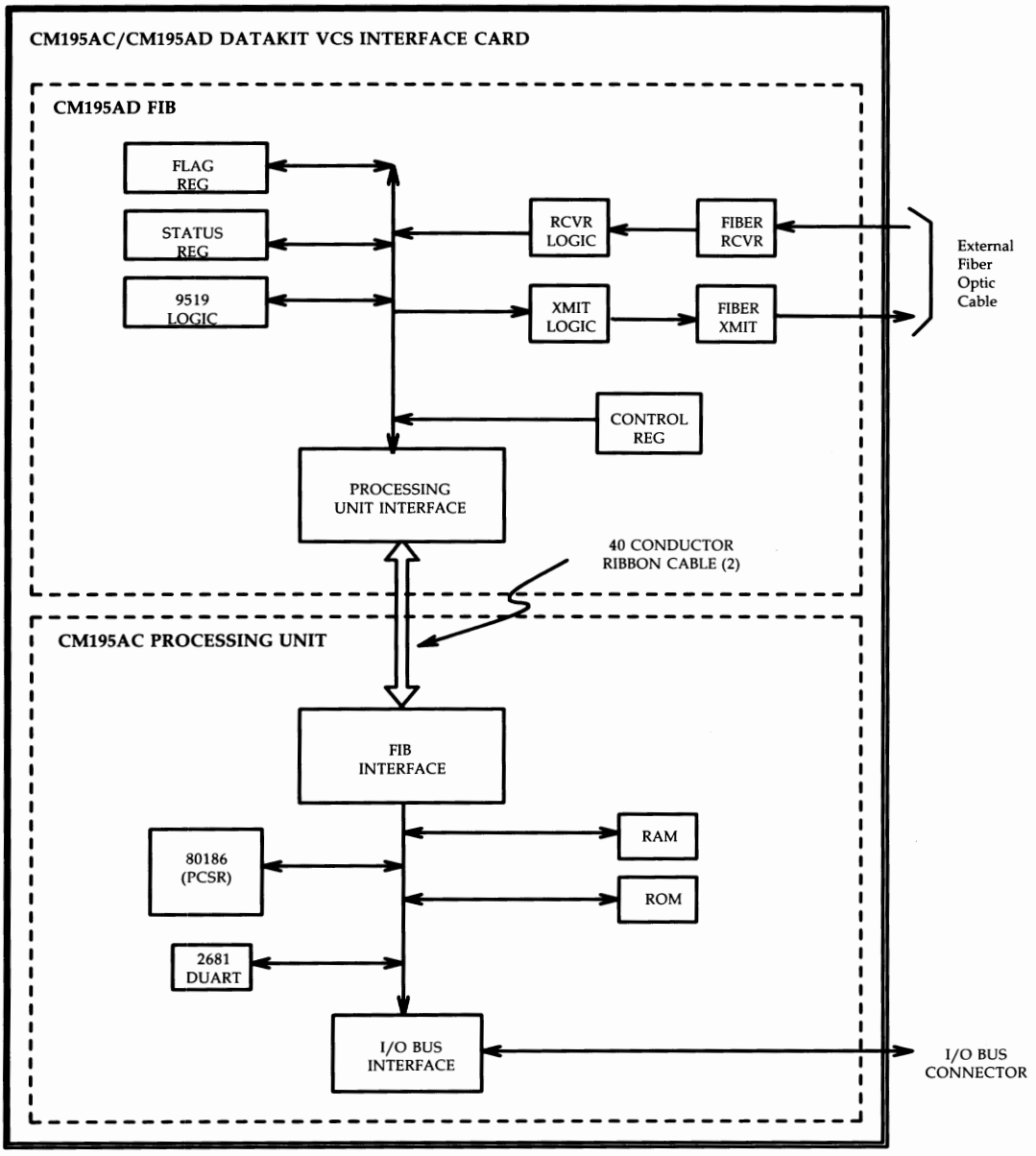


Figure 3-57: CM195AC/CM195AD Datakit VCS Interface Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the Datakit VCS Interface card is provided by an INTEL 80186, 16-bit microprocessor operating at 16 MHz. Figure 3-58 shows the CM195AC Datakit VCS Processing Unit Card address map.

CM195AC/CM195AD CARD ADDRESS MAP

MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	RAM (VECTOR TABLE)	READ/WRITE	16	256K
0x 80000	—	MCS0	DPDRAM	READ/WRITE	16	128K
0x 90000	—	MCS1	DPDRAM	READ/WRITE	16	128K
0x A0000	—	MCS2	DPDRAM	READ/WRITE	16	128K
0x B0000	—	MCS3	DPDRAM	READ/WRITE	16	128K
0x C0000	—	UCS	ROM	READ/WRITE	16	32K
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	1
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	1
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	—
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	—
0x C008A	0x 048A	PS1	PCSR BIT 2 (NOT USED)	—	1	—
0x C008B	0x 048B	PS1	PCSR BIT 3 (NOT USED)	—	1	—
0x C008C	0x 048C	PS1	PCSR BIT 4 (NOT USED)	—	1	—
0x C008D	0x 048D	PS1	PCSR BIT 5 (ARDY)	(NOTE 2)	1	—
0x C008E	0x 048E	PS1	PCSR BIT 6 (BAF)	(NOTE 2)	1	—
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT1[0])	(NOTE 1)	1	—
0x C0100	0x 0500	PS2	CLEAR NMI REQUEST	—	—	—
0x C0102	0x 0502	PS2	CLEAR INT0 REQUEST	—	—	—
0x C0104	0x 0504	PS2	CLEAR INT1 REQUEST	—	—	—
0x C0106	0x 0506	PS2	CLEAR INT2 REQUEST	—	—	—
0x C0180	0x 0580	PS3	CM195AD INTERFACE	—	—	—
0x C0200	0x 0600	PS4	CM195AD INTERFACE	READ/WRITE	8	16
0x C0280	0x 0680	PS5	CM195AD INTERFACE	READ/WRITE	8	16
0x C0300	0x 0700	PS6	CM195AD INTERFACE	READ/WRITE	8	4
0x C0400	0x FF00	80186	80186 CONTROL BLOCK	—	16	—
0x C0420	0x FF20	80186	INTERRUPT CONTROL	READ/WRITE	16	—
0x C0450	0x FF50	80186	TIMER 0 CONTROL	—	16	—
0x C0458	0x FF58	80186	TIMER 1 CONTROL	—	16	—
0x C0460	0x FF60	80186	TIMER 2 CONTROL	—	16	—
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL	—	16	—
0x C04C0	0x FFC0	80186	DMA 0 CONTROL	—	16	—
0x C04D0	0x FFD0	80186	DMA 1 CONTROL	—	16	—
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	—	16	—

NOTES:

1. Bit is cleared by 80186 Microprocessor access.
2. Bit is set to 0 by 80186 Microprocessor access unless a "dummy" read is pending.

LEGEND:

ARDY	Asynchronous Data Ready
BAF	Bus Abort Feature
DMA	Direct Memory Access
DPDRAM	Dual Port Dynamic Random Access Memory
LCS	Lower Memory Chip Select
MCS	Memory Chip Select
NMI	Nonmaskable Interrupt
PCSR	Peripheral Control and Status Register
PS	Peripheral Select
UCS	Upper RAM Chip Select

Figure 3-58: CM195AC Processing Unit Card Address Map

Input/Output Bus Interface

The bus interface provides the following functions:

- I/O Control—Provides the functionality of recognizing, controlling, and responding to the I/O bus states. The actions are initiated by the 3B2 CPU or the 80186 Microprocessor.
- Address Drivers—Provides 24 bits of address information over the I/O bus.
  - 17 bits of bus address directly from the 80186 Microprocessor
  - 7 bits as Page Register.
- Data Transceivers—Holds ID information and Interrupt vectors as well as buffering bidirectional data to and from the I/O bus. There is a byte swap performed with processing unit data bits 0 through 7 being mapped to I/O data bits 8 through 15 and data bits 8 through 15 being mapped to I/O data bits 0 through 7.
- 3B2 Computer Invoked Interrupts—The 3B2 computer may cause interrupts on the processing unit by accessing particular locations (location 1) in the processing unit I/O space.

Nonvolatile Memory

The processing unit supports up to 32K bytes of Erasable Programmable Read Only Memory (EPROM) in the form of two INTEL 27128 PROMs.

Volatile Memory

The processing unit is equipped with 256K bytes of Static Random Access Memory (SRAM). This memory is in the form of two 128K by 16-bit SRAM modules.

External Interface

The external interface is handled through the FIB. The signals for the FIB are passed through the two 40-conductor ribbon cables. These signals are grouped as follows:

- Address lines
- Data lines
- Control lines
- Timer Input/Output.

Address Signals

The processing unit provides all 20 address lines to the FIB. These lines are buffered to allow driving from an external interface. The control of the lines is determined by the HOLDA1 signal. A low (0) indicates that the processing unit is driving the address bus and a high (1) indicates that the external board is generating the address information.

Data Lines

The processing unit provides all 16 data bits. The direction control of these signals is driven by the IDT1R0 signal, which is driven by the processing unit or the external board.

Control Lines

The processing unit uses 28 control signals. They can be subgrouped as bus control, external chip selects, and externally generated interrupts. Bus control signals may come from the INTEL 80186 Microprocessor, the external interface, or both. The following table shows the control lines and their purpose.

SIGNAL	GROUP	PURPOSE
PIHOLD1	Bus	Asserted to request the 80186 relinquish the bus (external).
PIDRQ11	Bus	Request a DMA cycle from DMA Channel 1 (external).
PIURDY1	Bus	External device has transferred data (external).
PITEST1	Bus	Suspends execution of a wait instruction (external).
BRDPRES0	Bus	When LOW, indicates an external board is present (external).
PIHLDA1	Bus	Indicates the 80186 has yielded the bus.
PILOCK0	Bus	Used to acquire sole control of a resource on a multibus.
PICLKOUT1	Bus	8-MHz system clock.
PIRST1	Bus	Reset from CPU.
PIIS[0-2]0	Bus	Indicates bus cycle type.
PIRAMACK0	Bus	RAM has completed a cycle.
PIALE1	Bus	Address latch enable (valid on address leads).
PIWR0	Bus	Data valid for a write operation.
PIRD0	Bus	Data being strobed for a read operation.
PIBHE0	Bus	Used to indicate a word/byte transfer in conjunction with PIADR001.
PIDT1R0	Bus	Indicates data flow direction.
PIDEN0	Bus	Indicates that data may be placed on the bus.
PIPCS[2-5]0	Chip Select	I/O chip select lines.
PIMCS[23]0	Chip Select	Memory chip selects.
PINMI1	External Interrupt	Used by an external board to generate a nonmaskable interrupt.
PIINTRA1	External Interrupt	Used by an external board to raise maskable interrupt 2 on the 80186.
PIINTRB1	External Interrupt	Used by an external board to raise maskable interrupt 3 on the 80186.

Timer Input/Output

There are four timer inputs/outputs used to provide timer/counter capabilities to an external board. Two timer inputs (PITMRIN0 and PITMRIN1) and two timer outputs (PITMR00 and PITMR10) are available and connected to timers 0 and 1 on the 80186 Microprocessor.

CM195AC/CM195AD Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for the CM195AC/CM195AD Cards. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0308
DEVICE NAME (dev_name)	DKIT
REQUEST QUEUE SIZE (rq_size)	0x 0a
COMPLETION QUEUE SIZE (cq_size)	0x 19
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM195AE GPSC CARD

General

The CM195AE General Purpose Synchronous Controller (GPSC) Card provides two physical interfaces for synchronous data transmission. The card is capable of providing simultaneous full-duplex, full-occupancy data transmission at rates up to 64K bits per second. The output connectors contain the required signals to support a variety of industry standard electrical interfaces. Separate cables provide the electrical connections for the desired interface (see Appendix B). Figure 3-59 shows the functional block diagram of a CM195AE GPSC Card.

GPSC Card Features

The major components of the GPSC card are listed below.

- An INTEL 80186 Microprocessor
- Bus interface circuitry
- 768K bytes of Dynamic Random Access Memory (DRAM)
- Up to 32K bytes of Erasable Programmable Read Only Memory (EPROM)
- Dual Port Arbiter/Controller and Support Logic.

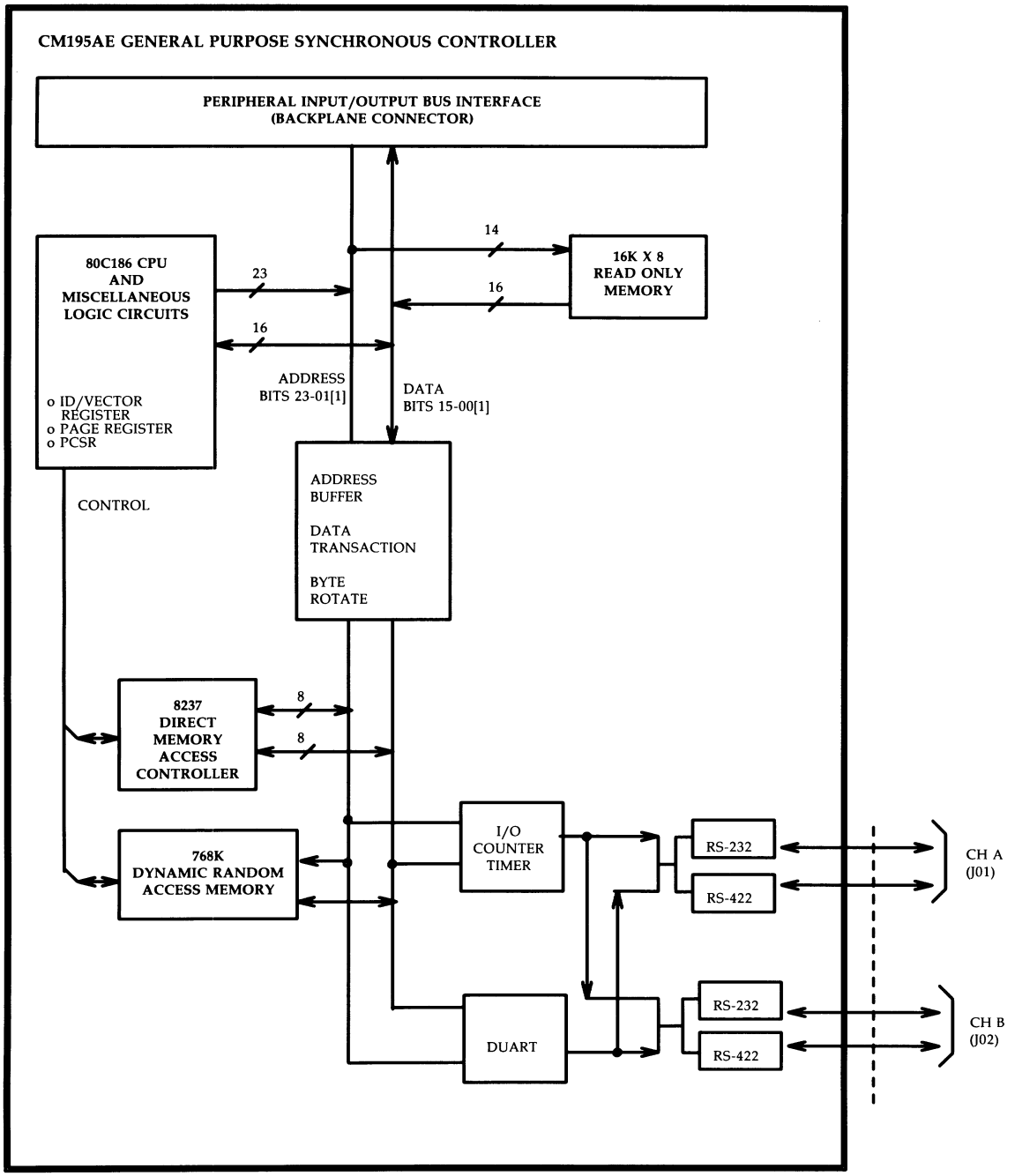


Figure 3-59: CM195AE GPSC Card—Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the GPSC card is provided by an INTEL 80C186, 16-bit microprocessor operating at 16 MHz. Some of the microprocessor features used for the GPSC card are described in the following paragraphs. Figure 3-60 shows the GPSC card address map.

DMA Channels

Four independent 4-bit Page Registers, one for each channel, are provided to allow access to the entire DRAM address range. All four are used by supporting both transmit and receive on each port. Note that for Direct Memory Access (DMA), DRAM is partitioned into 64-kilobyte segments and that a single DMA job cannot cross the segment boundaries.

Channel 0 and 1 are Receive Channel A and Transmit Channel A, respectively. Channel 2 and 3 are Receive Channel B and Transmit Channel B, respectively.

Interrupt Controller

The internal Interrupt Controller of the 80C186 Microprocessor is programmed to accept five separate interrupts: INT3 through INT0, and NMI. Interrupts INT0 and INT1 are reserved for common I/O firmware use. INT2 is dedicated to the 82C37A DMA Controller. INT3 is a combined 85C30/8536 interrupt. Nonmaskable Interrupt (NMI) is used by the common I/O firmware to control the Bus Abort Feature (BAF).

Internal Timers

Timer 0 is a DRAM refresh timer. Timer 1 controls the BAF. Timer 2 is used as a general purpose timer.

The 8536 Counter/Timer Parallel I/O (CT/PIO) device contains three independent 16-bit counter/timers. Timers 1 and 2 are the clock tick counters for Channel B transmit clock and Channel A transmit clock, respectively. Timer 3 is the zero counter for Channel A.

Memory and Peripheral Chip Selects

The memory and peripheral chip selects are programmed by the GPSC firmware to provide chip selects in the 80C186 Microprocessor memory map (Figure 3-60).

GPSC CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	GPSC LOCAL DRAM	READ/WRITE	16	256K
0x 40000	—	LCS	GPSC LOCAL DRAM	READ/WRITE	16	512K
0x C0000	—	MCS0	3B2 MAIN MEMORY	READ/WRITE	16	32K
0x C8000	—	MCS1	3B2 MAIN MEMORY	READ/WRITE	16	32K
0x D0000	—	MCS2	3B2 MAIN MEMORY	READ/WRITE	16	32K
0x D8000	—	MCS3	3B2 MAIN MEMORY	READ/WRITE	16	32K
0x E0000	0x 0400	PCS0	NOT USED (DEBUGGING ONLY)	READ/WRITE	8	16
0x E0080	0x 0480	PCS1	ID/VECTOR REGISTER	WRITE	16	2
0x E0082	0x 0482	PCS1	CIO PAGE REGISTER	WRITE	8	1
0x E0084	0x 0484	PCS1	PCSR[7-0]	READ	8	1
0x E0086	0x 0486	PCS1	RESERVED			
0x E0088	0x 0488	PCS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	
0x E0089	0x 0489	PCS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	
0x E008A	0x 048A	PCS1	PCSR BIT 2 (INT2)	(NOTE 1)	1	
0x E008B	0x 048B	PCS1	PCSR BIT 3 (NMI)	(NOTE 1)	1	
0x E008C	0x 048C	PCS1	PCSR BIT 4 (BAF-DMA BLOCK)		1	
0x E008D	0x 048D	PCS1	PCSR BIT 5 (RESERVED)		1	
0x E008E	0x 048E	PCS1	PCSR BIT 6 (BAF-ABORT)	(NOTE 1)	1	
0x E008F	0x 048F	PCS1	PCSR BIT 7 (PINT00)	(NOTE 1)	1	
0x E0100	0x 0500	PCS2	ADMA PAGE REGISTER	WRITE	16	2
0x E0180	0x 0580	PCS3	APPL. CONTROL REGISTER	READ/WRITE	16	2
0x E0200	0x 0600	PCS4	ADMAC	READ/WRITE	8	32
0x E0280	0x 0680	PCS5	DUART CHANNEL B (85C30)	READ/WRITE	8	1
0x E0281	0x 0681	PCS5	DUART CHANNEL A (85C30)	READ/WRITE	8	1
0x E02C0	0x 06C0	PCS5	8536	READ/WRITE	8	4
0x E0300	0x 0700	PCS6	UNDEFINED			
—	0x FF00	80C186	80186 CONTROL BLOCK (NOTE 2)	READ/WRITE	16	256
0x E0600	—	80C186	RELOCATED CTL BLOCK	READ/WRITE	16	256
0x F8000	—	UCS	EPROM	READ	16	32K

NOTES:

1. Bit is cleared by 80186 Microprocessor access.
2. After a reset, the 80C186 control block is located at I/O address 0x0FF00.

LEGEND:

ADMAC	Application Direct Memory Access Controller
BAF	Bus Abort Feature
DMA	Direct Memory Access
LCS	Lower RAM Chip Select
MCS	Memory Chip Select
PCS	Peripheral Chip Select
PCSR	Peripheral Control and Status Register
UCS	Upper RAM Chip Select

Figure 3-60: CM195AE GPSC Card Address Map

Application Control Register

The Application Control Register (ACR) bits are defined in the following table. All GPSC card resets clear ALL bits in this register to logical "0."

BIT	SIGNAL	FUNCTION
0	DIVA00[1]	Port A Clock Division
1	DIVA01[1]	(Note 1)
2	TCKOUTA[0]	Tx Clock Out Enable Port A Write "0" to enable output.
3	NEWSIGA[0]	Port A New Signal
4	DIVB00[1]	Port B Clock Division
5	DIVB01[1]	(Note 1)
6	TCKOUTB[0]	Tx Clock Out Enable Port B Write "0" to enable output.
7	NEWSIGB[0]	Port B New Signal
8	EECS[1]	EEPROM Chip Select (Note 2)
9	EECLK[1]	EEPROM Serial Clock
10	EEDIN[1]	Serial Data Input To EEPROM
11	EEDOUT[1]	Serial Data Output From EEPROM
12	TCLKINA[0]	Transmit Clock Input Enable (CH A) Write "0" to enable clock input.
13	TCLKINB[0]	Transmit Clock Input Enable (CH B) Write "0" to enable clock input.
14	FAIL[1]	PFAIL—Activates PFAIL0
15	—	Unassigned

NOTES:

1. Transmit clock division is required in some instances. The transmit clock division is designated as follows:

DIVx01	DIVx00	
0	0	No Division
0	1	Clock divided by 16 before output
1	0	Clock divided by 32 before output
1	1	Undefined

2. Timing of EEPROM accesses are controlled by software.

ID/Vector Register

The GPSC card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit GPSC card ID code. The GPSC card ID code is 0x 0104. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal.

Page Register

The GPSC card uses a 24-bit address to do main memory operations. The lower 17 bits are provided by the 80C186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80C186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482.

Peripheral Control and Status Register

The GPSC card contains an 8-bit Peripheral Control and Status Register (PCSR) addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80C186 Microprocessor read or write access except for PCSR6 that is controlled by the Bus Abort Feature (BAF).

GPSC PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT0[0] and is asserted by the GPSC firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is used for the BAF. Bit 6 is set by hardware when the 80C186 Microprocessor is delayed in accessing main memory and must be cleared by firmware. During normal operation, PCSR6 is cleared by the 80C186 Microprocessor addressing PCSR6 unless a "dummy" read is pending. Addressing PCSR6 (0x 048E) clears (negates) the bit.
5	**RESERVED**: A "1" indicates BAF occurred during DMA; a "0" indicates BAF occurred during PIO.
4	**BAF OCCURRED AND DMA BLOCKED**: A BAF has occurred and the DMA has been blocked from further use.
3	**NONMASKABLE INTERRUPT**: This bit indicates that the GPSC received a peripheral fault during a DMA transfer or a fault from the debugger. Bit 3 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 048B.
2	**CLEAR INT2—EOP**: This 80C186 Microprocessor interrupt is set by the 8274 Dual Channel Communications Chip. Bit 2 is cleared during the interrupt service routine by an access of the 80C186 Microprocessor address 0x 048A.
1	**CLEAR INT1**: This 80C186 Microprocessor interrupt is set by a system board CPU access of the GPSC PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80C186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the GPSC firmware.
0	**CLEAR INT0**: This 80C186 Microprocessor interrupt is set by an access of the GPSC ID/Vector register (except on an interrupt acknowledge cycle). Bit 0 is cleared during the interrupt service routine by an access of the 80C186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The GPSC card contains 768K bytes of Dynamic Random Access Memory (DRAM) composed of eight 256K by 4-bit chips.

Local ROM

Firmware for the 80C186 Microprocessor is stored in the Read Only Memory (ROM). The GPSC card ROM contains either 16K bytes configured as 8K by 16 bits or 32K bytes configured as 16K by 16 bits.

CM195AE Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM195AE GPSC Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI).

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0104
DEVICE NAME (dev_name)	GPSC
REQUEST QUEUE SIZE (rq_size)	0x 14
COMPLETION QUEUE SIZE (cq_size)	0x 14
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM195AY EPORTS CARD

General

The CM195AY Enhanced Peripheral Port Controller (EPORTS) Card provides eight separate, asynchronous serial ports (RS-232C). Functionally, the EPORTS card consists of the Common Input/Output (CIO) circuits, and four Serial Communication Controllers (SCCs). The Serial Communication Controllers function as Dual Universal Asynchronous Receiver/Transmitter (DUART) circuits. The eight asynchronous serial ports are identified as subdevices. DUART 0 (SCC 0) supports subdevices SD0 and SD1; DUART 1 (SCC 1) supports subdevices SD2 and SD3. DUART 2 (SCC 2) supports subdevices SD4 and SD5; DUART 3 (SCC 3) supports subdevices SD6 and SD7. Drivers and receiver circuits are used to interface the DUARTs to MODEMS and/or data terminals (RS-232C). Figure 3-61 is a functional block diagram of the CM195Y EPORTS Card.

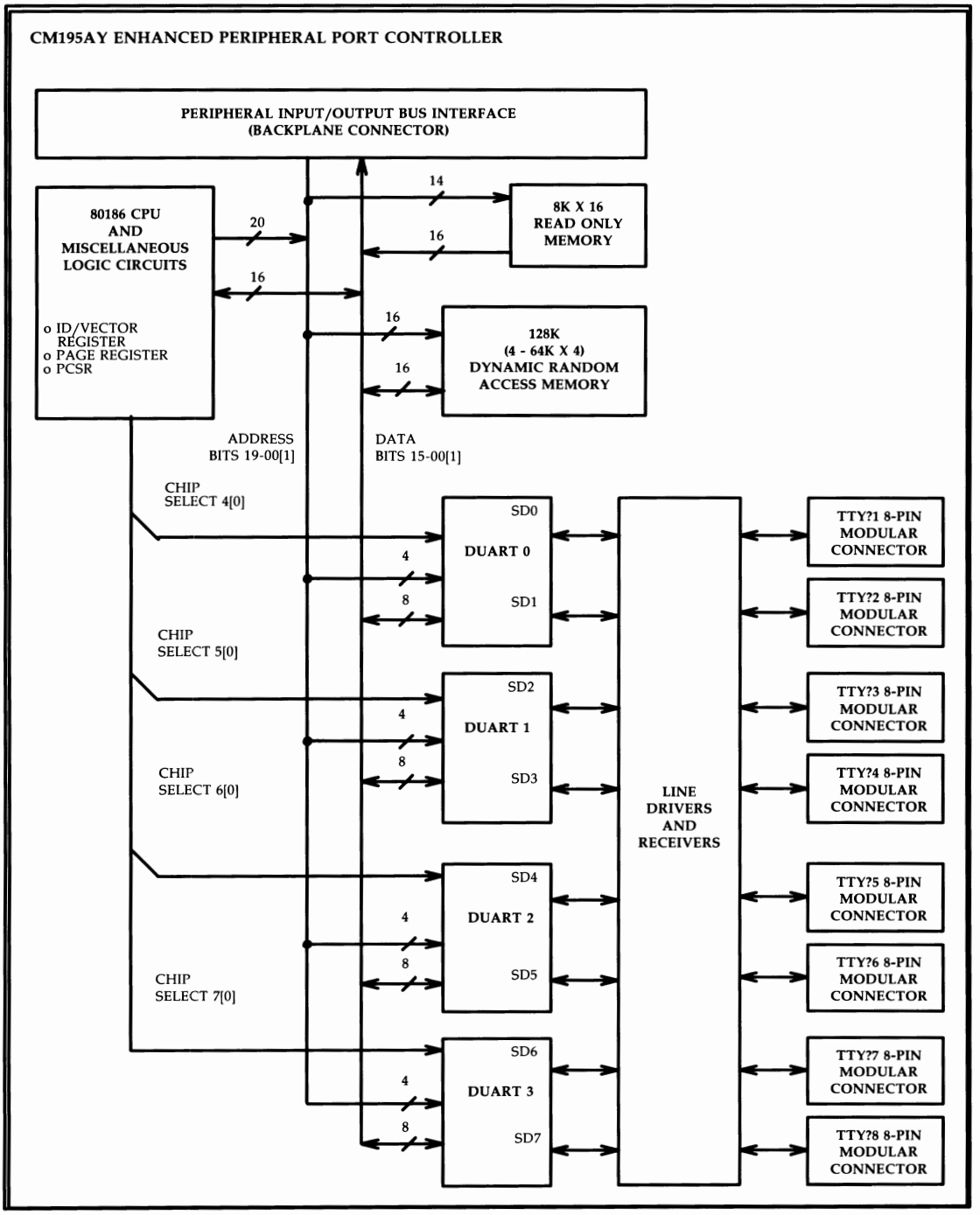


Figure 3-61: CM195AY EPORTS Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the EPORTS card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the EPORTS card are described in the following paragraphs. Figure 3-62 shows the EPORTS card address map.

ID/Vector Register

The EPORTS card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit EPORTS card ID code. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the EPORTS card ID code to the high order bits (byte 1) of the ID/Vector Register and waits. The EPORTS card ID code is 0x 0102. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Page Register

The EPORTS card uses a 24-bit I/O address to do main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128-kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

EPORTS CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	DRAM (VECTOR TABLE)	READ/WRITE	16	128K
0x 80000	—	MCS	DPDRAM(3B2 MAIN MEMORY)	READ/WRITE	16	128K
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	1
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	1
0x C0086	0x 0486	PS1	NOT USED	—	—	—
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	—
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	—
0x C008A	0x 048A	PS1	PCSR BIT 2 (EOP0)	(NOTE 1)	1	—
0x C008B	0x 048B	PS1	PCSR BIT 3 (EOP1)	(NOTE 1)	1	—
0x C008C	0x 048C	PS1	PCSR BIT 4 (EOP2)	(NOTE 1)	1	—
0x C008D	0x 048D	PS1	PCSR BIT 5 (EOP3)	(NOTE 1)	1	—
0x C008E	0x 048E	PS1	PCSR BIT 6 (NOT USED)	—	—	—
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT00)	(NOTE 1)	1	—
0x C0100	0x 0500	PS2	DTR REGISTER	READ/WRITE	8	1
0x C0200	0x 0600	PS4	DMAC0	READ/WRITE	8	32
0x C0220	0x 0620	PS4	DMAC1	READ/WRITE	8	32
0x C0240	0x 0640	PS4	DMAC2	READ/WRITE	8	32
0x C0260	0x 0660	PS4	DMAC3	READ/WRITE	8	32
0x C0280	0x 0680	PS5	SCC0 (CH B)	READ/WRITE	8	1
0x C0281	0x 0681	PS5	SCC0 (CH A)	READ/WRITE	8	1
0x C02A0	0x 06A0	PS5	SCC1 (CH B)	READ/WRITE	8	1
0x C02A1	0x 06A1	PS5	SCC1 (CH A)	READ/WRITE	8	1
0x C02C0	0x 06C0	PS5	SCC2 (CH B)	READ/WRITE	8	1
0x C02C1	0x 06C1	PS5	SCC2 (CH A)	READ/WRITE	8	1
0x C02E0	0x 06E0	PS5	SCC3 (CH B)	READ/WRITE	8	1
0x C02E1	0x 06E1	PS5	SCC3 (CH A)	READ/WRITE	8	1
0x C0300	0x 0700	PS6	SCCIACK	READ	8	1
(NOTE 2)	—	80186	80186 CONTROL BLOCK	READ/WRITE	16	256
0x F8000	—	UCS	EPROM	READ	16	32K

NOTES:
1. Bit is cleared by 80186 Microprocessor access.
2. After a reset, this address is an I/O address, 0x 0FF00. It may be reprogrammed to a different address.

LEGEND:

DMAC	Direct Memory Access Controller
DTR	Data Terminal Ready
EOP	End of Process
LCS	Lower Chip Select
MCS	Memory Chip Select
PCSR	Peripheral Control and Status Register
PS	Peripheral Select
SCC	Serial Communication Controller
SCCIACK	Serial Communication Controller Interrupt Acknowledge
UCS	Upper Chip Select

Figure 3-62: CM195AY EPORTS Card Address Map

Peripheral Control and Status Register

The EPORTS card contains an 8-bit Peripheral Control and Status Register (PCSR) addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access except for PCSR6 that is controlled by the Bus Abort Feature (BAF).

EPORTS PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT0[0] and is asserted by the EPORTS firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is normally used for the BAF. EPORTS does not use PCSR6.
5	Used to control the End-of-Page 3 (EOP3) interrupt. Addressing PCSR6 (0x 048D) clears (negates) the bit.
4	Used to control End-of-Page 2 (EOP2) interrupt. Addressing PCSR6 (0x 048C) clears (negates) the bit.
3	Used to control End-of-Page 1 (EOP1) interrupt. Addressing PCSR6 (0x 048B) clears (negates) the bit.
2	Used to control End-of-Page 0 (EOP0) interrupt. Addressing PCSR6 (0x 048A) clears (negates) the bit.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the EPORTS PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the EPORTS firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by an access of the EPORTS ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The EPORTS card contains 128K bytes of Dual Ported Dynamic Random Access Memory (DPDRAM) configured as 64K by 16 bits. Four Direct Memory Access Controllers (DMACs) are used to provide individual transmit and receive DMA channels for each of the eight RS-232C ports.

Local ROM

The EPORTS card firmware is in 16K bytes of Read Only Memory (ROM) configured as 8K by 16 bits.

CM195AY Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for an EPORTS card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are EPORTS software defined values. As such, the rq_size and cq_size values may differ between versions of EPORTS software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0102
DEVICE NAME (dev_name)	EPORTS
REQUEST QUEUE SIZE (rq_size)	0x 21
COMPLETION QUEUE SIZE (cq_size)	0x 46
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	1
CONSOLE FILE (cons_file)	1
INDIRECT DEVICE (indir_dev)	0

CM195B/CM195BA PORTS CARD

General

The CM195B/CM195BA Peripheral Port Controller (PORTS) Card provides four separate, asynchronous serial ports (RS-232C) and one parallel (CENTRONICS) port. Functionally, the PORTS card consists of the Common Input/Output (CIO) circuits, two Dual Universal Asynchronous Receiver/Transmitter (DUART) circuits, and a parallel interface circuit. The four asynchronous serial ports are identified as subdevices. DUART 0 supports subdevices SD0 and SD1; DUART 1 supports subdevices SD2 and SD3. The DUART circuits are polled by the 80186 Microprocessor. Neither the DUART or parallel interface circuits can interrupt the 80186 Microprocessor. Drivers and receiver circuits are used to interface the DUARTs to MODEMS and/or data terminals (RS-232C). The parallel interface (CENTRONICS interface) is intended to be used to interface a printer. Figure 3-63 is a functional block diagram of the CM195B/CM195BA PORTS Card.

The CIO circuits include the following:

- INTEL 80186 Microprocessor
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Local Random Access Memory (RAM)
- Local Read Only Memory (ROM)
- Miscellaneous Circuits.

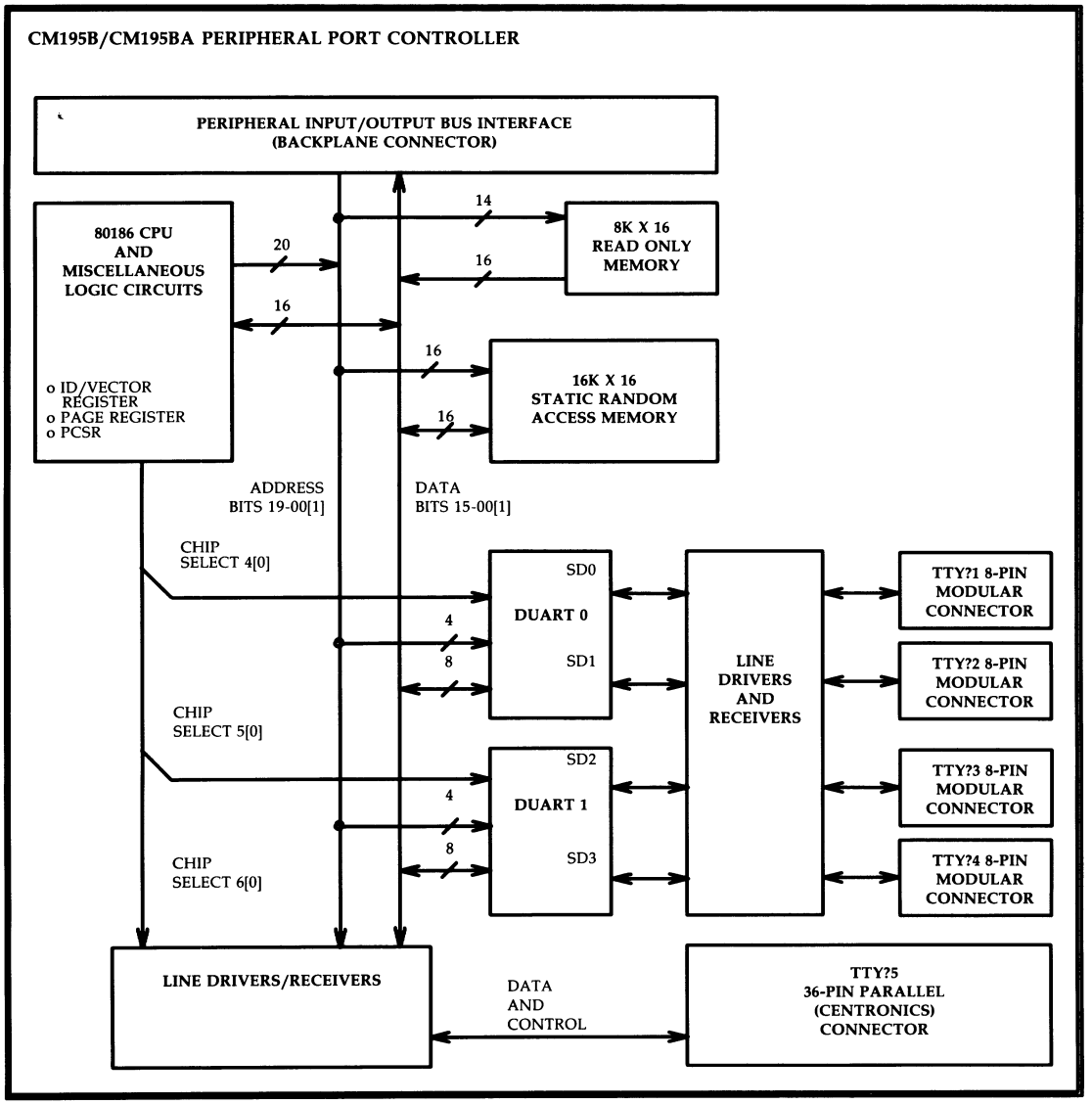


Figure 3-63: CM195B/CM195BA PORTS Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the PORTS card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the PORTS card are described in the following paragraphs. Figure 3-64 shows the PORTS card address map.

ID/Vector Register

The PORTS card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 8-bit PORTS card ID code. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the PORTS card ID code to the high order bits (byte 1) of the ID/Vector Register and waits. The PORTS card ID code is 0x 03. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Page Register

The PORTS card uses a 24-bit I/O address to do main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0480. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

PORTS CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	RAM (VECTOR TABLE)	READ/WRITE	16	32K
0x 80000	—	MCS	DPDRAM	READ/WRITE	16	128K
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	1
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	1
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	—
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	—
0x C008A	0x 048A	PS1	PCSR BIT 2 (NOT USED)	—	1	—
0x C008B	0x 048B	PS1	PCSR BIT 3 (NOT USED)	—	1	—
0x C008C	0x 048C	PS1	PCSR BIT 4 (NOT USED)	—	1	—
0x C008D	0x 048D	PS1	PCSR BIT 5 (ARDY)	(NOTE 2)	1	—
0x C008E	0x 048E	PS1	PCSR BIT 6 (BAF)	(NOTE 2)	1	—
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT1[0])	(NOTE 1)	1	—
0x C0100	0x 0500	PS2	CLEAR NMI REQUEST	—	—	—
0x C0102	0x 0502	PS2	CLEAR INT0 REQUEST	—	—	—
0x C0104	0x 0504	PS2	CLEAR INT1 REQUEST	—	—	—
0x C0106	0x 0506	PS2	CLEAR INT2 REQUEST	—	—	—
0x C0180	0x 0580	PS3	REQUEST RESET	—	—	—
0x C0200	0x 0600	PS4	DUART 0	READ/WRITE	8	16
0x C0280	0x 0680	PS5	DUART 1	READ/WRITE	8	16
0x C0300	0x 0700	PS6	PARALLEL PORT	READ/WRITE	8	4
0x C0400	0x FF00	80186	80186 CONTROL BLOCK	—	16	—
0x C0420	0x FF20	80186	INTERRUPT CONTROL	READ/WRITE	16	—
0x C0450	0x FF50	80186	TIMER 0 CONTROL	—	16	—
0x C0458	0x FF58	80186	TIMER 1 CONTROL	—	16	—
0x C0460	0x FF60	80186	TIMER 2 CONTROL	—	16	—
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL	—	16	—
0x C04C0	0x FFC0	80186	DMA 0 CONTROL	—	16	—
0x C04D0	0x FFD0	80186	DMA 1 CONTROL	—	16	—
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	—	16	—
0x FC000	—	UCS	ROM	READ/WRITE	16	16K

NOTES:

1. Bit is cleared by 80186 Microprocessor access.
2. Bit is set to 0 by 80186 Microprocessor access unless a "dummy" read is pending.

LEGEND:

ARDY	Asynchronous Data Ready
BAF	Bus Abort Feature
DMA	Direct Memory Access
DPDRAM	Dual Port Dynamic Random Access Memory
LCS	Lower RAM Chip Select
MCS	Memory Chip Select
NMI	Nonmaskable Interrupt
PCSR	Peripheral Control and Status Register
PS	Peripheral Select
UCS	Upper RAM Chip Select

Figure 3-64: CM195B/CM195BA PORTS Card Address Map

Peripheral Control and Status Register

The PORTS card contains an 8-bit Peripheral Control and Status Register (PCSR) addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access except for PCSR6 that is controlled by the Bus Abort Feature (BAF).

PORTS PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT0[0] and is asserted by the PORTS firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is used for the BAF. Bit 6 is set by hardware when the 80186 Microprocessor is delayed in accessing main memory and must be cleared by firmware. During normal operation, PCSR6 is cleared by the 80186 Microprocessor addressing PCSR6 unless a "dummy" read is pending. Addressing PCSR6 (0x 048E) clears (negates) the bit.
5	Used to control Asynchronous Data Ready (ARDY[1]).
4	Not used by PORTS.
3	Not used by PORTS.
2	Not used by PORTS.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the PORTS PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the PORTS firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by an access of the PORTS ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The PORTS card contains 32K bytes of Static Random Access Memory (SRAM) configured as 16K by 16 bits.

Local ROM

The PORTS card firmware is in 16K bytes of ROM configured as 8K by 16 bits.

CM195B/CM195BA Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a PORTS card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are PORTS software defined values. As such, the rq_size and cq_size values may differ between versions of PORTS software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0003
DEVICE NAME (dev_name)	PORTS
REQUEST QUEUE SIZE (rq_size)	0x 03
COMPLETION QUEUE SIZE (cq_size)	0x 23
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	1
CONSOLE FILE (cons_file)	1
INDIRECT DEVICE (indir_dev)	0

CM195H CARTRIDGE TAPE CONTROLLER CARD

General

Figure 3-65 is a functional block diagram of the CM195H Cartridge Tape Controller (CTC) Card. Functionally, the CTC card consists of the Common Input/Output (CIO) circuits and Cartridge Tape/Floppy Disk Interface circuits. Driver and receiver circuits are used to interface one cartridge tape drive and one floppy disk drive. Two devices can be connected to a Cartridge Tape Controller; however, only one of the two devices can be accessed at a given time. The CIO circuits include the following:

- INTEL 80186 Microprocessor
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Local Random Access Memory (RAM)
- Local Read Only Memory (ROM)
- Direct Memory Access Controller (AM 9517A)
- Miscellaneous Circuits.

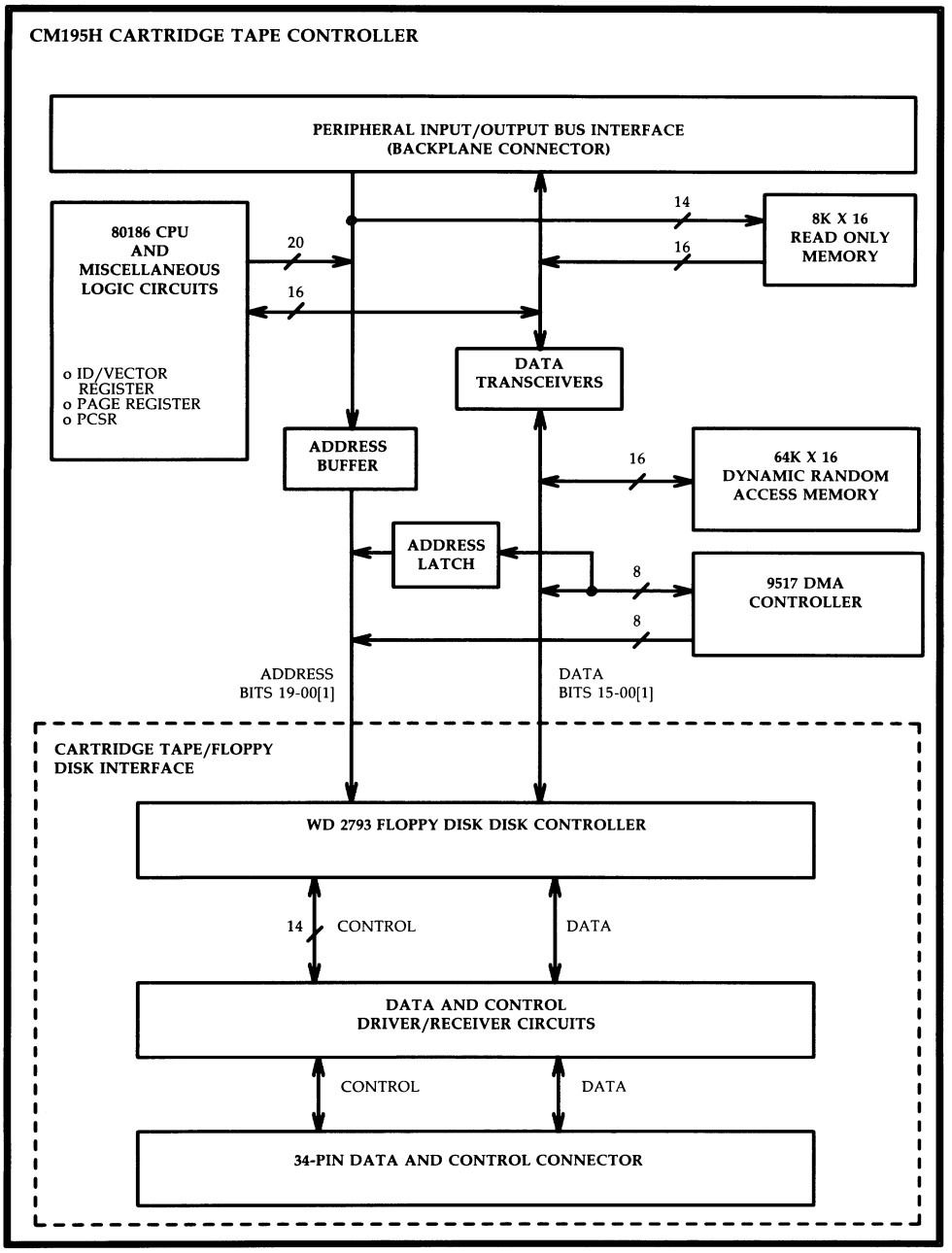


Figure 3-65: CM195H CTC Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the CTC card is provided by an INTEL 80186, 16-bit microprocessor operating at 6 MHz. Some of the microprocessor features used for the CTC card are described in the following paragraphs. Figure 3-66 shows the CTC card address map.

ID/Vector Register

The CTC card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit CTC card ID code. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the CTC card ID code to the high order bits (byte 1) of the ID/Vector Register and waits. The CTC card ID code is 0x 0005. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Page Register

The CTC card uses a 24-bit I/O address to do main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

CTC CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	CTC DRAM (VECTOR TABLE)	READ/WRITE	—	128K
0x 80000	—	MCS	SBD DPDRAM	READ/WRITE	16	128K
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	1
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	1
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	—
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	—
0x C008A	0x 048A	PS1	PCSR BIT 2 (INT2)	(NOTE 1)	1	—
0x C008B	0x 048B	PS1	PCSR BIT 3 (INT3)	(NOTE 1)	1	—
0x C008C	0x 048C	PS1	PCSR BIT 4 (NOT USED)	—	1	—
0x C008D	0x 048D	PS1	PCSR BIT 5 (RESERVED)	—	1	—
0x C008E	0x 048E	PS1	PCSR BIT 6 (BAF)	(NOTE 2)	1	—
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT)	(NOTE 1)	1	—
0x C0100	0x 0500	PS2	8237 DMA CONTROLLER	READ/WRITE	—	128K
0x C0200	0x 0600	PS4	FLOPPY DISK CONTROLLER	READ/WRITE	—	128K
0x C0300	0x 0700	PS6	SELECT/CONFIGURATION REGISTER	WRITE	16	2
0x C0450	0x FF50	80186	TIMER 0 CONTROL	—	—	—
0x C04A0	0x FFA0	80186	ADDRESS DECODER	—	—	—
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	—	16	2
0x FC000	—	UCS	ROM	READ	16	16K

NOTES:

1. Bit is cleared by 80186 Microprocessor access.
2. Bit is set to 0 by 80186 Microprocessor access unless a "dummy" read is pending.
3. Firmware can re-program the UCS addresses for 32K bytes.

LEGEND:

BAF	Bus Abort Feature
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
LCS	Lower RAM Chip Select
MCS	Memory Chip Select
PS	Peripheral Select
PCSR	Peripheral Control and Status Register
UCS	Upper RAM Chip Select

Figure 3-66: CM195H CTC Card Address Map

Peripheral Control and Status Register

The CTC card contains an 8-bit Peripheral Control and Status Register (PCSR) addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access except for PCSR6 that is controlled by the Bus Abort Feature (BAF).

CTC PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT0[0] and is asserted by the PORTS firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is used for the BAF. Bit 6 is set by hardware when the 80186 Microprocessor is delayed in accessing main memory and must be cleared by firmware. During normal operation, PCSR6 is cleared by the 80186 Microprocessor addressing PCSR6 unless a "dummy" read is pending. Addressing PCSR6 (0x 048E) clears (negates) the bit.
5	Used to control Asynchronous Data Ready (ARDY[1]).
4	Not used by CTC.
3	Not used by CTC.
2	Not used by CTC.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the CTC PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the CTC firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by an access of the CTC ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The CTC card contains 128K bytes of Dynamic Random Access Memory (DRAM) configured as 64K by 16 bits.

Local ROM

The CTC card firmware is in 16K bytes of ROM configured as 8K by 16 bits.

Cartridge Tape/Floppy Disk Interface

The Cartridge Tape/Floppy Disk Interface is a WD 2793 Floppy Disk Controller. The chip contains write precompensation and data separation circuits. The 34-pin data and control connector is a SA-450 interface.

CM195H Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CTC card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are CTC software defined values. As such, the rq_size and cq_size values may differ between versions of CTC software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0005
DEVICE NAME (dev_name)	CTC
REQUEST QUEUE SIZE (rq_size)	0x 10
COMPLETION QUEUE SIZE (cq_size)	0x 20
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	0
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	0
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM195K EXPANSION DISK CONTROLLER CARD

General

The CM195K Expansion Disk Controller (XDC) Card is an intelligent feature card used to interface a maximum of two external hard disk drives to a 3B2 computer. The interface is ST-506. Figure 3-67 is a functional block diagram of the XDC card. The XDC card consists of the Common Input/Output (CIO) circuits and the Disk Interface circuits. The CIO circuits include the following:

- INTEL 80186 Microprocessor
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Local Random Access Memory (RAM)
- Local Read Only Memory (ROM)
- Miscellaneous Circuits.

The Disk Interface circuits include the following:

- Hard Disk Controller
- Data Separator
- Write Precompensation.

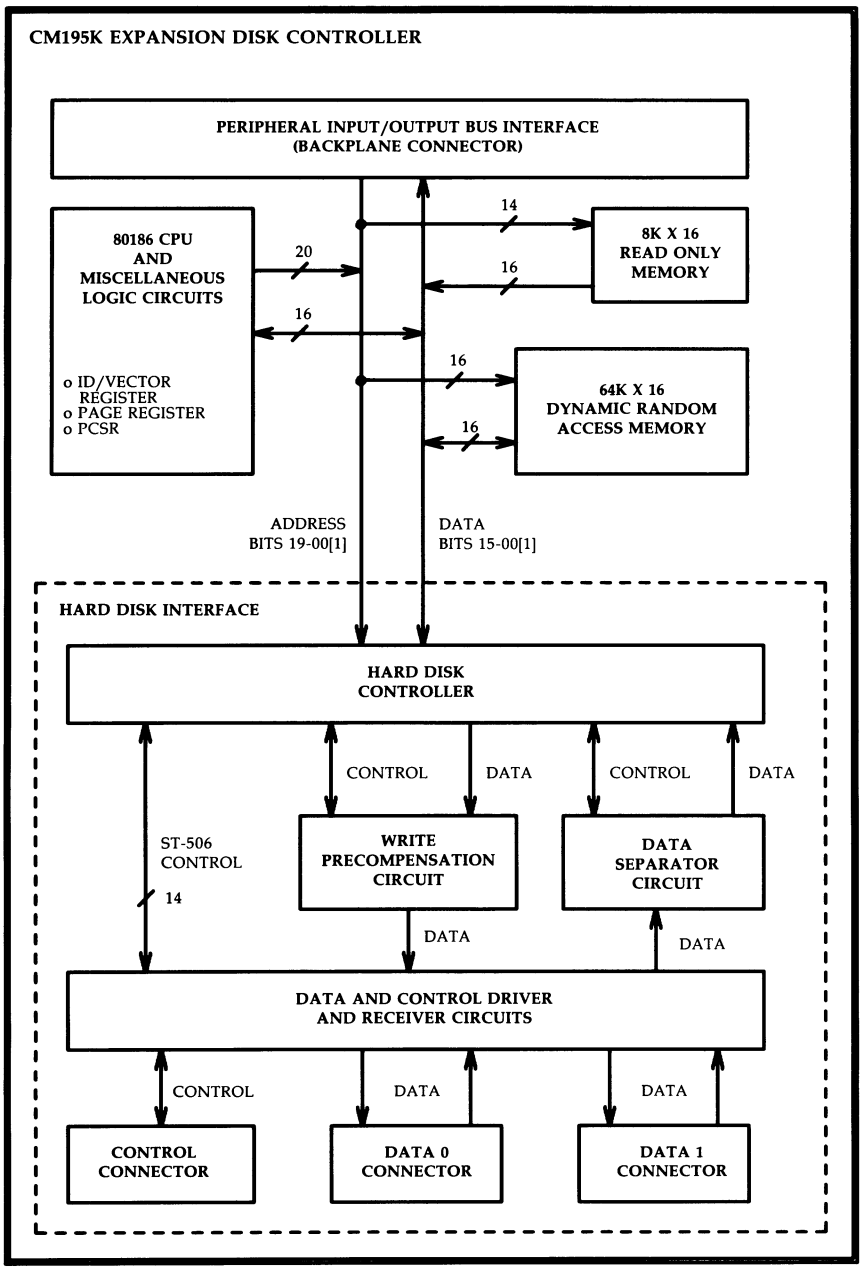


Figure 3-67: CM195K XDC Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the XDC card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the XDC card are described in the following paragraphs. Figure 3-68 shows the XDC card address map.

The Direct Memory Access (DMA) Channel 0 is used to move data from the XDC card RAM to the system board main memory and vice-versa. Data is transferred on DMA Channel 0 in either 8- or 16-bit words, to and from even and odd addresses.

DMA Channel 1 is used by the XDC card to transfer data between the XDC RAM and the disk drives connected to the XDC card, via the hard disk controller. This channel supports a transfer rate of 625 kilobytes per second.

Input/Output Bus Control

The XDC card does not support the Bus Abort Feature (BAF). I/O bus control circuitry responds to I/O bus and 80186 Microprocessor control signals. Three major paths are listed below:

- 80186 Microprocessor read or write of the system board main memory
- System board CPU read or write XDC card
- Interrupt Acknowledge (PIAK[0]).

The I/O bus control circuitry responds to the I/O bus and to the 80186 Microprocessor control signals by selectively enabling the appropriate I/O bus signals. Certain Peripheral Control and Status Register (PCSR) bits can also be set when the XDC card is accessed.

XDC CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	DRAM (VECTOR TABLE)	READ/WRITE	16	128
0x 00080	—	LCS	DRAM (APPLICATION)	READ/WRITE	16	127.9K
0x 20000	—	LCS	NOT USED	—	—	128K
0x 40000	—	—	NOT USED	—	—	256K
0x 80000	—	MCS	SBD DPDRAM	READ/WRITE	16	128K/PAGE
0x A0000	—	MCS	NOT USED	—	—	128K
0x C0000	0x 0400	PS0	NOT USED	—	—	128
0x C0080	0x 0480	PS0	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	1
0x C0086	0x 0486	PS1	RESERVED			
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	
0x C008A	0x 048A	PS1	PCSR BIT 2 (INT2)	(NOTE 1)	1	
0x C008B	0x 048B	PS1	PCSR BIT 3 (INT3)	(NOTE 1)	1	
0x C008C	0x 048C	PS1	PCSR BIT 4 (RESET PCSR4)	(NOTE 2)	1	
0x C008D	0x 048D	PS1	PCSR BIT 5 (ARDY)	READ/WRITE	1	
0x C008E	0x 048E	PS1	PCSR BIT 6 (SET PCSR4)	(NOTE 2)	1	
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT1[0])	(NOTE 1)	1	
0x C0090	0x 0490	PS1	NOT USED	—	16	111
0x C0100	0x 0500	PS2	NOT USED	—	—	128
0x C0180	0x 0580	PS3	NOT USED	—	—	128
0x C0200	0x 0600	PS4	HDC CHIP FIFO	READ/WRITE	8	1
0x C0202	0x 0602	PS4	HDC COMMAND REGISTER	WRITE	8	1
0x C0202	0x 0602	PS4	HDC STATUS REGISTER	READ	8	1
0x C0204	0x 0604	PS4	NOT USED	—	16	126
0x C0280	0x 0680	PS5	NOT USED	—	16	128
0x C0300	0x 0700	PS6	NOT USED	—	16	128
0x C0400	0x FF00	80186	80186 CONTROL BLOCK	—	16	256
0x C0420	0x FF20	80186	INTERRUPT CONTROL	—	16	32
0x C0450	0x FF50	80186	TIMER 0 CONTROL	—	16	8
0x C0458	0x FF58	80186	TIMER 1 CONTROL	—	16	8
0x C0460	0x FF60	80186	TIMER 2 CONTROL	—	16	6
0x C0466	0x FF66	80186	NOT USED	—	—	58
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL	—	16	10
0x C04AA	0x FFAA	80186	NOT USED	—	—	22
0x C04C0	0x FFC0	80186	DMA 0 CONTROL	—	16	12
0x C04CC	0x FFCC	80186	NOT USED	—	—	4
0x C04D0	0x FFD0	80186	DMA 1 CONTROL	—	16	12
0x C04DC	0x FFDC	80186	NOT USED	—	—	34
0x C04FE	0x FFFE	80186	RELOCATION REGISTER		16	2
0x C0500	—	80186	NOT USED	—	—	47872
0x FC000	—	UCS	ROM	READ	16	16K

NOTES:

1. Bit is cleared (reset) by 80186 Microprocessor access.
2. PCSR6 is set [1] by 80186 Microprocessor access to reset the hard disk controller.
   PCSR4 is set [1] by either system reset or by addressing PCSR6.
   PCSR4 (HDC reset) is turned off [0] by addressing PCSR4.

LEGEND:

ARDY	Asynchronous Data Ready
DMA	Direct Memory Access
DPDRAM	Dual Port Dynamic Random Access Memory
DRAM	Dynamic Random Access Memory
HDC	Hard Disk Controller
LCS	Lower RAM Chip Select
MCS	Memory Chip Select
PCSR	Peripheral Control and Status Register
PS	Peripheral Select
SBD	System Board
UCS	Upper RAM Chip Select

Figure 3-68: CM195K XDC Card Address Map

ID/Vector Register

The XDC card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit XDC card ID code. Later the register contains an 8-bit interrupt vector. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the XDC card ID code to the ID/Vector Register and waits. The XDC card ID code is 0x 0204. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register are a unique 16-bit ID code of the card.

Page Register

The XDC card uses a 24-bit I/O address to do system board main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

Peripheral Control and Status Register

The XDC card contains an 8-bit Peripheral Control and Status Register (PCSR) which is addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access.

XDC PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT1[0] and is asserted by the XDC firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	PCSR6 is not registered; however, the PCSR6 address (0x 048E) is used to set PCSR4. Addressing PCSR6 asserts PCSR4. This provides the XDC the ability to reset the hard disk controller under XDC firmware control.
5	Used to control Asynchronous Data Ready (ARDY[1]).
4	**HARD DISK CONTROLLER RESET**: This bit resets the hard disk controller when asserted [1]. Addressing PCSR4 (0x 048C) clears the bit and negates the reset. The hard disk controller is reset by either a system reset or by the 80186 Microprocessor addressing PCSR6 (0x 048E) which asserts PCSR4.
3	Not used by the XDC card. Addressing PCSR3 (0x 048B) clears (resets) the bit.
2	**CLEAR INT2**: This 80186 Microprocessor interrupt is set by the hard disk controller on seek end, disk ready change, seek error, or equipment check conditions. PCSR2 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 048A.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the XDC PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the XDC firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by a system board CPU access of the XDC ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the XDC firmware.

Local RAM

The XDC card contains 128K bytes of Dynamic Random Access Memory (DRAM) configured as 64K by 16 bits. The DRAM is accessed via the Low Memory Chip Select (LCS0) from 80186 Microprocessor. The 16-bit address consists of the row address (bits 15—08) and the column address (bits 07—00).

The DRAM refresh operations are interleaved with CPU read/write accesses. If a memory access is in progress when the refresh timer requests a refresh operation, the memory refresh operation occurs immediately following the access. If a memory refresh operation is in progress when the CPU attempts a DRAM access, the memory refresh operation is allowed to complete before the CPU access is permitted. The CPU access is suspended by a maximum of three wait states to allow for the completion of the refresh cycle.

Local ROM

Firmware for the 80186 Microprocessor is stored in the ROM. The XDC card ROM contains 16K bytes configured as 8K by 16 bits. The ROM is accessed via the Upper Memory Chip Select (UCS[0]) and address bits 14—00.

Disk Interface

The Disk Interface consists of the following circuits.

Hard Disk Controller

The hard disk controller (NEC μPD7261) connects to the lower half of the demultiplexed 80186 Microprocessor data bus. Under the control of the 80186 Microprocessor, the hard disk controller generates the ST-506 signals to control the associated disk drives.

Data Separator

The data separator processes (separates) the serial stream of bits read from the disk drive into clock and data signals that are applied to the μPD7261.

Write Precompensation

The bits recorded on the inner tracks of a disk are more densely packed than the outer tracks. Write precompensation is necessary to ensure that the data bits are stored at the right place on the disk. The controller sends two signals to enable either an early or a late write to the disk. These write enables are actually too late to correctly adjust the data. The precompensation circuit is a 10 tap, 100-nanosecond delay line with the 50 percent tap delaying the data enough to have valid early and late enable. The 80, 90, and 100 percent taps provide the early, normal, and late data. The write precompensation is turned on or off by the Reduced Write Current (RWC) signal from the hard disk controller.

Driver/Receiver

The driver and receiver circuits interface the Control Bus, Data 0, and the Data 1 with the associated disk drives.

CM195K Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for an XDC card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are XDC software defined values. As such, the rq_size and cq_size values may differ between versions of XDC software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0204
DEVICE NAME (dev_name)	XDC
REQUEST QUEUE SIZE (rq_size)	0x 14
COMPLETION QUEUE SIZE (cq_size)	0x 28
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM195T INTELLIGENT SERIAL CONTROLLER CARD

General

The CM195T Intelligent Serial Controller (ISC) Card is a general purpose, synchronous communications peripheral interface card providing a two channel, full duplex, synchronous interface. The ISC card supports both synchronous and asynchronous peripheral device operation. The ISC supports multiple applications depending on the software executing in the ISC Random Access Memory (RAM). The ISC card can provide communication over synchronous channels such as Systems Network Architecture/Synchronous Data Link Control (SNA/SDLC), bi-sync and X.25 as a function of the appropriate software being loaded on the ISC card. Figure 3-69 is a functional block diagram of the ISC card.

ISC Card Features

The ISC card features include the following:

- Serial communications for the 3B2 computer Common I/O (CIO) bus
- Intelligent INTEL 80186 Microprocessor-based controller
- Local RAM
- Local Read Only Memory (ROM)
- Two, fully duplex, synchronous RS-232C channels
- Nonreturn to Zero (NRZ)/Nonreturn to Zero Insertion (NRZI) encoding/decoding
- Direct Memory Access (DMA) for communications ports.

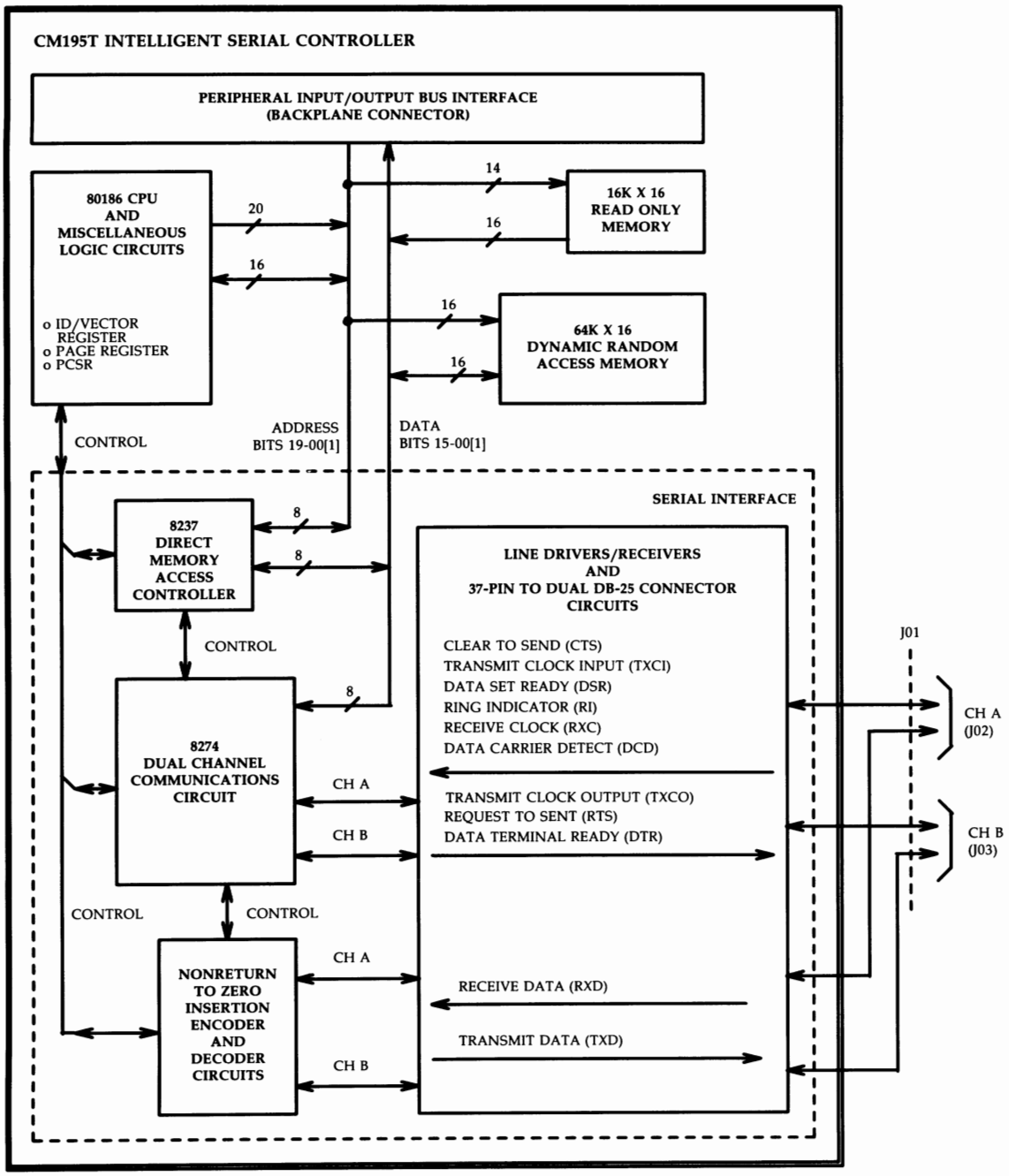


Figure 3-69: CM195T ISC Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the ISC card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the ISC card are described in the following paragraphs. Figure 3-70 shows the ISC card address map.

DMA Channels

Direct Memory Access (DMA) Channel 0 is used by the CIO firmware to move data between the ISC card RAM and the 3B2 computer main memory. DMA Channel 1 is programmed to do memory refresh operations for the ISC internal RAM (along with Timer 2).

Interrupt Controller

The internal Interrupt Controller of the 80186 Microprocessor is programmed to accept five separate interrupts: INT3 through INT0, and NMI. Interrupts INT0 and INT1 are reserved for CIO firmware use. INT2 is dedicated to the 8274 Dual Channel Communications Chip. INT3 is dedicated to the 8237 DMA controller. Nonmaskable Interrupt (NMI) is used by the CIO firmware to control the Bus Abort Feature (BAF).

Internal Timers

Timer 0 is available to applications software since external hardware is used to generate the I/O bus PFAIL0 signal. Timer 1 controls the BAF. Timer 2 is used to generate DMA requests to DMA Channel 1 for starting memory refresh operations.

Memory and Peripheral Chip Selects

The memory and peripheral chip selects are programmed by the ISC firmware to provide chip selects in the 80186 Microprocessor memory map (Figure 3-70).

Internal Clock Generator

The 80186 Microprocessor operates at 8 MHz (crystal controlled). The 80186 Microprocessor provides an 8-MHz output for other ISC functions. The 8-MHz signal is divided to provide 4 MHz to the 8237 DMA Controller and the 8274 Dual Channel Communications Chip.

ISC CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	RAM (VECTOR TABLE)	READ/WRITE	16	128
0x 00080	—	LCS	RAM (DEMON)	READ/WRITE	16	256
0x 00180	—	LCS	RAM (USER)	READ/WRITE	16	127.6K
0x 20000	—	LCS	NOT USED	—	—	128K
0x 40000	—	—	NOT USED	—	—	128K
0x 60000	—	—	RAM REFRESH	READ/WRITE	16	128K
0x 80000	—	MCS	DPDRAM	READ/WRITE	16	128K
0x A0000	—	MCS	NOT USED	—	—	128K
0x C0000	0x 0400	PS0	DEMON	—	—	—
0x C0080	0x 0480	PS0	ID/VECTOR REGISTER	WRITE	16	
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	
0x C0086	0x 0486	PS1	RESERVED			
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	
0x C008A	0x 048A	PS1	PCSR BIT 2 (INT2)	(NOTE 1)	1	
0x C008B	0x 048B	PS1	PCSR BIT 3 (INT3)	(NOTE 1)	1	
0x C008C	0x 048C	PS1	PCSR BIT 4 (NOT USED)		1	
0x C008D	0x 048D	PS1	PCSR BIT 5 (NOT USED)		1	
0x C008E	0x 048E	PS1	PCSR BIT 6 (BAF)	(NOTE 2)	1	
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT)	(NOTE 1)	1	
0x C0100	0x 0500	PS2	8237 DMA CONTROLLER (NOTE 3)	READ/WRITE	8	
⋮	⋮	⋮	⋮	⋮	⋮	
0x C011F	0x 051F	PS2	8237 DMA CONTROLLER	READ/WRITE	8	
0x C0180	0x 0580	PS3	8274 CHANNEL A DATA	READ/WRITE	12/8	
0x C0182	0x 0582	PS3	8274 CHANNEL B DATA	READ/WRITE	12/8	
0x C0184	0x 0584	PS3	8274 CHANNEL A CONTROL	READ/WRITE	12/8	
0x C0186	0x 0586	PS3	8274 CHANNEL B CONTROL	READ/WRITE	12/8	
0x C0200	0x 0600	PS4	NRZI CHANNEL A OFF	READ/WRITE	16	
0x C0202	0x 0602	PS4	NRZI CHANNEL A ON	READ/WRITE	16	
0x C0204	0x 0604	PS4	NRZI CHANNEL B OFF	READ/WRITE	16	
0x C0206	0x 0606	PS4	NRZI CHANNEL B ON	READ/WRITE	16	
0x C0280	0x 0680	PS5	SANITY FLIP-FLOP RESET	READ/WRITE	16	
0x C0300	0x 0700	PS6	RESERVED			
0x C0400	0x FF00	80186	80186 CONTROL BLOCK		16	
0x C0420	0x FF20	80186	INTERRUPT CONTROL		16	
0x C0450	0x FF50	80186	TIMER 0 CONTROL		16	
0x C045B	0x FF5B	80186	TIMER 1 CONTROL		16	
0x C0460	0x FF60	80186	TIMER 2 CONTROL	(NOTE 4)	16	
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL		16	
0x C04C0	0x FFC0	80186	DMA 0 CONTROL		16	
0x C04FD	0x FFD0	80186	DMA 1 CONTROL	(NOTE 4)	16	
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	—	16	
0x F8000	—	UCS	ROM	READ/WRITE	16	32K

NOTES:

1. Bit is cleared by 80186 Microprocessor access.
2. Bit is set to 0 by 80186 Microprocessor access unless a "dummy" read is pending.
3. Only even addresses are used in this range.
4. Timer 2 and DMA channel 1 provide RAM refresh for ISC.

LEGEND:

BAF	Bus Abort Feature
DMA	Direct Memory Access
DPDRAM	Dual Port Dynamic Random Access Memory
LCS	Lower RAM Chip Select
MCS	Memory Chip Select
NRZI	Nonreturn to Zero Insertion
PCSR	Peripheral Control and Status Register
PS	Peripheral Chip Select
UCS	Upper RAM Chip Select

Figure 3-70: CM195T ISC Card Address Map

Communications Processing

The ISC card supports a variety of synchronous protocols. This diversity is provided by the 8274 Dual Channel Communications Chip. The 8274 controls two independent, full duplexed channels and directly supports certain of the RS-232C MODEM control signals. The MODEM control signals not supported by the 8274 are supported by other components of the ISC and are available to the 80186 Microprocessor on data bits D11—D08 during a read operation of the 8274 Dual Channel Communications Chip.

ID/Vector Register

The ISC card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit ISC card ID code. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. The ISC card ID code is 0x 0201.

Page Register

The ISC card uses a 24-bit address to do main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482.

Peripheral Control and Status Register

The ISC card contains an 8-bit Peripheral Control and Status Register (PCSR) which is addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access except for PCSR6 that is controlled by the BAF.

ISC PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT1[0] and is asserted by the ISC firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is used for the BAF. Bit 6 is set by hardware when the 80186 Microprocessor is delayed in accessing main memory and must be cleared by firmware. During normal operation, PCSR6 is cleared by the 80186 Microprocessor addressing PCSR6 unless a "dummy" read is pending. Addressing PCSR6 (0x 048E) clears (negates) the bit.
5	Not used by the ISC card.
4	Not used by the ISC card.
3	**CLEAR INT3**: This 80186 Microprocessor interrupt is set by the 8237 DMA Controller. Bit 3 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 048B.
2	**CLEAR INT2**: This 80186 Microprocessor interrupt is set by the 8274 Dual Channel Communications Chip. Bit 2 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 048A.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the ISC PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the ISC firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by an access of the ISC ID/Vector Register (except on an interrupt acknowledge cycle). Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The ISC card contains 128K bytes of Dynamic Random Access Memory (DRAM) configured as 64K by 16 bits.

Local ROM

Firmware for the 80186 Microprocessor is stored in the ROM. The ISC card ROM contains either 16K bytes configured as 8K by 16 bits or 32K bytes configured as 16K by 16 bits. The ROM is accessed via the Upper Memory Chip Select (UCS[0]) and address bits 14—00.

CM195T Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for an ISC card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are ISC software defined values. As such, the rq_size and cq_size values may differ between versions of ISC software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0201
DEVICE NAME (dev_name)	ISC
REQUEST QUEUE SIZE (rq_size)	0x 1E
COMPLETION QUEUE SIZE (cq_size)	0x 3C
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM195U STARLAN INTERFACE CARD

General

The AT&T STARLAN network is a low-cost, local area network for linking MS-DOS and UNIX system-based computers. STARLAN runs at 1 megabit per second on twisted pair wiring. The wiring is based on AT&T's Premises Distribution System (PDS). The lowest level protocols conform to the IEEE 802.3 standards for Carrier Sense Multiple Access with Collision Detection (CSMA/CD) local area networking. The high-level protocols support applications written for Microsoft Networks.

Connection to STARLAN from a 3B2 computer is provided by a CM195U STARLAN Interface Card, which plugs into a 3B2 computer feature card slot. This card is called a Network Access Unit (NAU) in terms of STARLAN. The CM195U Card supports asynchronous terminals at speeds up to 19.2 kilobits per second.

Figure 3-71 is a functional block diagram of the CM195U Card. The CM195U Network Access Unit Card consists of the Common Input/Output (CIO) circuits and the Network Interface circuits. The CIO circuits include the following:

- INTEL 80186 Microprocessor
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Local Random Access Memory (RAM)
- Local Read Only Memory (ROM)
- Miscellaneous Circuits.

The Network Interface is an INTEL 82586 Ethernet Controller. The Network Interface circuits function as a network coprocessor and is an INTEL 82586 Local Area Network (LAN) Coprocessor.

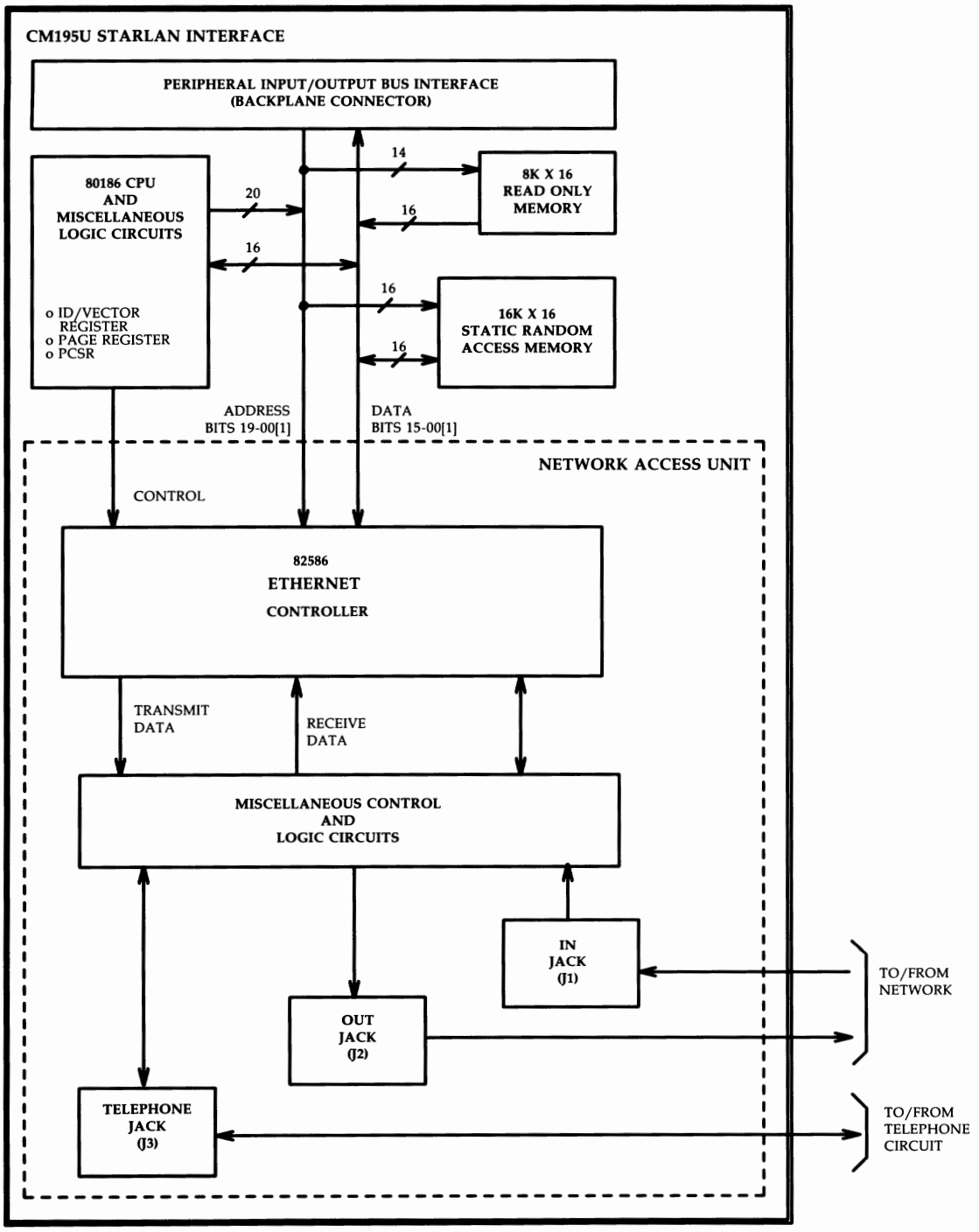


Figure 3-71: CM195U STARLAN Interface Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the STARLAN card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the STARLAN card are described in the following paragraphs. Figure 3-72 shows the STARLAN Interface card address map.

Input/Output Bus Control

I/O bus control circuitry responds to I/O bus and 80186 Microprocessor control signals. Three major paths are listed below:

- 80186 Microprocessor read or write of the system board main memory
- System board CPU read or write STARLAN card
- Interrupt Acknowledge (PIAK[0]).

The I/O bus control circuitry responds to the I/O bus and to the 80186 Microprocessor control signals by selectively enabling the appropriate I/O bus signals. In addition, the Bus Abort Feature (BAF) can be prematurely forced. Certain PCSR bits can also be set when the STARLAN Interface card is accessed.

ID/Vector Register

The STARLAN Interface card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit STARLAN Interface card ID code. Later the register contains an 8-bit interrupt vector. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the ID code to the ID/Vector Register and waits. The STARLAN Interface card ID code is 0x 0002. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register are a unique 16-bit ID code of the card.

Page Register

The STARLAN Interface card uses a 24-bit I/O address to do system board main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

STARLAN INTERFACE CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	RAM (VECTOR TABLE)	READ/WRITE	16	128
0x 00180	—	LCS	RAM (APPLICATION)	READ/WRITE	16	31.9K
0x 08000	—	—	NOT USED	—	—	—
0x 80000	—	MCS	DPDRAM	READ/WRITE	16	128K/PAGE
0x A0000	—	MCS	NOT USED	—	—	—
0x C0000	0x 0400	PS0	NOT USED	—	—	—
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	—
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	—
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	—
0x C0086	0x 0486	PS1	RESERVED	—	—	—
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	—
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	—
0x C008A	0x 048A	PS1	PCSR BIT 2 (INT2)	(NOTE 1)	1	—
0x C008B	0x 048B	PS1	PCSR BIT 3 (INT3)	(NOTE 1)	1	—
0x C008C	0x 048C	PS1	PCSR BIT 4 (NOT USED)	—	—	—
0x C008D	0x 048D	PS1	PCSR BIT 5	RESERVED	1	—
0x C008E	0x 048E	PS1	PCSR BIT 6 (BAF)	(NOTE 2)	1	—
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT1[0])	(NOTE 1)	1	—
0x C0100	0x 0500	PS2	(NOT USED)	—	—	—
0x C0180	0x 0580	PS3	(NOT USED)	—	—	—
0x C0200	0x 0600	PS4	(NOT USED)	—	—	—
0x C0280	0x 0680	PS5	(NOT USED)	—	—	—
0x C0300	0x 0700	PS6	82586 CHANNEL ATTENTION	—	—	—
0x C0400	0x FF00	80186	80186 CONTROL BLOCK	—	16	—
0x C0420	0x FF20	80186	INTERRUPT CONTROL	—	16	—
0x C0450	0x FF50	80186	TIMER 0 CONTROL	—	16	—
0x C0458	0x FF58	80186	TIMER 1 CONTROL	—	16	—
0x C0460	0x FF60	80186	TIMER 2 CONTROL	—	16	—
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL	—	16	—
0x C04C0	0x FFC0	80186	DMA 0 CONTROL	—	16	—
0x C04D0	0x FFD0	80186	DMA 1 CONTROL	—	16	—
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	—	16	—
0x FC000	—	UCS	ROM	READ	16	16K

NOTES:

1. Bit is cleared [0] (reset) by 80186 Microprocessor access.
2. Bit is cleared [0] (reset) by 80186 Microprocessor access unless "dummy" read of BAF is pending.

LEGEND:

BAF	Bus Abort Feature
DMA	Direct Memory Access
DPDRAM	Dual Port Dynamic Random Access Memory
LCS	Lower RAM Chip Select
MCS	Memory Chip Select
NRZI	Nonreturn to Zero Insertion
PCSR	Peripheral Control and Status Register
PS	Peripheral Select
UCS	Upper RAM Chip Select

Figure 3-72: CM195U STARLAN Interface Card Address Map

Peripheral Control and Status Register

The STARLAN Interface card contains an 8-bit Peripheral Control and Status Register (PCSR) which is addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access.

STARLAN INTERFACE PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT1[0] and is asserted by the STARLAN Interface card firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is used for the BAF. The BAF is not supported on the CM195U STARLAN Interface Card. Bit 6 is set [1] by hardware when the 80186 Microprocessor is delayed in accessing main memory and must be cleared by firmware. During normal operation, PCSR6 is cleared by the 80186 Microprocessor addressing PCSR6 unless a "dummy" read is pending. The 80186 Microprocessor cannot access DPDRAM when PCSR6 is set [1]. Addressing PCSR6 (0x 048E) clears (negates) the bit.
5	Bit 5 is not used by the STARLAN Interface card. Addressing PCS5[1] (0x 48D) clears (negates) the bit.
4	PCSR4 is reserved for future STARLAN Interface card development. Addressing PCS4[1] (0x 48C) clears (negates) the bit.
3	PCSR3 is not used by the STARLAN Interface card. Addressing PCSR3 (0x 048B) clears (resets) the bit.
2	PCSR2 is used by the 82586 LAN Coprocessor to interrupt the 80186 Microprocessor. Addressing PCSR3 (0x 048A) clears (resets) the bit.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the STARLAN Interface PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the STARLAN firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by a system board CPU access of the STARLAN Interface card ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the STARLAN firmware.

Local RAM

The STARLAN Interface card contains 32K bytes of Static Random Access Memory (SRAM) configured as 16K by 16 bits. The DRAM is accessed via the Low Memory Chip Select (LCS0) from 80186 Microprocessor and address bits 12—00. Note that 256K bytes of RAM address space is reserved. The 32K bytes of RAM is used for intermediate data storage of the data being transmitted to/received from the network.

Local ROM

Firmware for the 80186 Microprocessor is stored in the ROM. The STARLAN Interface card ROM contains 16K bytes configured as 8K by 16 bits. The ROM is accessed via the Upper Memory Chip Select (UCS[0]) and address bits 14—00.

Network Interface

The AT&T STARLAN is an Ethernet compatible, local area network. Data is transferred over the network by attaching a destination identification to the data to be transferred. The **nisend** command is used to attach a destination code and file name to the data to be transferred. The STARLAN Interface Card firmware handles the transfer of the data between the 3B2 computer main memory and the Network Interface local RAM. The data to be transferred is divided into packets of 1024 bytes for transfer over the network. The Ethernet Controller autonomously reads the data from local RAM, converts the data to serial stream, and transmits the stream over the network. If collisions are detected, the information packet is retransmitted automatically. The receiving system acknowledges the receipt of the data.

Ethernet Controller Circuit

The Network Interface is a 82586 Ethernet Controller that manages the process of transmitting and receiving data over the network. The primary functions of the controller are to do the following:

- Decode the serial data
- Check for data integrity
- Convert serial data into parallel data format
- Store parallel data in the local RAM
- Save and report networking errors for the node.

The Network Access Unit Serial Interface provides the connection between the 82586 LAN Coprocessor and the transmission media. The interface consists of the following signals.

Receive Pair
A differential signal that is active when any data is received.

Transmit Pair
A differential signal that is active when any data is transmitted.

Collision Presence Pair
A differential signal that is active while a collision is in progress.

Connectors are provided to support both daisy-chained and star connections (J1 and J2). A connector (J3) is also provided for a telephone link to an AT&T Premises Distribution System.

CM195U Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a STARLAN Interface card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are STARLAN software defined values. As such, the rq_size and cq_size values may differ between versions of STARLAN software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0002
DEVICE NAME (dev_name)	NI
REQUEST QUEUE SIZE (rq_size)	0x 0A
COMPLETION QUEUE SIZE (cq_size)	0x 19
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

Ethernet Data Packet Format

The format of an Ethernet Data Packet is as follows:

FIELD	PREAMBLE	DESTINATION ADDRESS	SOURCE ADDRESS	TYPE	DATA	CRC
SIZE	64 BITS	48 BITS	48 BITS	16 BITS	46 TO 1500 BYTES	32 BITS

PREAMBLE The Preamble is a 64-bit field of alternating 1's and 0's, ending with two consecutive 1's. This field synchronizes the receiving circuits to the incoming data packet.

DESTINATION ADDRESS
The 48-bit Destination Address field is the nodal address to which the data is being transmitted.

SOURCE ADDRESS
The 48-bit Source Address field is the nodal address from which the data is being transmitted.

TYPE The 16-bit Type field is used for a high-level data protocol.

DATA The Data field is the data to be sent over the network and is from 46 to 1500 bytes in length.

CRC The 32-bit Cyclic Redundancy Check (CRC) field is calculated on all of the other fields. This field is also called the Frame Check Sequence field.

CM195W SCSI HOST ADAPTER CARD

General

The CM195W Small Computer Systems Interface (SCSI) Host Adapter Card provides an asynchronous, single-ended interface to the industry standard SCSI bus. Functionally, the CM195W Card consists of the Common Input/Output (CIO) circuits, and SCSI Protocol Controller. Figure 3-73 is a functional block diagram of the CM195W SCSI Host Adapter Card. The CM195W Card consists of the CIO circuits and a SCSI Protocol Controller. The CIO circuits include the following:

- INTEL 80186 Microprocessor
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Local Random Access Memory (RAM)
- Local Read Only Memory (ROM)
- Miscellaneous Circuits.

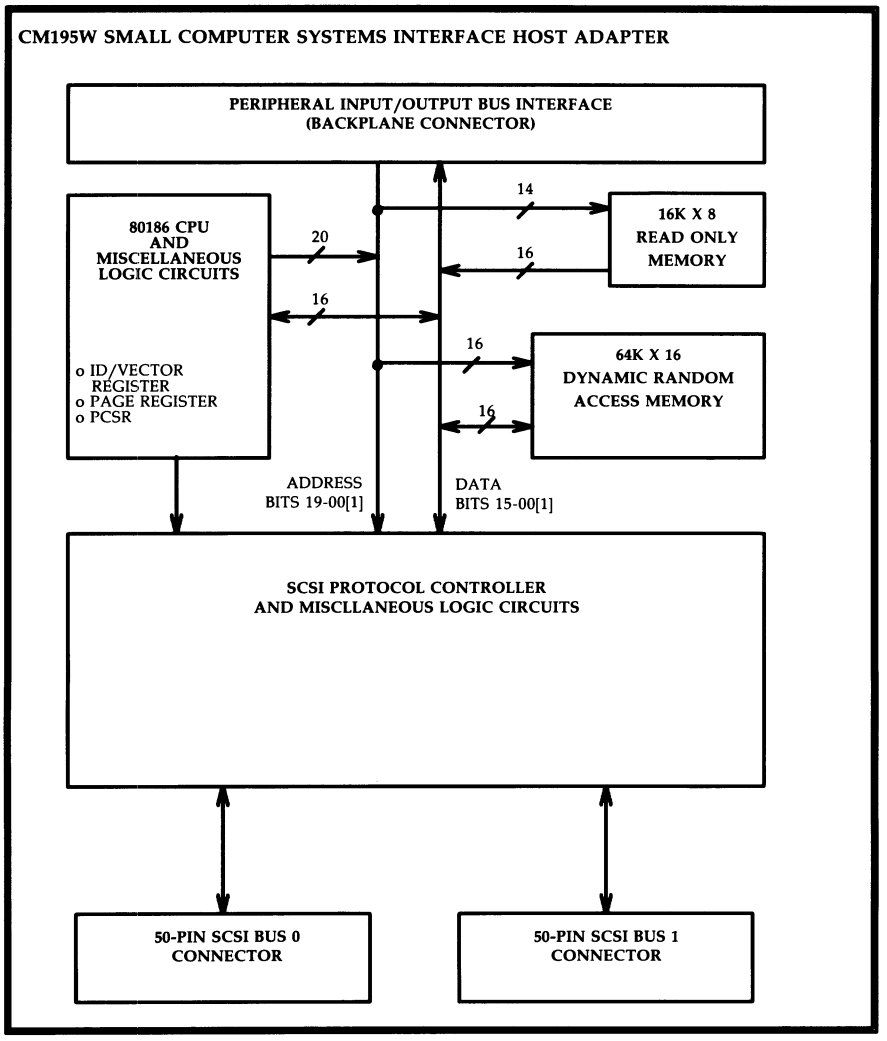


Figure 3-73: CM195W SCSI Host Adapter Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the CM195W Card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the CM195W Card are described in the following paragraphs. Figure 3-74 shows the CM195W SCSI Host Adapter Card address map.

ID/Vector Register

The CM195W SCSI Host Adapter Card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit CM195W Card ID code. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the CM195W Card ID code to the high order bits (byte 1) of the ID/Vector Register and waits. The CM195W Card ID code is 0x 0100. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Page Register

The CM195W Card uses a 24-bit I/O address to do main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

SCSI HOST ADAPTER CARD OUTPUT ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	DRAM (VECTOR TABLE)	READ/WRITE	16	128
0x 00080	—	LCS	DRAM (DEMON)	READ/WRITE	16	123.9K
0x 1F060	—	LCS	DRAM (EDT, SANITY, STATE FLAGS)	READ/WRITE	16	4K
0x 20000	—	LCS	NOT USED	—	—	128K
0x 40000	—	—	NOT USED	—	—	256K
0x 80000	—	MCS	DPDRAM	READ/WRITE	16	128K
0x A0000	—	MCS	NOT USED	—	—	256K
0x C0000	0x 0400	PS0	(NOT USED)	—	—	1
0x C0001	0x 0401	PS0	5386 DATA REGISTER	READ/WRITE	8	1
0x C0003	0x 0403	PS0	5386 COMMAND REGISTER	READ/WRITE	8	1
0x C0005	0x 0405	PS0	5386 CONTROL REGISTER	READ/WRITE	8	1
0x C0007	0x 0407	PS0	5386 DESTINATION ID	READ/WRITE	8	1
0x C0009	0x 0409	PS0	5386 AUXILIARY STATUS REGISTER	READ	8	1
0x C000B	0x 040B	PS0	5386 ID REGISTER	READ	8	1
0x C000D	0x 040D	PS0	5386 INTERRUPT REGISTER	READ	8	1
0x C000F	0x 040F	PS0	5386 SOURCE ID	READ	8	1
0x C0013	0x 0413	PS0	5386 DIAGNOSTIC REGISTER	READ	8	1
0x C0019	0x 0419	PS0	5386 TRANSFER CONTROL MSB	READ/WRITE	8	1
0x C001D	0x 041D	PS0	5386 TRANSFER CONTROL LSB	READ/WRITE	8	1
0x C001F	0x 041F	PS0	5386 (RESERVED)	—	8	1
0x C001F	0x 041F	PS0	5386 FIFO ACCESS	READ/WRITE	8	1
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	80186 PAGE REGISTER	WRITE	7	1
0x C0084	0x 0484	PS1	PCSR BITS 15—0	READ	8	2
0x C0086	0x 0486	PS1	SCSI BUS RESET	WRITE	1	
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	—	1	
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	—	1	
0x C008A	0x 048A	PS1	PCSR BIT 2 (INT2)	—	1	
0x C008B	0x 048B	PS1	PCSR BIT 3 (INT3)	—	1	
0x C008C	0x 048C	PS1	PCSR BIT 4 (INT3)	—	1	
0x C008D	0x 048D	PS1	PCSR BIT 5 (NMI)	—	1	
0x C008E	0x 048E	PS1	PCSR BIT 6 (INT2)	—	1	
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT)	—	1	
0x C00A2	0x 04A2	PS1	SCSI TO 3B2 PAGE REGISTER	WRITE	7	1
0x C00C2	0x 04C2	PS1	3B2 TO SCSI PAGE REGISTER	WRITE	7	1
0x C0100	0x 0500	PS2	RESET 3B2 FIFO	—	—	1
0x C0180	0x 0580	PS3	RESET SCSI FIFO	—	—	1
0x C0200	0x 0600	PS4	3B2 FIFO WORD ACCESS	READ/WRITE	16	2
0x C0280	0x 0680	PS5	8237 CHANNEL 0 ADDRESS REGISTER	READ/WRITE	8	1
0x C0282	0x 0682	PS5	8237 CHANNEL 0 CONTROL REGISTER	READ/WRITE	8	1
0x C0284	0x 0684	PS5	8237 CHANNEL 1 ADDRESS REGISTER	READ/WRITE	8	1
0x C0286	0x 0682	PS5	8237 CHANNEL 1 CONTROL REGISTER	READ/WRITE	8	1
0x C0290	0x 0690	PS5	8237 COMMAND AND STATUS REGISTER	READ/WRITE	8	1
0x C0292	0x 0692	PS5	8237 ILLEGAL REQUEST REGISTER	READ/WRITE	8	1
0x C0294	0x 0694	PS5	8237 ILLEGAL MASK REGISTER	READ/WRITE	3	1
0x C0296	0x 0696	PS5	8237 ILLEGAL MODE REGISTER	READ/WRITE	8	1
0x C0298	0x 0698	PS5	8237 ILLEGAL BYTE FLIPFLOP	READ/WRITE	1	1
0x C029A	0x 069A	PS5	8237 TEMPORARY REG MASTER CLEAR	READ/WRITE	8	1
0x C029C	0x 069C	PS5	8237 ILLEGAL CLEAR MASK REGISTER	READ/WRITE	1	1
0x C029E	0x 069E	PS5	8237 ILLEGAL MASK REGISTER BITS	READ/WRITE	4	
0x C029F	0x 069F	PS5	8237 (RESERVED)	—	—	96

Figure 3-74: CM195W SCSI Host Adapter Card Address Map (Sheet 1 of 2)

SCSI HOST ADAPTER CARD OUTPUT ADDRESS MAP (Contd)						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x C0300	0x 0700	PS6	DUART MODE REGISTER A	READ/WRITE	16	2
0x C0302	0x 0702	PS6	DUART STATUS REGISTER A	READ	16	2
0x C0302	0x 0702	PS6	DUART CLOCK REGISTER A	WRITE	16	2
0x C0304	0x 0704	PS6	DUART (RESERVED	READ	16	2
0x C0304	0x 0704	PS6	DUART COMMAND REGISTER A	WRITE	16	2
0x C0306	0x 0706	PS6	DUART RECEIVE HOLD REGISTER A	READ	16	2
0x C0306	0x 0706	PS6	DUART TRANSMIT HOLD REGISTER A	WRITE	16	2
0x C0308	0x 0708	PS6	DUART IPC REGISTER	READ	16	2
0x C0308	0x 0708	PS6	DUART AUXILIARY CONTROL REGISTER	WRITE	16	2
0x C030A	0x 070A	PS6	DUART INTERRUPT STATUS REGISTER	READ	16	2
0x C030A	0x 070A	PS6	DUART INTERRUPT MASK REGISTER	WRITE	16	2
0x C030C	0x 070C	PS6	DUART CONTROL, TIMER UPPER REGISTER	READ/WRITE	16	2
0x C030E	0x 070E	PS6	DUART CONTROL, TIMER LOWER REGISTER	READ/WRITE	16	2
0x C0310	0x 0710	PS6	DUART MODE REGISTER B	READ/WRITE	16	2
0x C0312	0x 0712	PS6	DUART STATUS REGISTER B	READ	16	2
0x C0312	0x 0712	PS6	DUART CLOCK REGISTER B	WRITE	16	2
0x C0314	0x 0714	PS6	DUART (RESERVED	READ	16	2
0x C0314	0x 0714	PS6	DUART COMMAND REGISTER B	WRITE	16	2
0x C0316	0x 0716	PS6	DUART RECEIVE HOLD REGISTER B	READ	16	2
0x C0316	0x 0716	PS6	DUART TRANSMIT HOLD REGISTER B	WRITE	16	2
0x C0318	0x 0718	PS6	(RESERVED)	READ/WRITE	16	2
0x C031A	0x 071A	PS6	DUART INPUT PORT	READ	16	2
0x C031A	0x 071A	PS6	DUART OUTPUT PORT	WRITE	16	2
0x C031C	0x 071C	PS6	DUART START COUNT COMMAND	—	—	1
0x C031C	0x 071C	PS6	DUART SET OP BITS	—	—	1
0x C031E	0x 071E	PS6	DUART STOP COUNT COMMAND	—	—	1
0x C031E	0x 071E	PS6	DUART RESET OP BITS	—	—	1
0x C0320	0x 0720	PS6	DUART RESET	WRITE	—	16
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0x C032F	0x 072F	PS6	DUART RESET	WRITE	—	16
0x C0400	0x FF00	80186	80186 CONTROL BLOCK	—	—	256
0x C0420	0x FF20	80186	INTERRUPT CONTROL	READ/WRITE	16	32
0x C0450	0x FF50	80186	TIMER 0 CONTROL	READ/WRITE	16	8
0x C0458	0x FF58	80186	TIMER 1 CONTROL	READ/WRITE	16	8
0x C0460	0x FF60	80186	TIMER 2 CONTROL	READ/WRITE	16	8
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL	READ/WRITE	16	10
0x C04C0	0x FFC0	80186	DMA 0 CONTROL	READ/WRITE	16	12
0x C04D0	0x FFD0	80186	DMA 1 CONTROL	READ/WRITE	16	12
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	READ/WRITE	16	2
0x F8000	—	UCS	ROM	READ/WRITE	16	32K

Figure 3-74: CM195W SCSI Host Adapter Card Address Map (Sheet 2 of 2)

Peripheral Control and Status Register

The CM195W Card contains a 16-bit Peripheral Control and Status Register (PCSR) used to control and monitor certain CM195W functions. The CM195W PCSR bits are defined in the following table.

CM195W PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
15	**BYTE WRITE POINTER**: PCSR15[1] points to the FIFO, FIFO 0 or 1, in which the next byte of data will be written. PCSR15 is incremented after each access by hardware. PCSR15 is zeroed by activating the 80186 Microprocessor Peripheral Chip Select 3 (PSC3).
14	**BYTE READ POINTER**: PCSR14[1] points to the FIFO, FIFO 0 or 1, from which the next byte of data will be read. PCSR14 is incremented after each access by hardware. PCSR14 is zeroed by activating the 80186 Microprocessor Peripheral Chip Select 2 (PSC2).
13	**BYTE EMPTY INDICATOR**: PCSR13[1] indicates if the FIFO pointed to by the Byte Read Pointer is empty. The 80186 Microprocessor checks PCSR13 before attempting to read data from the FIFO. If PCSR13 is set, data read from the FIFO by the 80186 Microprocessor is invalid.
12	**BYTE FULL INDICATOR**: PCSR12[1] indicates if the FIFO pointed to by the Byte Write Pointer is full. The 80186 Microprocessor checks PCSR12 before attempting to write data to the FIFO. If PCSR12 is set, data written to the FIFO by the 80186 Microprocessor is lost.
11	**WORD FULL FLAG 1**: PCSR11[0] is used to indicate if the FIFO containing the most significant byte is full. Additional writes to the word side of the FIFO by the 80186 Microprocessor while PCSR11 is set results in lost data.
10	**WORD FULL FLAG 0**: PCSR10[0] is used to indicate if the FIFO containing the least significant byte is full. Additional writes to the word side of the FIFO by the 80186 Microprocessor while PCSR10 is set results in lost data.
09	**WORD EMPTY FLAG 1**: PCSR09[0] is used to indicate if the most significant byte of the word side of the FIFO is available. PCSR09 is polled prior to an 80186 Microprocessor read of the word side of the FIFO.
08	**WORD EMPTY FLAG 0**: PCSR08[0] is used to indicate if the least significant byte of the word side of the FIFO is available. PCSR08 is polled prior to an 80186 Microprocessor read of the word side of the FIFO.

CM195W PERIPHERAL CONTROL AND STATUS REGISTER (Contd)	
BIT	**DESCRIPTION**
07	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR07[0] maps to the I/O bus signal PINT0[0] and is asserted by the CM195W firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
06	**INT2—SCSI PROTOCOL CONTROLLER CHIP (SPCC) INTERRUPT**: PCSR06[0] is used to indicate the current state of the NCR 5386 SPCC interrupt request. PCSR06 is cleared by reading the 5386 Interrupt Request Register. Addressing PCSR6 (0x 040D) clears (negates) the bit.
05	**NONMASKABLE INTERRUPT**: PCSR05[0] is used to indicate the CM195W received a peripheral fault during a DMA transfer between the FIFO and main memory. Addressing PCSR05 (0x 048D) clears (negates) the bit. On powerup, PCSR05 is undefined and is cleared by firmware.
04	**INT3—8237 DMA COMPLETION INTERRUPT**: PCSR04[0] is used to indicate an end of process has been reached during a DMA transfer from the main memory to the FIFO. PCSR04 is set by the 8237 and is cleared by addressing PCSR04 (0x 048C). On powerup, PCSR04 is undefined and is cleared by firmware.
03	**INT3—8237 DMA COMPLETION INTERRUPT**: PCSR03[0] is used to indicate an end of process has been reached during a DMA transfer from the main memory to the FIFO. PCSR04 is set by the 8237 and is cleared by addressing PCSR03 (0x 048B). On powerup, PCSR03 is undefined and is cleared by firmware.
02	**INT2—SCSI BUS RESET**: PCSR02[0] is set when a SCSI bus reset condition is detected. Addressing PCSR02 (0x 048A) clears the bit; however, the bit remains set as long as the SCSI bus reset condition exists. On powerup, PCSR02 is undefined and is cleared by firmware.
01	**INT1—SYSGEN ATTENTION INTERRUPT**: PCSR01 is set by a CPU system board access of the CM195W Control Register. PCSR01 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the CM195W firmware.
00	**INT0—PRE-SYSGEN/EXPRESS INTERRUPT**: This 80186 Microprocessor interrupt is set by an access of the CM195W ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. PCSR00 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The CM195W Card contains 128K bytes of Dynamic Random Access Memory (DRAM) configured as 64K by 16 bits.

Local ROM

The CM195W Card firmware is in 32K bytes of ROM configured as 16K by 16 bits.

CM195W Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM195W Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0100
DEVICE NAME (dev_name)	SCSI
REQUEST QUEUE SIZE (rq_size)	0x 56
COMPLETION QUEUE SIZE (cq_size)	0x 56
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	1

CM195Y EPORTS CARD

General

The CM195Y Enhanced Peripheral Port Controller (EPORTS) Card provides eight separate, asynchronous serial ports (RS-232C). Functionally, the EPORTS card consists of the Common Input/Output (CIO) circuits, and four Serial Communication Controllers (SCCs). The SCCs function as Dual Universal Asynchronous Receiver/Transmitter (DUART) circuits. The eight asynchronous serial ports are identified as subdevices. DUART 0 (SCC 0) supports subdevices SD0 and SD1; DUART 1 (SCC 1) supports subdevices SD2 and SD3. DUART 2 (SCC 2) supports subdevices SD4 and SD5; DUART 3 (SCC 3) supports subdevices SD6 and SD7. Drivers and receiver circuits are used to interface the DUARTs to MODEMS and/or data terminals (RS-232C). Figure 3-75 is a functional block diagram of the CM195Y EPORTS Card.

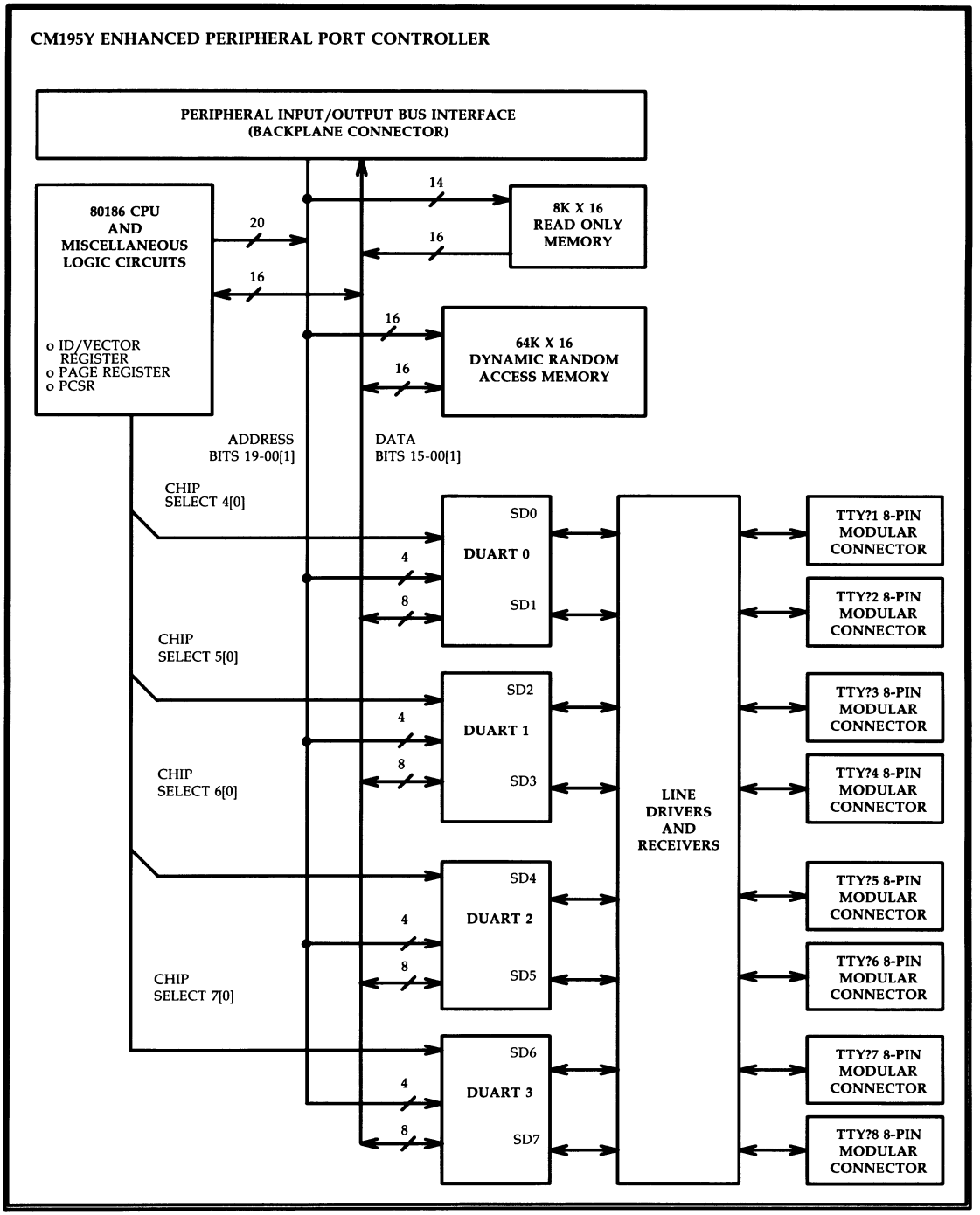


Figure 3-75: CM195Y EPORTS Card — Functional Block Diagram

INTEL 80186 Microprocessor

The intelligence of the EPORTS card is provided by an INTEL 80186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the EPORTS card are described in the following paragraphs. Figure 3-76 shows the EPORTS card address map.

ID/Vector Register

The EPORTS card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit EPORTS card ID code. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the EPORTS card ID code to the high order bits (byte 1) of the ID/Vector Register and waits. The EPORTS card ID code is 0x 0102. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Page Register

The EPORTS card uses a 24-bit I/O address to do main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

EPORTS CARD ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	DRAM (VECTOR TABLE)	READ/WRITE	16	128K
0x 80000	—	MCS	DPDRAM(3B2 MAIN MEMORY)	READ/WRITE	16	128K
0x C0080	0x 0480	PS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PS1	PAGE REGISTER	WRITE	7	1
0x C0084	0x 0484	PS1	PCSR BITS 7—0	READ	8	1
0x C0086	0x 0486	PS1	NOT USED	—	—	—
0x C0088	0x 0488	PS1	PCSR BIT 0 (INT0)	(NOTE 1)	1	—
0x C0089	0x 0489	PS1	PCSR BIT 1 (INT1)	(NOTE 1)	1	—
0x C008A	0x 048A	PS1	PCSR BIT 2 (EOP0)	(NOTE 1)	1	—
0x C008B	0x 048B	PS1	PCSR BIT 3 (EOP1)	(NOTE 1)	1	—
0x C008C	0x 048C	PS1	PCSR BIT 4 (EOP2)	(NOTE 1)	1	—
0x C008D	0x 048D	PS1	PCSR BIT 5 (EOP3)	(NOTE 1)	1	—
0x C008E	0x 048E	PS1	PCSR BIT 6 (NOT USED)	—	—	—
0x C008F	0x 048F	PS1	PCSR BIT 7 (PINT00)	(NOTE 1)	1	—
0x C0100	0x 0500	PS2	DTR REGISTER	READ/WRITE	8	1
0x C0200	0x 0600	PS4	DMAC0	READ/WRITE	8	32
0x C0220	0x 0620	PS4	DMAC1	READ/WRITE	8	32
0x C0240	0x 0640	PS4	DMAC2	READ/WRITE	8	32
0x C0260	0x 0660	PS4	DMAC3	READ/WRITE	8	32
0x C0280	0x 0680	PS5	SCCO (CH B)	READ/WRITE	8	1
0x C0281	0x 0681	PS5	SCCO (CH A)	READ/WRITE	8	1
0x C02A0	0x 06A0	PS5	SCC1 (CH B)	READ/WRITE	8	1
0x C02A1	0x 06A1	PS5	SCC1 (CH A)	READ/WRITE	8	1
0x C02C0	0x 06C0	PS5	SCC2 (CH B)	READ/WRITE	8	1
0x C02C1	0x 06C1	PS5	SCC2 (CH A)	READ/WRITE	8	1
0x C02E0	0x 06E0	PS5	SCC3 (CH B)	READ/WRITE	8	1
0x C02E1	0x 06E1	PS5	SCC3 (CH A)	READ/WRITE	8	1
0x C0300	0x 0700	PS6	SCCIACK	READ	8	1
(NOTE 2)	—	80186	80186 CONTROL BLOCK	READ/WRITE	16	256
0x F8000	—	UCS	ROM	READ	16	32K

NOTES:

1. Bit is cleared by 80186 Microprocessor access.
2. After a reset, this address is an I/O address, 0x 0FF00. It may be reprogrammed to a different address.

LEGEND:

DMAC	DIRECT MEMORY ACCESS CONTROLLER
DPDRAM	DUAL PORT DYNAMIC RANDOM ACCESS MEMORY
DTR	DATA TERMINAL READY
EOP	END OF PROCESS
LCS	LOWER CHIP SELECT
MCS	MEMORY CHIP SELECT
PCSR	PERIPHERAL CONTROL AND STATUS REGISTER
PS	PERIPHERAL SELECT
SCC	SERIAL COMMUNICATION CONTROLLER
SCCIACK	SERIAL COMMUNICATION CONTROLLER INTERRUPT ACKNOWLEDGE
UCS	UPPER CHIP SELECT

Figure 3-76: CM195Y EPORTS Card Address Map

Peripheral Control and Status Register

The EPORTS card contains an 8-bit Peripheral Control and Status Register (PCSR) addressable on the lower data byte of the I/O address (0x 048F—0x 0488). Each address corresponds to a single bit of the PCSR. These bits are reset by an 80186 Microprocessor read or write access except for PCSR6 that is controlled by the Bus Abort Feature (BAF).

EPORTS PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
7	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR7[0] maps to the I/O bus signal PINT0[0] and is asserted by the EPORTS firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
6	**I/O BUS LOCKED**: This bit is normally used for the BAF. EPORTS does not use PCSR6.
5	Used to control the End-of-Page 3 (EOP3) interrupt. Addressing PCSR6 (0x 048D) clears (negates) the bit.
4	Used to control End-of-Page 2 (EOP2) interrupt. Addressing PCSR6 (0x 048C) clears (negates) the bit.
3	Used to control End-of-Page 1 (EOP1) interrupt. Addressing PCSR6 (0x 048B) clears (negates) the bit.
2	Used to control End-of-Page 0 (EOP0) interrupt. Addressing PCSR6 (0x 048A) clears (negates) the bit.
1	**CLEAR INT1**: This 80186 Microprocessor interrupt is set by a system board CPU access of the EPORTS PCSR (attention interrupt). PCSR1 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the EPORTS firmware.
0	**CLEAR INT0**: This 80186 Microprocessor interrupt is set by an access of the EPORTS ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. Bit 0 is cleared during the interrupt service routine by an access of the 80186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The EPORTS card contains 128K bytes of Dual Ported Dynamic Random Access Memory (DPDRAM) configured as 64K by 16 bits. Four Direct Memory Access Controllers (DMACs) are used to provide individual transmit and receive DMA channels for each of the eight RS-232C ports.

Local ROM

The EPORTS card firmware is in 16K bytes of ROM configured as 8K by 16 bits.

CM195Y Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for an EPORTS card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are EPORTS software defined values. As such, the rq_size and cq_size values may differ between versions of EPORTS software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0102
DEVICE NAME (dev_name)	EPORTS
REQUEST QUEUE SIZE (rq_size)	0x 21
COMPLETION QUEUE SIZE (cq_size)	0x 46
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	1
CONSOLE FILE (cons_file)	1
INDIRECT DEVICE (indir_dev)	0

CM521A DIFFERENTIAL SCSI HOST ADAPTER CARD

General

The CM521A Differential Small Computer Systems Interface (SCSI) Host Adapter Card provides an asynchronous, differential interface to the industry standard SCSI bus. Functionally, the CM521A Card consists of the Common Input/Output (CIO) circuits, and SCSI Protocol Controller. Figure 3-77 is a functional block diagram of the CM521A SCSI Host Adapter Card. The CM521A Card consists of the CIO circuits and a SCSI Protocol Controller. The CIO circuits include the following:

- INTEL 80C186 Microprocessor
- Input/Output (I/O) Bus Control
- Identification/Vector (ID/Vector) Register
- Page Register
- Peripheral Control and Status Register (PCSR)
- Local Random Access Memory (RAM)
- Local Read Only Memory (ROM)
- Miscellaneous Circuits.

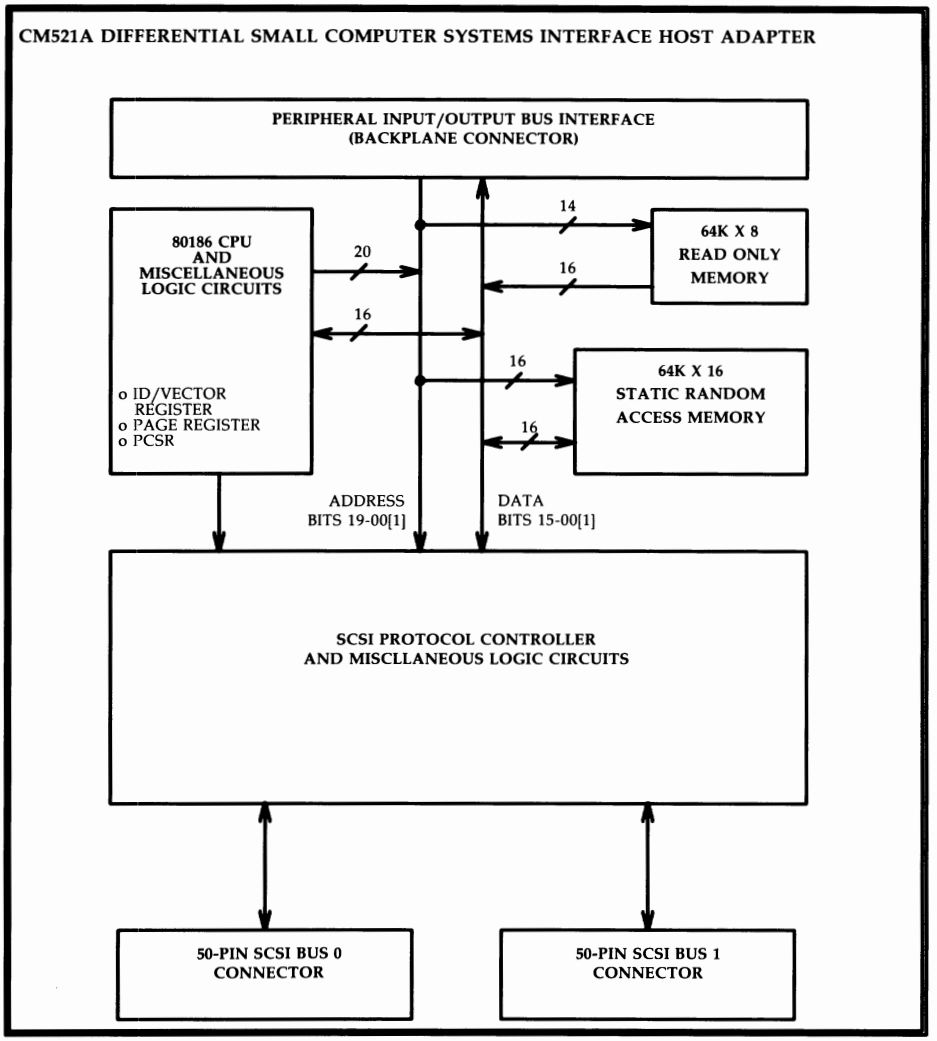


Figure 3-77: CM521A Differential SCSI Host Adapter Card — Functional Block Diagram

INTEL 80C186 Microprocessor

The intelligence of the CM521A Card is provided by an INTEL 80C186, 16-bit microprocessor operating at 8 MHz. Some of the microprocessor features used for the CM521A Card are described in the following paragraphs. Figure 3-78 shows the CM521A Differential SCSI Host Adapter Card address map.

ID/Vector Register

The CM521A Differential SCSI Host Adapter Card ID/Vector Register is a 16-bit register that is used for two functions. Initially the register contains the 16-bit CM521A Card ID code. Later the register contains an 8-bit interrupt vector for the ID code. The interrupt vector is returned in response to an Interrupt Acknowledge (PIAK[0]) signal. On reset, the 80186 Microprocessor writes the CM521A Card ID code to the high order bits (byte 1) of the ID/Vector Register and waits. The CM521A Card ID code is 0x 0100. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Page Register

The CM521A Card uses a 24-bit I/O address to do main memory operations. The lower 17 bits are provided by the 80186 Microprocessor. The most significant 7 bits are provided by the Page Register. The Page Register is a write only register for the 80186 Microprocessor. The two most significant address bits (bits 06 and 05) of the Page Register are always zero. This allows the Page Register to select thirty-two 128 kilobyte segments of main memory. The Page Register is addressed by the 80186 Microprocessor at its I/O address 0x 0482. Bits 06—00 of the Page Register map to Peripheral Physical Address bits 23—17 (PPA23—17[1]).

DIFFERENTIAL SCSI HOST ADAPTER CARD OUTPUT ADDRESS MAP						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x 00000	—	LCS	DRAM (VECTOR TABLE)	READ/WRITE	16	128
0x 00080	—	LCS	DRAM (DEMON)	READ/WRITE	16	59.9K
0x 0F060	—	LCS	DRAM (EDT, SANITY, STATE FLAGS)	READ/WRITE	16	4K
0x 10000	—	LCS	NOT USED	—	—	458K
0x 80000	—	MCS	DPDRAM	READ/WRITE	16	128K
0x A0000	—	MCS	NOT USED	—	—	256K
0x C0000	0x 0400	PCS0	87030 SCSI BUS ID	READ/WRITE	8	1
0x C0001	0x 0401	PCS0	NOT USED	—	8	1
0x C0002	0x 0402	PCS0	87030 CONTROL REGISTER	—	—	1
0x C0004	0x 0404	PCS0	87030 COMMAND REGISTER	—	—	1
0x C0006	0x 0406	PCS0	87030 TRANSFER MODE REGISTER	—	—	1
0x C0008	0x 0408	PCS0	87030 INTERRUPT REGISTER	8	—	1
0x C000A	0x 040A	PCS0	87030 PHASE/DIAGNOSTIC REG.	—	—	1
0x C000C	0x 040C	PCS0	87030 STATUS REGISTER	—	—	1
0x C000E	0x 040E	PCS0	87030 ERROR STATUS REG.	—	—	1
0x C0010	0x 0410	PCS0	87030 PHASE/MODIFIED BYTE CONTROL	—	24	3
0x C0014	0x 0414	PCS0	87030 DATA/TEMPORARY/TRANS. HIGH REG.	—	40	5
0x C001A	0x 041A	PCS0	87030 TRANS. MID REG.	—	8	1
0x C001C	0x 041C	PCS0	87030 TRANS. LOW REG.	—	8	1
0x C001E	0x 041E	PCS0	87030 EXBUFFER REG.	—	8	1
0x C0080	0x 0480	PCS1	ID/VECTOR REGISTER	WRITE	16	2
0x C0082	0x 0482	PCS1	80186 PAGE REGISTER	WRITE	16	1
0x C0084	0x 0484	PCS1	PCSR BITS 15—0	READ	16	2
0x C0088	0x 0488	PCS1	PCSR BIT 0 (INT0)	—	1	
0x C0089	0x 0489	PCS1	PCSR BIT 1 (INT1)	—	1	
0x C008A	0x 048A	PCS1	PCSR BIT 2 (INT2)	—	1	
0x C008B	0x 048B	PCS1	PCSR BIT 3 (INT3)	—	1	
0x C008C	0x 048C	PCS1	PCSR BIT 4 (INT3)	—	1	
0x C008D	0x 048D	PCS1	PCSR BIT 5 (NMI)	—	1	
0x C008E	0x 048E	PCS1	PCSR BIT 6 (INT2)	—	1	
0x C008F	0x 048F	PCS1	PCSR BIT 7 (PINT10)	—	1	
0x C00A2	0x 04A2	PCS1	SCSI TO 3B2 PAGE REGISTER	WRITE	16	1
0x C0C2	0x 04C2	PCS1	3B2 TO SCSI PAGE REGISTER	WRITE	16	1
0x C0100	0x 0500	PCS2	ACCESSING SCSI ID	READ	8	1
0x C0100	0x 0500	PCS2	RESET PARITY	—	—	1
0x C0180	0x 0580	PCS3	RESET SCSI FIFO	—	8	1
0x C0200	0x 0600	PCS4	3B2 FIFO WORD ACCESS	READ/WRITE	16	2
0x C0280	0x 0680	PCS5	8237 CHANNEL 0 ADDRESS REGISTER	READ/WRITE	8	1
0x C0282	0x 0682	PCS5	8237 CHANNEL 0 CONTROL REGISTER	READ/WRITE	8	1
0x C0284	0x 0684	PCS5	8237 CHANNEL 1 ADDRESS REGISTER	READ/WRITE	8	1
0x C0286	0x 0686	PCS5	8237 CHANNEL 1 CONTROL REGISTER	READ/WRITE	8	1
0x C0290	0x 0690	PCS5	8237 COMMAND AND STATUS REGISTER	READ/WRITE	8	1
0x C0292	0x 0692	PCS5	8237 ILLEGAL REQUEST REGISTER	READ/WRITE	8	1
0x C0294	0x 0694	PCS5	8237 ILLEGAL MASK REGISTER	READ/WRITE	3	1
0x C0296	0x 0696	PCS5	8237 ILLEGAL MODE REGISTER	READ/WRITE	8	1
0x C0298	0x 0698	PCS5	8237 ILLEGAL BYTE FLIPFLOP	READ/WRITE	1	—
0x C029A	0x 069A	PCS5	8237 TEMPORARY REG MASTER CLEAR	READ/WRITE	8	1
0x C029C	0x 069C	PCS5	8237 ILLEGAL CLEAR MASK REGISTER	READ/WRITE	1—1	
0x C029E	0x 069E	PCS5	8237 ILLEGAL MASK REGISTER BITS	READ/WRITE	4	
0x C029F	0x 069F	PCS5	8237 (RESERVED)	—	768	96

Figure 3-78: CM521A Differential SCSI Host Adapter Card Address Map (Sheet 1 of 2)

DIFFERENTIAL SCSI HOST ADAPTER CARD OUTPUT ADDRESS MAP (Contd)						
MEMORY ADDRESS	I/O ADDRESS	CHIP SELECT	DESCRIPTION	ACCESS	WIDTH (BITS)	SIZE (BYTES)
0x C0300	0x 0700	PCS6	DUART MODE REGISTER A	READ/WRITE	16	2
0x C0302	0x 0702	PCS6	DUART STATUS REGISTER A	READ	16	2
0x C0302	0x 0702	PCS6	DUART CLOCK REGISTER A	WRITE	16	2
0x C0304	0x 0704	PCS6	DUART (RESERVED	READ	16	2
0x C0304	0x 0704	PCS6	DUART COMMAND REGISTER A	WRITE	16	2
0x C0306	0x 0706	PCS6	DUART RECEIVE HOLD REGISTER A	READ	16	2
0x C0306	0x 0706	PCS6	DUART TRANSMIT HOLD REGISTER A	WRITE	16	2
0x C0308	0x 0708	PCS6	DUART IPC REGISTER	READ	16	2
0x C0308	0x 0708	PCS6	DUART AUXILIARY CONTROL REGISTER	WRITE	16	2
0x C030A	0x 070A	PCS6	DUART INTERRUPT STATUS REGISTER	READ	16	2
0x C030A	0x 070A	PCS6	DUART INTERRUPT MASK REGISTER	WRITE	16	2
0x C030C	0x 070C	PCS6	DUART CONTROL, TIMER UPPER REGISTER	READ/WRITE	16	2
0x C030E	0x 070E	PCS6	DUART CONTROL, TIMER LOWER REGISTER	READ/WRITE	16	2
0x C0310	0x 0710	PCS6	DUART MODE REGISTER B	READ/WRITE	16	2
0x C0312	0x 0712	PCS6	DUART STATUS REGISTER B	READ	16	2
0x C0312	0x 0712	PCS6	DUART CLOCK REGISTER B	WRITE	16	2
0x C0314	0x 0714	PCS6	DUART (RESERVED	READ	16	2
0x C0314	0x 0714	PCS6	DUART COMMAND REGISTER B	WRITE	16	2
0x C0316	0x 0716	PCS6	DUART RECEIVE HOLD REGISTER B	READ	16	2
0x C0316	0x 0716	PCS6	DUART TRANSMIT HOLD REGISTER B	WRITE	16	2
0x C0318	0x 0718	PCS6	(RESERVED)	READ/WRITE	16	2
0x C031A	0x 071A	PCS6	DUART INPUT PORT	READ	16	2
0x C031A	0x 071A	PCS6	DUART OUTPUT PORT	WRITE	16	2
0x C031C	0x 071C	PCS6	DUART START COUNT COMMAND	—	8	1
0x C031C	0x 071C	PCS6	DUART SET OP BITS	—	8	1
0x C031E	0x 071E	PCS6	DUART STOP COUNT COMMAND	—	8	1
0x C031E	0x 071E	PCS6	DUART RESET OP BITS	—	8	1
0x C0320	0x 0720	PCS6	DUART RESET	WRITE	128	16
¦	¦	¦	¦	¦	¦	¦
0x C032F	0x 072F	PCS6	DUART RESET	WRITE	128	16
0x C0400	0x FF00	80186	80186 CONTROL BLOCK	—	2048	256
0x C0420	0x FF20	80186	INTERRUPT CONTROL	READ/WRITE	16	32
0x C0450	0x FF50	80186	TIMER 0 CONTROL	READ/WRITE	16	8
0x C0458	0x FF58	80186	TIMER 1 CONTROL	READ/WRITE	16	8
0x C0460	0x FF60	80186	TIMER 2 CONTROL	READ/WRITE	16	8
0x C04A0	0x FFA0	80186	CHIP SELECT CONTROL	READ/WRITE	16	10
0x C04C0	0x FFC0	80186	DMA 0 CONTROL	READ/WRITE	16	12
0x C04D0	0x FFD0	80186	DMA 1 CONTROL	READ/WRITE	16	12
0x C04FE	0x FFFE	80186	RELOCATION REGISTER	READ/WRITE	16	2
0x F8000	—	UCS	EPROM	READ/WRITE	16	32K

Figure 3-78: CM521A Differential SCSI Host Adapter Card Address Map (Sheet 2 of 2)

Peripheral Control and Status Register

The CM521A Card contains a 16-bit Peripheral Control and Status Register (PCSR) used to control and monitor certain CM521A functions. The CM521A Card PCSR bits are defined in the following table.

CM521A PERIPHERAL CONTROL AND STATUS REGISTER	
BIT	**DESCRIPTION**
15	**BYTE WRITE POINTER**: PCSR15[1] points to the FIFO, FIFO 0 or 1, in which the next byte of data will be written. PCSR15 is incremented after each access by hardware. PCSR15 is zeroed by activating the 80186 Microprocessor Peripheral Chip Select 3 (PSC3).
14	**BYTE READ POINTER**: PCSR14[1] points to the FIFO, FIFO 0 or 1, from which the next byte of data will be read. PCSR14 is incremented after each access by hardware. PCSR14 is zeroed by activating the 80C186 Microprocessor Peripheral Chip Select 2 (PSC2).
13	**BYTE EMPTY INDICATOR**: PCSR13[1] indicates if the FIFO pointed to by the Byte Read Pointer is empty. The 80C186 Microprocessor checks PCSR13 before attempting to read data from the FIFO. If PCSR13 is set, data read from the FIFO by the 80C186 Microprocessor is invalid.
12	**BYTE FULL INDICATOR**: PCSR12[1] indicates if the FIFO pointed to by the Byte Write Pointer is full. The 80C186 Microprocessor checks PCSR12 before attempting to write data to the FIFO. If PCSR12 is set, data written to the FIFO by the 80C186 Microprocessor is lost.
11	**WORD FULL FLAG 1**: PCSR11[0] is used to indicate if the FIFO containing the most significant byte is full. Additional writes to the word side of the FIFO by the 80C186 Microprocessor while PCSR11 is set results in lost data.
10	**WORD FULL FLAG 0**: PCSR10[0] is used to indicate if the FIFO containing the least significant byte is full. Additional writes to the word side of the FIFO by the 80C186 Microprocessor while PCSR10 is set results in lost data.
09	**WORD EMPTY FLAG 1**: PCSR09[0] is used to indicate if the most significant byte of the word side of the FIFO is available. PCSR09 is polled prior to an 80C186 Microprocessor read of the word side of the FIFO.
08	**WORD EMPTY FLAG 0**: PCSR08[0] is used to indicate if the least significant byte of the word side of the FIFO is available. PCSR08 is polled prior to an 80C186 Microprocessor read of the word side of the FIFO.

CM521A PERIPHERAL CONTROL AND STATUS REGISTER (Contd)	
BIT	**DESCRIPTION**
07	**REQUEST SYSTEM BOARD CPU INTERRUPT**: PCSR07[0] maps to the I/O bus signal PINT0[0] and is asserted by the CM521A firmware. When negated [1] by hardware, the interrupt has been acknowledged by the system board CPU. When asserted [0], the interrupt request is pending. A system reset negates the bit to a logic 1 (interrupt acknowledged). Addressing PCSR7[1] (0x 048F) clears (negates) the bit.
06	**SPINTR[1]—SCSI PROTOCOL CONTROLLER CHIP (SPCC) INTERRUPT**: PCSR06[0] is used to indicate the current state of the MB87030 SPCC interrupt request. PCSR06 is cleared by reading the 5386 Interrupt Request Register. Addressing PCSR6 (0x 040D) clears (negates) the bit.
05	**NONMASKABLE INTERRUPT**: PCSR05[0] is used to indicate the CM521A received a peripheral fault during a DMA transfer between the FIFO and main memory. Addressing PCSR05 (0x 048D) clears (negates) the bit. On powerup, PCSR05 is undefined and is cleared by firmware.
04	**82C37 DMA COMPLETION INTERRUPT**: PCSR04[0] is used to indicate an end of process has been reached during a DMA transfer from the FIFO to the main memory. PCSR04 is set by the 82C37 and is cleared by addressing PCSR04 (0x 048C). On powerup, PCSR04 is undefined and is cleared by firmware.
03	**CINT3—82C37 DMA COMPLETION INTERRUPT**: PCSR03[0] is used to indicate an end of process has been reached during a DMA transfer from the main memory to the FIFO. PCSR04 is set by the 82C37 and is cleared by addressing PCSR03 (0x 048B). On powerup, PCSR03 is undefined and is cleared by firmware.
02	**PSSSA0—SYSTEM BOARD SUPPORTS SEQUENTIAL ACCESS**: PCSR02[0] is set when the system board supports sequential access data transfers. Addressing PCSR02 (0x 048A) clears the bit. On powerup, PCSR02 is undefined and is cleared by firmware.
01	**CINT1—SYSGEN ATTENTION INTERRUPT**: PCSR01 is set by a CPU system board access of the CM521A Control Register. PCSR01 is cleared during the interrupt service routine by an access of the 80C186 Microprocessor address 0x 0489. Following a system reset the state of PCSR1 is undefined and is cleared by the CM521A firmware.
00	**CINT0—PRE-SYSGEN/EXPRESS INTERRUPT**: This 80C186 Microprocessor interrupt is set by an access of the CM521A ID/Vector Register (except on an interrupt acknowledge cycle). This interrupt is the SYSGEN and Express Queue interrupt. PCSR00 is cleared during the interrupt service routine by an access of the 80C186 Microprocessor address 0x 0488. Bit 0 is undefined on powerup and is cleared by the firmware.

Local RAM

The CM521A Card contains 64K bytes of Static Random Access Memory (SRAM) configured as 32K by 16 bits.

Local ROM

The CM521A Card firmware is in 64K bytes of ROM configured as 32K by 16 bits.

CM521A Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM521A Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 0100
DEVICE NAME (dev_name)	SCSI
REQUEST QUEUE SIZE (rq_size)	0x 56
COMPLETION QUEUE SIZE (cq_size)	0x 56
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	1
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	1

CM522A VCACHE CARD

General

The CM522A Virtual Cache (VCACHE) Card stores instructions and data for the Central Processing Unit (CPU). Electrically, the virtual cache is accessed between the CPU and the main memory and operates in parallel with the virtual to physical translation of the Memory Management Unit (MMU). When the CPU makes a memory address request, the virtual cache compares the requested memory address to the addresses currently stored in its own memory to see if there is a match.

If the requested address is in the virtual cache, the information is sent to the CPU and the request is halted before it goes to memory through the MMU. This is accomplished by returning the "data ready" signal to the CPU and canceling the control signals that would have gone to the main memory.

If the virtual cache makes the comparison and determines it does not have the data, then it remains passive and the request is passed on to main memory through the MMU as though the virtual cache were not present. The block diagram for the VCACHE card is shown in Figure 3-79.

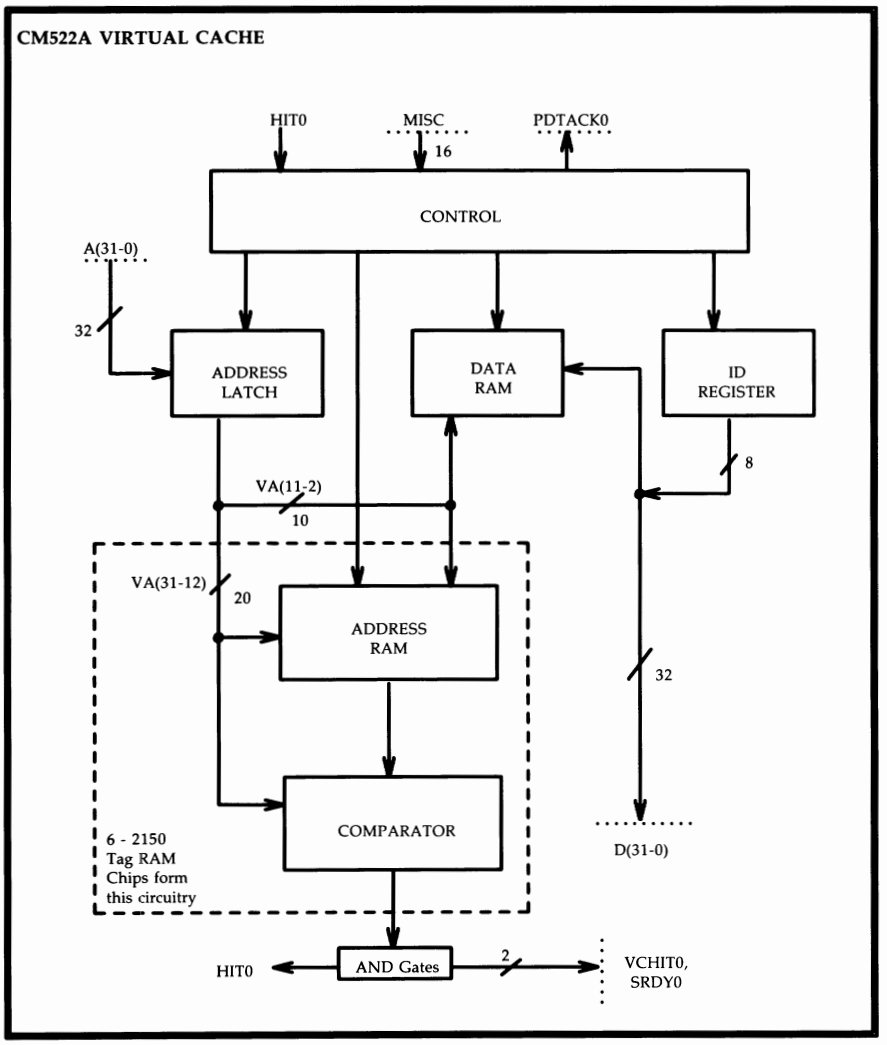


Figure 3-79: CM522A VCACHE Card — Functional Block Diagram

Address Spectrum

The VCACHE card provides "pulse points" to control the operation of the cache. By accessing the addresses shown in Figure 3-80, the listed operations are performed.

ADDRESS	OPERATION	ACCESS
0x1C00000	READ ID REGISTER	READ
0x1C00004	TURN VCACHE OFF	READ/WRITE
0x1C00008	TURN VCACHE ON	READ/WRITE
0x1C0000C	FLUSH ENTIRE CACHE	READ/WRITE
0x1C00010	TURN DIAGNOSTIC MODE OFF	READ/WRITE
0x1C00014	TURN DIAGNOSTIC MODE ON	READ/WRITE
0x1C00018	UNUSED	READ/WRITE
0x1C0001C	FLUSH DATA CACHE	READ/WRITE
0x1C02000 ⋮ 0x1C03FFF	RAM	READ/WRITE

Figure 3-80: CM522A VCACHE Card Address Map

ID Register

The VCACHE card provides a one byte ID Register at byte 0 of address 0x1C00000. Reading this register will return the ID of 0x00.

CM522A Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM522A Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x FE00
DEVICE NAME (dev_name)	VCACHE
REQUEST QUEUE SIZE (rq_size)	0x 00
COMPLETION QUEUE SIZE (cq_size)	0x 00
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	0
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	0
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM524A PROCESSING ELEMENT CARD

General

The CM524A Processing Element (PE) Card improves system performance by providing another processing unit similar to that of the system board. The CM524A contains a Central Processing Unit (CPU), Memory Management Unit (MMU), and Math Acceleration Unit (MAU), and 24-megahertz clock to form the secondary processing unit.

The PE feature requires UNIX System V Release 3.2.2 or later and a CM519B or CM519C Backplane. Also, the Multiprocessor Enhancement Utilities software must be installed before any system performance can be obtained.

The major circuits of the CM524A Card are listed below:

- A WE 32200 chipset processing unit (CPU, MMU, MAU)
- An ID Register
- A Control Status Register (CSR)
- A 24-MHz oscillator.

The block diagram for the CM524A PE Card is shown in Figure 3-81.

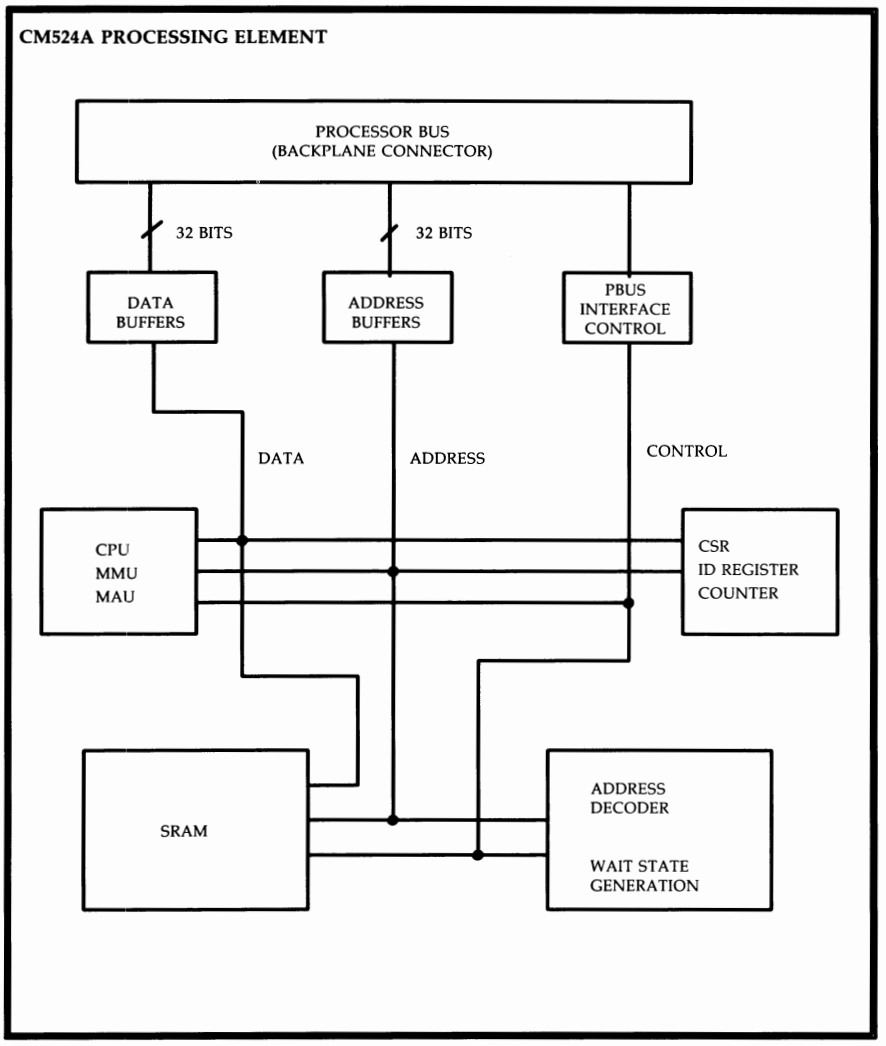


Figure 3-81: CM524A PE Card — Functional Block Diagram

Address Spectrum

Figure 3-82 lists the board addresses for the main circuits on the PE card.

ADDRESS	DESCRIPTION	SIZE (BYTES)
0x00000000-0x00008FFF	SRAM	32K
0x00010000-0x00010048	CSR	128
0x00014003	ID REGISTER	1
0x0004F000-0x0004FFFF	MMU	4K
0x0004B000	COUNTER	2
0x02000000-0x05FFFFFF	MAINSTORE	64M
0xC0F00000-0xC0FFFFFF	RESERVED	1M

Figure 3-82: CM524A PE Card Address Map

ID/Vector Register

The CM524A Card ID/Vector Register is a 16-bit register that is used for two functions. The CM524A Card ID code is 0x fe01. Initially the register contains the lower byte (0x01) of the CM524A Card ID code. The 0xfe is supplied by firmware. Later the register contains an 8-bit interrupt vector for the ID code. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Control Status Register

The CM524A Card contains a 16-bit Control Status Register (CSR) used to control and monitor certain CM524A functions. Each bit is readable/writable. During the read operation, it is output to the bus as 32 bits with the upper 16 bits unknown.

The write operation will only write the specified bit. The CM524A Card CSR bits are defined in the following table.

CM524A CONTROL STATUS REGISTER	
BIT	**DESCRIPTION**
15	**ADPINT10**: This bit is set under program control. When set, a level 10 interrupt will be generated to the PE card CPU. It must be cleared under program control. After a powerup reset, this bit will be cleared. This bit is required by the common PBus interface.
14	**ADPINT12**: This bit is set under program control. When set, a level 12 interrupt will be generated to the PE card CPU. It must be cleared under program control. After a powerup reset, this bit will be cleared. This bit is required by the common PBus interface.
13	**ADPINT15**: This bit is set under program control. When set, a level 15 interrupt will be generated to the PE card CPU. It must be cleared under program control. After a powerup reset, this bit will be cleared. This bit is required by the common PBus interface.
12	**ADPNMI**: This bit is set under program control. When set, a nonmaskable interrupt will be generated to the PE card CPU. It will be cleared through hardware after being acknowledged. After a powerup reset, this bit will be cleared. This bit is required by the common PBus interface.
11	**ULFLT**: This bit is set by hardware when the PE card encounters an alignment fault condition. It is cleared under program control. After a powerup reset, the state of this bit is indeterminate.
4-10	**RESERVED**: These bits and their corresponding addresses are reserved for the PBus Common Interface. They will always be returned as unknown when read.
03	**ERROR**: This bit should be set whenever the PE card generates or detects any error condition on the PBus. Since the PE card does not generate UFLT0 or UFAIL0, it is only set by hardware when the PE card encounters a fault on the BUB when it is accessing main memory. Note that in the case of a BUB fault while the PE card is accessing memory, an external memory exception will be generated to the PE card CPU. This bit is cleared under program control. After a powerup reset, the state of this bit is indeterminate. This bit is required by the common PBus interface.
02	**OPINT15**: This bit can be set under program control. When set, it will cause a level 15 interrupt to be sent over the PBus to the system CPU. The bit is also cleared under program control. After a PE card reset, this bit will be cleared. This bit is required by the common PBus interface.
01	**HALT**: This bit is automatically set on PE card reset, causing the PE card processor to remain in a quiescent state until the bit is cleared under program control. In addition, this bit can be set under program control. This will provide the system with a means to synchronously inhibit the PE card from accessing the PBus. Clearing the bit after being set will allow the PE card to start execution where it left off when it was set. (Note that the PBus connector inhibit will turn off the board asynchronously and should not be used during normal operation.) This bit is required by the common PBus interface.
00	**RESET**: This bit can be written under program control to reset the PE card. It is automatically cleared on uMPB reset. This bit is required by the common PBus interface.

CM524A Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM524A Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x fe01
DEVICE NAME (dev_name)	MPB
REQUEST QUEUE SIZE (rq_size)	0x 00
COMPLETION QUEUE SIZE (cq_size)	0x 00
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	0
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

CM525B VMEbus CARD

The Versa Modula Europa bus (VMEbus) is an industry standard bus for a variety of character and networking controllers. The CM525B VMEbus Card provides the circuit interface between the 3B2 computer Buffered Microbus (BUB) backplane slot and the VMEbus System Controller.

The CM525B VMEbus Card is a double-width card measuring 13.0 inches wide by 7.4 inches deep. The card contains four, 37-pin D-type connectors to provide the connection to the VMEbus System Controller. Connector pinout information is provided in Appendix B. The major components of the CM525B Card are listed below.

- A 16-MHz internal clock
- Data transfer circuitry
- Transfer control logic circuitry
- Interrupt handling circuitry.

The functional block diagram for the VMEbus card is shown in Figure 3-83.

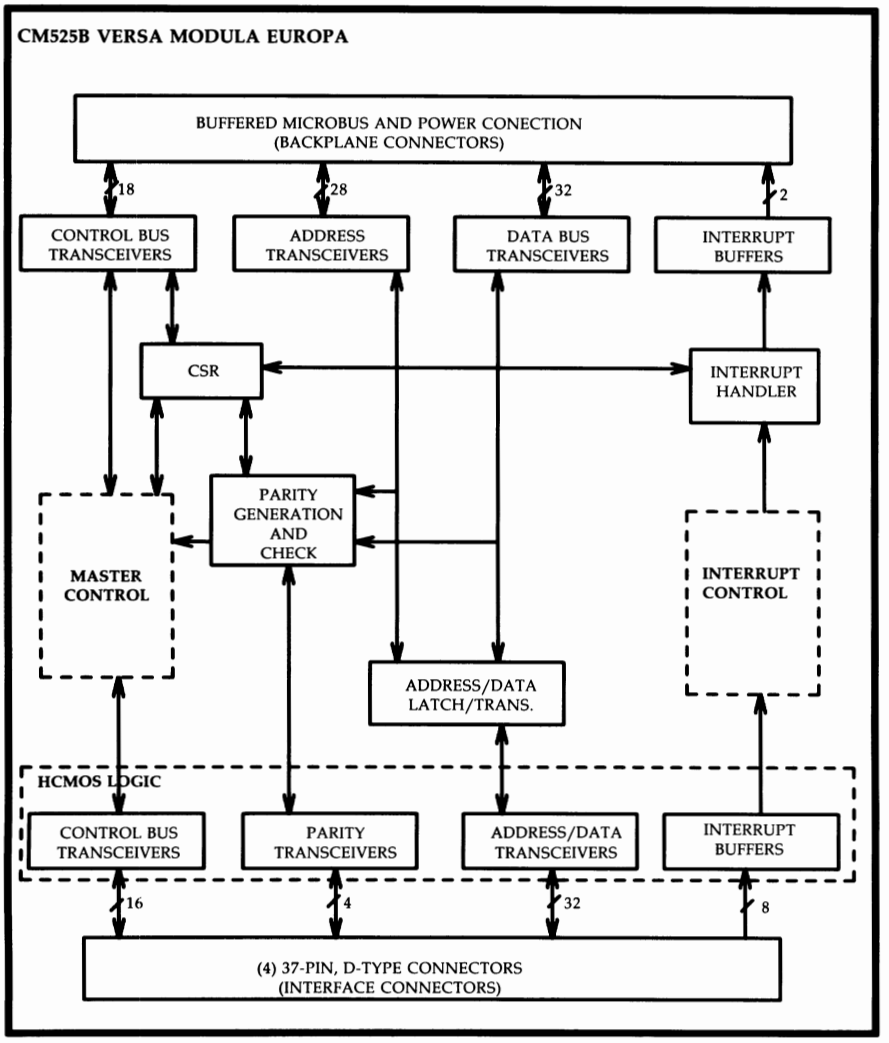


Figure 3-83: CM525B VMEbus Card — Functional Block Diagram

Address Spectrum

The address spectrum for the VMEbus card is 32 megabytes. As shown in Figure 3-84, 16 megabytes are dedicated to the VMEbus spectrum where VME target controllers will reside.

ADDRESS	DESCRIPTION	ACCESS	WIDTH (BITS) [NOTE 1]
0x0000000-0x0008FFF	VME SYSTEM CONTROLLER ADDRESS SPECTRUM	READ/WRITE	8,16,32
0x0010000-0x001007F	CONTROL AND STATUS REGISTER	READ/WRITE	8,16
0x0014000	ID REGISTER	READ	8
0x0032000-0x0033FFF	XEDT SRAM	READ/WRITE	8,16,32
0x0040000	INTERRUPT CONTROL MASTER CLEAR	WRITE	8
0x0040004	INTERRUPT CONTROL END OF SERVICE	WRITE	8
0x0041000	MASK REGISTER (IMR)	READ/WRITE	8
0x0042000	IN-SERVICE REGISTER (ISR)	READ/WRITE	8
0x0043000	PENDING REGISTER (IPR)	READ/WRITE	8
0x0044000	SOFT INTERRUPT ACKNOWLEDGE REGISTER	READ	8
0x0050000	ADDRESS LATCH (AL)	READ/WRITE	32
0x0052000	DATA LATCH (DL)	READ/WRITE	32
0x0062000	CLEAR CURRENT INTERRUPT (CCIR) [NOTE 2]	WRITE	8
0x1000000-0x1FFFFFF	16 MEGABYTE VMEBUS	READ/WRITE	8,16,32

NOTES:

1. This is the largest quantity of data that can be accessed at the location. All data should read and write with 32-bit accesses to ensure proper alignment (except SRAM).
2. A write to this location clears the bit in the IPR that corresponds to the highest priority bit in the ISR.

Figure 3-84: CM525B VMEbus Card Address Map

ID/Vector Register

The CM525B Card ID/Vector Register is an 8-bit, hard-wired, read only buffer. The buffer contents (0x 01) are read on receive data bits 07—00 (RD07—00) and controlled by ID register chip select from the host address decoder circuit.

Control Status Register

The CM525B Card contains a 26-bit Control and Status Register (CSR). The CSR is a modified version of the standard CSR for a buffered microbus peripheral. For normal operation, each bit is individually controlled by hardware, firmware/software, or both. For diagnostic purposes, each bit is designed to be individually written (set or clear) by firmware/software. This is accomplished by performing a byte write to the specified address plus three and driving a "1" or "0" onto bit 0 of byte 3.

The CSR is read by performing a 32-bit read access at the base address (0x 0010000). The CSR bits are defined in the following table.

VME CONTROL AND STATUS REGISTER BIT ASSIGNMENTS

BIT	DESCRIPTION	WRITE ADDRESS	INITIAL STATE	CONTROL				
25	XBUS INTERRUPT BUFFER ENABLE	—		HS				SR
24	UNEQUIPPED ADDRESS ERROR	0x 0010060	CLEAR	HS		PC		
23	DIRECTOR FAULT	0x 001005C	CLEAR	HS		PC		
22	RESERVED	0x 0010058						
21	RESERVED	0x 0010054						
20	XBUS REQUEST LOCK	0x 0010050	CLEAR		PS	PC	CR	
19	INHIBIT XBUS RESERVATION	0x 001004C	OPTIONAL		PS	PC		SR
18	RESERVED	0x 0010048						
17	XBUS RESET	0x 0010044	CLEAR		PS	PC	CR	
16	TRANSACTION DIRECTION	0x 0010040	—	HS		PC		
15	RECEIVED XBUS ERROR	0x 001003C	CLEAR	HS		PC		
14	RECEIVED BUBUS FAULT	0x 0010038	CLEAR	HS		PC		
13	RESERVED	0x 0010034						
12	INHIBIT XBUS PARITY	0x 0010030	CLEAR		PS	PC		SR
11	RESERVED	0x 001002C						
10	RESERVED	0x 0010028						
9	RESERVED	0x 0010024						
8	LEVEL 10 INTERRUPT	0x 0010020	CLEAR	HS	PS		CR	
7	RESERVED	0x 001001C						
6	DATA PARITY ERROR	0x 0010018	CLEAR	HS		PC		
5	ADDRESS PARITY ERROR	0x 0010014	CLEAR	HS		PC		
4	INHIBIT ERROR REPORTING	0x 0010010	CLEAR		PS	PC		SR
3	ERROR DETECTED	0x 001000C	CLEAR	HS		PC		
2	LEVEL 15 INTERRUPT	0x 0010008	CLEAR	HS		PC		
1	HALT	0x 0010004	CLEAR		PS	PC	CR	
0	RESET	0x 0010000	CLEAR	HC	PS		CR	

LEGEND:

CR	Cleared by "system reset" signal
HC	Cleared by hardware
HS	Set by hardware
PC	Cleared by programmed control
PS	Set by programmed control
SR	Set by "system reset" signal

Local RAM

The CM525B Card contains 32K bytes of Static Random Access Memory (SRAM) configured as 8K by 32 bits.

CM525B Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM525B Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x 1FF01
DEVICE NAME (dev_name)	VXI
REQUEST QUEUE SIZE (rq_size)	0x 0
COMPLETION QUEUE SIZE (cq_size)	0x 0
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	0
BOARD SIZE (brd_size)	1
SMART BOARD (smrt_brd)	0
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	1

CM527A MULTIPROCESSOR ENHANCEMENT CARD

The CM527A Multiprocessor Enhancement (MPE) Card improves system performance by providing another processing unit similar to that of the system board. The CM527A Card contains a Central Processing Unit (CPU), Memory Management Unit (MMU), and Math Acceleration Unit (MAU), and 6-kilobyte virtual cache (4-kilobyte instruction and 2-kilobyte data) to form the secondary processing unit.

The Multiprocessor Enhancement Utilities software must be installed before any system performance can be obtained.

The major circuits of the CM527A Card are listed below:

- A WE 32100 chipset processing unit (CPU, MMU, MAU)
- An Identification (ID) Register
- A Control Status Register (CSR)
- A oscillator compatible for 18 through 22 MHz.

The block diagram for the CM527A MPE Card is shown in Figure 3-85.

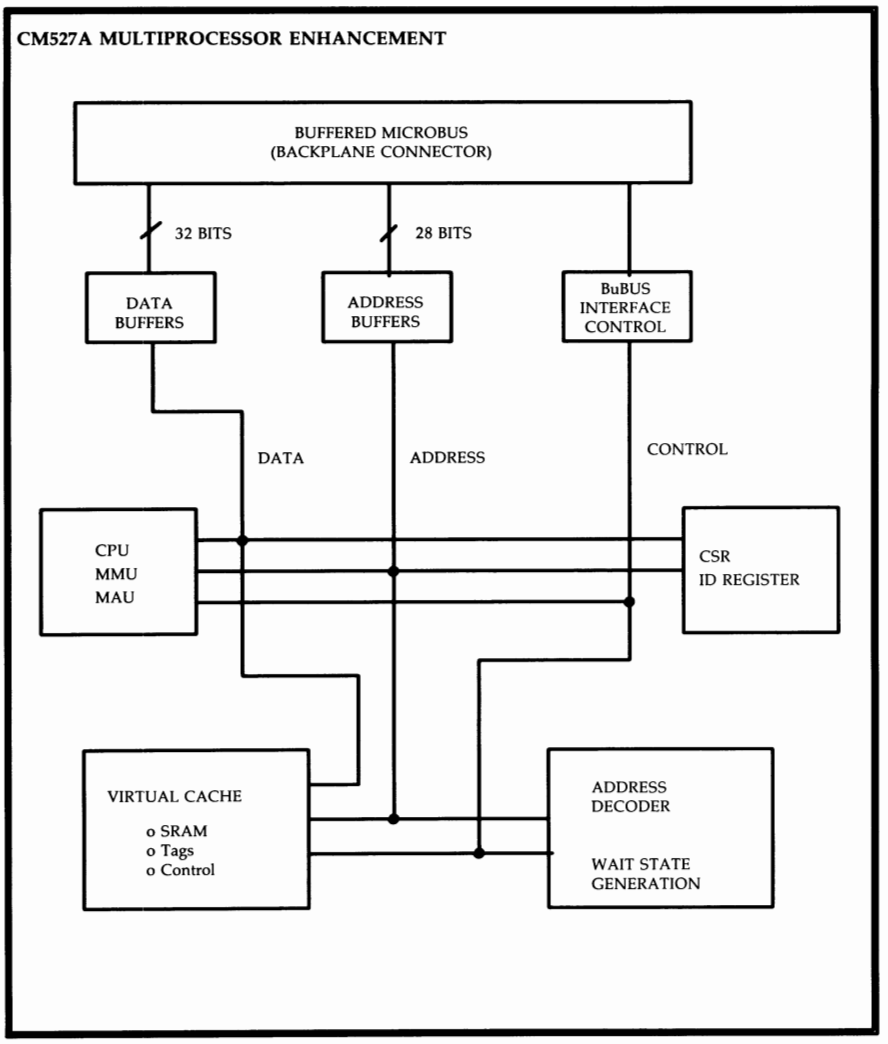


Figure 3-85: CM527A MPE Card — Functional Block Diagram

Address Spectrum

Figure 3-86 lists the board addresses for the main circuits on the MPE card.

ADDRESS	DESCRIPTION	SIZE (BYTES)
0x00000000-0x00001FFF	SRAM	8K
0x00010000-0x0001004B	CSR	128
0x00014000	ID REGISTER	1
0x0004F000-0x0004FFFF	MMU	4K
0x02000000-0x11FFFFFF	MAINSTORE	256M
0xC0F00000-0xC0FFFFFF	RESERVED	1M
0xFFFFFFFC-0xFFFFFFFF	DGN. RESERVED	1 word

Figure 3-86: CM527A MPE Card Address Map

ID/Vector Register

The CM527A Card ID/Vector Register is a 16-bit register that is used for two functions. The CM527A Card ID code is 0x ff00. Initially the register contains the lower byte (0x00) of the CM527A Card ID code. The 0xff is supplied by firmware. Later the register contains an 8-bit interrupt vector for the ID code. During system self-configuration, the system board CPU polls each feature card slot. This polling reads the ID/Vector Register. The two bytes of the ID/Vector Register form a unique 16-bit ID code of the card.

Control Status Register

The CM527A Card contains a 16-bit Control Status Register (CSR) used to control and monitor certain CM527A functions. Each bit is readable/writable. During the read operation, it is output to the bus as 32 bits with the upper 16 bits unknown.

The write operation will only write the specified bit. The CM527A Card CSR bits are defined in the following table.

CM527A CONTROL STATUS REGISTER	
BIT	**DESCRIPTION**
15	**RESERVED**: This bit is reserved for future needs. This bit will always return a "0" and can not be modified.
14	**VCOFF**: When set, the virtual cache is turned OFF. This bit is both set and cleared under program control. After a powerup reset, this bit is set. Also, two CSR addresses are provided to flush the entire virtual cache (0x10044) or flush the data section of the virtual cache (0x10048).
13	**ADPINT15**: This bit is set under program control. When set, a level 15 interrupt will be generated to the MPE card CPU. It must be cleared under program control. After powerup reset, this bit is indeterminate.
12	**RESERVED**: This bit is reserved for future needs. This bit will always return a "0" and can not be modified.
11	**ALFLT**: This bit is set by hardware when the MPE card encounters an alignment fault condition. It is cleared under program control. After a powerup reset, the state of this bit is indeterminate.
4-10	**RESERVED**: These bits and their corresponding addresses are reserved for the BUB Common Interface. They will always be returned as "0" when read.
03	**ERROR**: This bit should be set whenever the MPE card generates or detects any error condition on the BUB. Since the MPE card does not generate BFLT0 or BFAIL0, it is only set by hardware when the MPE card encounters a fault on the BUB when it is accessing main memory. Note that in the case of a BUB fault while the MPE card is accessing memory, an external memory exception will be generated to the MPE card CPU. This bit is cleared under program control. After powerup reset, the state of this bit is indeterminate.
02	**OPINT15**: This bit can be set under program control. When set, it will cause a level 15 interrupt to be sent over the BUB to the system CPU. The bit is also cleared under program control. After a powerup reset, this bit will be cleared.
01	**HALT**: This bit is automatically set on MPE card reset, causing the MPE card processor to remain in a quiescent state until the bit is cleared under program control. In addition, this bit can be set under program control. This will provide the system with a means to synchronously inhibit the MPE card from accessing the BUB. Clearing the bit after being set will allow the MPE card to start execution where it left off when it was set. (Note that the BUB connector inhibit will turn off the board asynchronously and should not be used during normal operation.)
00	**RESET**: This bit can be written under program control to reset the MPE card. It is automatically cleared on uMPB reset.

CM527A Equipped Device Table Data

The following table shows the Equipped Device Table (EDT) data for a CM527A Card. A value of 0 means NO; a value of 1 means YES. The indirect device (indir_dev) is only applicable to systems equipped with Small Computer System Interface (SCSI). The request queue size (rq_size) and the completion queue size (cq_size) are SCSI software defined values. As such, the rq_size and cq_size values may differ between versions of SCSI software.

EDT ITEM	DATA
IDENTIFICATION CODE (ID_code)	0x ff00
DEVICE NAME (dev_name)	MPB
REQUEST QUEUE SIZE (rq_size)	0x 00
COMPLETION QUEUE SIZE (cq_size)	0x 00
BOOT DEVICE (boot_dev)	0
WORD SIZE (word_size)	1
BOARD SIZE (brd_size)	0
SMART BOARD (smrt_brd)	0
CONSOLE CAPABILITY (cons_cap)	0
CONSOLE FILE (cons_file)	0
INDIRECT DEVICE (indir_dev)	0

FLOPPY DISK DRIVE

Floppy Disk Layout

Figure 3-87 shows the physical layout of a 5.25-inch floppy disk media. The floppy disk has 80 cylinders, numbered 0 through 79. Side 0 is the bottom side of the floppy diskette; side 1 is the top of the floppy diskette.

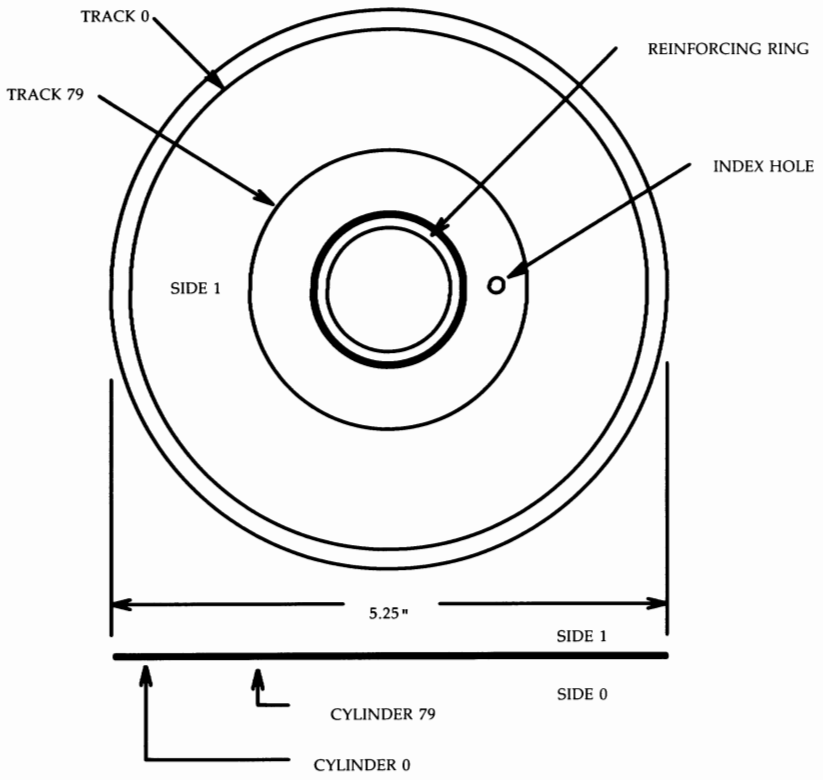


Figure 3-87: Floppy Disk Physical Layout

TANDON Model TM 55-4 Floppy Disk Drive

Figure 3-88 is a functional block diagram of a floppy disk drive. The floppy disk drive consists of a spindle drive mechanism, head positioning mechanism, control logic, and read/write logic. Some of the features are as follows.

Index Generator/Detector

An index pulse is generated once every revolution of the floppy disk to indicate the beginning of a track to the control logic.

Write Protection Logic

When the Write Protect lead is asserted (low) the diskette is write protected by disabling the write logic. When the Write Protect signal is high, the write logic is enabled. A write protect tab on the diskette asserts the Write Protect signal.

Logical Drive/Side Selection

The floppy disk drive is selected by the Drive Select Lead 0 from the Integral Floppy Disk Controller or CM195H Cartridge Tape Controller depending on the application. The drive identification jumpers are set for a drive 0 identification for all 3B2 computer floppy disk configurations. Drive Select leads 3—1 are not connected. The side selection (0 or 1) is controlled by the Side Select lead. Side 0 is selected by a high (1) Side Select signal. Side 1 is selected by a low (0) Side Select signal. (Head 0 is the lower of the two heads.)

Head Positioning Mechanism

The heads are positioned over the desired cylinder by a 4-phase stepper motor. When the drive is selected the read/write heads are positioned to track 0. The Track 0[0] signal is asserted by the positioning logic as long as the heads are positioned at track 0.

Disk Hub Speed Control

The drive hub is maintained at a constant speed of 300 revolutions per minute by a servo-controlled DC motor. Motor speed stablizes at 300 revolutions per minute in less than 250 milliseconds.

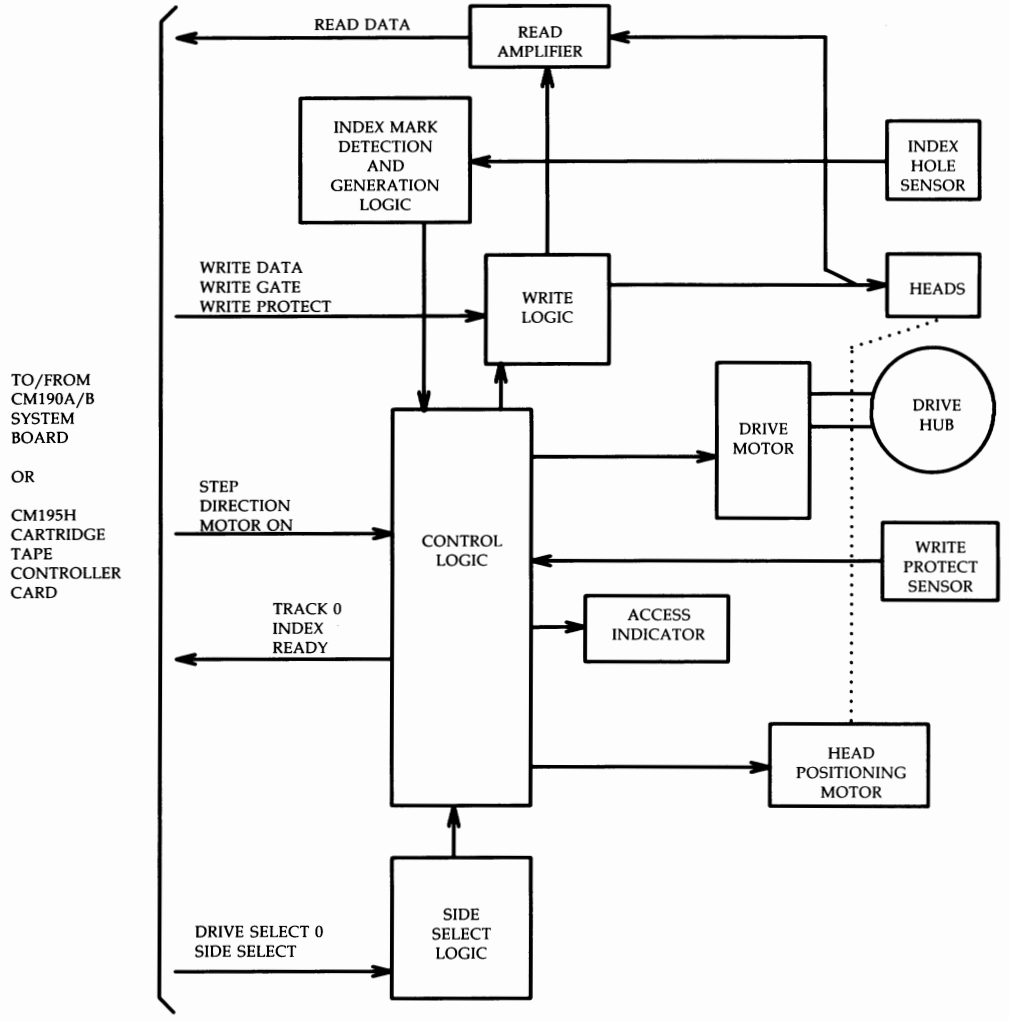


Figure 3-88: Floppy Disk Drive — Functional Block Diagram

23-MEGABYTE CARTRIDGE TAPE DRIVE

Cartridge Tape Format

Figure 3-89 shows the physical layout of the 0.25-inch tape media. The media is configured as six streams (tracks) which are used in a serpentine recording technique. Each stream consists of 255 segments; only 245 segments (0 through 244) are used for the storage of data. Segments are separated by Index Marks.

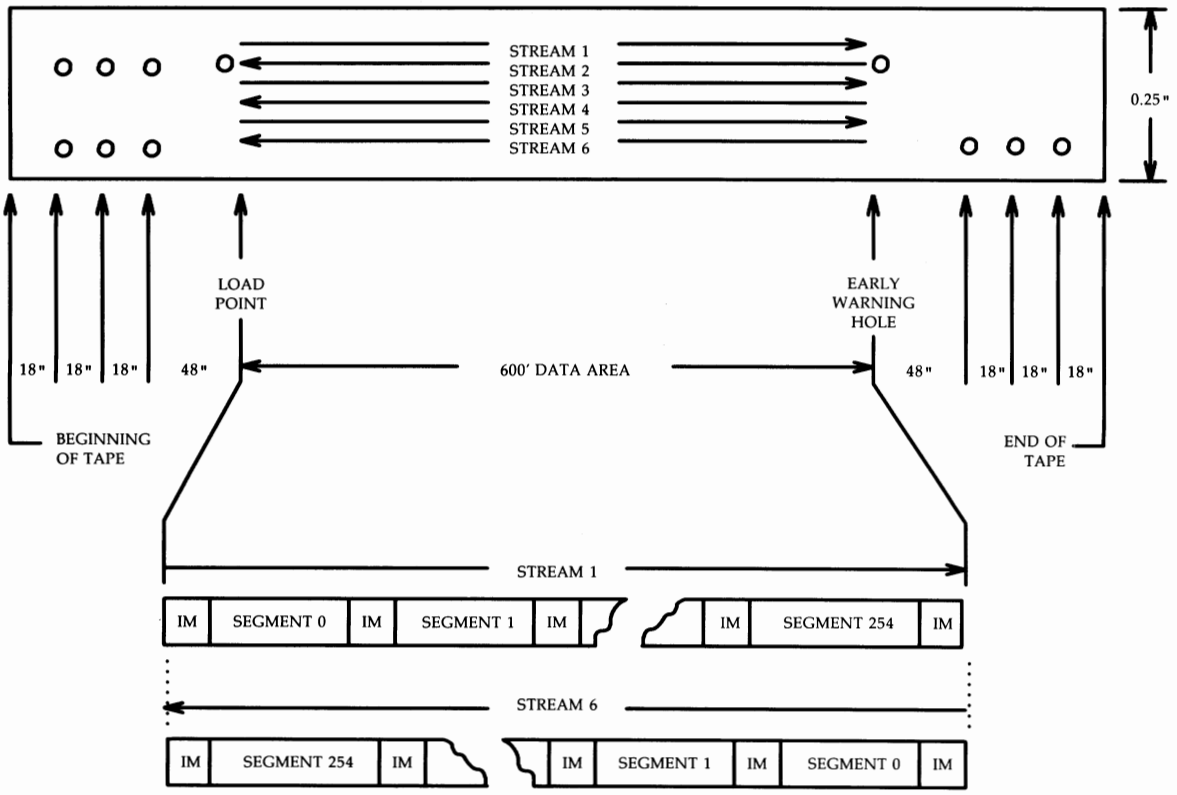


Figure 3-89: Cartridge Tape Physical Layout

23-Megabyte Cartridge Tape Drive

Figure 3-90 is a functional block diagram of a 23-megabyte cartridge tape drive. The cartridge tape drive is a floppy disk-like device, using an SA-450 interface. The cartridge tape drive circuits include the following:

- Index Detector/Generator
- Write Current Driver
- Read Amplifier and Transition Detector
- Write Protection Logic
- Logical Drive/Stream Selection
- Tape Speed/Capstan Control
- End-of-Tape/Beginning-of-Tape (EOT/BOT) Monitor
- Door Lock Solenoid (not used on all versions).

The cartridge tape drive circuits combine to do the following:

- Decode, generate, and emulate floppy disk drive type control signals
- Position the read/write head to the selected stream
- Monitor and control tape speed
- Read/write data from/to the media.

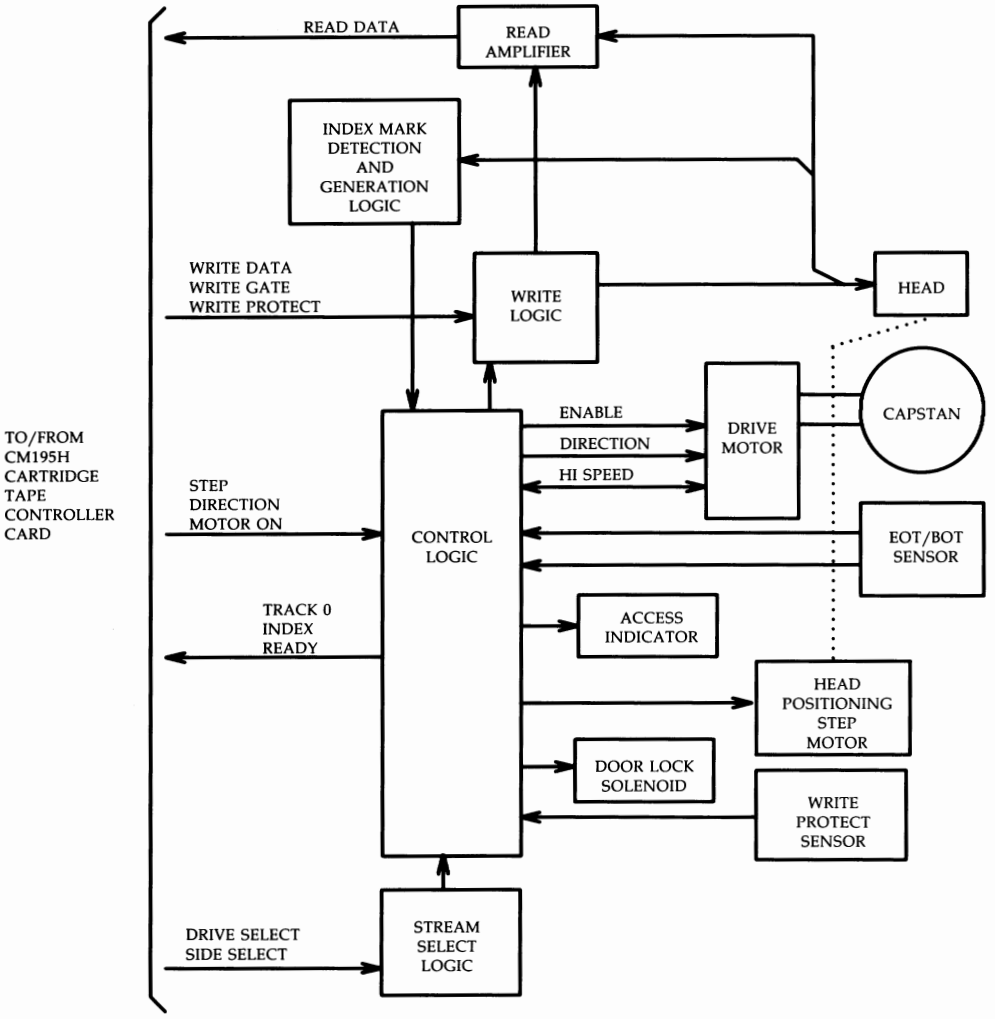


Figure 3-90: 23-Megabyte Cartridge Tape Drive — Functional Block Diagram

Tape Drive

Tape motion is via a capstan driven by a 3-phase, brushless DC motor. The motor speed is controlled by an onboard microprocessor using pulse-width modulated signals. Tape speed is 78 inches per second.

Read/write head positioning is done by a stepper motor controlled by the control logic in response to the Drive/Side Select signals. The read/write head is always returned to a home position before positioning the head to a new stream. This technique provides optimum positioning accuracy. Each position step requires 200 milliseconds.

60-MEGABYTE SCSI CARTRIDGE TAPE DRIVE

Cartridge Tape Format

Figure 3-91 shows the physical layout of the 60-megabyte tape media. The media is configured as nine streams (tracks) which are used in a nonsequential serpentine recording technique. Each stream consists of a preamble, data block marker (1 byte), data field (512 bytes), block address (4 bytes), Cyclical Redundancy Check (CRC) (2 bytes), and a postamble.

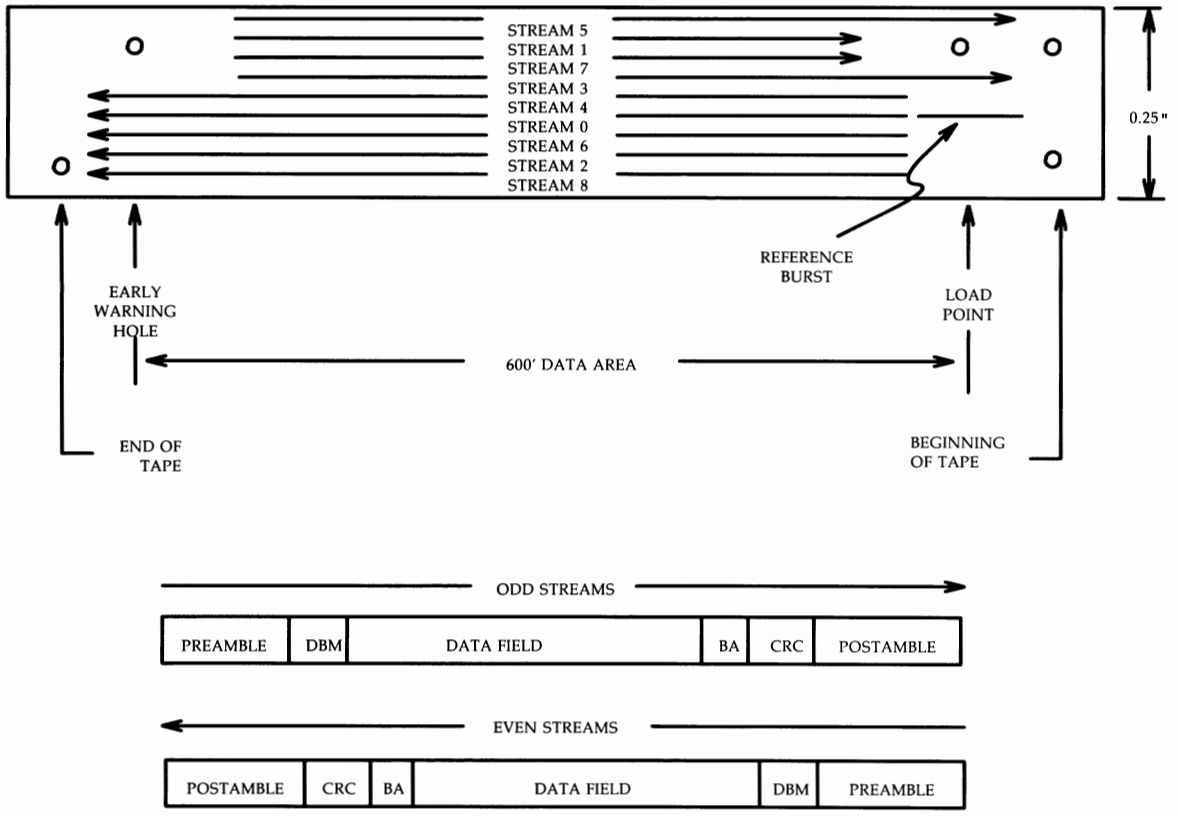


Figure 3-91: 60-Megabyte Cartridge Tape Physical Layout

60-Megabyte Cartridge Tape Drive

Figure 3-92 is a functional block diagram of a 60-megabyte cartridge tape drive. The cartridge tape drive interfaces with the host computer using the Small Computer System Interface (SCSI) industry standard. The cartridge tape drive circuits include the following:

- Drive Motion Control
- Data Formatting Control
- Read/Write Control
- Buffer
- Sensor Group
- Head Stepper
- Capstan Drive Motor
- Read/Write Head.

The cartridge tape drive circuits combine to do the following:

- Decode, generate, and emulate drive control signals
- Position the read/write head to the selected stream
- Monitor and control tape speed
- Read/write data from/to the media.

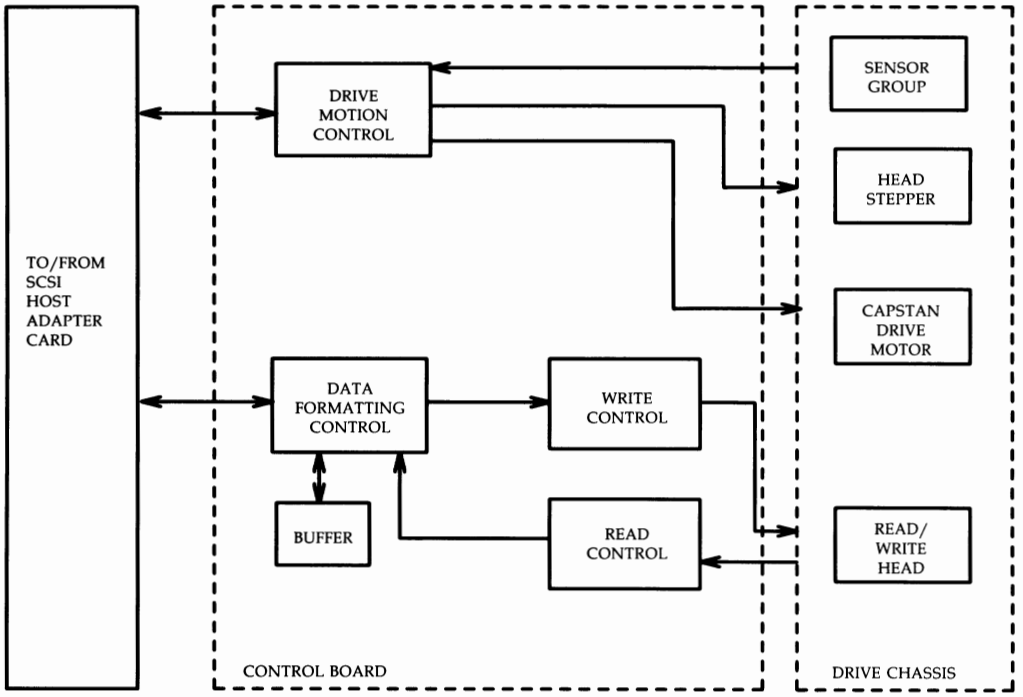


Figure 3-92: 60-Megabyte Cartridge Tape Drive — Functional Block Diagram

Tape Drive

Tape motion is via a capstan driven by a 8-pole, 3-phase, brushless DC motor. The motor speed is controlled by an onboard microprocessor using pulse-width modulated signals. Tape speed is 90 inches per second.

Read/write head positioning is done by a stepper motor controlled by the onboard CPU in response to the interface signals. These signals are converted into discrete mechanical movements referred to as steps. The steps are changed in a logical sequence to move the stepper motor the desired number of steps for the required stream selected.

120-MEGABYTE SCSI CARTRIDGE TAPE DRIVE

Cartridge Tape Format

Figure 3-93 shows the physical layout of the 120-megabyte tape media. The media is configured as 15 streams (tracks) which are used in a nonsequential serpentine recording technique. Each stream consists of a preamble, data block marker (1 byte), data field (512 bytes), block address (4 bytes), Cyclical Redundancy Check (CRC) (2 bytes), and a postamble.

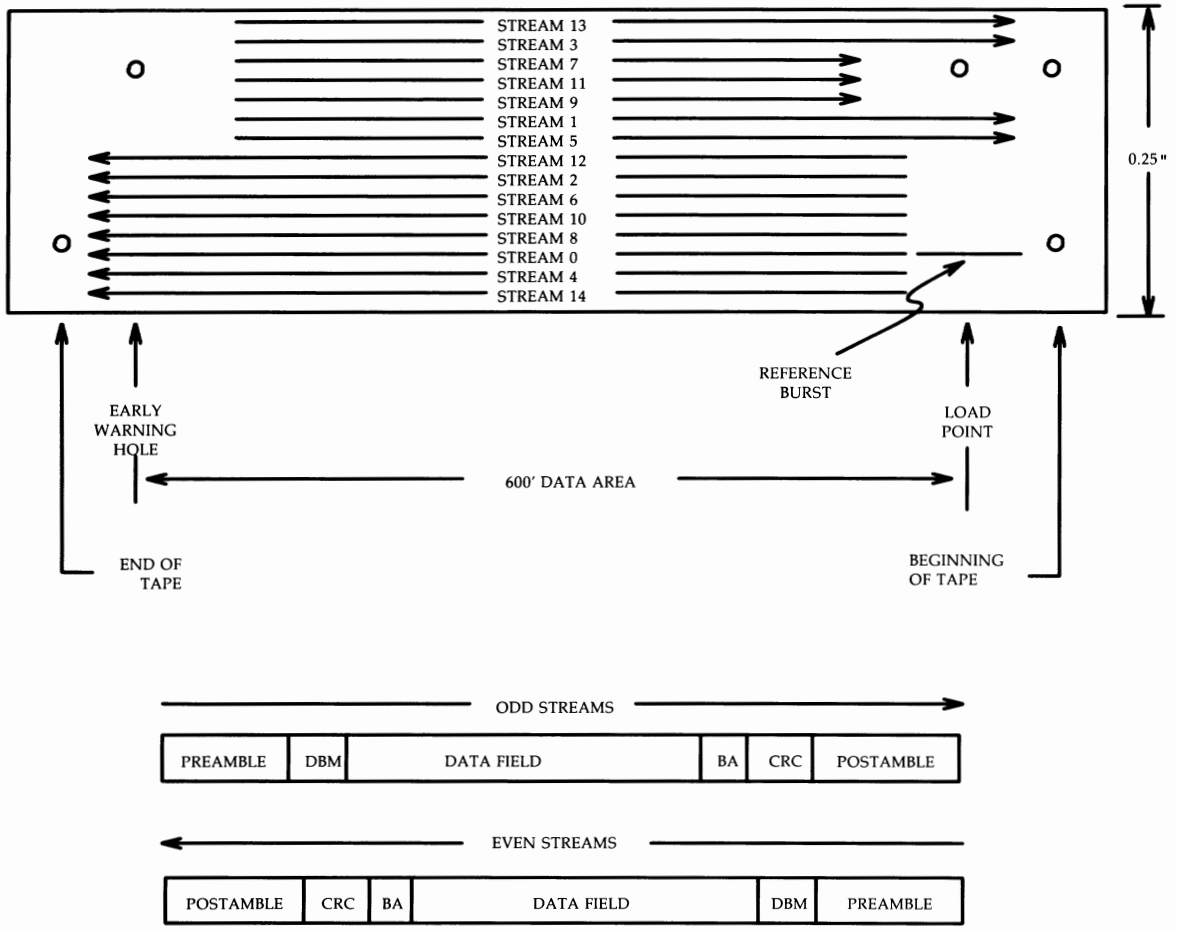


Figure 3-93: 120-Megabyte Cartridge Tape Physical Layout

120-Megabyte Cartridge Tape Drive

Figure 3-94 is a functional block diagram of a 120-megabyte cartridge tape drive. The cartridge tape drive interfaces with the host computer using the Small Computer System Interface (SCSI) industry standard. The cartridge tape drive circuits include the following:

- Drive Motion Control
- Data Formatting Control
- Read/Write Control
- Buffer
- Sensor Group
- Head Stepper
- Capstan Drive Motor
- Read/Write Head.

The cartridge tape drive circuits combine to do the following:

- Decode, generate, and emulate drive control signals
- Position the read/write head to the selected stream
- Monitor and control tape speed
- Read/write data from/to the media.

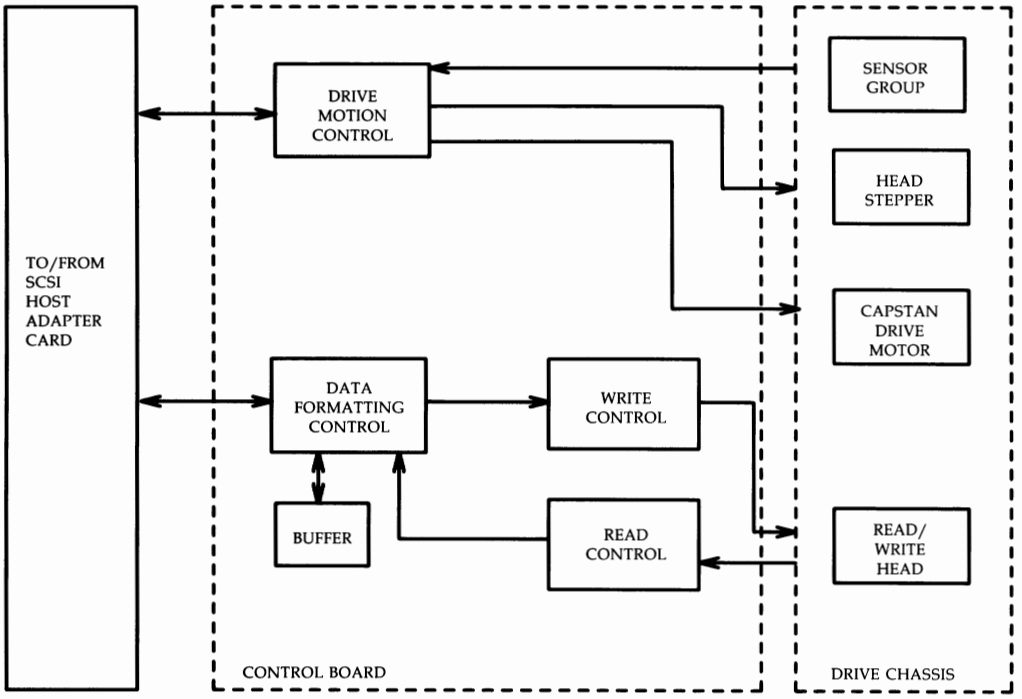


Figure 3-94: 120-Megabyte Cartridge Tape Drive — Functional Block Diagram

Tape Drive

Tape motion is via a capstan driven by a 8-pole, 3-phase, brushless DC motor. The motor speed is controlled by an onboard microprocessor using pulse-width modulated signals. Tape speed is 90 inches per second.

Read/write head positioning is done by a stepper motor controlled by the onboard CPU in response to the interface signals. These signals are converted into discrete mechanical movements referred to as steps. The steps are changed in a logical sequence to move the stepper motor the desired number of steps for the required stream selected.

AT&T SCSI REWRITABLE OPTICAL DISK DRIVE

Optical Disk Format

The format for the rewritable optical disk is like a standard hard disk. The main difference is that the optical disk can be removed. The media is formatted and partitioned as though it were another hard disk.

AT&T SCSI Rewritable Optical Disk Drive

Figure 3-95 is a functional block diagram of a Small Computer System Interface (SCSI) Rewritable Optical Disk Drive. The optical disk drive interfaces with the host computer using the SCSI industry standard. The optical disk drive circuits include the following:

- Mechanical components to rotate the disk and move the head
- Read/Write Laser
- Writing magnet
- Analog circuitry for data separation
- Digital circuitry for drive control, formatting, and controller communication.

The optical disk drive circuits combine to do the following:

- Control motor speed
- Decode, generate, and emulate drive control signals
- Position the read/write laser to the selected position
- Read/write data from/to the media.

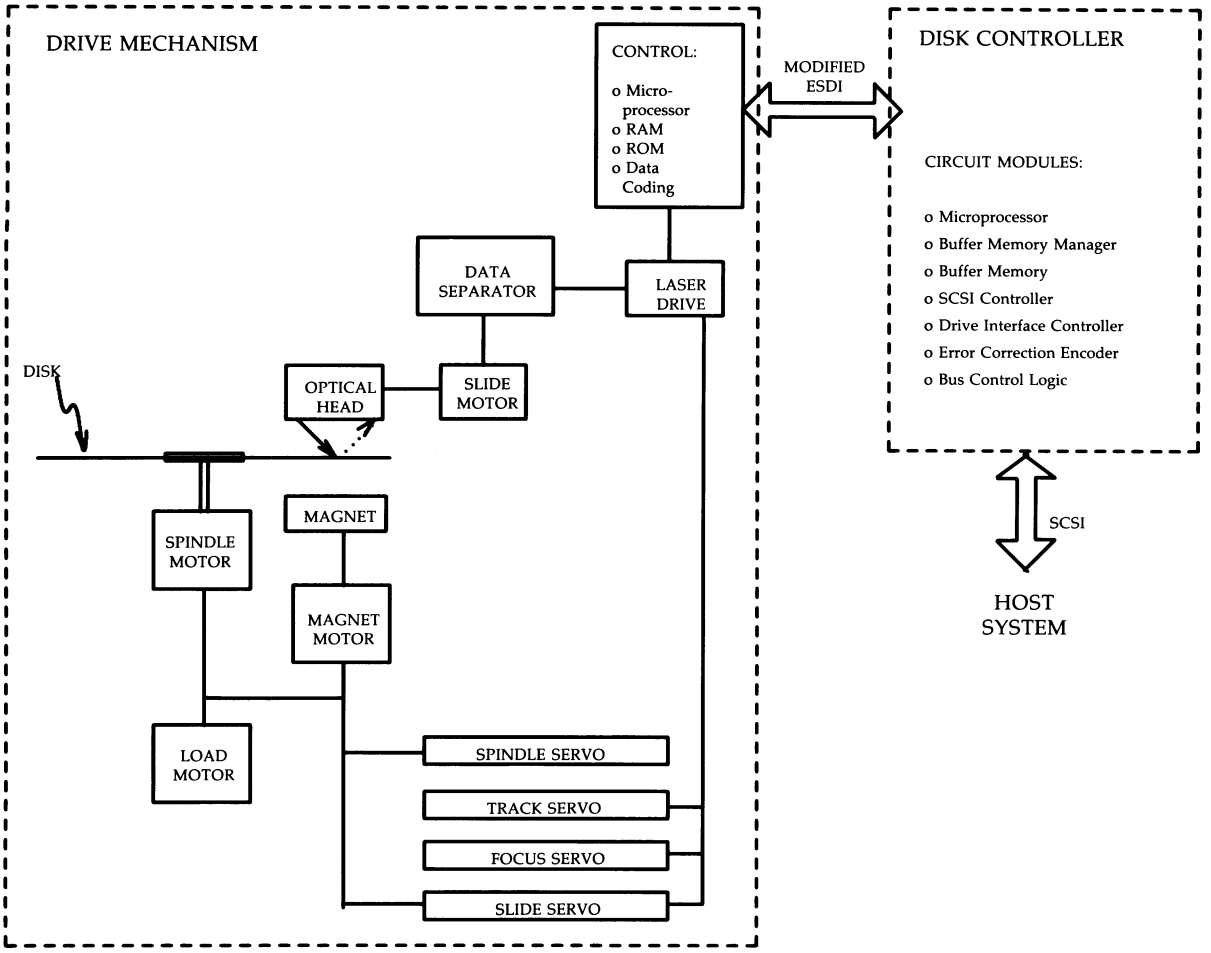


Figure 3-95: SCSI Rewritable Optical Disk Drive — Functional Block Diagram

Optical Disk Drive

Disk motion is controlled by the drive mechanism circuitry. The motor speed is controlled by the spindle servo mechanism which keeps the spindle motor at a constant 2400 rpm.

Read/write head positioning is done by a slide motor and servo system controlled by the data separator in response to the interface signals. These signals are converted into discrete mechanical movements which move the motors the proper amount for the required head position.

The laser drive controls the power to the laser diode. A low power beam is used for reading while a powerful heating beam is required for writing and erasing.

HARD DISK DRIVES

A variety of hard disk drive types are used with a 3B2 computer. Refer to the applicable vendor document for detailed functional information.

POWER—FUNCTIONAL DESCRIPTION

Version 2 System Power

Figure 3-96 shows a functional block diagram of a typical 3B2/300 or 3B2/310 computer and AT&T/XM power arrangement. Figure 3-97 shows a functional block diagram of a typical 3B2/400 computer and AT&T/XM power arrangement. Domestic arrangements are set for 115 volt AC operation. In general, international arrangements are set for 220 to 240 volt AC operation. International markets using 115 volt AC operation are also supported via the applicable solution packages providing that arrangement.

The AT&T/XM Power Supply is controlled by the +5 volt Power Control signal from the 3B2 computer Power Supply. As additional AT&T Expansion Modules are added to a system, the Soft Power Control lead is multipled from module to module.

Version 3 System Power

The typical power arrangements for Version 3 computers would be the same as for the Version 2 computers. However, since the Version 3 computers are equipped with a "smart" power supply, the voltage settings are done automatically.

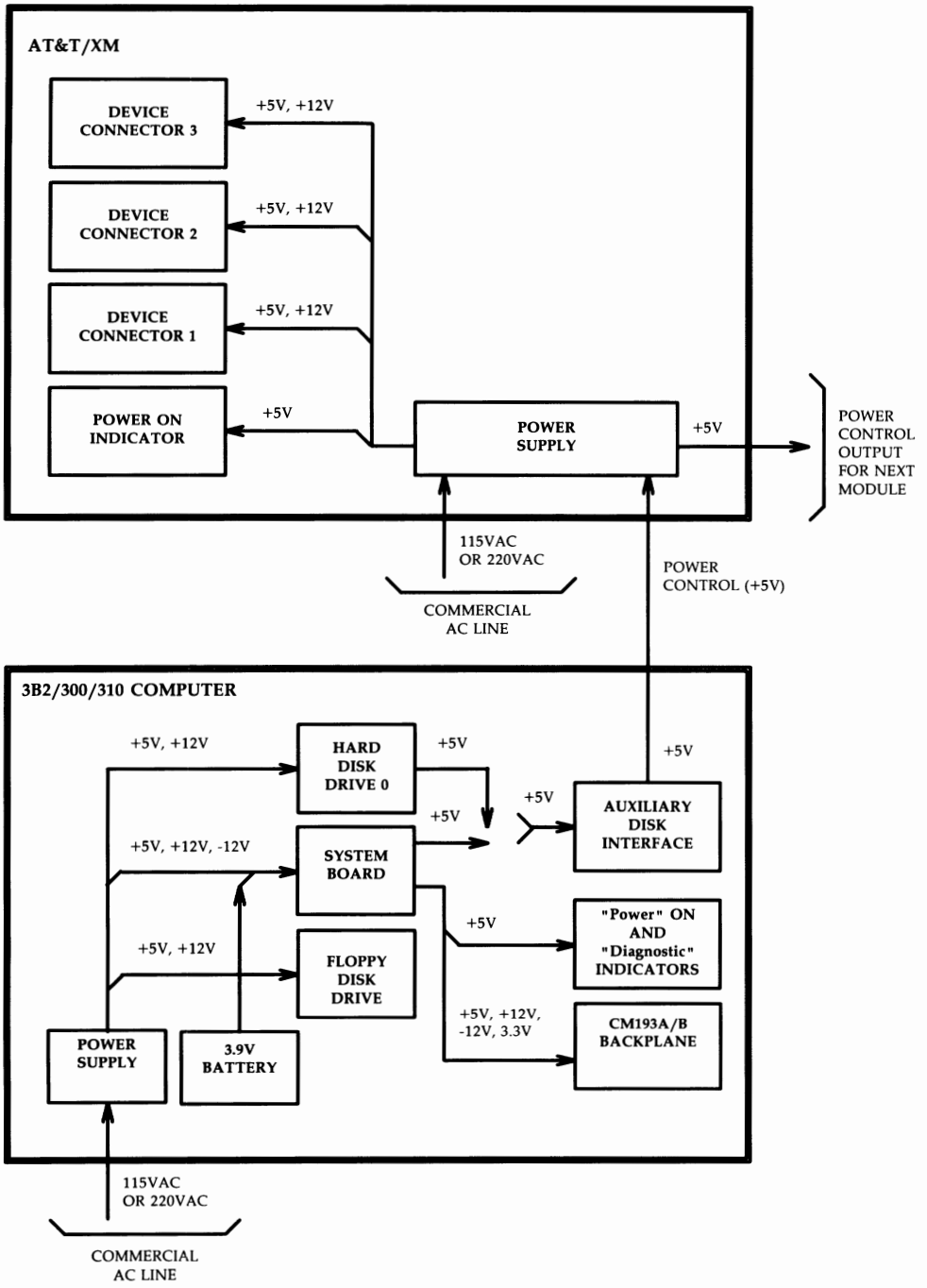


Figure 3-96: 3B2/300 or 310 Computer and AT&T/XM Power — Functional Block Diagram

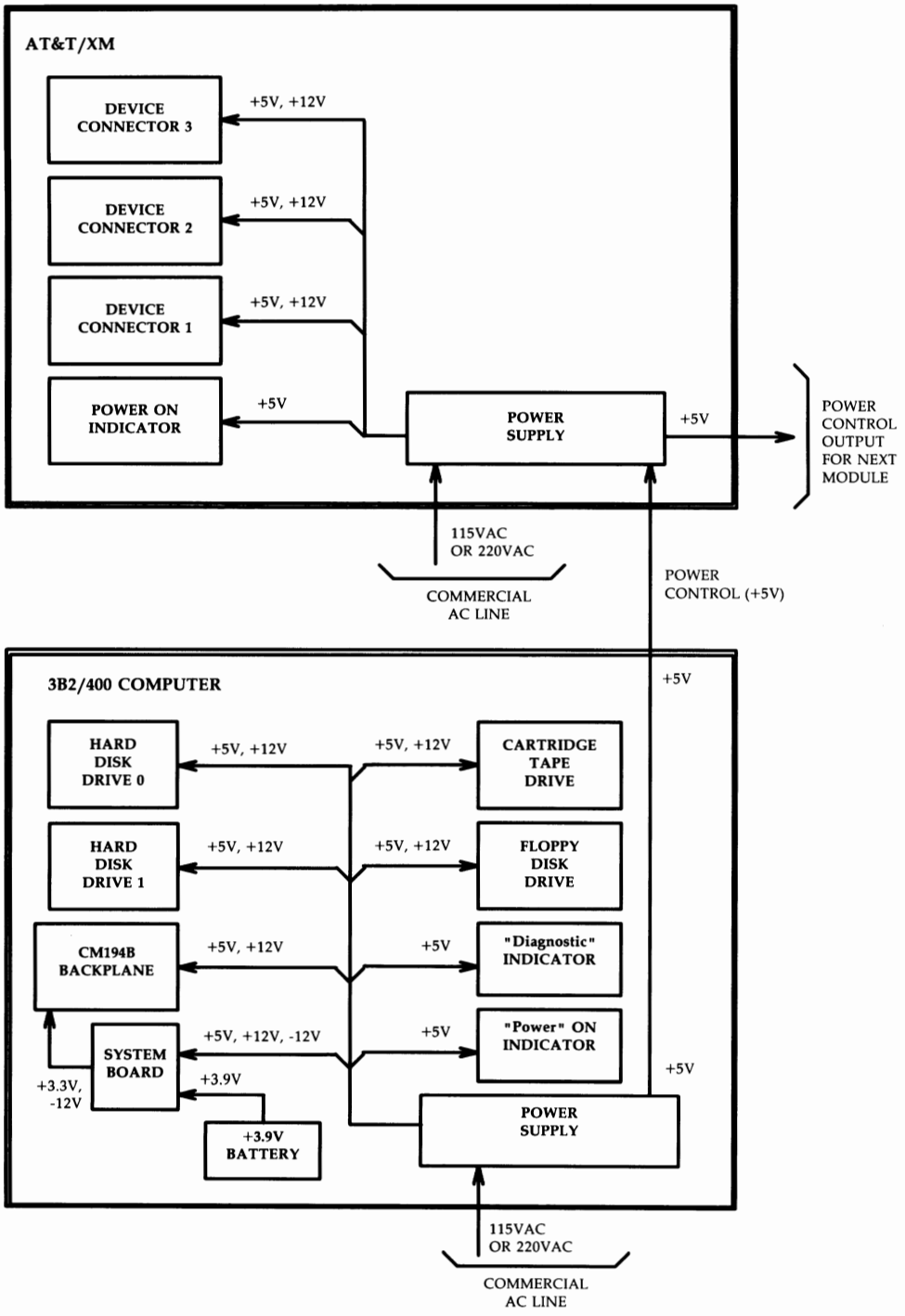


Figure 3-97: 3B2/400 Computer and AT&T/XM Power — Functional Block Diagram

Version 2 3B2 Computer Power

Figures 3-98 and 3-99 are functional block diagrams of the 3B2/300 and 310 computers Power Supply and the 3B2/400 computer Power Supply. Color codes and power connector pin identification for the power cables are shown in these figures. The 3B2 computer requires +5 volt (VCC), +12 volt, and -12 volt power. Logic power is +5 volt. The power supply upper trip point for VCC is between +6.00 volt and +6.75 volt. The DUART uses +12 volt and -12 volt. The various drives (hard disk, floppy, and cartridge tape) require +5 volt and +12 volt.

The commercial AC line is fused and filtered at the Power Supply Set input. The input AC line voltage is selected for either 115 volt AC or 220 to 240 volt AC operation. The Voltage Select Jumper is a factory installed jumper. Different solution packages are provided to support the different input AC lines.

Cooling for the power supply and the 3B2 computer is provided by a current load sensitive fan in the power supply assembly. As additional equipment is added to the configuration, the fan speed increases in response to the increased load. Unfiltered air is pulled from the front and left side of the cabinet and is exhausted at the back of the power supply.

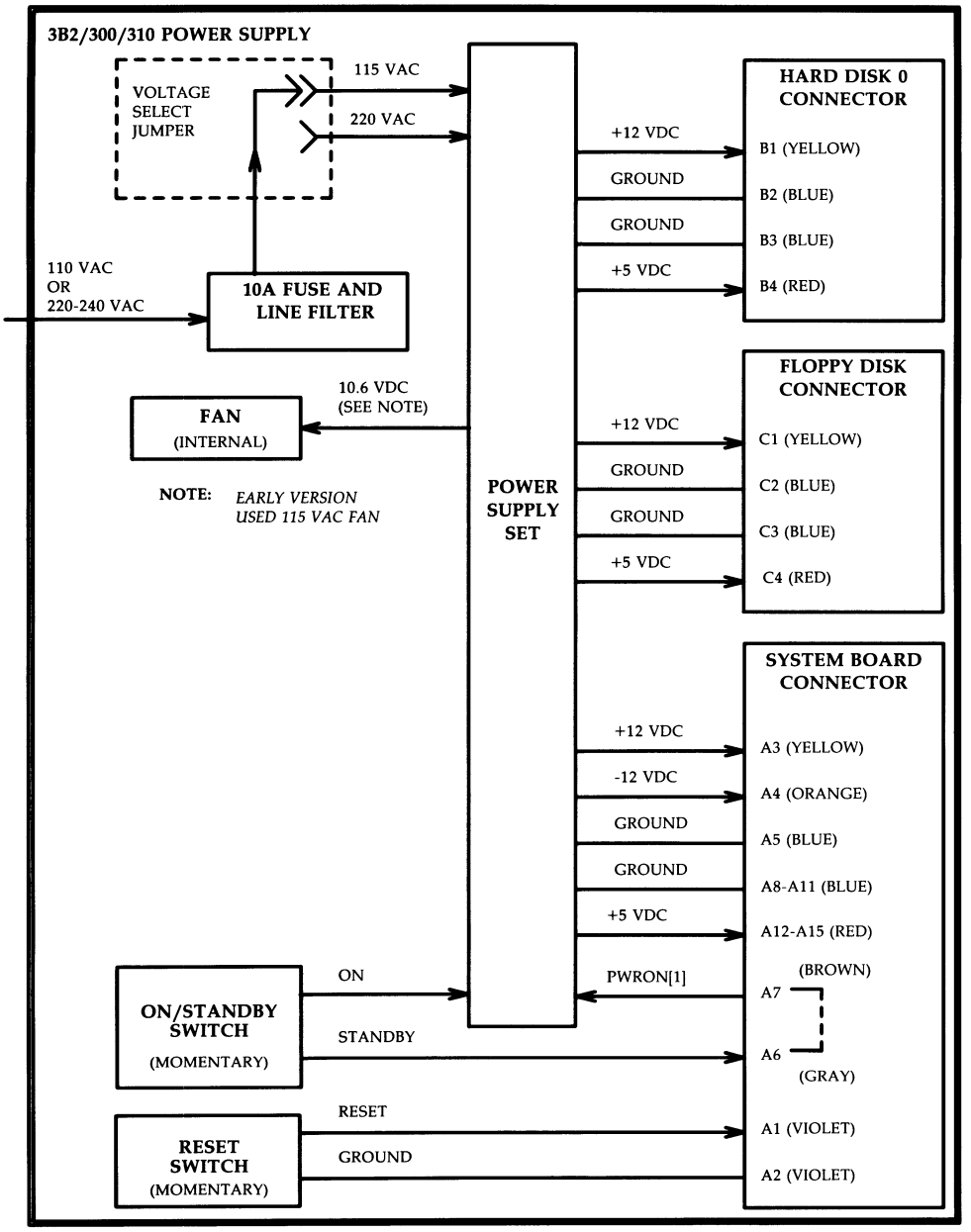


Figure 3-98: 3B2/300 and 310 Computer Power Supply — Functional Block Diagram

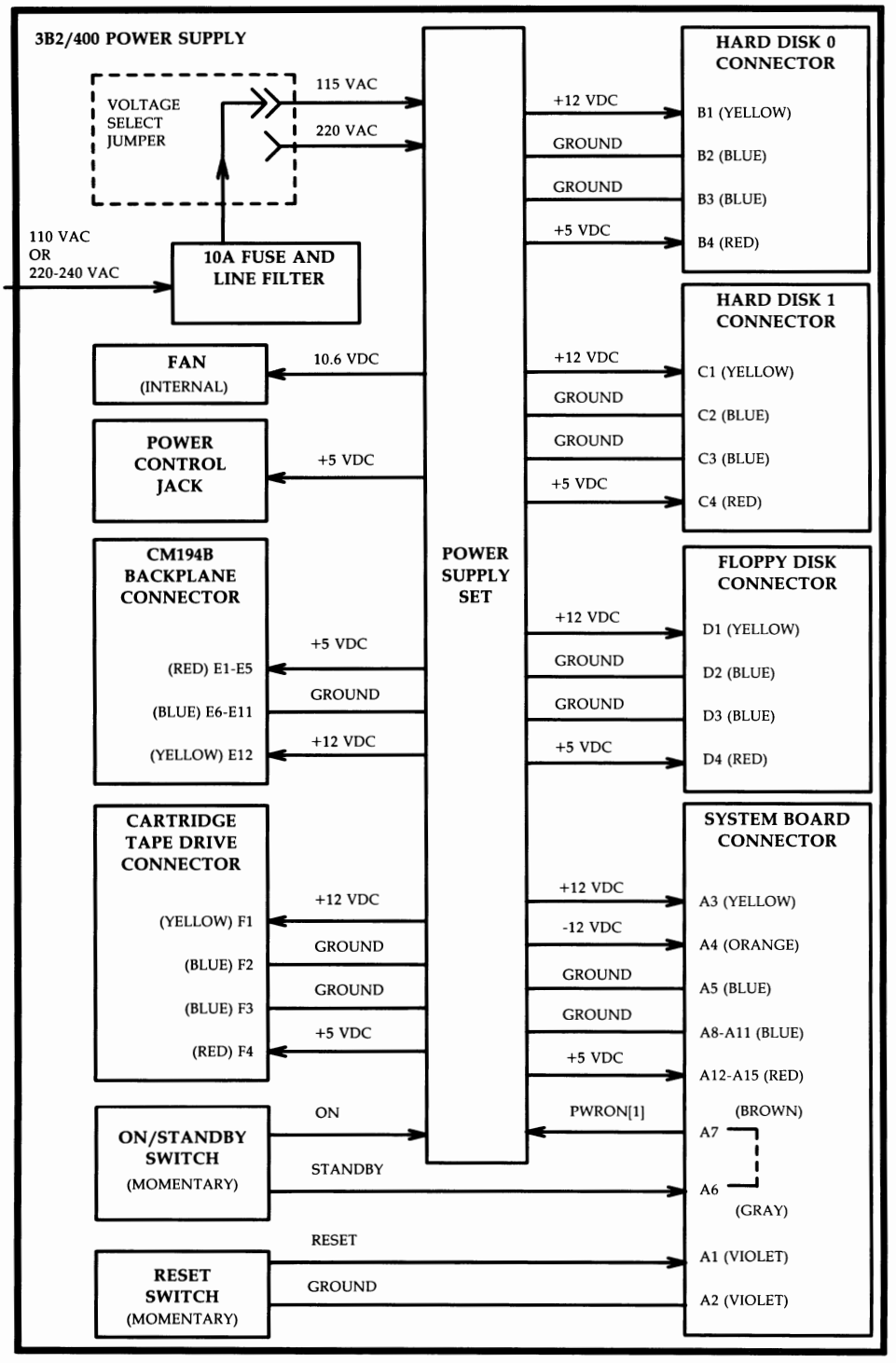


Figure 3-99: 3B2/400 Computer Power Supply — Functional Block Diagram

Version 3 3B2 Computer Power

Figures 3-100 and 3-101 are functional block diagrams of the 3B2/500 computer Power Supply and the 3B2/600 and 700 computers Power Supply. Figure 3-102 is a functional block diagram of a power supply for a 3B2 computer with embedded SCSI.

Color codes and power connector pin identification for the power cables are shown in the figures. The 3B2 computer requires +5 volt (VCC), +12 volt, and -12 volt power. Logic power is +5 volt. The power supply upper trip point for VCC is between +5.5 volt and +7.0 volt. The Dual Universal Asynchronous Receiver/Transmitter (DUART) uses +12 volt and -12 volt. The various drives (hard disk, floppy, and cartridge tape) require +5 volt and +12 volt.

The commercial AC line is fused and filtered at the Power Supply Set input. The input AC line voltage is automatically set for either 115 volt AC or 220 to 240 volt AC operation.

Cooling for the power supply and the 3B2 computer is provided by a current load sensitive fan in the power supply assembly. As additional equipment is added to the configuration, the fan speed increases in response to the increased load. Unfiltered air is pulled from the front and left side of the cabinet and is exhausted at the back of the power supply.

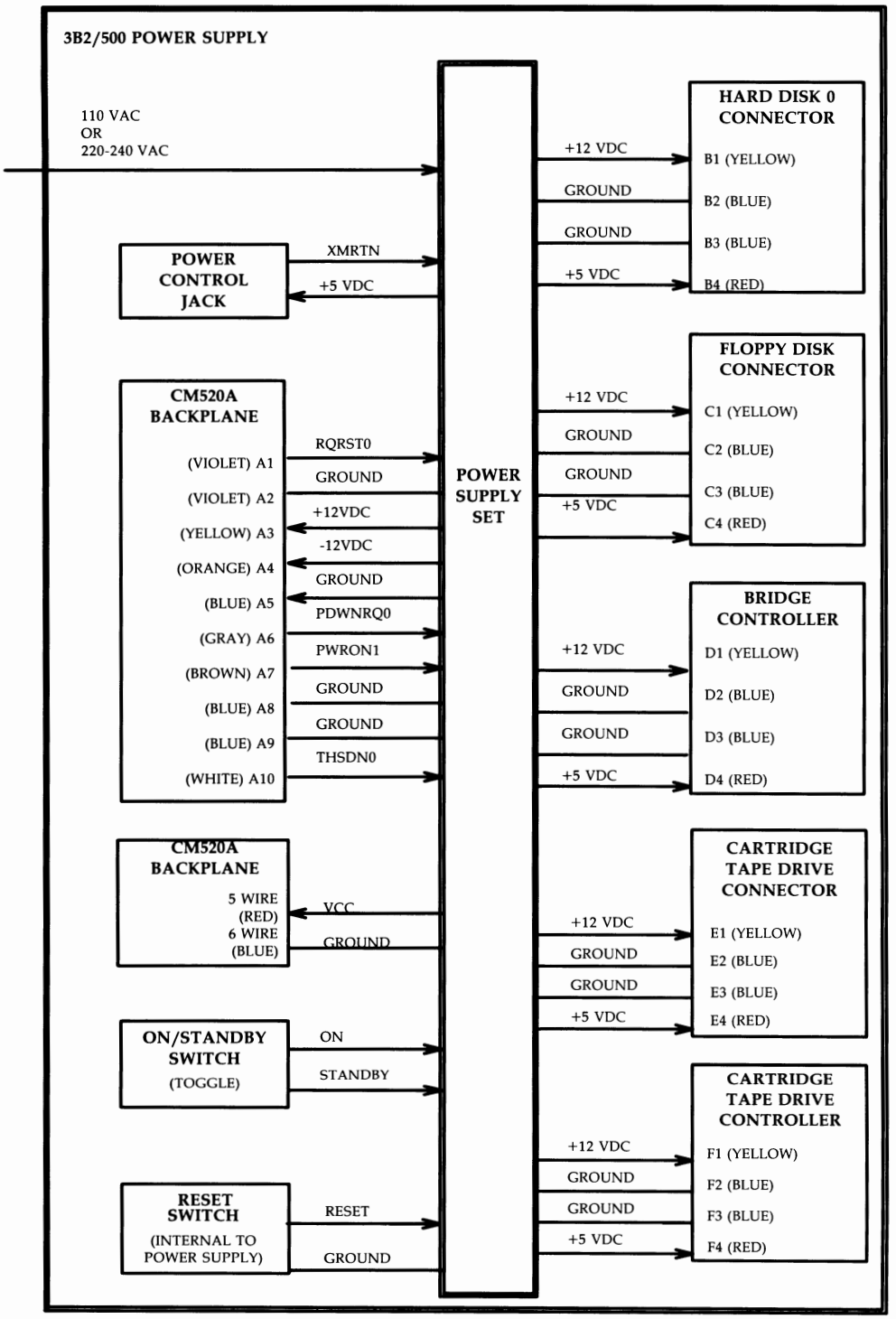


Figure 3-100: 3B2/500 Computer Power Supply — Functional Block Diagram

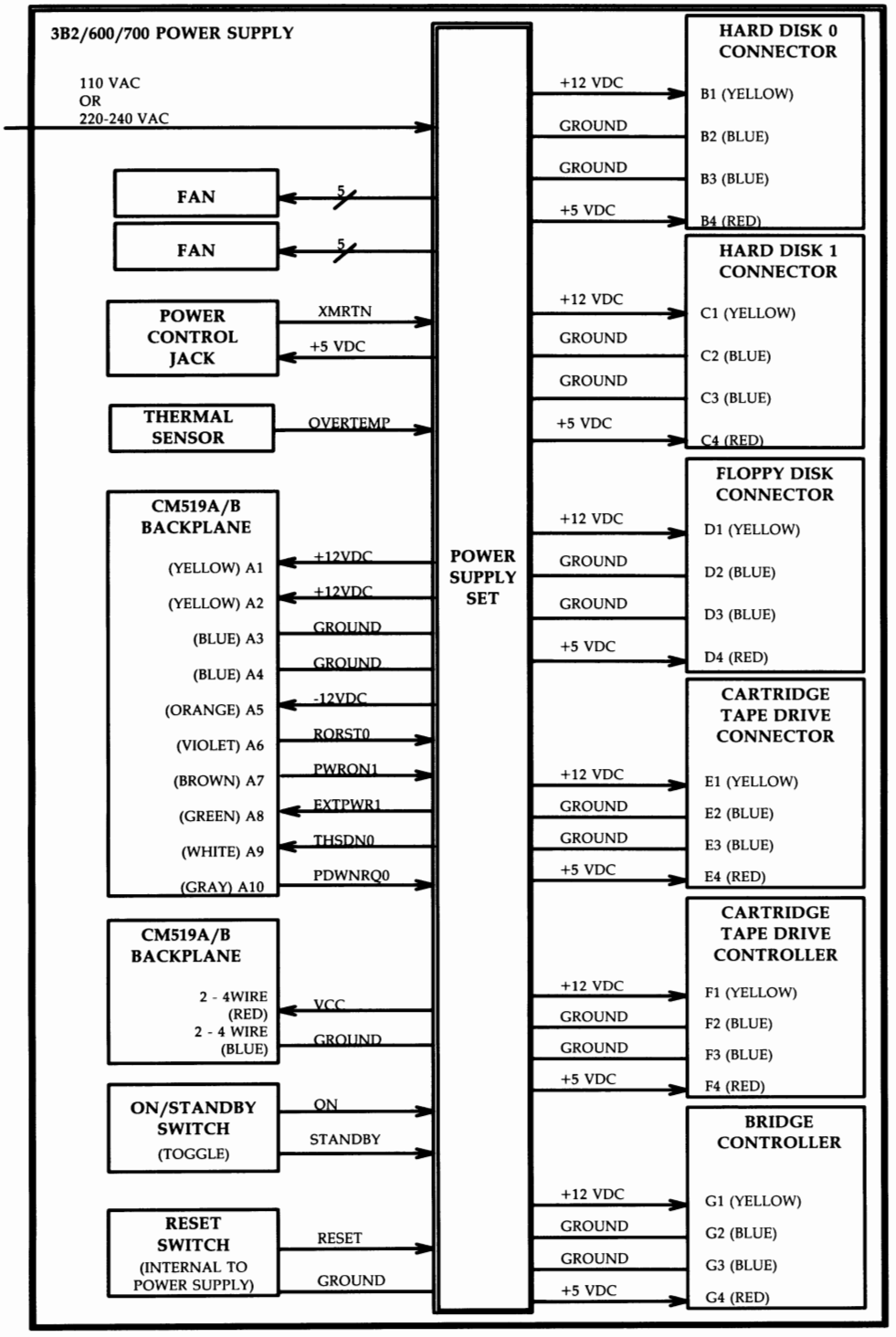


Figure 3-101: 3B2/600 and 700 Computer Power Supply — Functional Block Diagram

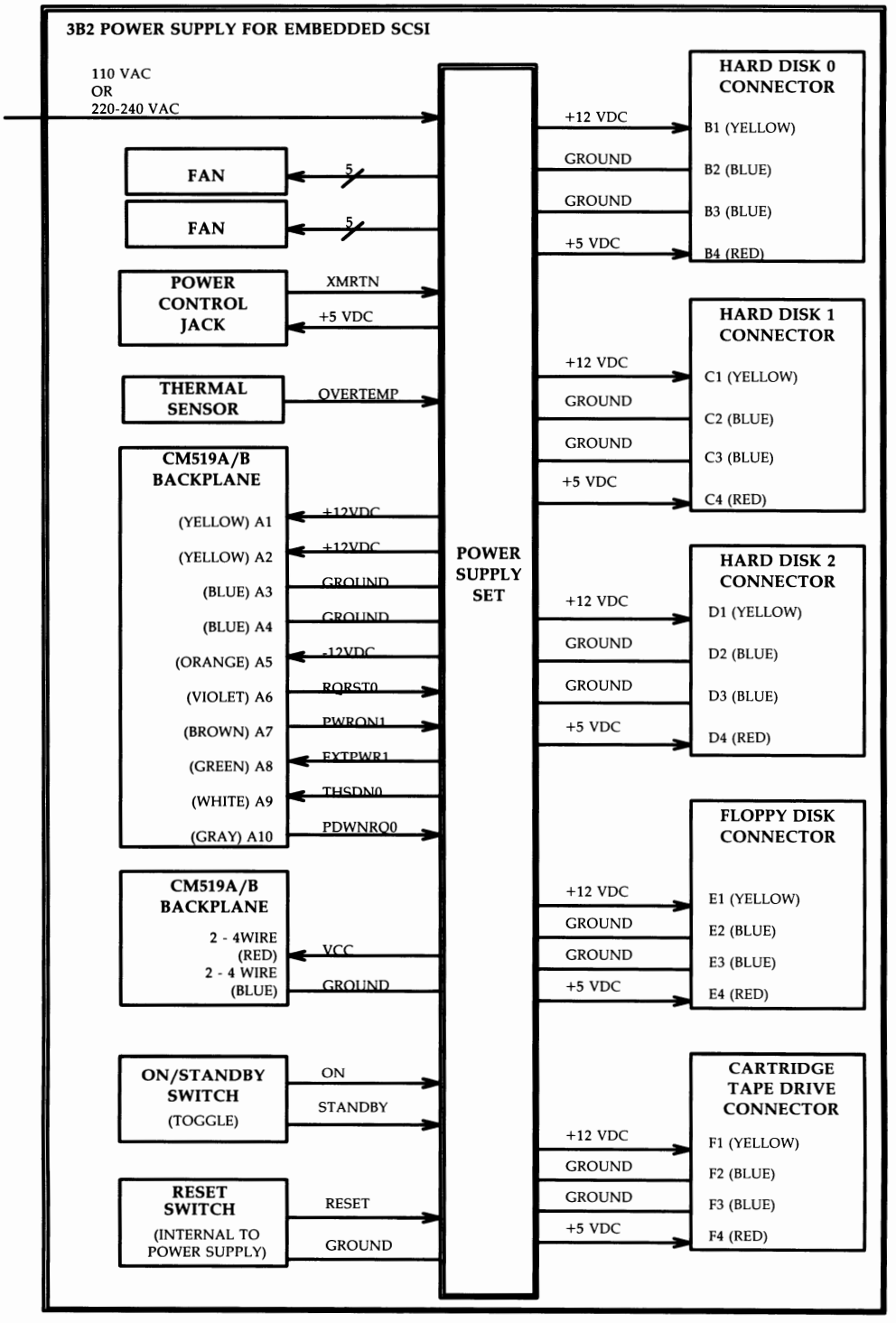


Figure 3-102: 3B2 Power Supply for Embedded SCSI— Functional Block Diagram

3B2 Computer Backup Battery Supply

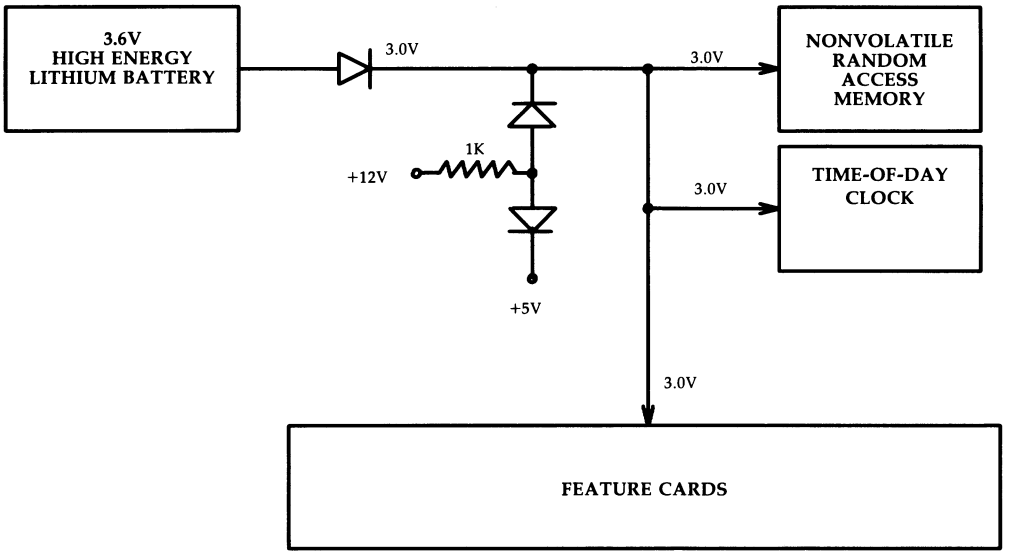
Figure 3-103 is a functional block diagram of the 3B2 computer Backup Battery Supply. A 3.6 volt DC high energy lithium battery is used to supply approximately 3.3 volt DC standby power for the following:

- Time-of-Day Clock
- Nonvolatile Random Access Memory (NVRAM)
- Feature Card Slots.

A reverse biased diode isolates the battery from the connecting circuits when VCC and +12 volt DC are applied to the system board. A small leakage current of approximately 100 microamperes serves to maintain the battery in the fresh state while the external power is applied. When VCC and 12 volt DC are absent, the battery supplies approximately 3.0 volt DC to the connecting circuits. The expected battery life is approximately six years if only the system board current drain is considered.* The battery life will be less than six years depending on the amount of standby current drawn by the feature cards.

FEATURE CARD CURRENT DRAIN (microamperes)	BATTERY LIFE (Years)
0	6.0
10	4.0
20	3.0
30	2.4
40	2.0
50	1.5
60	1.1

* Some of the newer 3B2/400 computers may use Performance Semiconductor P4C148L-35 (1K by 4 bits) Static Random Access Memory (SRAM) which will decrease this "system board only" lifetime to about 4.8 years.



NOTE: The battery connects to the system board on Version 2 computers and to the backplane on Version 3 computers.

Figure 3-103: 3B2 Computer Backup Battery Supply — Functional Block Diagram

AT&T Expansion Module Power Supply

Figure 3-104 is a functional block diagram of an AT&T/XM Power Supply and Figure 3-105 is a functional block diagram of an AT&T XM/405S/900S Power Supply. Color codes and power connector pin identification for the power cables are shown in these figures. The equipment mounted in the AT&T/XM requires +5 volt (VCC) and +12 volt power. The power supply upper trip point for VCC is between +6.00 volt and +6.75 volt. The various drives (hard disk, floppy, and cartridge tape) require +5 volt and +12 volt.

The commercial AC line is fused and filtered at the Power Supply Set input. The input AC line voltage is selected for either 115 volt AC or 220 to 240 volt AC operation. The Voltage Select Jumper is a factory installed jumper. Different solution packages are provided to support the different input AC lines.

Cooling for the power supply and the equipment mounted in the AT&T/XM cabinet is provided by a current load sensitive fan in the power supply assembly. As additional equipment is added to the configuration, the fan speed increases in response to the increased load. Unfiltered air is pulled from the front and left side of the cabinet and is exhausted at the back of the power supply.

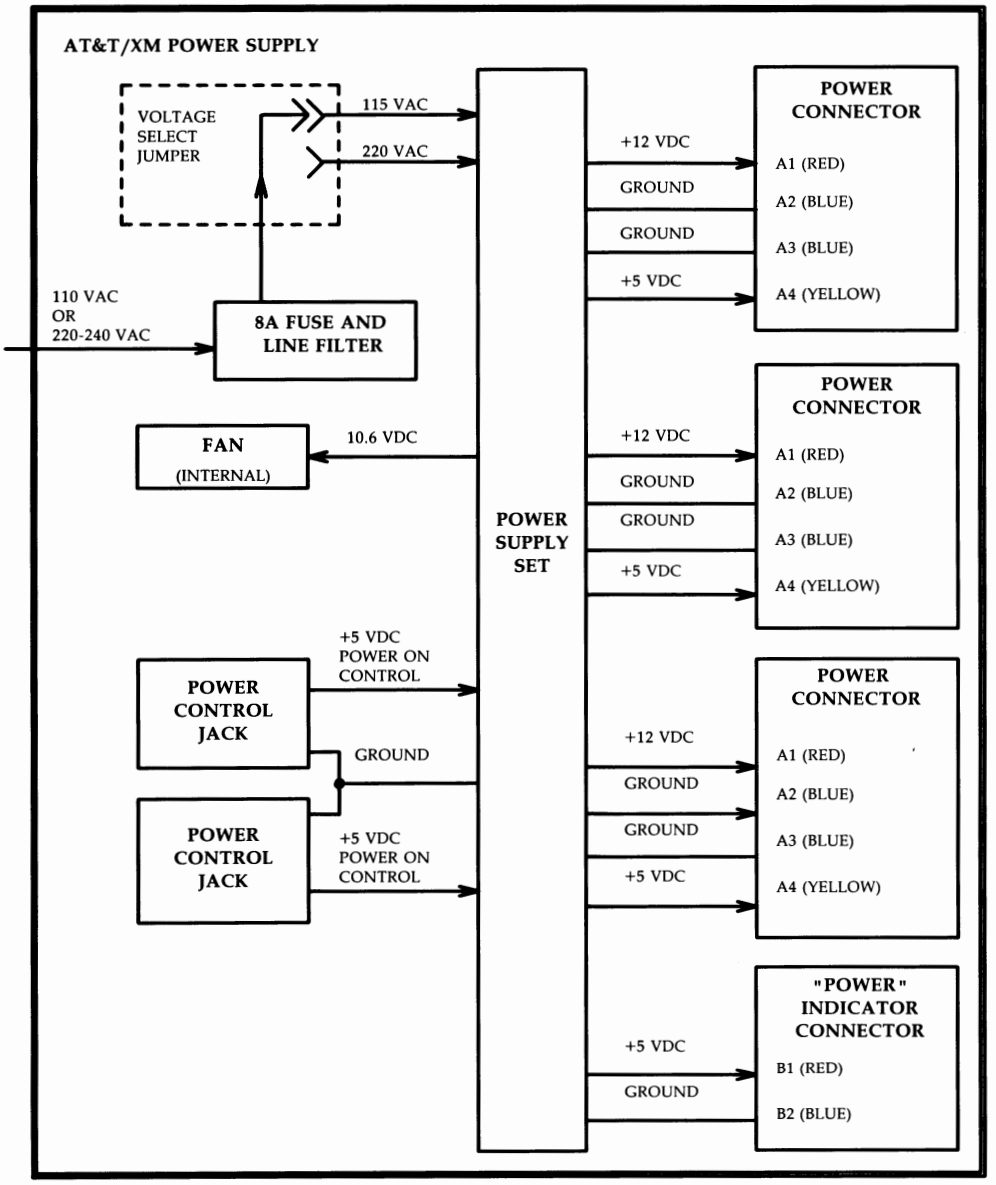


Figure 3-104: AT&T/XM Power Supply — Functional Block Diagram

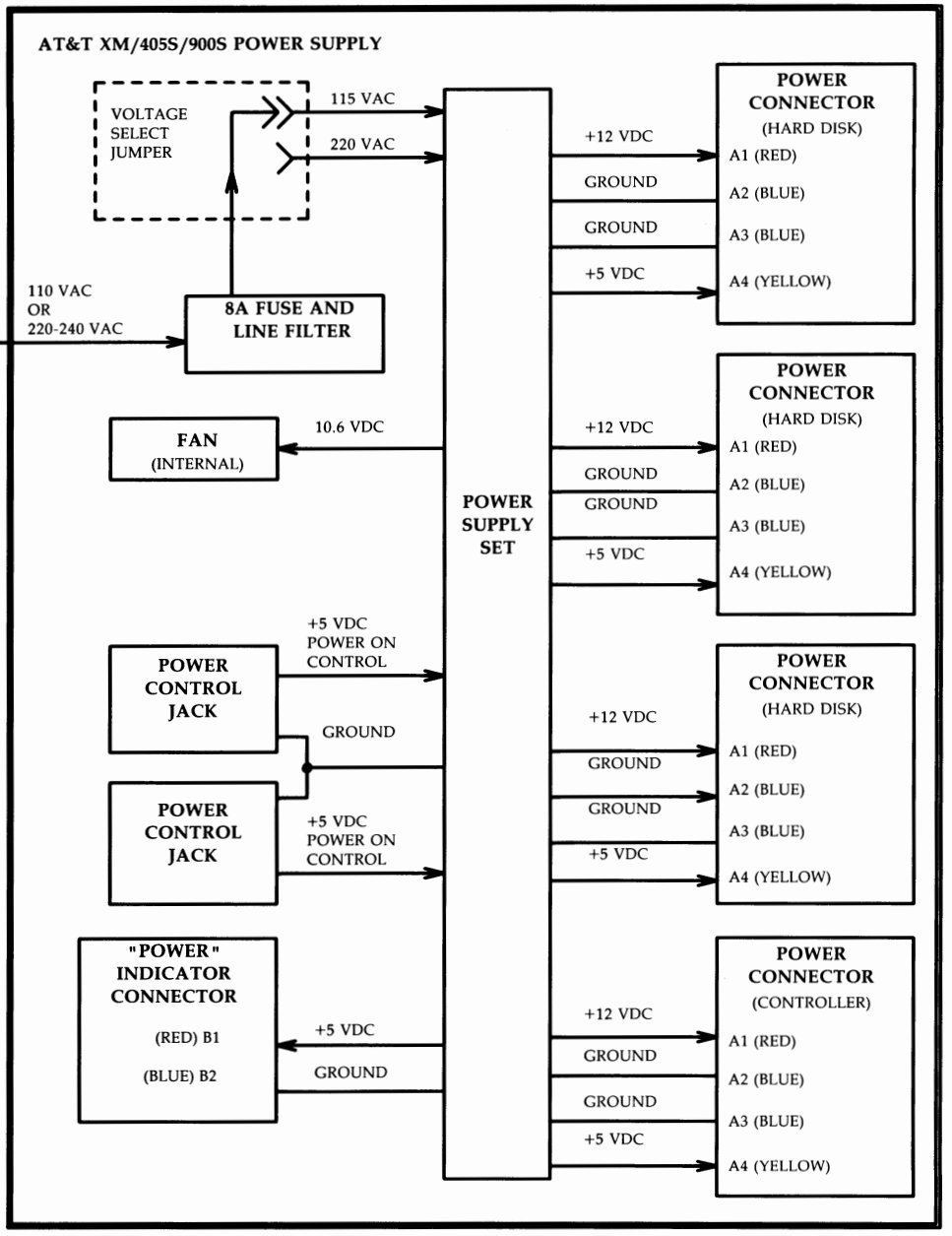


Figure 3-105: AT&T XM/405S/900S Power Supply — Functional Block Diagram

Appendix A: VIRTUAL ADDRESS SPACE

Appendix A : VIRTUAL ADDRESS SPACE A-1
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Paging Virtual Address Space A-4

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Appendix A: VIRTUAL ADDRESS SPACE

Swapping Virtual Address Space

Translation of virtual memory addresses to physical memory addresses is done by the WE 32101 Memory Management Unit (MMU). The WE 32101 MMU divides the virtual address space into four address subspaces called *sections*. Each *section* is 1 gigabyte in length. Each section is divided into 128 kilobyte segments. The MMU provides for both contiguous and paged segments. A contiguous segment can be as large as 128 kilobytes. A paged segment can contain up to sixty-four 2-kilobyte pages. Three virtual address sections are assigned as user address space and one virtual address section is assigned as system address space. The system address space is common for all processes and is not changed in a context switch. The operating system is located in the system address space. Therefore, all operating system functions are shared by all processes and are available to all user processes.

The user address space is separate for each process. However, several processes can access the same memory pages (controlled sharing). The layout of the user address space is shown in Figure A-1. The program text begins at address 0x A0000000 and is write protected. Nonshared, writable data begins at the first segment after the program text. The size of the data segment is extendible by a system call. The stack begins at address 0x C0020000 and is grown automatically by the operating system when the process runs out of stack space. The segment in the user address space at address 0x C0000000 is reserved for storing operating system related information about user processes (u_block).

A process executing in the user mode has access only to sections 1, 2, and 3 of the virtual address space. When the operating system is running in the kernel mode for a user process, the process has access to both the user and kernel address spaces. Figures A-2 through A-5 show the layout of sections 0 through 3 of the virtual address space.

SYSTEM VIRTUAL ADDRESS SPACE		
SECTION	**ADDRESS**	**DESCRIPTION**
0	0x 00000000—0x 3FFFFFFF	KERNEL INPUT/OUTPUT AND SYSTEM BOARD
1	0x 40000000—0x 7FFFFFFF	KERNEL TEXT AND DATA
2	0x 80000000—0x BFFFFFFF	PROCESS TEXT AND DATA
3	0x C0000000—0x FFFFFFFF	PROCESS U_BLOCK AND STACK

Figure A-1: Virtual Address Space Sections

SECTION 0 KERNEL VIRTUAL ADDRESS SPACE						
SEGMENT NUMBER	VIRTUAL ADDRESS	SEGMENT SIZE	SECTION NAME	SEGMENT CONTENTS	SEGMENT ACCESS	LOADER OPTION
0x 0	0x 00000000	2 KB	.gate	GATE TABLE	KR	
0x 1	0x 00020000	64 KB	KV_demot	SYSTEM BOARD ROM	KR	NOLOAD
0x 2	0x 00040000	64 KB	KV_ccmmu	SYSTEM BOARD REGISTERS	KRW	NOLOAD
0x 3—0x 12	0x 00060000	2 MB		FEATURE CARD SLOT 1	KRW	
0x 13				NOT USED		
0x 14—0x 23	0x 00280000	2 MB		FEATURE CARD SLOT 2	KRW	
0x 24				NOT USED		
0x 25—0x 34	0x 004A0000	2 MB		FEATURE CARD SLOT 3	KRW	
0x 35				NOT USED		
0x 36—0x 45	0x 006C0000	2 MB		FEATURE CARD SLOT 4	KRW	
0x 46				NOT USED		
0x 47—0x 56	0x 008E0000	2 MB		FEATURE CARD SLOT 5	KRW	
0x 57				NOT USED		
0x 58—0x 67	0x 00B00000	2 MB		FEATURE CARD SLOT 6	KRW	
0x 68				NOT USED		
0x 69—0x 78	0x 00D20000	2 MB		FEATURE CARD SLOT 7	KRW	
0x 79				NOT USED		
0x 80—0x 8F	0x 01000000	2 MB		FEATURE CARD SLOT 8	KRW	
0x 90				NOT USED		
0x 91—0x A0	0x 01220000	2 MB		FEATURE CARD SLOT 9	KRW	
0x A1				NOT USED		
0x A2—0x B1	0x 01440000	2 MB		FEATURE CARD SLOT A	KRW	
0x B2				NOT USED		
0x B3—0x C2	0x 01660000	2 MB		FEATURE CARD SLOT B	KRW	
0x C3				NOT USED		
0x C4—0x D3	0x 01880000	2 MB		FEATURE CARD SLOT C	KRW	
0x D4				NOT USED		
0x D5—0x E4	0x 01AA0000	2 MB		FEATURE CARD SLOT D	KRW	
0x E5				NOT USED		
0x E6—0x F5	0x 01CC0000	2 MB		FEATURE CARD SLOT E	KRW	
0x F6—0x FF				NOT USED		
0x 100—0x 1FF	0x 02000000	16 MB		MAIN MEMORY	KRW	

LEGEND:

KB	KILOBYTE
KR	KERNEL READ
KRW	KERNEL READ/WRITE
MB	MEGABYTE

Figure A-2: Virtual Address Space — Section 0

SECTION 1 KERNEL VIRTUAL ADDRESS SPACE						
SEGMENT NUMBER	VIRTUAL ADDRESS	SEGMENT SIZE	SECTION NAME	SEGMENT CONTENTS	SEGMENT ACCESS	LOADER OPTION
0x 0—0x 7	0x 44000000	1 MB	.text	KERNEL TEXT	KR	
0x 8—0x F	0x 44100000	1 MB	.data	KERNEL DATA	KRW	
0x 10—0x 1F	0x 44200000	2 MB	.bss	KERNEL STATIC DATA	KRW	
0x 20—0x 2F	0x 44400000	2 MB	KV_resmm	KERNEL SCRATCH	KRW	NOLOAD
0x 30—0x 3F	0x 44600000	2 MB	KV_sysseg	NETWORK INTERFACE SCRATCH	KRW	NOLOAD
0x 40	0x 44800000	128 KB	KV_prfdat	PAGE FRAME DATA	KRW	NOLOAD
0x 41	0x 44820000	128 KB	KV_tables	SYSTEM TABLES	KRW	NOLOAD

LEGEND:

KB	KILOBYTE
KR	KERNEL READ
KRW	KERNEL READ/WRITE
MB	MEGABYTE

Figure A-3: Virtual Address Space — Section 1

SECTION 2 USER VIRTUAL ADDRESS SPACE					
VIRTUAL ADDRESS	SEGMENT SIZE	SECTION NAME	SEGMENT CONTENTS	SEGMENT ACCESS	LOADER OPTION
0x A0000000	1 MB	.text	USER TEXT	KR/UR	
0x A0000000 + n*20000	1 MB	.data	USER DATA	KRW/URW	

LEGEND:

KR	KERNEL READ
KRW	KERNEL READ/WRITE
UR	USER READ
URW	USER READ/WRITE

Figure A-4: Virtual Address Space — Section 2

SECTION 3 USER VIRTUAL ADDRESS SPACE					
VIRTUAL ADDRESS	SEGMENT SIZE	SECTION NAME	SEGMENT CONTENTS	SEGMENT ACCESS	LOADER OPTION
0x C0000000 0x C0020000	1 BYTE		USER U_BLOCK USER STACK DATA	KRW KRW/URW	

LEGEND:

KRW KERNEL READ/WRITE
URW USER READ/WRITE

Figure A-5: Virtual Address Space — Section 3

Paging Virtual Address Space

Figure A-6 shows the minimal virtual address map for a 3B2 computer running a paging operating system.

PAGING VIRTUAL ADDRESS SPACE	
ADDRESS	DESCRIPTION
0x 00000000—0x 7FFFFFFF	OPERATING SYSTEM
0x 80000000—0x 807FFFFF	RESERVED
0x 80800000—0x 9FFFFFFF	Start of the user .text segment. At next 512 KB boundary (after end of text) .data begins. The .data segment typically grows toward higher addresses as a process executes.
0x 0A0000000—0x BFFFFFFF	RESERVED
0x C00000000—0x DFFFFFFF	RESERVED
0x E00000000—0x FFFFFFFF	RESERVED

Figure A-6: Paging Virtual Address Map (Minimum Configuration)

Appendix B: CONNECTOR AND CABLING INFORMATION

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Appendix B: CONNECTOR AND CABLING INFORMATION

GENERAL

This appendix contains specific card interconnection information. Interconnection information is provided for following equipment:

- CM190A/ED-4C637-30 and CM518A/B/C System Boards
- CM191A/B/C/D, CM192B, CM523A/AA/B/D Memory Cards
- CM193A/B, CM194B, CM519A/B, and CM520A Backplanes
- CM195A Network Interface (NI) Card
- CM195AA Alarm Interface Circuit (AIC) Card
- CM195AC/CM195AD Datakit Virtual Circuit Switch (VCS) Interface Card
- CM195AE General Purpose Synchronous Controller (GPSC) Card
- CM195AY/CM195Y Enhanced Peripheral Port Controller (EPORTS) Card
- CM195B/CM195BA Peripheral Port Controller (PORTS) Cards
- CM195H Cartridge Tape Controller (CTC) Card
- CM195K Expansion Disk Controller (XDC) Card
- CM195T Intelligent Serial Controller (ISC) Card
- CM195U STARLAN Interface Card
- CM195W Small Computer System Interface (SCSI) Host Adapter Card
- CM521A Differential SCSI Host Adapter Card
- CM522A Virtual Cache (VCACHE) Card
- CM524A Processing Element (PE) Card
- CM525B Versa Modula Europa bus (VMEbus) Card
- CM527A Multiprocessor Enhancement (MPE) Card
- Miscellaneous Connectors and Cables.

CM190A/ED-4C637-30 SYSTEM BOARD INTERCONNECTIONS

Figure B-1 shows the layout of the CM190A System Board. Figure B-2 shows the layout of the System Board, ED-4C637-30. Refer to these figures for system board connector location information. Pin and signal information is provided in tables following the figures for each of the system board connectors. The connector tables are presented in sequence by connector designation. The figures are printed front and back with a blank unit so that either figure can be used in conjunction with any table.

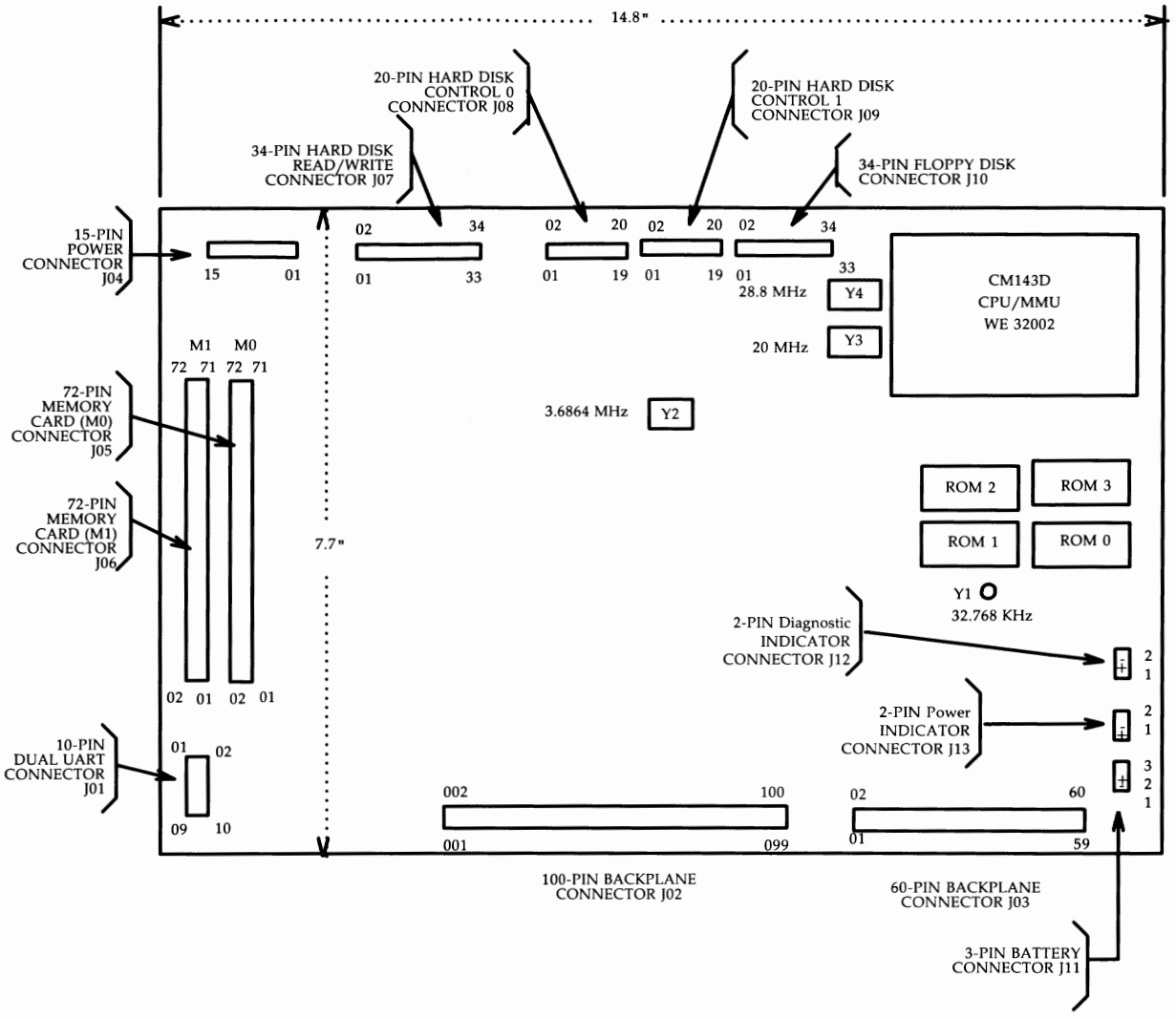


Figure B-1: CM190A System Board Layout

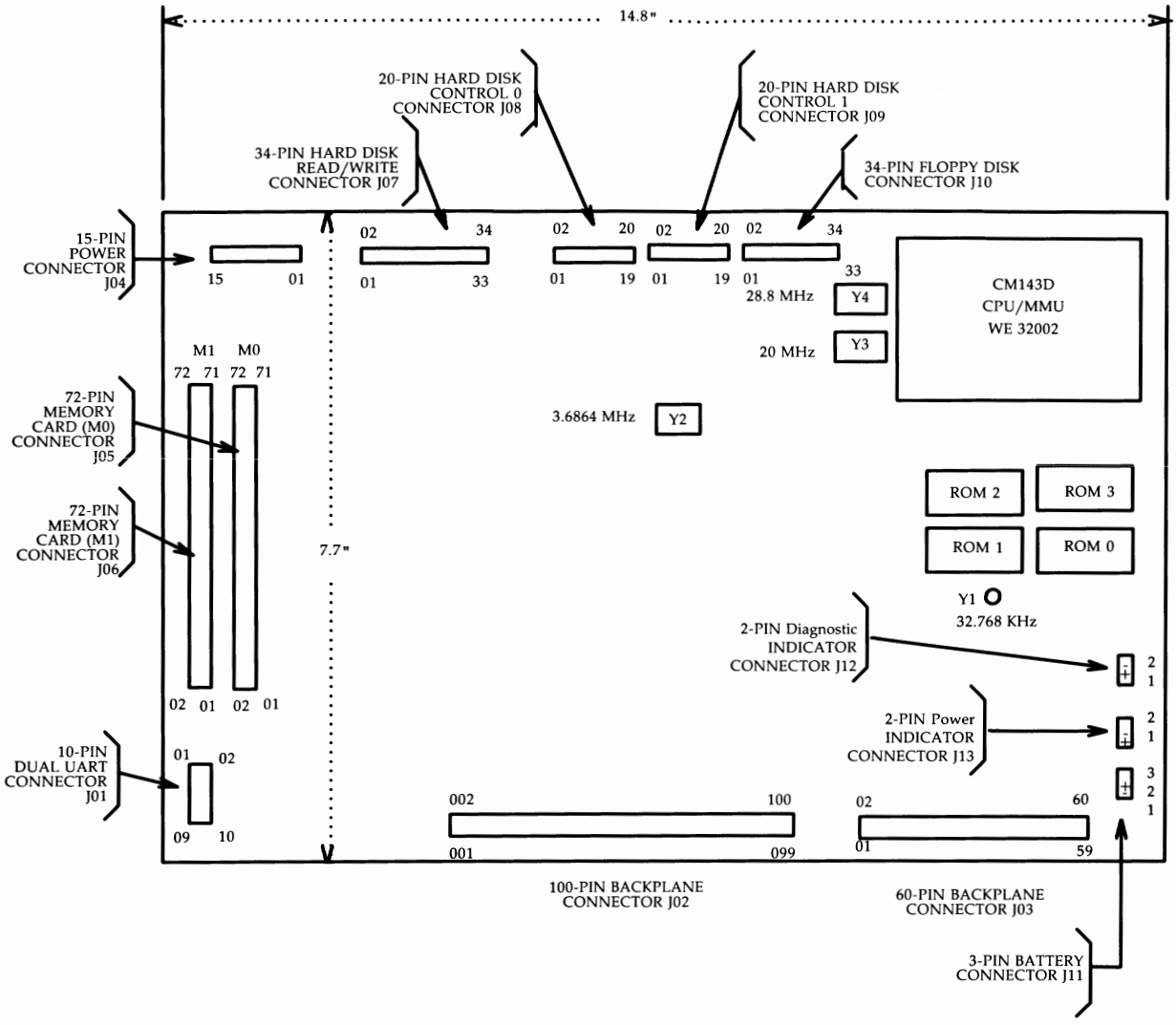


Figure B-1: CM190A System Board Layout

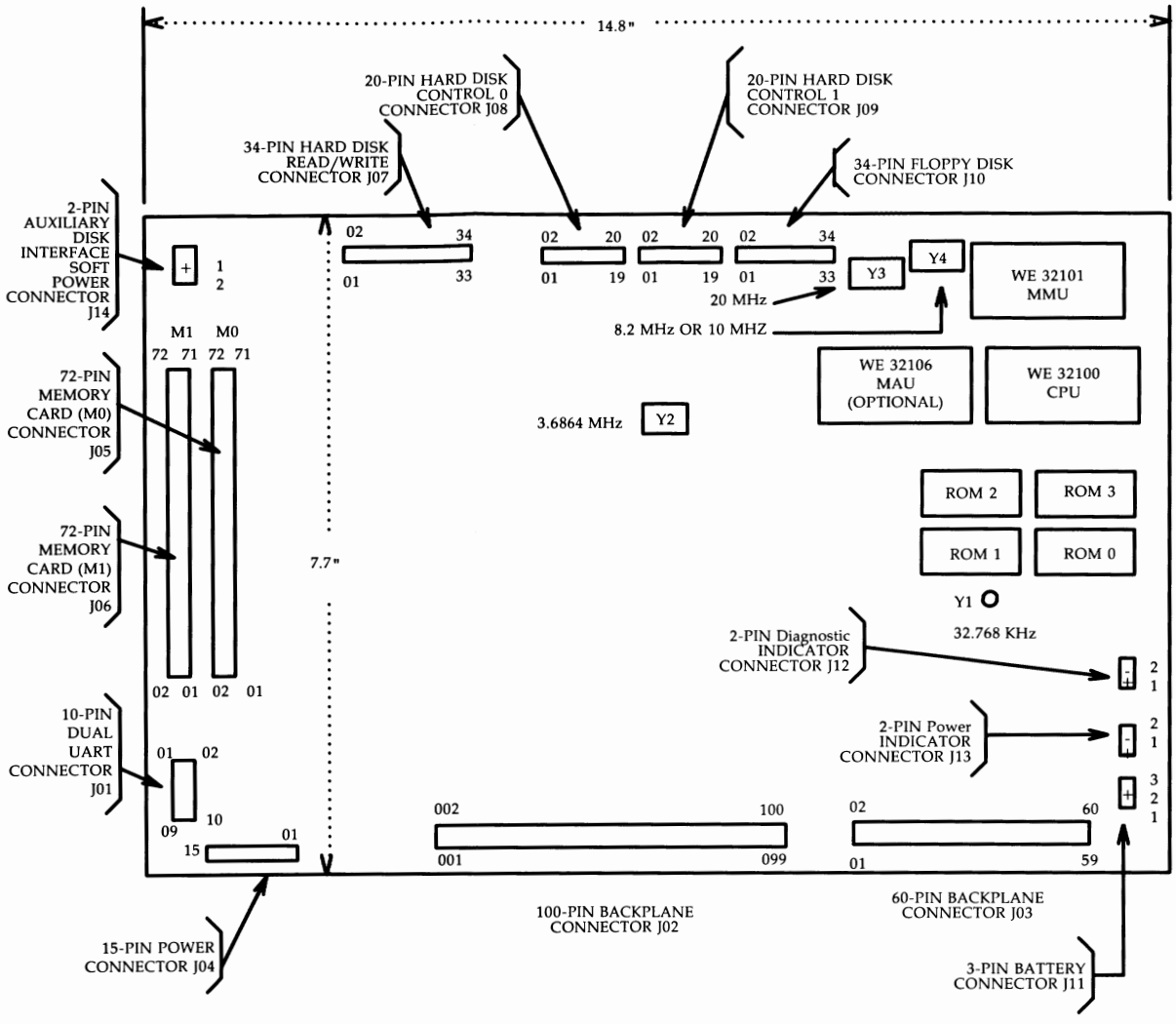


Figure B-2: System Board, ED-4C637-30 Layout

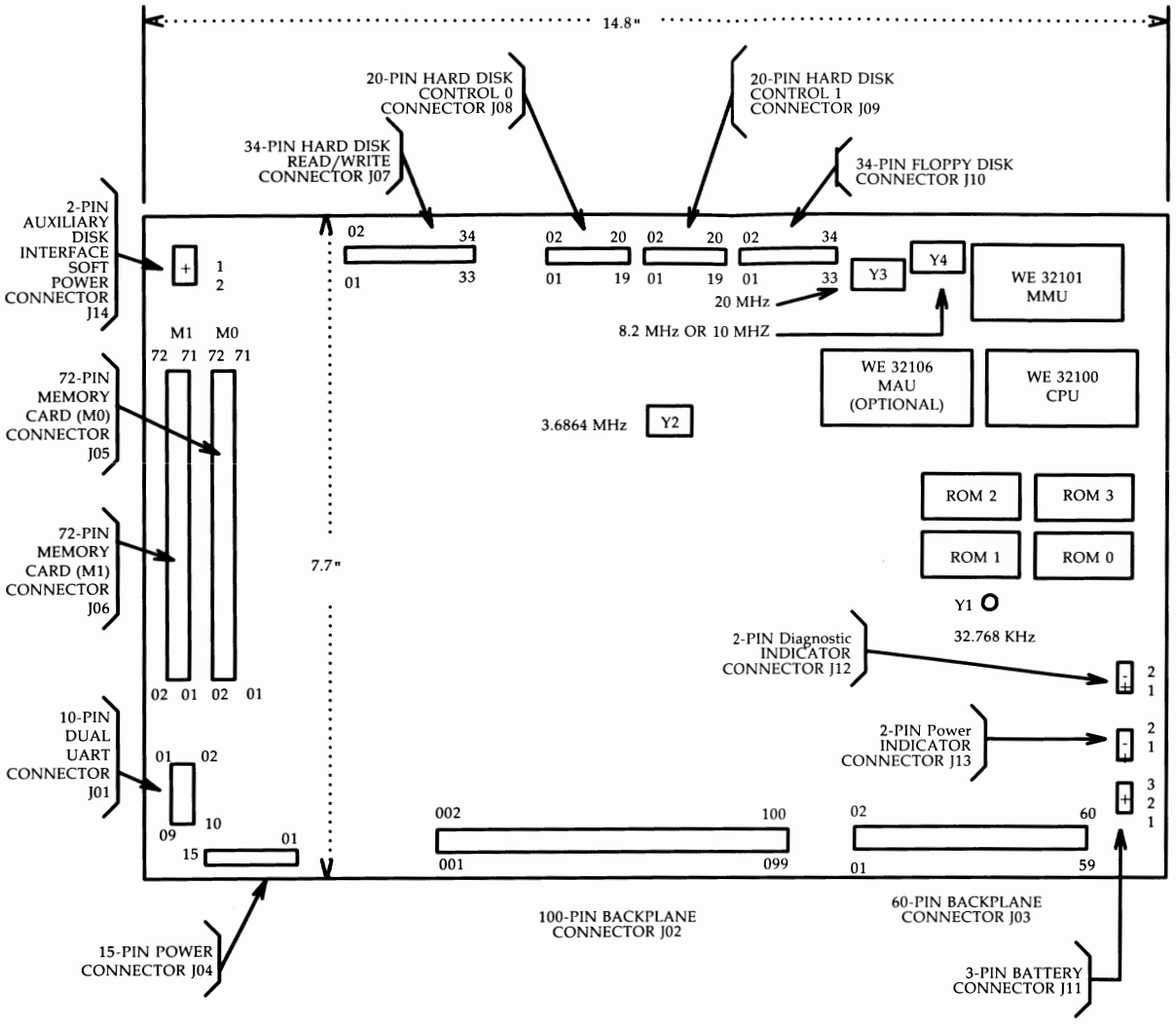


Figure B-2: System Board, ED-4C637-30 Layout

10-PIN DUAL UART CONNECTOR, J01		
PIN	**DESCRIPTION**	**FUNCTION**
1	CONSOLE RECEIVE DATA (BB 2) (RXD0[0])	INPUT
2	CONSOLE TRANSMIT DATA (BA 3) (TXD0[0])	OUTPUT
3	CONSOLE DATA TERMINAL READY (CD 20) (DTR0[0])	OUTPUT
4	CONSOLE DATA CARRIER DETECT (CF 8) (DCD0[0])	INPUT
5	GROUND (GRD)	GROUND
6	CONTTY TRANSMIT DATA (BA 3) (TXD1[0])	OUTPUT
7	CONTTY RECEIVE DATA (BB 2) (RXD1[0])	INPUT
8	CONTTY DATA TERMINAL READY (CD 20) (DTR1[0])	OUTPUT
9	CONTTY DATA CARRIER DETECT (CF 8) (DCD1[0])	INPUT
10	GROUND (GRD)	GROUND

NOTE: The CONSOLE AND CONTTY are classed as Data Terminal Equipment (DTE) connections.

100-PIN BACKPLANE CONNECTOR, J02		
PIN	DESCRIPTION	FUNCTION
1	+5V (VCC)	POWER
2	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	INPUT/OUTPUT
3	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	INPUT/OUTPUT
4	GROUND (GRD)	GROUND
5	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	INPUT/OUTPUT
6	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	INPUT/OUTPUT
7	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	INPUT/OUTPUT
8	GROUND (GRD)	GROUND
9	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	INPUT/OUTPUT
10	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	INPUT/OUTPUT
11	+5V (VCC)	POWER
12	GROUND (GRD)	GROUND
13	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	INPUT/OUTPUT
14	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	INPUT/OUTPUT
15	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	INPUT/OUTPUT
16	GROUND (GRD)	GROUND
17	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	INPUT/OUTPUT
18	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	INPUT/OUTPUT
19	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	INPUT/OUTPUT
20	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	INPUT/OUTPUT
21	+5V (VCC)	POWER
22	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	INPUT/OUTPUT
23	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	INPUT/OUTPUT
24	GROUND (GRD)	GROUND
25	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	INPUT/OUTPUT
26	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	INPUT/OUTPUT
27	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	INPUT/OUTPUT
28	GROUND (GRD)	GROUND
29	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	INPUT/OUTPUT
30	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	INPUT/OUTPUT
31	+5V (VCC)	POWER
32	GROUND (GRD)	GROUND
33	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
34	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
35	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
36	GROUND (GRD)	GROUND
37	PERIPHERAL INTERLOCK (PLOCK[0])	INPUT/OUTPUT
38	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
39	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
40	GROUND (GRD)	GROUND
41	+5V (VCC)	POWER
42	PERIPHERAL BUS ACKNOWLEDGE (PBACK[0])	INPUT/OUTPUT
43	PERIPHERAL BUS REQUEST (PBRQ[0])	INPUT/OUTPUT
44	GROUND (GRD)	GROUND
45	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
46	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
47	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
48	GROUND (GRD)	GROUND
49	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
50	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT

100-PIN BACKPLANE CONNECTOR, J02 (Contd)		
PIN	**DESCRIPTION**	**FUNCTION**
51	+5V (VCC)	POWER
52	GROUND (GRD)	GROUND
53	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
54	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
55	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
56	GROUND (GRD)	GROUND
57	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
58	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
59	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
60	GROUND (GRD)	GROUND
61	+5V (VCC)	POWER
62	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
63	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
64	GROUND (GRD)	GROUND
65	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
66	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
67	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
68	GROUND (GRD)	GROUND
69	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
70	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
71	+5V (VCC)	POWER
72	GROUND (GRD)	GROUND
73	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
74	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	INPUT/OUTPUT
75	PERIPHERAL BUS FAULT (PFLT[0])	INPUT/OUTPUT
76	GROUND (GRD)	GROUND
77	PERIPHERAL CARD FAILURE (PFAIL[0])	INPUT/OUTPUT
78	PERIPHERAL BUS BUSY (PBUSY[0])	INPUT/OUTPUT
79	SYSTEM RESET (SYSRST[0])	INPUT/OUTPUT
80	GROUND (GRD)	GROUND
81	+5V (VCC)	POWER
82	PERIPHERAL INTERRUPT ACKNOWLEDGE 0 (PIAK0[0])	INPUT/OUTPUT
83	REQUEST SYSTEM RESET (RQRST[0])	INPUT/OUTPUT
84	PERIPHERAL INTERRUPT ACKNOWLEDGE 1 (PIAK1[0])	INPUT/OUTPUT
85	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	INPUT/OUTPUT
86	PERIPHERAL INTERRUPT ACKNOWLEDGE 2 (PIAK2[0])	INPUT/OUTPUT
87	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	INPUT/OUTPUT
88	GROUND (GRD)	GROUND
89	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])	INPUT/OUTPUT
90	BACKUP BATTERY (+3.9V) (VBKUP)	POWER
91	+5V (VCC)	POWER
92	GROUND (GRD)	GROUND
93	PERIPHERAL CARD SELECT 01 (PCS01[0])	OUTPUT
94	-12V (V12N)	POWER
95	PERIPHERAL CARD SELECT 02 (PCS02[0])	OUTPUT
96	GROUND (GRD)	GROUND
97	PERIPHERAL CARD SELECT 03 (PCS03[0])	OUTPUT
98	+12V (V12P)	INPUT/OUTPUT
99	PERIPHERAL CARD SELECT 04 (PCS04[0])	OUTPUT
100	GROUND (GRD)	GROUND

60-PIN BACKPLANE CONNECTOR, J03		
PIN	DESCRIPTION	FUNCTION
1	+5V (VCC)	POWER
2	PERIPHERAL CARD SELECT 05 (PCS05[0])	OUTPUT
3	+5V (VCC)	POWER
4	GROUND (GRD)	GROUND
5	PERIPHERAL CARD SELECT 06 (PCS06[0])	OUTPUT
6	GROUND (GRD)	GROUND
7	+5V (VCC)	POWER
8	GROUND (GRD)	GROUND
9	+5V (VCC)	POWER
10	GROUND (GRD)	GROUND
11	PERIPHERAL CARD SELECT 07 (PCS07[0])	OUTPUT
12	GROUND (GRD)	GROUND
13	+5V (VCC)	POWER
14	GROUND (GRD)	GROUND
15	+5V (VCC)	POWER
16	GROUND (GRD)	GROUND
17	PERIPHERAL CARD SELECT 08 (PCS08[0])	OUTPUT
18	GROUND (GRD)	GROUND
19	+5V (VCC)	POWER
20	GROUND (GRD)	GROUND
21	+5V (VCC)	POWER
22	GROUND (GRD)	GROUND
23	PERIPHERAL CARD SELECT 09 (PCS09[0])	OUTPUT
24	GROUND (GRD)	GROUND
25	+5V (VCC)	POWER
26	GROUND (GRD)	GROUND
27	+5V (VCC)	POWER
28	GROUND (GRD)	GROUND
29	PERIPHERAL CARD SELECT 10 (PCS10[0])	OUTPUT
30	GROUND (GRD)	GROUND

60-PIN BACKPLANE CONNECTOR, J03 (Contd)		
PIN	DESCRIPTION	FUNCTION
31	+5V (VCC)	POWER
32	GROUND (GRD)	GROUND
33	+5V (VCC)	POWER
34	GROUND (GRD)	GROUND
35	PERIPHERAL CARD SELECT 11 (PCS11[0])	OUTPUT
36	GROUND (GRD)	GROUND
37	+5V (VCC)	POWER
38	GROUND (GRD)	GROUND
39	+5V (VCC)	POWER
40	GROUND (GRD)	GROUND
41	PERIPHERAL CARD SELECT 12 (PCS12[0])	OUTPUT
42	GROUND (GRD)	GROUND
43	+5V (VCC)	POWER
44	GROUND (GRD)	GROUND
45	+5V (VCC)	POWER
46	GROUND (GRD)	GROUND
47	PERIPHERAL CARD SELECT 13 (PCS13[0])	OUTPUT
48	GROUND (GRD)	GROUND
49	+5V (VCC)	POWER
50	GROUND (GRD)	GROUND
51	+5V (VCC)	POWER
52	GROUND (GRD)	GROUND
53	PERIPHERAL CARD SELECT 14 (PCS14[0])	OUTPUT
54	GROUND (GRD)	GROUND
55	+5V (VCC)	POWER
56	GROUND (GRD)	GROUND
57	+5V (VCC)	POWER
58	GROUND (GRD)	GROUND
59	PERIPHERAL CARD SELECT 15 (PCS15[0])	OUTPUT
60	GROUND (GRD)	GROUND

15-PIN POWER CONNECTOR, J04		
PIN	DESCRIPTION	FUNCTION
1	RESET SWITCH (RTSTSW[0])	CONTROL
2	RESET SWITCH GROUND	CONTROL
3	+12V RS-232C SUPPLY (V12P)	POWER
4	-12V RS-232C SUPPLY (V12N)	POWER
5	GROUND (GRD)	GROUND
6	REMOTE VCC SENSE (PONSW[0]) (SOFT POWER CONTROL) (POWER DOWN REQUEST)	CONTROL
7	REMOTE GROUND SENSE (PWRON[1]) (SOFT POWER CONTROL) (ac POWER CONTROL)	CONTROL
8	GROUND (GRD)	GROUND
9	GROUND (GRD)	GROUND
10	GROUND (GRD)	GROUND
11	GROUND (GRD)	GROUND
12	+5V LOGIC SUPPLY (VCC)	POWER
13	+5V LOGIC SUPPLY (VCC)	POWER
14	+5V LOGIC SUPPLY (VCC)	POWER
15	+5V LOGIC SUPPLY (VCC)	POWER

72-PIN MEMORY CARD CONNECTOR, J05 AND J06		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND (GRD)	GROUND
2	VCC	POWER
3	MULTIPLEXED ADDRESS BIT 7 (MUXA7[1])	OUTPUT
4	MULTIPLEXED ADDRESS BIT 0 (MUXA0[1])	OUTPUT
5	MULTIPLEXED ADDRESS BIT 6 (MUXA6[1])	OUTPUT
6	MULTIPLEXED ADDRESS BIT 1 (MUXA1[1])	OUTPUT
7	MULTIPLEXED ADDRESS BIT 5 (MUXA5[1])	OUTPUT
8	GROUND (GRD)	GROUND
9	MULTIPLEXED ADDRESS BIT 4 (MUXA4[1])	OUTPUT
10	MULTIPLEXED ADDRESS BIT 2 (MUXA2[1])	OUTPUT
11	MULTIPLEXED ADDRESS BIT 8 (MUXA8[1])	OUTPUT
12	MULTIPLEXED ADDRESS BIT 3 (MUXA3[1])	OUTPUT
13	GROUND (GRD)	GROUND
14	MULTIPLEXED ADDRESS BIT 9 (MUXA9[1])	OUTPUT
15	WRITE ENABLE (WE[0])	OUTPUT
16	ROW ADDRESS SELECT (RAS[0])	OUTPUT
17	BANK ENABLE 0 (BANKEN0[0])	OUTPUT
18	BANK ENABLE 1 (BANKEN1[0])	OUTPUT
19	ONEBANK[0]	(0 = 191A/B/C) (1 = 191D and 192A/B)
20	COLUMN ADDRESS SELECT 2 (CAS2[0])	OUTPUT
21	COLUMN ADDRESS SELECT 0 (CAS0[0])	OUTPUT
22	COLUMN ADDRESS SELECT 3 (CAS3[0])	OUTPUT
23	GROUND (GRD)	GROUND
24	SIZE64K[0]	(0 = 191A and 192A) (1 = 191B/C/D and 192B)
25	COLUMN ADDRESS SELECT 1 (CAS1[0])	OUTPUT
26	MEMORY DATA BIT 31 (MD31[1])	INPUT/OUTPUT
27	MEMORY DATA BIT 30 (MD30[1])	INPUT/OUTPUT
28	GROUND (GRD)	GROUND
29	MEMORY DATA BIT 28 (MD28[1])	INPUT/OUTPUT
30	MEMORY DATA BIT 29 (MD29[1])	INPUT/OUTPUT
31	MEMORY DATA BIT 26 (MD26[1])	INPUT/OUTPUT
32	MEMORY DATA BIT 27 (MD27[1])	INPUT/OUTPUT
33	GROUND (GRD)	GROUND
34	MEMORY DATA BIT 25 (MD25[1])	INPUT/OUTPUT
35	MEMORY DATA BIT 24 (MD24[1])	INPUT/OUTPUT
36	MEMORY DATA BIT 23 (MD23[1])	INPUT/OUTPUT
37	MEMORY DATA BIT 22 (MD22[1])	INPUT/OUTPUT

72-PIN MEMORY CARD CONNECTOR, J05 AND J06 (Contd)		
PIN	DESCRIPTION	FUNCTION
38	GROUND (GRD)	GROUND
39	MEMORY DATA BIT 20 (MD20[1])	INPUT/OUTPUT
40	MEMORY DATA BIT 21 (MD21[1])	INPUT/OUTPUT
41	MEMORY DATA BIT 18 (MD18[1])	INPUT/OUTPUT
42	MEMORY DATA BIT 19 (MD19[1])	INPUT/OUTPUT
43	GROUND (GRD)	GROUND
44	MEMORY DATA BIT 17 (MD17[1])	INPUT/OUTPUT
45	MEMORY DATA BIT 16 (MD16[1])	INPUT/OUTPUT
46	MEMORY DATA BIT 15 (MD15[1])	INPUT/OUTPUT
47	MEMORY DATA BIT 14 (MD14[1])	INPUT/OUTPUT
48	GROUND (GRD)	GROUND
49	MEMORY DATA BIT 12 (MD12[1])	INPUT/OUTPUT
50	MEMORY DATA BIT 13 (MD13[1])	INPUT/OUTPUT
51	MEMORY DATA BIT 10 (MD10[1])	INPUT/OUTPUT
52	MEMORY DATA BIT 11 (MD11[1])	INPUT/OUTPUT
53	GROUND (GRD)	GROUND
54	MEMORY DATA BIT 09 (MD09[1])	INPUT/OUTPUT
55	MEMORY DATA BIT 08 (MD08[1])	INPUT/OUTPUT
56	MEMORY DATA BIT 07 (MD07[1])	INPUT/OUTPUT
57	MEMORY DATA BIT 06 (MD06[1])	INPUT/OUTPUT
58	MEMORY DATA BIT 05 (MD05[1])	INPUT/OUTPUT
59	MEMORY DATA BIT 04 (MD04[1])	INPUT/OUTPUT
60	GROUND (GRD)	GROUND
61	MEMORY DATA BIT 02 (MD02[1])	INPUT/OUTPUT
62	MEMORY DATA BIT 03 (MD03[1])	INPUT/OUTPUT
63	GROUND (GRD)	GROUND
64	MEMORY DATA BIT 01 (MD01[1])	INPUT/OUTPUT
65	MEMORY DATA BIT 00 (MD00[1])	INPUT/OUTPUT
66	MEMORY CARD EQUIPPED (MCEQUIP[0])	GROUND
67	MEMORY PARITY ADDRESS REGISTER BIT 0 (MPAR0[1])	INPUT/OUTPUT
68	MEMORY PARITY ADDRESS REGISTER BIT 2 (MPAR2[1])	INPUT/OUTPUT
69	MEMORY PARITY ADDRESS REGISTER BIT 1 (MPAR1[1])	INPUT/OUTPUT
70	MEMORY PARITY ADDRESS REGISTER BIT 3 (MPAR3[1])	INPUT/OUTPUT
71	GROUND (GRD)	GROUND
72	+5V (VCC)	POWER

34-HARD DISK READ/WRITE CONNECTOR, J07		
PIN	DESCRIPTION	FUNCTION
1	GROUND	GROUND
2	HEAD SELECT 3 (HS3[0])	OUTPUT
	REDUCED WRITE CURRENT (RWC[0])	OUTPUT
3	GROUND	GROUND
4	HEAD SELECT 2 (HS2[0])	OUTPUT
5	GROUND	GROUND
6	WRITE GATE (WGATE[0])	OUTPUT
7	GROUND	GROUND
8	SEEK COMPLETE (SKC[0])	INPUT
9	GROUND	GROUND
10	TRACK 0 (TRK[0])	INPUT
11	GROUND	GROUND
12	WRITE FAULT (WRTFLT[0])	INPUT
13	GROUND	GROUND
14	HEAD SELECT 0 (HS0[0])	OUTPUT
15	GROUND	GROUND
16	CONNECTOR COMMON (J2P7)	GROUND
17	GROUND	GROUND
18	HEAD SELECT 1 (HS1[0])	OUTPUT
19	GROUND	GROUND
20	INDEX (INDEX[0])	INPUT
21	GROUND	GROUND
22	READY (RDY[0])	INPUT
23	GROUND	GROUND
24	STEP (XSTEP[0])	OUTPUT
25	GROUND	GROUND
26	DRIVE SELECT 0 (DSEL0[0])	OUTPUT
27	GROUND	GROUND
28	DRIVE SELECT 1 (DSEL1[0])	OUTPUT
29	GROUND	GROUND
30	NOT USED	NC
31	GROUND	GROUND
32	NOT USED	NC
33	GROUND	GROUND
34	DIRECTION IN (DIR[0])	OUTPUT

LEGEND:

NC No Connection

20-PIN HARD DISK CONTROL 0 CONNECTOR, J08		
PIN	**DESCRIPTION**	**FUNCTION**
1	DRIVE SELECTED (DSD[0])	INPUT
2	GROUND	GROUND
3	NOT USED	NC
4	GROUND	GROUND
5	GROUND	GROUND
6	GROUND	GROUND
7	CONNECTOR COMMON (J1P16)	GROUND
8	GROUND	GROUND
9	NOT USED	NC
10	GROUND	GROUND
11	GROUND	GROUND
12	GROUND	GROUND
13	+MFM WRITE DATA (MFMOP[0])	OUTPUT
14	-MFM WRITE DATA (MFMON[0])	OUTPUT
15	GROUND	GROUND
16	GROUND	GROUND
17	+MFM READ DATA (MFMIP[0])	INPUT
18	-MFM READ DATA (MFMIN[0])	INPUT
19	GROUND	GROUND
20	NOT USED	NC

LEGEND:

MFM Modified Frequency Modulation
NC No Connection

20-PIN HARD DISK CONTROL 1 CONNECTOR, J09		
PIN	**DESCRIPTION**	**FUNCTION**
1	DRIVE SELECTED (DSD[0])	INPUT
2	GROUND	GROUND
3	NOT USED	NC
4	GROUND	GROUND
5	GROUND	GROUND
6	GROUND	GROUND
7	CONNECTOR COMMON (J1P16)	—
8	GROUND	GROUND
9	NOT USED	NC
10	GROUND	GROUND
11	GROUND	GROUND
12	GROUND	GROUND
13	+MFM WRITE DATA (MFMOP[1])	OUTPUT
14	-MFM WRITE DATA (MFMON[1])	OUTPUT
15	GROUND	GROUND
16	GROUND	GROUND
17	+MFM READ DATA (MFMIP[1])	INPUT
18	-MFM READ DATA (MFMIN[1])	INPUT
19	GROUND	GROUND
20	NOT USED	NC

LEGEND:

MFM Modified Frequency Modulation
NC No Connection

34-PIN FLOPPY DISK CONNECTOR, J10		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND	GROUND
2	NOT USED	NC
3	GROUND	GROUND
4	NOT USED	NC
5	GROUND	GROUND
6	NOT USED	NC
7	GROUND	GROUND
8	INDEX (FINDEX[0])	INPUT
9	GROUND	GROUND
10	FLOPPY DRIVE SELECT 0 (FDSEL[0])	OUTPUT
11	GROUND	GROUND
12	NOT USED	NC
13	GROUND	GROUND
14	NOT USED	NC
15	GROUND	GROUND
16	MOTOR ON (MON[0])	OUTPUT
17	GROUND	GROUND
18	FLOPPY DIRECTION SELECT (FDIRC[0])	OUTPUT
19	GROUND	GROUND
20	FLOPPY STEP (FSTEP[0])	OUTPUT
21	GROUND	GROUND
22	WRITE DATA (FWDATA[0])	OUTPUT
23	GROUND	GROUND
24	FLOPPY WRITE GATE (FWGATE[0])	OUTPUT
25	GROUND	GROUND
26	FLOPPY TRACK 0 (FTR0[0])	INPUT
27	GROUND	GROUND
28	FLOPPY WRITE PROTECT (FWRTPRT[0])	INPUT
29	GROUND	GROUND
30	READ DATA (FRDATA[0])	INPUT
31	GROUND	GROUND
32	FLOPPY SIDE SELECT (FSSEL[0])	OUTPUT
33	GROUND	GROUND
34	FLOPPY READY (FRDY[0])	INPUT

LEGEND:

NC No Connection

3-PIN BATTERY CONNECTOR, J11	
PIN	**DESCRIPTION**
1	+3.9V (VBAT)
2	NOT USED
3	GROUND

2-PIN DIAGNOSTIC INDICATOR CONNECTOR, J12	
PIN	**DESCRIPTION**
1	D1PU1 (+)
2	ERLED0 (-)

2-PIN POWER INDICATOR CONNECTOR, J13	
PIN	**DESCRIPTION**
1	D2PU2 (+)
2	GLEDON0 (-)

2-PIN AUXILIARY DISK INTERFACE SOFT POWER CONNECTOR, J14	
PIN	**DESCRIPTION**
1	VCC (+5V)
2	GROUND

CM518A/B/C SYSTEM BOARD INTERCONNECTIONS

Figures B-3, B-4, and B-5 show the layouts of the CM518 series System Boards. Refer to these figures for system board connector location information. Pin and signal information is provided in tables following the figures for each of the system board connectors. The connector tables are presented in sequence by connector designation. The figures are printed front and back with a blank unit so that either figure can be used in conjunction with any table.

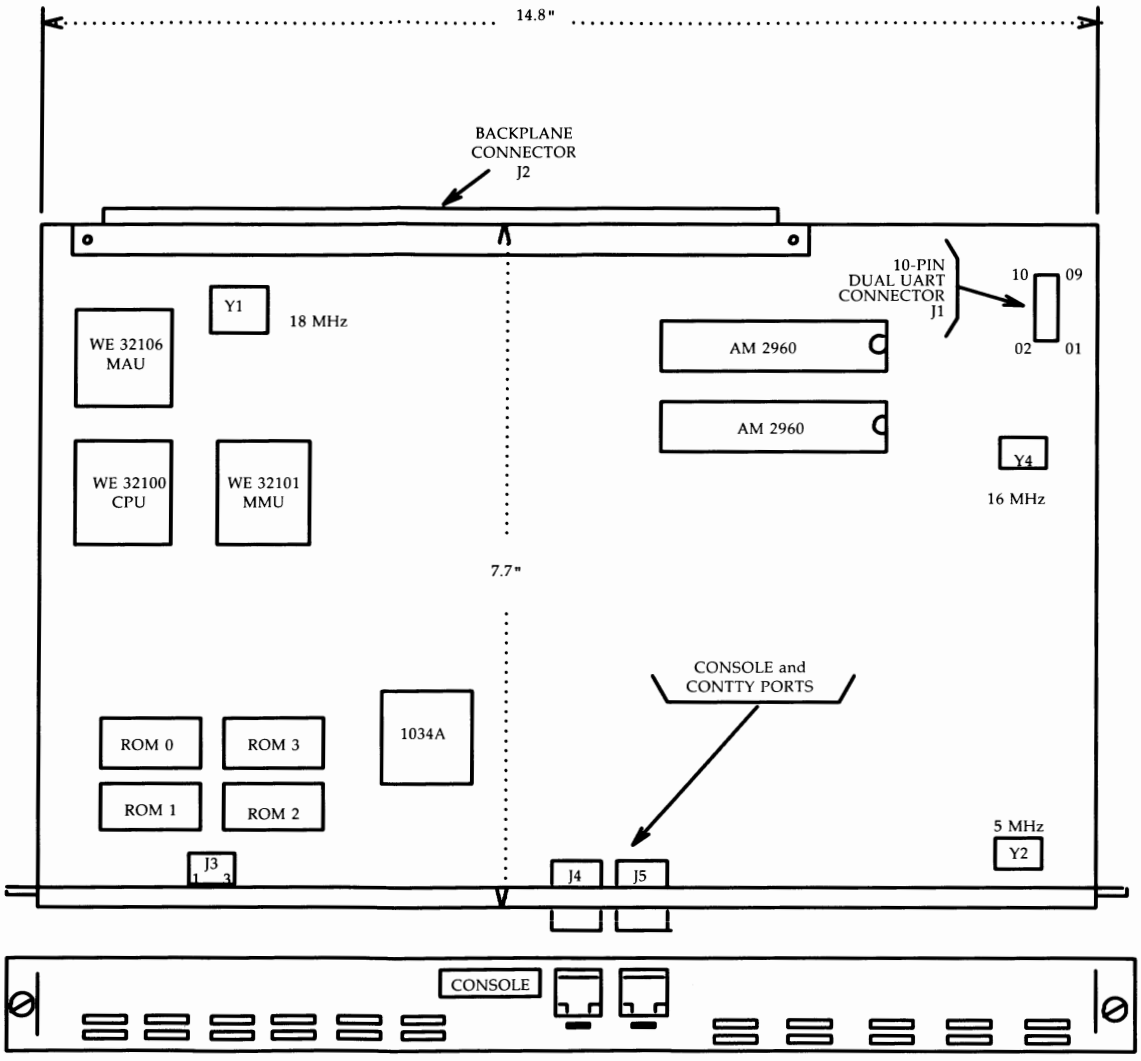


Figure B-3: CM518A System Board Layout

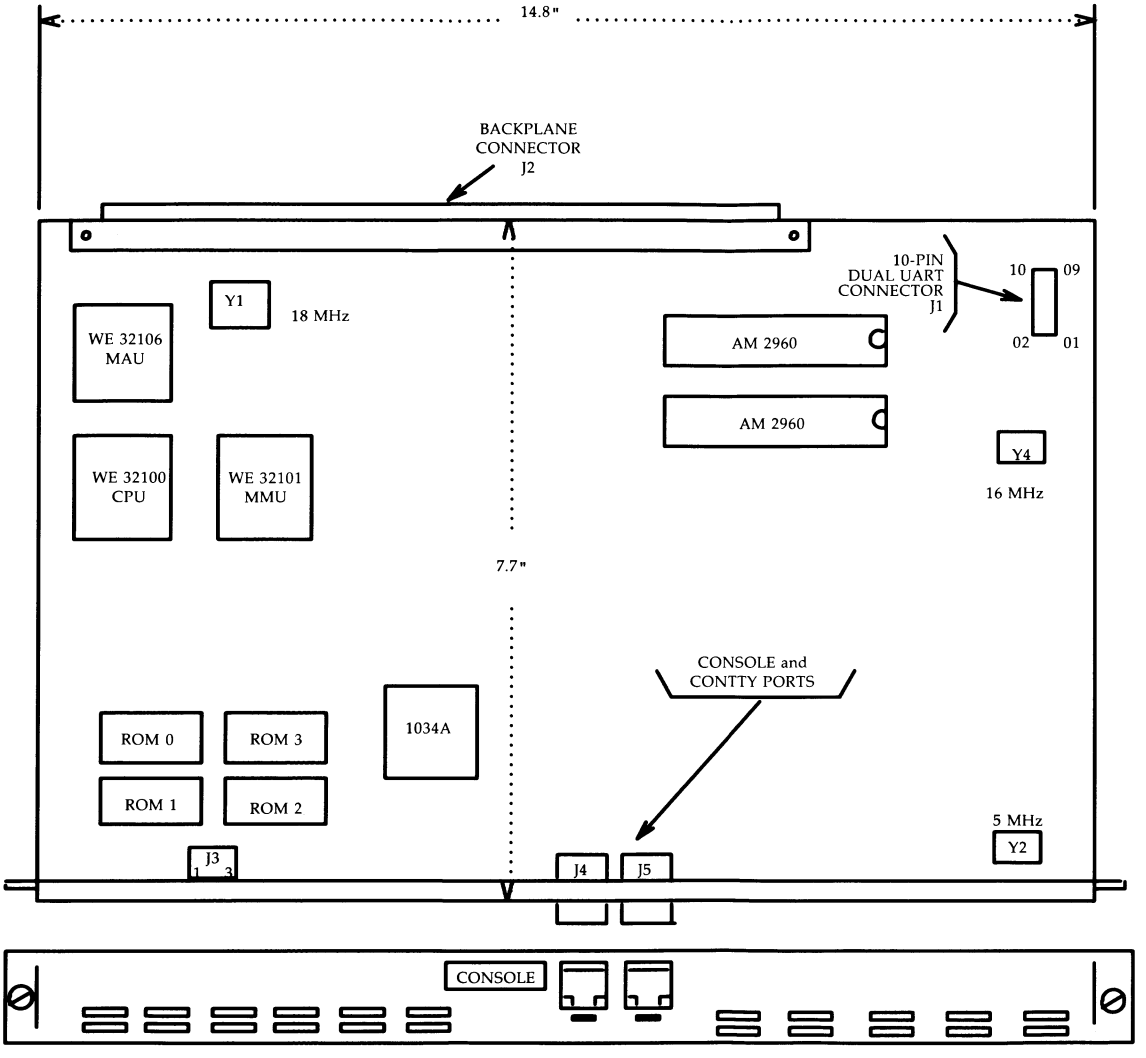


Figure B-3: CM518A System Board Layout

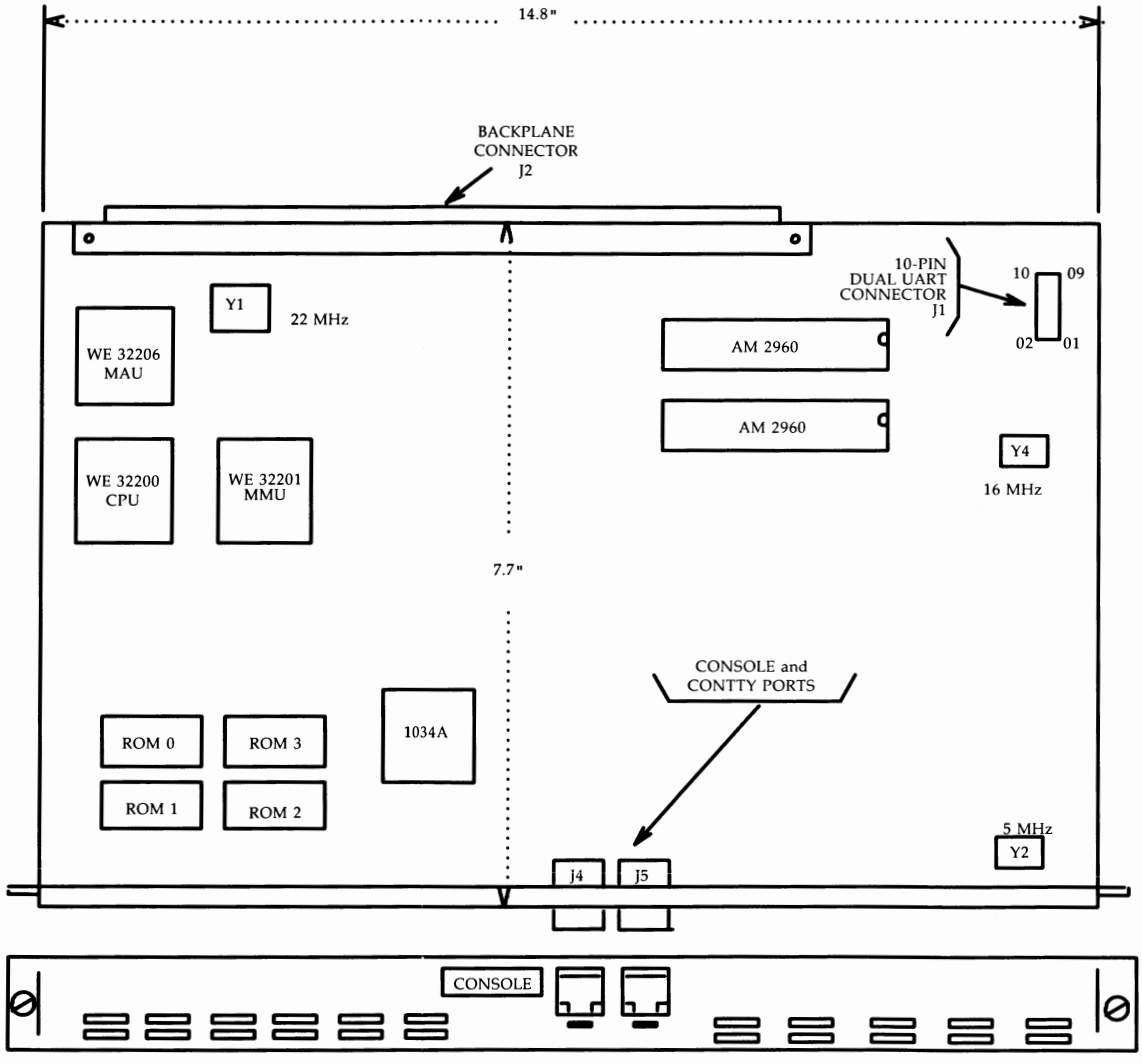


Figure B-4: CM518B System Board Layout

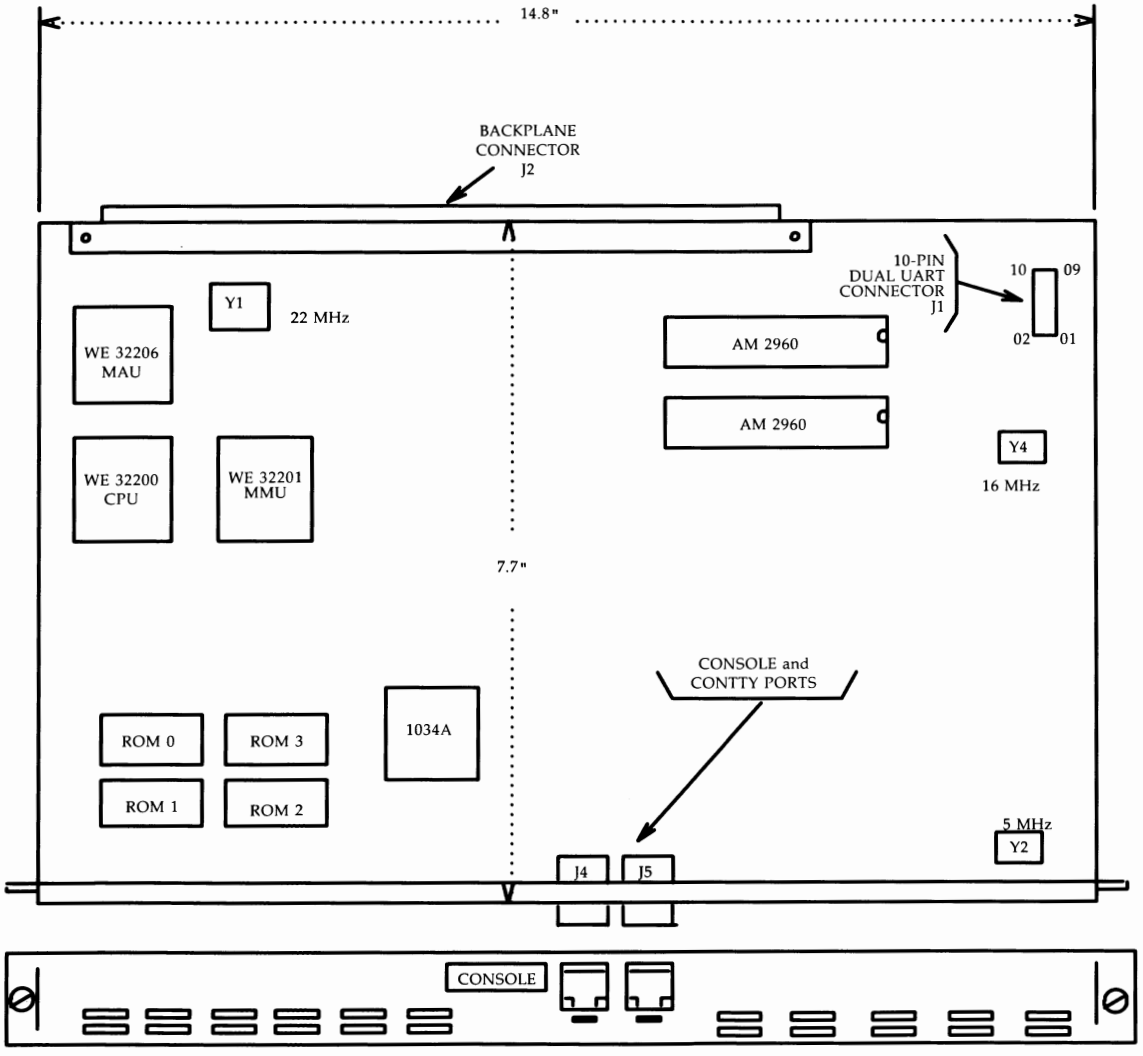


Figure B-4: CM518B System Board Layout

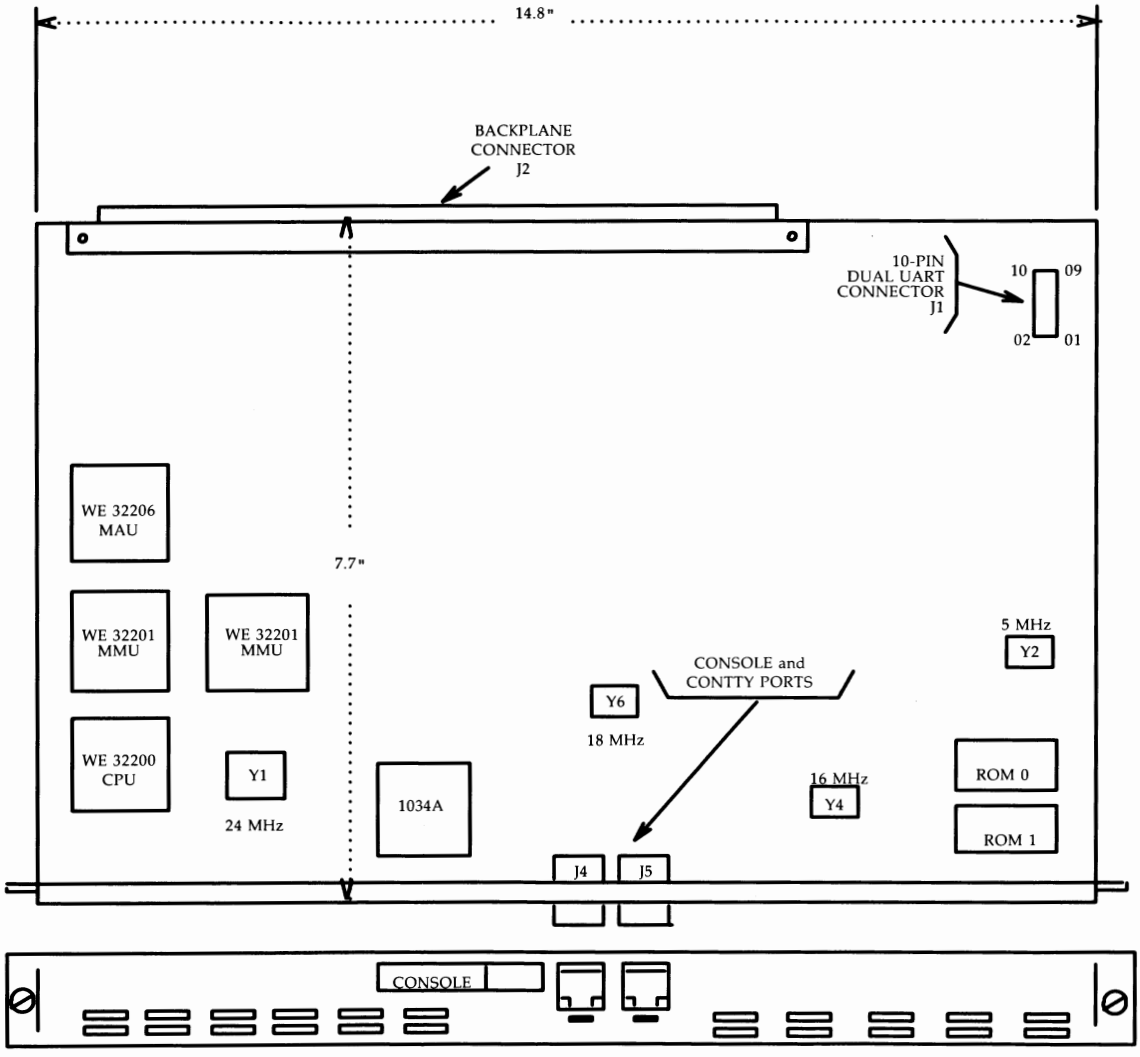


Figure B-5: CM518C System Board Layout

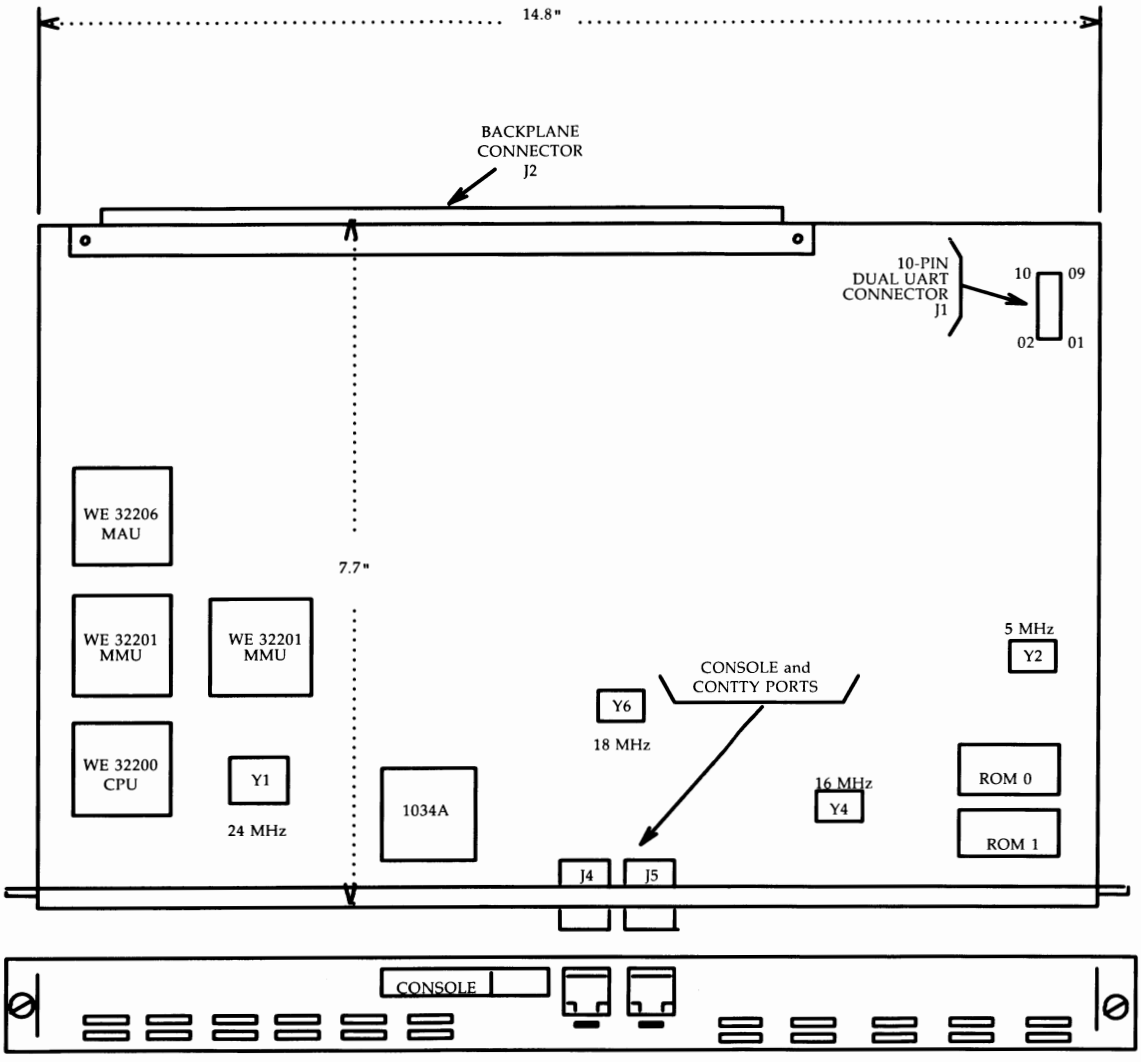


Figure B-5: CM518C System Board Layout

464-PIN BACKPLANE CONNECTOR, J02		
PIN	DESCRIPTION	FUNCTION
001	+12V (V12P)	POWER
002	+5V (VCC)	POWER
003	FLOPPY READY (FRDY[0])	INPUT
004	FLOPPY SIDE SELECT (FSSEL[0])	OUTPUT
005	-12V (V12N)	POWER
006	FLOPPY READ DATA (FRDATA[0])	INPUT
007	GROUND (GRD)	GROUND
008	FLOPPY WRITE PROTECT (FWRPRT[0])	INPUT
009	FLOPPY TRACK 0 (FTR0[0])	INPUT
010	GROUND (GRD)	GROUND
011	FLOPPY WRITE GATE (FWGATE[0])	OUTPUT
012	FLOPPY WRITE DATA (FWDATA[0])	OUTPUT
013	FLOPPY STEP (FSTEP[0])	OUTPUT
014	FLOPPY DIRECTION SELECT (FDIRC[0])	OUTPUT
015	FLOPPY MOTOR ON (FMOTON[0])	OUTPUT
016	FLOPPY DRIVE SELECT 2 (FDS2[0])	OUTPUT
017	FLOPPY DRIVE SELECT 1 (FDS1[0])	OUTPUT
018	FLOPPY DRIVE SELECT 0 (FDS0[0])	OUTPUT
019	+5V (VCC)	POWER
020	FLOPPY LOW RPM (FLOW[0])	OUTPUT
021	FLOPPY INDEX (FINDEX[0])	INPUT
022	FLOPPY DRIVE SELECT 3 (FDS3[0])	OUTPUT
023	NOT USED (FSPARE[0])	INPUT
024	MEMORY CHECK BIT 00 (MCB00[1])	INPUT/OUTPUT
025	MEMORY CHECK BIT 01 (MCB01[1])	INPUT/OUTPUT
026	GROUND (GRD)	GROUND
027	MEMORY CHECK BIT 03 (MCB03[1])	INPUT/OUTPUT
028	MEMORY CHECK BIT 02 (MCB02[1])	INPUT/OUTPUT
029	MEMORY CHECK BIT 05 (MCB05[1])	INPUT/OUTPUT
030	MEMORY CHECK BIT 04 (MCB04[1])	INPUT/OUTPUT
031	+5V (VCC)	POWER
032	MEMORY CHECK BIT 09 (MCB09[1])	INPUT/OUTPUT
033	MEMORY CHECK BIT 06 (MCB06[1])	INPUT/OUTPUT
034	MEMORY CHECK BIT 07 (MCB07[1])	INPUT/OUTPUT
035	MEMORY CHECK BIT 08 (MCB08[1])	INPUT/OUTPUT
036	MEMORY CHECK BIT 11 (MCB11[1])	INPUT/OUTPUT
037	MEMORY CHECK BIT 10 (MCB10[1])	INPUT/OUTPUT
038	GROUND (GRD)	GROUND
039	MEMORY DATA BIT 00 (MD00[1])	INPUT/OUTPUT
040	MEMORY DATA BIT 01 (MD01[1])	INPUT/OUTPUT
041	MEMORY DATA BIT 02 (MD02[1])	INPUT/OUTPUT
042	MEMORY DATA BIT 03 (MD03[1])	INPUT/OUTPUT
043	GROUND (GRD)	GROUND
044	MEMORY DATA BIT 04 (MD04[1])	INPUT/OUTPUT
045	MEMORY DATA BIT 05 (MDO5[1])	INPUT/OUTPUT
046	+5V (VCC)	POWER
047	MEMORY DATA BIT 06 (MD06[1])	INPUT/OUTPUT
048	MEMORY DATA BIT 07 (MD07[1])	INPUT/OUTPUT
049	MEMORY DATA BIT 08 (MD08[1])	INPUT/OUTPUT
050	MEMORY DATA BIT 09 (MD09[1])	INPUT/OUTPUT
051	MEMORY DATA BIT 10 (MD10[1])	INPUT/OUTPUT
052	MEMORY DATA BIT 11 (MD11[1])	INPUT/OUTPUT
053	MEMORY DATA BIT 12 (MD12[1])	INPUT/OUTPUT
054	MEMORY DATA BIT 13 (MD13[1])	INPUT/OUTPUT
055	GROUND (GRD)	GROUND
056	MEMORY DATA BIT 14 (MD14[1])	INPUT/OUTPUT
057	MEMORY DATA BIT 15 (MD15[1])	INPUT/OUTPUT
058	MEMORY DATA BIT 16 (MD16[1])	INPUT/OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)		
PIN	DESCRIPTION	FUNCTION
059	MEMORY DATA BIT 17 (MD17[1])	INPUT/OUTPUT
060	MEMORY DATA BIT 18 (MD18[1])	INPUT/OUTPUT
061	MEMORY DATA BIT 19 (MD19[1])	INPUT/OUTPUT
062	GROUND (GRD)	GROUND
063	MEMORY DATA BIT 20 (MD20[1])	INPUT/OUTPUT
064	MEMORY DATA BIT 21 (MD21[1])	INPUT/OUTPUT
065	MEMORY DATA BIT 22 (MD22[1])	INPUT/OUTPUT
066	MEMORY DATA BIT 23 (MD23[1])	INPUT/OUTPUT
067	MEMORY DATA BIT 24 (MD24[1])	INPUT/OUTPUT
068	MEMORY DATA BIT 25 (MD25[1])	INPUT/OUTPUT
069	MEMORY DATA BIT 26 (MD26[1])	INPUT/OUTPUT
070	MEMORY DATA BIT 27 (MD27[1])	INPUT/OUTPUT
071	GROUND (GRD)	GROUND
072	MEMORY DATA BIT 28 (MD28[1])	INPUT/OUTPUT
073	MEMORY DATA BIT 29 (MD29[1])	INPUT/OUTPUT
074	MEMORY DATA BIT 30 (MD30[1])	INPUT/OUTPUT
075	MEMORY DATA BIT 31 (MD31[1])	INPUT/OUTPUT
076	SLOT 3 EQUIPPED (S3EQUIP[0])	INPUT
077	SLOT 3 SIZE 1 (S3SIZ1[1])	INPUT
078	+5V (VCC)	POWER
079	SLOT 3 SIZE 0 (S3SIZ0[1])	INPUT
080	SLOT 2 EQUIPPED (S2EQUIP[0])	INPUT
081	SLOT 2 SIZE 1 (S2SIZ1[1])	INPUT
082	SLOT 2 SIZE 0 (S2SIZ0[1])	INPUT
083	GROUND (GRD)	GROUND
084	SLOT 1 EQUIPPED (S1EQUIP[0])	INPUT
085	SLOT 1 SIZE 1 (S1SIZ1[1])	INPUT
086	SLOT 1 SIZE 0 (S1SIZ0[1])	INPUT
087	SLOT 0 SIZE 1 (S0SIZ1[1])	INPUT
088	SLOT 0 EQUIPPED (S0EQUIP[0])	INPUT
089	SLOT 0 SIZE 0 (S0SIZ0[1])	INPUT
090	GROUND (GRD)	GROUND
091	COLUMN ADDRESS STROBE 1 (CAS1[0])	OUTPUT
092	BANK ENABLE 2 (BANKEN2[0])	OUTPUT
093	COLUMN ADDRESS STROBE 0 (CAS0[0])	OUTPUT
094	COLUMN ADDRESS STROBE 2 (CAS2[0])	OUTPUT
095	COLUMN ADDRESS STROBE 3 (CAS3[0])	OUTPUT
096	SLOT 3 BANK ENABLE 1 (S3BKEN1[0])	OUTPUT
097	SLOT 3 BANK ENABLE 0 (S3BKEN0[0])	OUTPUT
098	SLOT 2 BANK ENABLE 1 (S2BKEN1[0])	OUTPUT
099	GROUND (GRD)	GROUND
100	SLOT 1 BANK ENABLE 1 (S1BKEN1[0])	OUTPUT
101	SLOT 2 BANK ENABLE 0 (S2BKEN0[0])	OUTPUT
102	GROUND (GRD)	GROUND
103	SLOT 1 BANK ENABLE 0 (S1BKEN0[0])	OUTPUT
104	ROW ADDRESS STROBE 1 (RAS1[0])	OUTPUT
105	SLOT 0 BANK ENABLE 0 (S0BKEN0[0])	OUTPUT
106	SLOT 0 BANK ENABLE 1 (S0BKEN1[0])	OUTPUT
107	+5V (VCC)	POWER
108	ROW ADDRESS STROBE 0 (RAS0[0])	OUTPUT
109	WRITE ENABLE 1 (WE1[0])	OUTPUT
110	GROUND (GRD)	GROUND
111	MEMORY CYCLE STATUS (G[0])	OUTPUT
112	NOT USED	NC
113	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	INPUT/OUTPUT
114	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	INPUT/OUTPUT
115	WRITE ENABLE 0 (WE0[0])	OUTPUT
116	BUB CONNECTOR CHIP SELECT 2 (BCCS2[0])	OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)		
PIN	DESCRIPTION	FUNCTION
117	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	INPUT/OUTPUT
118	GROUND (GRD)	GROUND
119	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	INPUT/OUTPUT
120	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	INPUT/OUTPUT
121	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	INPUT/OUTPUT
122	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	INPUT/OUTPUT
123	+5V (VCC)	POWER
124	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	INPUT/OUTPUT
125	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	INPUT/OUTPUT
126	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	INPUT/OUTPUT
127	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	INPUT/OUTPUT
128	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	INPUT/OUTPUT
129	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	INPUT/OUTPUT
130	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	INPUT/OUTPUT
131	GROUND (GRD)	GROUND
132	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	INPUT/OUTPUT
133	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	INPUT/OUTPUT
134	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	INPUT/OUTPUT
135	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	INPUT/OUTPUT
136	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	INPUT/OUTPUT
137	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
138	+5V (VCC)	POWER
139	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
140	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	INPUT/OUTPUT
141	NOT USED	NC
142	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
143	GROUND (GRD)	GROUND
144	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	INPUT/OUTPUT
145	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
146	GROUND (GRD)	GROUND
147	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
148	PERIPHERAL READ-WRITE (PR1W[0])	INPUT/OUTPUT
149	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
150	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
151	+5V (VCC)	POWER
152	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
153	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
154	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
155	PERIPHERAL BUS REQUEST (PBRQ[0])	INPUT
156	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
157	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
158	GROUND (GRD)	GROUND
159	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
160	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
161	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
162	PERIPHERAL CARD WIDTH (8 OR 16 BITS) (PSIZE16[0])	INPUT
163	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
164	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
165	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
166	+5V (VCC)	POWER
167	PERIPHERAL BUS BUSY (PBUSY[0])	INPUT/OUTPUT
168	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
169	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
170	GROUND (GRD)	GROUND
171	PERIPHERAL INTERRUPT ACKNOWLEDGE 0 (PIAK0[0])	OUTPUT
172	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
173	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
174	PERIPHERAL INTERRUPT ACKNOWLEDGE 1 (PIAK1[0])	OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)			
PIN	DESCRIPTION		FUNCTION
175	GROUND (GRD)		GROUND
176	PERIPHERAL DATA STROBE 1 (PDS1[0])		INPUT/OUTPUT
177	RECEIVED FAILURE (RFAIL[0])		INPUT
178	+5V (VCC)		POWER
179	PERIPHERAL INTERRUPT ACKNOWLEDGE 2 (PIAK2[0])		OUTPUT
180	PERIPHERAL BUS FAULT (PFLT[0])		INPUT/OUTPUT
181	PERIPHERAL CARD SELECT 09 (PCS09[0])		OUTPUT
182	PERIPHERAL CARD SELECT 10 (PCS10[0])		OUTPUT
183	PERIPHERAL CARD SELECT 11 (PCS11[0])		OUTPUT
184	PERIPHERAL CARD SELECT 12 (PCS12[0])		OUTPUT
185	PERIPHERAL CARD SELECT 06 (PCS06[0])		OUTPUT
186	GROUND (GRD)		GROUND
187	PERIPHERAL CARD SELECT 07 (PCS07[0])		OUTPUT
188	PERIPHERAL CARD SELECT 08 (PCS08[0])		OUTPUT
189	PERIPHERAL CARD SELECT 03 (PCS03[0])		OUTPUT
190	PERIPHERAL CARD SELECT 04 (PCS04[0])		OUTPUT
191	GROUND (GRD)		GROUND
192	PERIPHERAL CARD SELECT 05 (PCS05[0])		OUTPUT
193	PERIPHERAL BUS ACKNOWLEDGE (PBACK[0])		OUTPUT
194	BUB GRANTED SLOT 1 (BUBGT1[0])		OUTPUT
195	PERIPHERAL CARD SELECT 01 (PCS01[0])		OUTPUT
196	PERIPHERAL CARD SELECT 02 (PCS02[0])		OUTPUT
197	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])		INPUT
198	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])		INPUT
199	GROUND (GRD)		GROUND
200	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])		INPUT
201	BACKUP BATTERY (VBKUP)		OUTPUT
202	GROUND (GRD)		GROUND
203	PERIPHERAL SEQUENTIAL ACCESS (PSEQACC[0])		OUTPUT
204	BUB BUS REQUEST SLOT 2 (BUBRQ2[0])		INPUT
205	BUB DATA STROBE (BDS[0])		INPUT/OUTPUT
206	BUB ADDRESS STROBE (BAS[0])		INPUT/OUTPUT
207	GROUND (GRD)		GROUND
208	BUB DATA ACKNOWLEDGE (BDTCK[0])		INPUT/OUTPUT
209	BUB GRANTED SLOT 0 (BUBGT0[0])		OUTPUT
210	GROUND (GRD)		GROUND
211	BUB BYPASS MODE ACCESS (BYPASS[0])		OUTPUT
212	BUB DATA FAULT (BFLT[0])		INPUT/OUTPUT
213	NOT USED		NC
214*	BUB BUS REQUEST SLOT 3 (BUBRQ3[0])	*NOT USED*	INPUT *NC*
215	+5V (VCC)		POWER
216	PERIPHERAL PARITY CHECK (PPCHECK[0])		INPUT
217	NOT USED		NC
218	GROUND (GRD)		GROUND
219	BUB BUS REQUEST SLOT 1 (BUBRQ1[0])		INPUT
220	BUB BUS REQUEST SLOT 0 (BUBRQ0[0])		INPUT
221	MULTIPLEXED ADDRESS BIT 02 (MUXA02[1])		OUTPUT
222	MULTIPLEXED ADDRESS BIT 01 (MUXA01[1])		OUTPUT
223	MULTIPLEXED ADDRESS BIT 00 (MUXA00[1])		OUTPUT
224	BUB GRANTED SLOT 2 (BUBGT2[0])		OUTPUT
225	MULTIPLEXED ADDRESS BIT 05 (MUXA05[1])		OUTPUT
226	MULTIPLEXED ADDRESS BIT 04 (MUXA04[1])		OUTPUT
227	GROUND (GRD)		GROUND
228	MULTIPLEXED ADDRESS BIT 03 (MUXA03[1])		OUTPUT
229	MULTIPLEXED ADDRESS BIT 08 (MUXA08[1])		OUTPUT
230	+5V (VCC)		POWER
231	MULTIPLEXED ADDRESS BIT 07 (MUXA07[1])		OUTPUT
232	MULTIPLEXED ADDRESS BIT 06 (MUXA06[1])		OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)		
PIN	DESCRIPTION	FUNCTION
233	MULTIPLEXED ADDRESS BIT 10 (MUXA10[1])	OUTPUT
234	MULTIPLEXED ADDRESS BIT 09 (MUXA09[1])	OUTPUT
235	BUB GRANTED SLOT 3 (BUBGT3[0])	OUTPUT
236	BUB PERIPHERAL PARITY CHECK (BPCHECK[0])	INPUT/OUTPUT
237	BUB CONNECTOR CHIP SELECT 0 (BCCS0[0])	OUTPUT
238	BUB DATA SIZE BIT 0 (BDSIZE0[1])	INPUT/OUTPUT
239	GROUND (GRD)	GROUND
240	BUB SEQUENTIAL ACCESS (BSEQACC[0])	INPUT/OUTPUT
241	NOT USED	NC
242	NOT USED	NC
243	+5V (VCC)	POWER
244	NOT USED	NC
245	NOT USED	NC
246	GROUND (GRD)	GROUND
247	BUB DATA SIZE BIT 1 (BDSIZE1[1])	INPUT/OUTPUT
248	BUB READ/WRITE (BR1W[0])	INPUT/OUTPUT
249	BUB ADDRESS BIT 02 (BA02[1])	INPUT/OUTPUT
250	BUB ADDRESS BIT 01 (BA01[1])	INPUT/OUTPUT
251	NOT USED	NC
252	NOT USED	NC
253	BUB ADDRESS BIT 05 (BA05[1])	INPUT/OUTPUT
254	BUB ADDRESS BIT 04 (BA04[1])	INPUT/OUTPUT
255	GROUND (GRD)	GROUND
256	NOT USED	NC
257	BUB ADDRESS BIT 08 (BA08[1])	INPUT/OUTPUT
258	+5V (VCC)	POWER
259	BUB ADDRESS BIT 00 (BA00[1])	INPUT/OUTPUT
260	BUB ADDRESS BIT 03 (BA03[1])	INPUT/OUTPUT
261	BUB ADDRESS BIT 11 (BA11[1])	INPUT/OUTPUT
262	BUB ADDRESS BIT 10 (BA10[1])	INPUT/OUTPUT
263	GROUND (GRD)	GROUND
264	BUB ADDRESS BIT 06 (BA06[1])	INPUT/OUTPUT
265	BUB BUSY (BUSY[0])	INPUT/OUTPUT
266	GROUND (GRD)	GROUND
267	BUB CONNECTOR CHIP SELECT 1 (BCCS1[0])	OUTPUT
268	BUB ADDRESS BIT 09 (BA09[1])	INPUT/OUTPUT
269	BUB ADDRESS BIT 12 (BA12[1])	INPUT/OUTPUT
270	BUB ADDRESS BIT 15 (BA15[1])	INPUT/OUTPUT
271	BUB ADDRESS BIT 07 (BA07[1])	INPUT/OUTPUT
272	BUB ADDRESS BIT 13 (BA13[1])	INPUT/OUTPUT
273	BUB ADDRESS BIT 16 (BA16[1])	INPUT/OUTPUT
274	BUB ADDRESS BIT 18 (BA18[1])	INPUT/OUTPUT
275	+5V (VCC)	POWER
276	BUB ADDRESS BIT 17 (BA17[1])	INPUT/OUTPUT
277	BUB ADDRESS BIT 19 (BA19[1])	INPUT/OUTPUT
278	GROUND (GRD)	GROUND
279	BUB ADDRESS BIT 14 (BA14[1])	INPUT/OUTPUT
280	BUB ADDRESS BIT 20 (BA20[1])	INPUT/OUTPUT
281	BUB ADDRESS BIT 22 (BA22[1])	INPUT/OUTPUT
282	BUB ADDRESS BIT 24 (BA24[1])	INPUT/OUTPUT
283	BUB ADDRESS BIT 21 (BA21[1])	INPUT/OUTPUT
284	BUB ADDRESS BIT 23 (BA23[1])	INPUT/OUTPUT
285	BUB ADDRESS BIT 25 (BA25[1])	INPUT/OUTPUT
286	+5V (VCC)	POWER
287	NOT USED	NC
288	NOT USED	NC
289	NOT USED	NC
290	BUB DATA BIT 01 (BD01[1])	INPUT/OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)				
PIN	DESCRIPTION		FUNCTION	
291	BUB DATA BIT 00 (BD00[1])		INPUT/OUTPUT	
292	NOT USED		NC	
293	BUB DATA BIT 02 (BD02[1])		INPUT/OUTPUT	
294	BUB DATA BIT 04 (BD04[1])		INPUT/OUTPUT	
295	GROUND (GRD)		GROUND	
296	BUB DATA BIT 03 (BD03[1])		INPUT/OUTPUT	
297	BUB DATA BIT 05 (BD05[1])		INPUT/OUTPUT	
298	GROUND (GRD)		GROUND	
299	BUB DATA BIT 07 (BD07[1])		INPUT/OUTPUT	
300	BUB DATA BIT 06 (BD06[1])		INPUT/OUTPUT	
301	BUB DATA BIT 08 (BD08[1])		INPUT/OUTPUT	
302	BUB DATA BIT 10 (BD10[1])		INPUT/OUTPUT	
303	+5V (VCC)		POWER	
304	BUB DATA BIT 09 (BD09[1])		INPUT/OUTPUT	
305	BUB DATA BIT 11 (BD11[1])		INPUT/OUTPUT	
306	GROUND (GRD)		GROUND	
307	BUB DATA BIT 13 (BD13[1])		INPUT/OUTPUT	
308	BUB DATA BIT 12 (BD12[1])		INPUT/OUTPUT	
309	BUB DATA BIT 14 (BD14[1])		INPUT/OUTPUT	
310	BUB DATA BIT 17 (BD17[1])		INPUT/OUTPUT	
311	BUB DATA BIT 16 (BD16[1])		INPUT/OUTPUT	
312	BUB DATA BIT 15 (BD15[1])		INPUT/OUTPUT	
313	BUB DATA BIT 18 (BD18[1])		INPUT/OUTPUT	
314	BUB DATA BIT 20 (BD20[1])		INPUT/OUTPUT	
315	GROUND (GRD)		GROUND	
316	BUB DATA BIT 19 (BD19[1])		INPUT/OUTPUT	
317	BUB DATA BIT 21 (BD21[1])		INPUT/OUTPUT	
318	GROUND (GRD)		GROUND	
319	BUB DATA BIT 23 (BD23[1])		INPUT/OUTPUT	
320	BUB DATA BIT 22 (BD22[1])		INPUT/OUTPUT	
321	BUB DATA BIT 24 (BD24[1])		INPUT/OUTPUT	
322	BUB DATA BIT 26 (BD26[1])		INPUT/OUTPUT	
323	GROUND (GRD)		GROUND	
324	BUB DATA BIT 25 (BD25[1])		INPUT/OUTPUT	
325	BUB DATA BIT 27 (BD27[1])		INPUT/OUTPUT	
326	GROUND (GRD)		GROUND	
327	BUB DATA BIT 29 (BD29[1])		INPUT/OUTPUT	
328	BUB DATA BIT 28 (BD28[1])		INPUT/OUTPUT	
329	SYSTEM RESET (SYSRST[0])		OUTPUT	
330	REQUEST SYSTEM RESET (RQRST[0])		INPUT/OUTPUT	
331	NOT USED		NC	
332	THERMAL SHUTDOWN (THSDN[0])		INPUT	
333	BUB DATA BIT 30 (BD30[1])		INPUT/OUTPUT	
334	RECEIVED FAILURE (RFAIL[0])		INPUT	
335	+5V (VCC)		POWER	
336	BUB DATA BIT 31 (BD31[1])		INPUT/OUTPUT	
337	BUB CONNECTOR INHIBIT (BINHIB0[0])		OUTPUT	
338	BUB INTERRUPT LEVEL 10 (BINT010[0])		INPUT	
339	BUB INTERRUPT LEVEL 12 (BINT012[0])		INPUT	
340	BUB INTERRUPT LEVEL 14 (BINT014[0])		INPUT	
341*	UBUS DATA BIT 01 (CD01[1])	*NOT USED*	INPUT/OUTPUT	*NC*
342	GROUND (GRD)		GROUND	
343*	UBUS DATA BIT 00 (CD00[1])	*NOT USED*	INPUT/OUTPUT	*NC*
344*	UBUS SEQUENTIAL ACCESS (CSEQACC[0])	*NOT USED*	INPUT	*NC*
345*	UBUS DATA BIT 05 (CD05[1])	*NOT USED*	INPUT/OUTPUT	*NC*
346*	UBUS DATA BIT 04 (CD04[1])	*NOT USED*	INPUT/OUTPUT	*NC*
347*	UBUS DATA BIT 03 (CD03[1])	*NOT USED*	INPUT/OUTPUT	*NC*
348*	UBUS DATA BIT 02 (CD02[1])	*NOT USED*	INPUT/OUTPUT	*NC*

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)			
PIN	DESCRIPTION		FUNCTION
349*	UBUS DATA BIT 08 (CD08[1])	*NOT USED*	INPUT/OUTPUT *NC*
350*	UBUS DATA BIT 07 (CD07[1])	*NOT USED*	INPUT/OUTPUT *NC*
351	+5V (VCC)		POWER
352*	UBUS DATA BIT 06 (CD06[1])	*NOT USED*	INPUT/OUTPUT *NC*
353*	UBUS DATA BIT 11 (CD11[1])	*NOT USED*	INPUT/OUTPUT *NC*
354	GROUND (GRD)		GROUND
355*	UBUS DATA BIT 10 (CD10[1])	*NOT USED*	INPUT/OUTPUT *NC*
356*	UBUS DATA BIT 09 (CD09[1])	*NOT USED*	INPUT/OUTPUT *NC*
357*	UBUS DATA BIT 14 (CD14[1])	*NOT USED*	INPUT/OUTPUT *NC*
358*	UBUS DATA BIT 13 (CD13[1])	*NOT USED*	INPUT/OUTPUT *NC*
359	GROUND (GRD)		GROUND
360*	UBUS DATA BIT 12 (CD12[1])	*NOT USED*	INPUT/OUTPUT *NC*
361*	UBUS DATA BIT 18 (CD18[1])	*NOT USED*	INPUT/OUTPUT *NC*
362*	UBUS DATA BIT 17 (CD17[1])	*NOT USED*	INPUT/OUTPUT *NC*
363*	UBUS DATA BIT 16 (CD16[1])	*NOT USED*	INPUT/OUTPUT *NC*
364*	UBUS DATA BIT 15 (CD15[1])	*NOT USED*	INPUT/OUTPUT *NC*
365*	UBUS DATA BIT 21 (CD21[1])	*NOT USED*	INPUT/OUTPUT *NC*
366	+5V (VCC)		POWER
367*	UBUS DATA BIT 20 (CD20[1])	*NOT USED*	INPUT/OUTPUT *NC*
368*	UBUS DATA BIT 19 (CD19[1])	*NOT USED*	INPUT/OUTPUT *NC*
369*	UBUS DATA BIT 24 (CD24[1])	*NOT USED*	INPUT/OUTPUT *NC*
370*	UBUS DATA BIT 23 (CD23[1])	*NOT USED*	INPUT/OUTPUT *NC*
371	GROUND (GRD)		GROUND
372*	UBUS DATA BIT 22 (CD22[1])	*NOT USED*	INPUT/OUTPUT *NC*
373*	UBUS DATA BIT 27 (CD27[1])	*NOT USED*	INPUT/OUTPUT *NC*
374	GROUND (GRD)		GROUND
375*	UBUS DATA BIT 26 (CD26[1])	*NOT USED*	INPUT/OUTPUT *NC*
376*	UBUS DATA BIT 25 (CD25[1])	*NOT USED*	INPUT/OUTPUT *NC*
377*	UBUS DATA BIT 31 (CD31[1])	*NOT USED*	INPUT/OUTPUT *NC*
378*	UBUS DATA BIT 30 (CD30[1])	*NOT USED*	INPUT/OUTPUT *NC*
379*	UBUS DATA BIT 29 (CD29[1])	*NOT USED*	INPUT/OUTPUT *NC*
380*	UBUS DATA BIT 28 (CD28[1])	*NOT USED*	INPUT/OUTPUT *NC*
381*	UBUS ADDRESS BIT 02 (CA02[1])	*NOT USED*	INPUT/OUTPUT *NC*
382*	UBUS ADDRESS BIT 01 (CA01[1])	*NOT USED*	INPUT/OUTPUT *NC*
383	+5V (VCC)		POWER
384*	UBUS ADDRESS BIT 00 (CA00[1])	*NOT USED*	INPUT/OUTPUT *NC*
385*	UBUS ADDRESS BIT 05 (CA05[1])	*NOT USED*	INPUT/OUTPUT *NC*
386*	UBUS ADDRESS BIT 06 (CA06[1])	*NOT USED*	INPUT/OUTPUT *NC*
387*	UBUS ADDRESS BIT 04 (CA04[1])	*NOT USED*	INPUT/OUTPUT *NC*
388*	UBUS ADDRESS BIT 03 (CA03[1])	*NOT USED*	INPUT/OUTPUT *NC*
389*	UBUS ADDRESS BIT 08 (CA08[1])	*NOT USED*	INPUT/OUTPUT *NC*
390*	UBUS ADDRESS BIT 07 (CA07[1])	*NOT USED*	INPUT/OUTPUT *NC*
391	GROUND (GRD)		GROUND
392*	UBUS ADDRESS BIT 09 (CA09[1])	*NOT USED*	INPUT/OUTPUT *NC*
393*	UBUS ADDRESS BIT 11 (CA11[1])	*NOT USED*	INPUT/OUTPUT *NC*
394	+5V (VCC)		POWER
395*	UBUS ADDRESS BIT 10 (CA10[1])	*NOT USED*	INPUT/OUTPUT *NC*
396*	UBUS ADDRESS BIT 12 (CA12[1])	*NOT USED*	INPUT/OUTPUT *NC*
397*	UBUS ADDRESS BIT 15 (CA15[1])	*NOT USED*	INPUT/OUTPUT *NC*
398*	UBUS ADDRESS BIT 14 (CA14[1])	*NOT USED*	INPUT/OUTPUT *NC*
399*	UBUS ADDRESS BIT 13 (CA13[1])	*NOT USED*	INPUT/OUTPUT *NC*
400*	UBUS ADDRESS BIT 16 (CA16[1])	*NOT USED*	INPUT/OUTPUT *NC*
401*	UBUS ADDRESS BIT 18 (CA18[1])	*NOT USED*	INPUT/OUTPUT *NC*
402*	UBUS ADDRESS BIT 17 (CA17[1])	*NOT USED*	INPUT/OUTPUT *NC*
403	GROUND (GRD)		GROUND
404*	UBUS ADDRESS BIT 19 (CA19[1])	*NOT USED*	INPUT/OUTPUT *NC*
405*	UBUS ADDRESS BIT 21 (CA21[1])	*NOT USED*	INPUT/OUTPUT *NC*
406	GROUND (GRD)		GROUND

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)				
PIN	DESCRIPTION		FUNCTION	
407*	UBUS ADDRESS BIT 20 (CA20[1])	*NOT USED*	INPUT/OUTPUT	*NC*
408*	UBUS ADDRESS BIT 22 (CA22[1])	*NOT USED*	INPUT/OUTPUT	*NC*
409*	UBUS ADDRESS BIT 24 (CA24[1])	*NOT USED*	INPUT/OUTPUT	*NC*
410*	UBUS ADDRESS BIT 23 (CA23[1])	*NOT USED*	INPUT/OUTPUT	*NC*
411	+5V (VCC)		POWER	
412*	UBUS ADDRESS BIT 25 (CA25[1])	*NOT USED*	INPUT/OUTPUT	*NC*
413*	UBUS ADDRESS BIT 27 (CA27[1])	*NOT USED*	INPUT/OUTPUT	*NC*
414*	GROUND (GRD)	*PBUS INHIBIT(UINHIB[0])*	GROUND	*OUTPUT*
415*	UBUS ADDRESS BIT 26 (CA26[1])	*NOT USED*	INPUT/OUTPUT	*NC*
416*	UBUS ADDRESS BIT 28 (CA28[1])	*NOT USED*	INPUT/OUTPUT	*NC*
417*	UBUS ADDRESS BIT 31 (CA31[1])	*NOT USED*	INPUT/OUTPUT	*NC*
418*	UBUS ADDRESS BIT 30 (CA30[1])	*NOT USED*	INPUT/OUTPUT	*NC*
419*	UBUS ADDRESS BIT 29 (CA29[1])	*NOT USED*	INPUT/OUTPUT	*NC*
420*	CLOCK 23 (CLK23[1])	*NOT USED*	OUTPUT	*NC*
421	HOLD REMOTE POWERON (PWRON[1])		OUTPUT	
422	REMOTE POWER DOWN REQUEST (PDWNRQ[0])		INPUT	
423	GROUND (GRD)		GROUND	
424*	CLOCK 34 (CLK34[1])	*NOT USED*	OUTPUT	*NC*
425*	UBUS GRANTED (BUSGT[0])	*CPU LATCH ADDRESS (CPULTCH[1])*	OUTPUT	*OUTPUT*
426	SANITY TIMER TIMEOUT (SANTO[0])		INPUT/OUTPUT	
427	OPERATIONAL INTERRUPT LEVEL 15 (OPINT15[0])		INPUT	
428*	VIRTUAL CACHE HIT (VCHIT[0])	*SLOT 3 VIRTUAL ADDRESS STROBE (C3VAS[0])*	INPUT	*INPUT/OUTPUT*
429*	UBUS EXECUTION MODE 1 (XMD1[1])	*NOT USED*	OUTPUT	*NC*
430	+5V (VCC)		POWER	
431*	UBUS BUS REQUEST (BUSRQ[0])	*SLOT 2 VIRTUAL ADDRESS STROBE (C2VAS[0])*	INPUT	*INPUT*
432*	UBUS COPROCESSOR DONE (DONE[0])	*SLOT 1 VIRTUAL ADDRESS STROBE (C1VAS[0])*	INPUT	*INPUT*
433*	UBUS VIRTUAL ADDRESS (BY CPU) (VAD[0])	*PBUS INTERLOCK (UINTLK[0])*	OUTPUT	*INPUT*
434*	UBUS ACCESS STATUS BIT 3 (SAS3[1])	*PBUS CARD SELECT SLOT 3 (UPCS3[0]*	OUTPUT	*OUTPUT*
435	GROUND (GRD)		GROUND	
436*	UBUS ACCESS STATUS BIT 2 (SAS2[1])	*PBUS CARD SELECT SLOT 2 (UPCS2[0])*	OUTPUT	*OUTPUT*
437*	UBUS DATA ACKNOWLEDGE (DTACK[0])	*PBUS SLOT 3 MEMORY REQUEST (CPU3MEM[0]*	INPUT	*INPUT*
438	GROUND (GRD)		GROUND	
439*	UBUS ABORT ACTIVATED (ABORT[0])	*NOT USED*	OUTPUT	*NC*

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)				
PIN	**DESCRIPTION**		**FUNCTION**	
440*	UBUS CACHE ABLE (CABLE[0])	*PBUS DATA ACKNOWLEDGE (UDTACK[0])*	INPUT/OUTPUT	*OUTPUT*
441*	UBUS EARLY PHYSICAL ADDRESS STROBE (EPAS[0])	*PBUS PHYSICAL ADDRESS STROBE (UPAS[0])*	OUTPUT	*INPUT*
442*	UBUS VIRTUAL ADDRESS STROBE (VAS[0])	*NOT USED*	OUTPUT	*NC*
443*	UBUS ACCESS STATUS BIT 1 (SAS1[1])	*PBUS CARD SELECT SLOT 1 (UPCS1[0])*	OUTPUT	*OUTPUT*
444*	UBUS ACCESS STATUS BIT 0 (SAS0[1])	*PBUS SLOT 3 OUTPUT ENABLE (C3ALOE[0])*	OUTPUT	*OUTPUT*
445*	UBUS DATA SIZE BIT 0 (CDSIZE0[1])	*PBUS DATA SIZE BIT 0 (UDSIZE0[1])*	OUTPUT	*INPUT*
446*	UBUS SYNCHRONOUS READY (SRDY[0])	*PBUS SLOT 2 MEMORY REQUEST (CPU2MEM[0])*	INPUT	*INPUT*
447	+5V (VCC)		POWER	
448*	UBUS CYCLE INITIATE (CYCLEI[0])	*PBUS SLOT 2 OUTPUT ENABLE (C2ALOE[0])*	OUTPUT	*OUTPUT*
449*	BUB CONNECTOR CHIP SELECT 3 (BCCS3[0])	*PBUS SLOT 1 OUTPUT ENABLE (C1ALOE[0])*	OUTPUT	*OUTPUT*
450	GROUND (GRD)		GROUND	
451*	UBUS DATA READY (DRDY[0])	*NOT USED*	OUTPUT	*NC*
452*	RECEIVED FAILURE (RFAIL[0])	*PBUS SLOT 1 MEMORY REQUEST (CPU1MEM[0])*	INPUT	*INPUT*
453	UBUS CHIP SELECT (CS1[0])	*PULLED UP*	OUTPUT	*OUTPUT*
454*	UBUS FAULT (FLT[0])	*PBUS FAULT (UFLT[0])*	INPUT	*OUTPUT*
455	ABORT PUSH BUTTON (ABUTTN[0])		INPUT	
456*	UBUS DATA SIZE BIT 1 (CDSIZE1[1])	*PBUS DATA SIZE BIT 1 (UDSIZE1[1])*	OUTPUT	*INPUT*
457*	UBUS DATA SHADOW (DSHAD[0])	*NOT USED*	OUTPUT	*NC*
458	GROUND (GRD)		GROUND	
459*	UBUS READ/WRITE (CR1W[0])	*PBUS READ/WRITE (UR1W[0])*	OUTPUT	*INPUT*
460*	UBUS DATA STROBE (DS[0])	*NOT USED*	OUTPUT	*NC*
461	POWER LED (GLED[0])		OUTPUT	
462	+5V (VCC)		POWER	
463	DIAGNOSTIC LED (ERLED[0])		OUTPUT	
464	+3.6V (VBAT)		INPUT	

* CM518C System Board signal description shown in *italics*.

LEGEND:

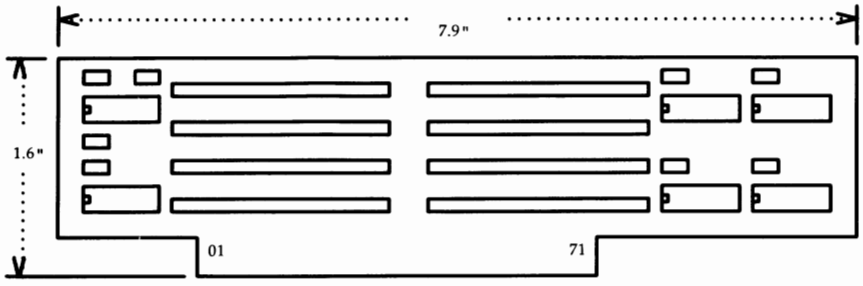
NC No Connection

CM191A/B/C/D AND CM192B MEMORY CARD INTERCONNECTIONS

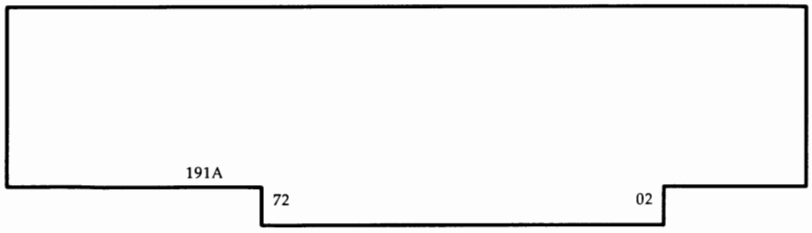
All memory card interconnections are provided by a 72-pin card edge connector. The following memory cards are used in the 3B2 computer.

CM191A	Figure B-6 shows the layout of the 0.25-Megabyte Memory Card, CM191A. The card is approximately 7.9 inches wide and 1.6 inches high.
CM191B	Figure B-7 shows the layout of the 1-Megabyte Memory Card, CM191B. The card is approximately 7.9 inches wide and 1.6 inches high.
CM191C	Figure B-8 shows the layout of the 1-Megabyte, Surface Mounted, Memory Card, CM191C. The card is approximately 7.7 inches wide and 1.7 inches high.
CM191D	Figure B-9 shows the layout of the 2-Megabyte, Surface Mounted, Memory Card, CM191D. The card is approximately 7.9 inches wide and 1.6 inches high.
CM192B	Figure B-10 shows the layout of the 2-Megabyte, Surface Mounted, Memory Card, CM192B. The card is approximately 7.9 inches wide and 3.6 inches high.

Refer to these figures for card connector location information. Card pin and signal information is provided in tables following the figures. The figures are printed front and back with a blank unit so that the figures can be used in conjunction with the tables.

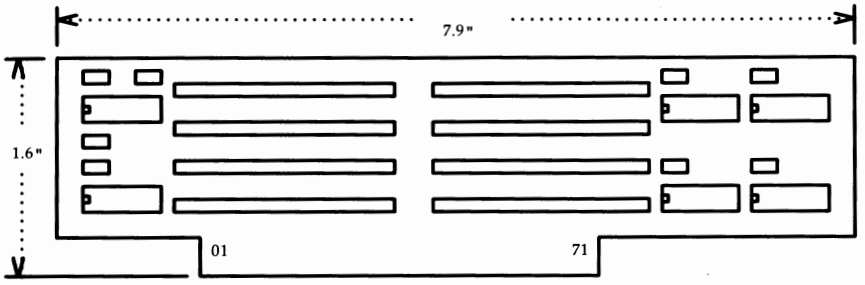


A. Front View

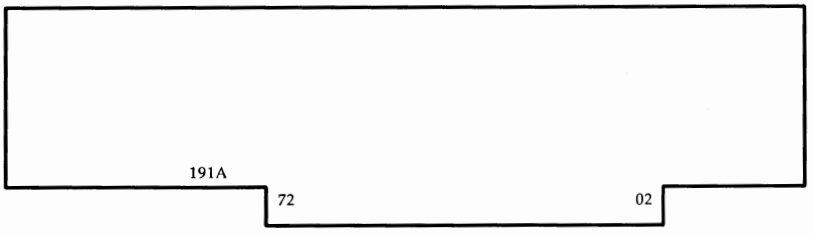


B. Rear View

Figure B-6: CM191A 0.25-Megabyte Memory Card Layout

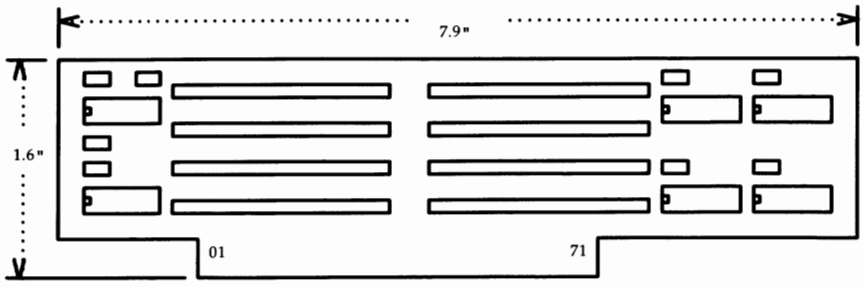


A. Front View

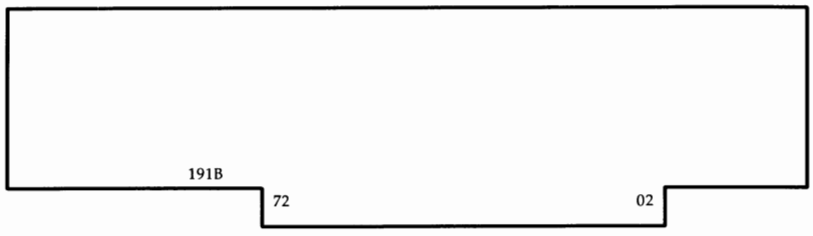


B. Rear View

Figure B-6: CM191A 0.25-Megabyte Memory Card Layout

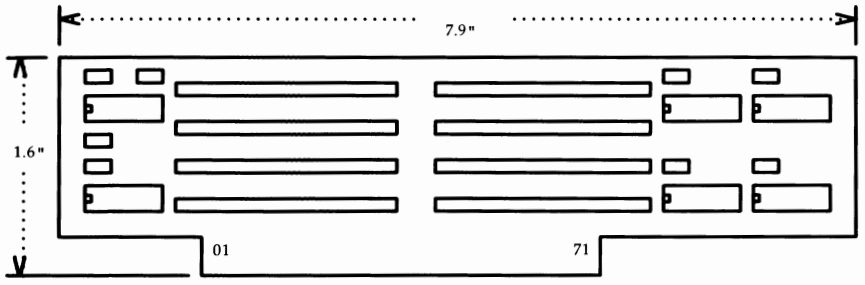


A. Front View

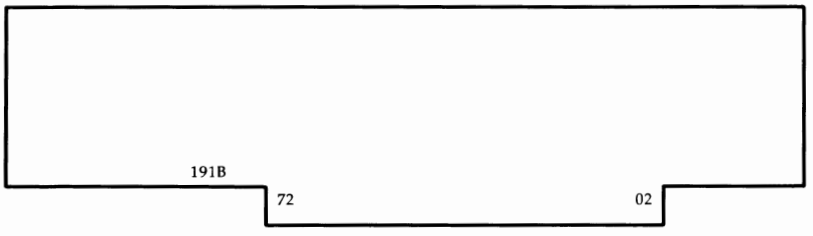


B. Rear View

Figure B-7: CM191B 1-Megabyte Memory Card Layout

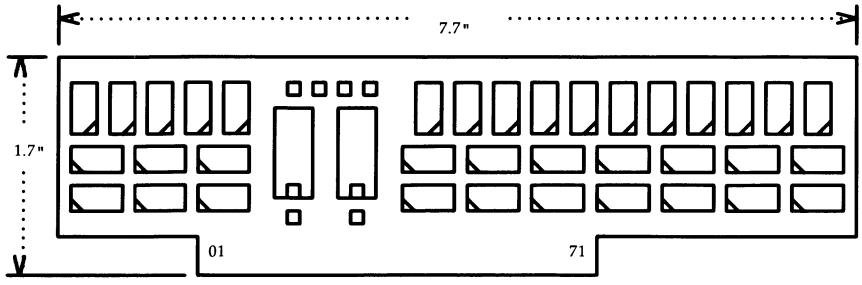


A. Front View

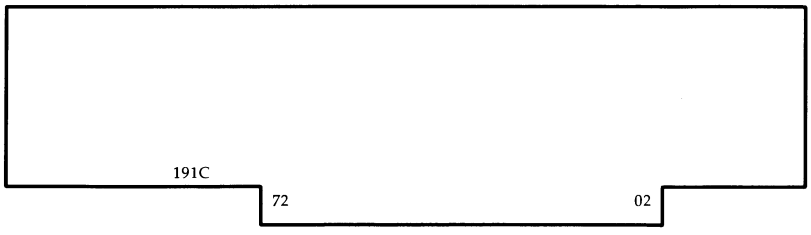


B. Rear View

Figure B-7: CM191B 1-Megabyte Memory Card Layout

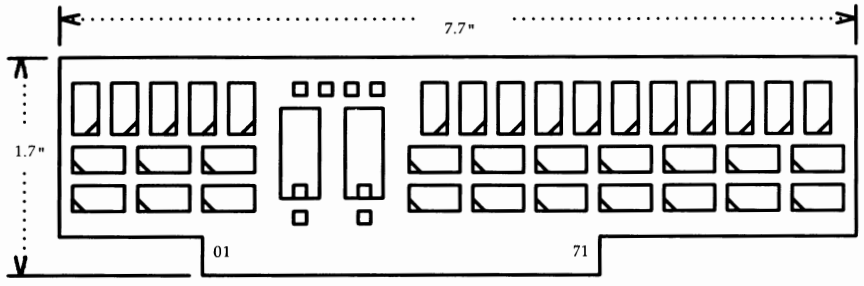


A. Front View

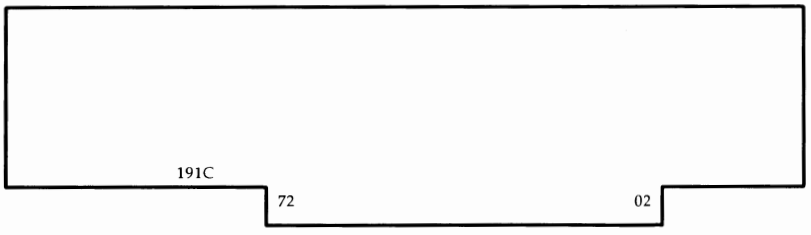


B. Rear View

Figure B-8: CM191C 1-Megabyte, Surface Mounted, Memory Card Layout

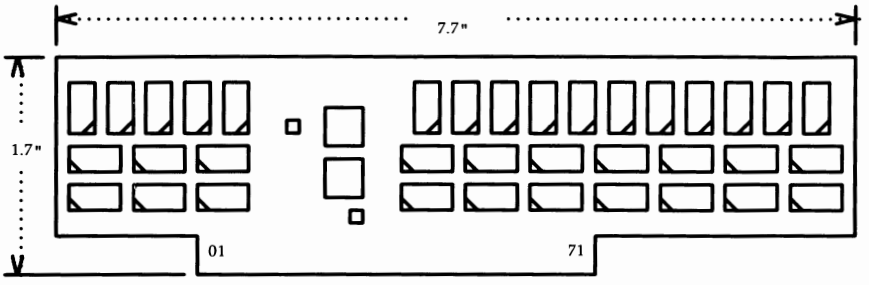


A. Front View

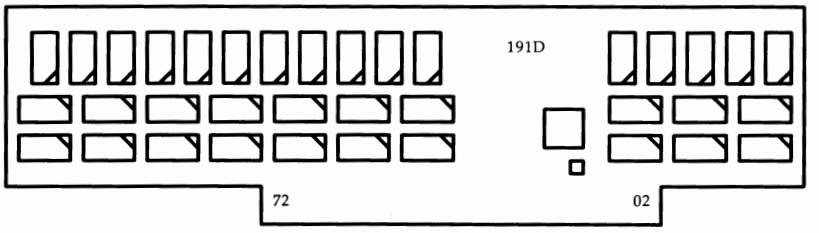


B. Rear View

Figure B-8: CM191C 1-Megabyte, Surface Mounted, Memory Card Layout

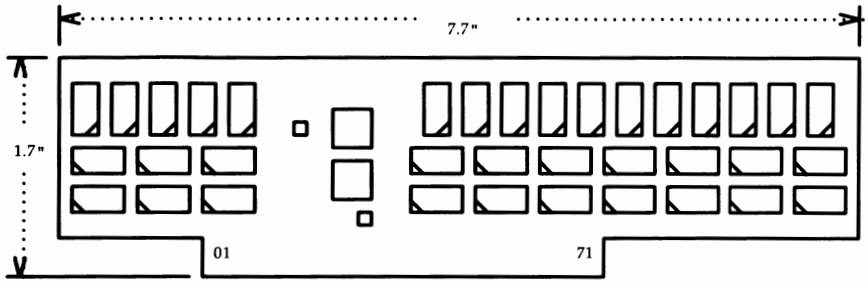


A. Front View

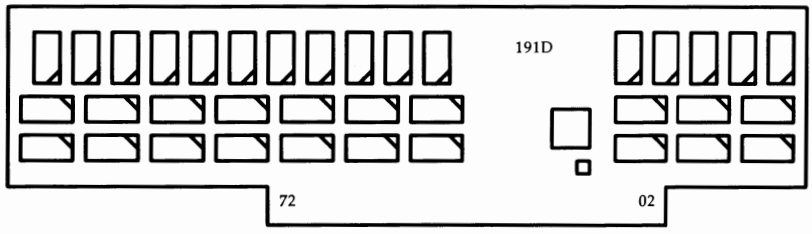


B. Rear View

Figure B-9: CM191D 2-Megabyte, Surface Mounted, Memory Card Layout

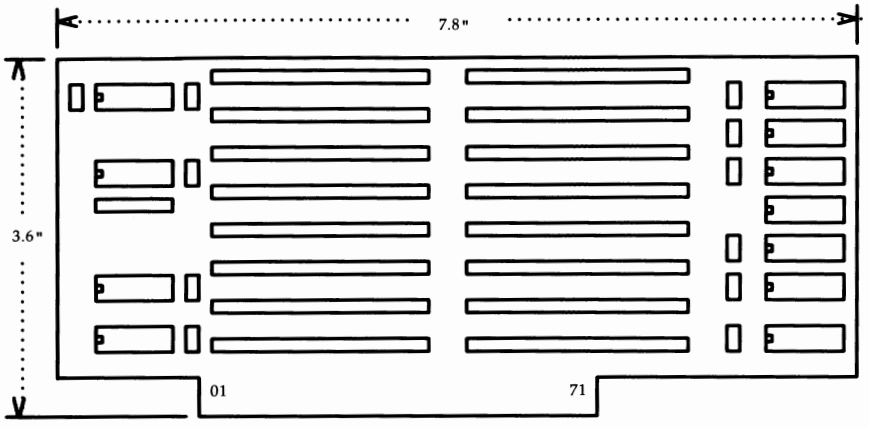


A. Front View

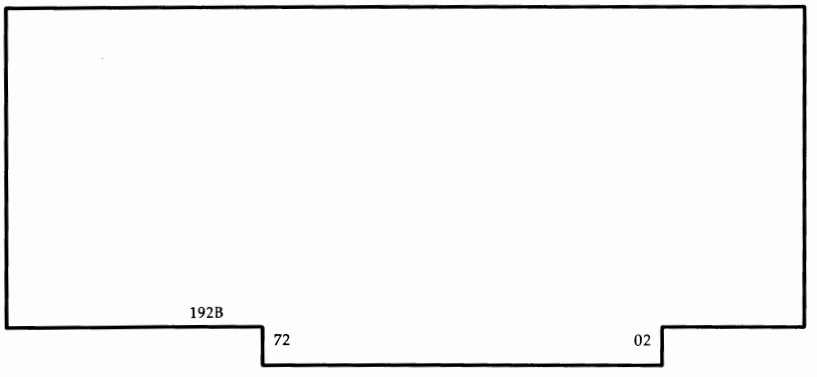


B. Rear View

Figure B-9: CM191D 2-Megabyte, Surface Mounted, Memory Card Layout

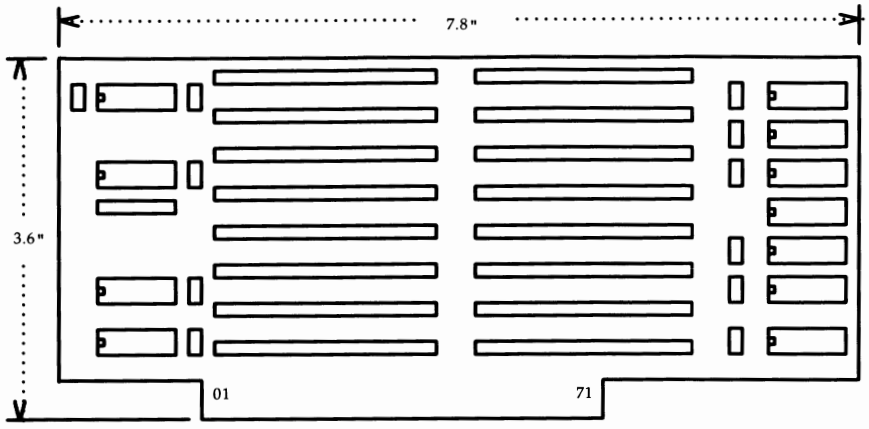


A. Front View

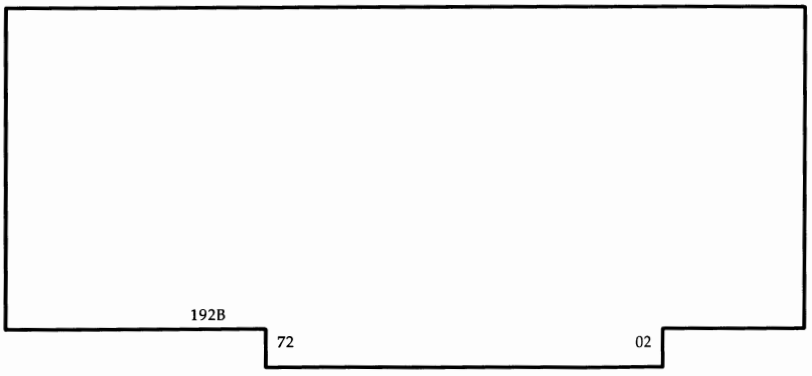


B. Rear View

Figure B-10: CM192B 2-Megabyte, Surface Mounted, Memory Card Layout



A. Front View



B. Rear View

Figure B-10: CM192B 2-Megabyte, Surface Mounted, Memory Card Layout

72-PIN CM191 AND CM192 MEMORY CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	GROUND (GRD)	GROUND
002	+5V (VCC)	POWER
003	MULTIPLEXED ADDRESS BIT 7 (MUXA7[1])	INPUT
004	MULTIPLEXED ADDRESS BIT 0 (MUXA0[1])	INPUT
005	MULTIPLEXED ADDRESS BIT 6 (MUXA6[1])	INPUT
006	MULTIPLEXED ADDRESS BIT 1 (MUXA1[1])	INPUT
007	MULTIPLEXED ADDRESS BIT 5 (MUXA5[1])	INPUT
008	GROUND (GRD)	GROUND
009	MULTIPLEXED ADDRESS BIT 4 (MUXA4[1])	INPUT
010	MULTIPLEXED ADDRESS BIT 2 (MUXA2[1])	INPUT
011	NOT USED for CM191A	NC
	MULTIPLEXED ADDRESS BIT 8 (MUXA8[1]) for CM191B/C/D and CM192A/B	INPUT
012	MULTIPLEXED ADDRESS BIT 3 (MUXA3[1])	INPUT
013	GROUND (GRD)	GROUND
014	NOT USED for CM191A	NC
	MULTIPLEXED ADDRESS BIT 9 (MUXA9[1]) for CM191B/C/D and CM192A/B	INPUT
015	WRITE ENABLE (WE[0])	INPUT
016	ROW ADDRESS STROBE (RAS[0])	INPUT
017	BANK ENABLE 0 (BANKEN0[0])	INPUT
018	NOT USED for CM191A/B/C	NC
	BANK ENABLE 1 (BANKEN1[0]) for CM191D and CM192A/B	INPUT
019	ONEBANK[0] for CM191A/B/C	GROUND
	ONEBANK[0] for CM191D and CM192A/B	VCC
020	COLUMN ADDRESS STROBE 2 (CAS2[0])	INPUT
021	COLUMN ADDRESS STROBE 0 (CAS0[0])	INPUT
022	COLUMN ADDRESS STROBE 3 (CAS3[0])	INPUT
023	GROUND (GRD)	GROUND
024	SIZE64K[0] for CM191A/B/C	GROUND
	SIZE64K[0] for CM191D and CM192A/B	VCC
025	COLUMN ADDRESS STROBE 1 (CAS1[0])	INPUT
026	MEMORY DATA BIT 31 (MD31[1])	INPUT/OUTPUT
027	MEMORY DATA BIT 30 (MD30[1])	INPUT/OUTPUT
028	GROUND (GRD)	GROUND
029	MEMORY DATA BIT 28 (MD28[1])	INPUT/OUTPUT
030	MEMORY DATA BIT 29 (MD29[1])	INPUT/OUTPUT
031	MEMORY DATA BIT 26 (MD26[1])	INPUT/OUTPUT
032	MEMORY DATA BIT 27 (MD27[1])	INPUT/OUTPUT
033	GROUND (GRD)	GROUND

72-PIN CM191 AND CM192 MEMORY CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
034	MEMORY DATA BIT 25 (MD25[1])	INPUT/OUTPUT
035	MEMORY DATA BIT 24 (MD24[1])	INPUT/OUTPUT
036	MEMORY DATA BIT 23 (MD23[1])	INPUT/OUTPUT
037	MEMORY DATA BIT 22 (MD22[1])	INPUT/OUTPUT
038	GROUND (GRD)	GROUND
039	MEMORY DATA BIT 20 (MD20[1])	INPUT/OUTPUT
040	MEMORY DATA BIT 21 (MD21[1])	INPUT/OUTPUT
041	MEMORY DATA BIT 18 (MD18[1])	INPUT/OUTPUT
042	MEMORY DATA BIT 19 (MD19[1])	INPUT/OUTPUT
043	GROUND (GRD)	GROUND
044	MEMORY DATA BIT 17 (MD17[1])	INPUT/OUTPUT
045	MEMORY DATA BIT 16 (MD16[1])	INPUT/OUTPUT
046	MEMORY DATA BIT 15 (MD15[1])	INPUT/OUTPUT
047	MEMORY DATA BIT 14 (MD14[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	MEMORY DATA BIT 12 (MD12[1])	INPUT/OUTPUT
050	MEMORY DATA BIT 13 (MD13[1])	INPUT/OUTPUT
051	MEMORY DATA BIT 10 (MD10[1])	INPUT/OUTPUT
052	MEMORY DATA BIT 11 (MD11[1])	INPUT/OUTPUT
053	GROUND (GRD)	GROUND
054	MEMORY DATA BIT 09 (MD09[1])	INPUT/OUTPUT
055	MEMORY DATA BIT 08 (MD08[1])	INPUT/OUTPUT
056	MEMORY DATA BIT 07 (MD07[1])	INPUT/OUTPUT
057	MEMORY DATA BIT 06 (MD06[1])	INPUT/OUTPUT
058	MEMORY DATA BIT 05 (MD05[1])	INPUT/OUTPUT
059	MEMORY DATA BIT 04 (MD04[1])	INPUT/OUTPUT
060	GROUND (GRD)	GROUND
061	MEMORY DATA BIT 02 (MD02[1])	INPUT/OUTPUT
062	MEMORY DATA BIT 03 (MD03[1])	INPUT/OUTPUT
063	GROUND (GRD)	GROUND
064	MEMORY DATA BIT 01 (MD01[1]	INPUT/OUTPUT
065	MEMORY DATA BIT 00 (MD00[1]	INPUT/OUTPUT
066	MEMORY CARD EQUIPPED (MCEQUIP[0])	GROUND
067	MEMORY PARITY ADDRESS REGISTER BIT 0 (MPAR0[1])	INPUT/OUTPUT
068	MEMORY PARITY ADDRESS REGISTER BIT 0 (MPAR2[1])	INPUT/OUTPUT
069	MEMORY PARITY ADDRESS REGISTER BIT 0 (MPAR1[1])	INPUT/OUTPUT
070	MEMORY PARITY ADDRESS REGISTER BIT 0 (MPAR3[1])	INPUT/OUTPUT
071	GROUND (GRD)	GROUND
072	+5V (VCC)	POWER

LEGEND:

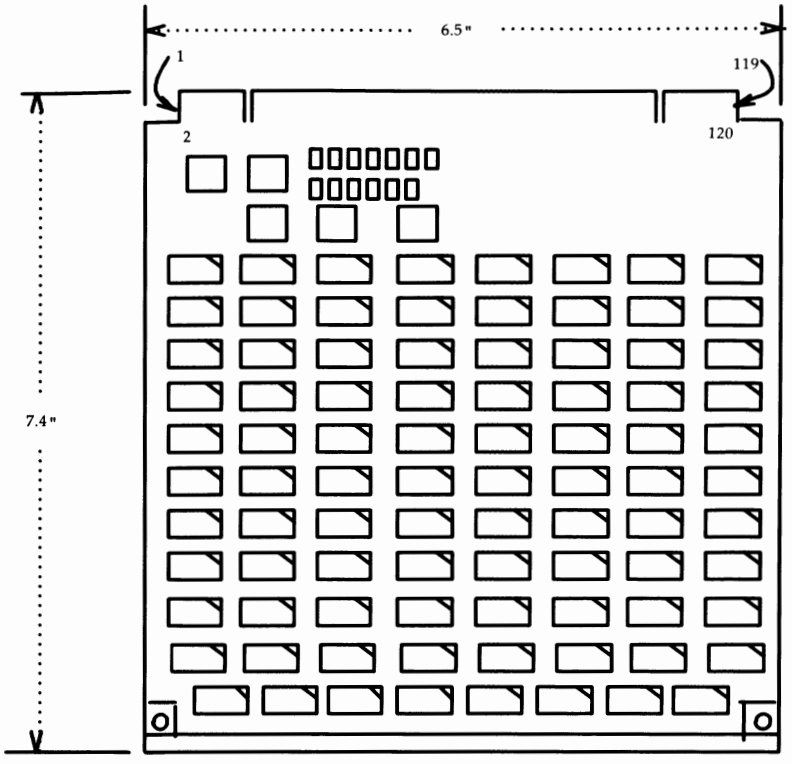
NC No Connection

CM523A/AA/B/D MEMORY CARD INTERCONNECTIONS

All CM523 series memory cards are surface mount technology. The interconnections are provided by a 120-pin card edge connector. The following memory cards are used in the Version 3 3B2 computer.

CM523A	Figure B-11 shows the layout of the 4-Megabyte Memory Card, CM523A. The card is approximately 6.5 inches wide and 7.4 inches deep.
CM523AA	Figure B-12 shows the layout of the 4-Megabyte Memory Card, CM523AA. The card is approximately 6.5 inches wide and 7.4 inches deep.
CM523B	Figure B-13 shows the layout of the 2-Megabyte Memory Card, CM523B. The card is approximately 6.5 inches wide and 7.4 inches deep.
CM523D	Figure B-14 shows the layout of the 16-Megabyte Memory Card, CM523D. The card is approximately 6.5 inches wide and 7.4 inches deep.

Refer to these figures for card connector location information. Card pin and signal information is provided in tables following the figures. The figures are printed front and back with a blank unit so that the figures can be used in conjunction with the tables.



Conventional Component Side (Top)
(Bottom Side also has Memory Chips)

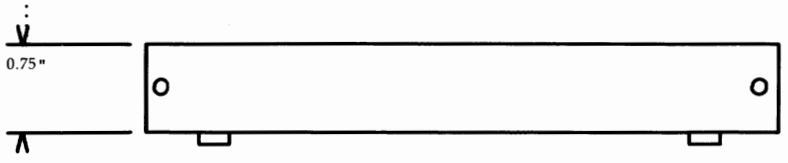
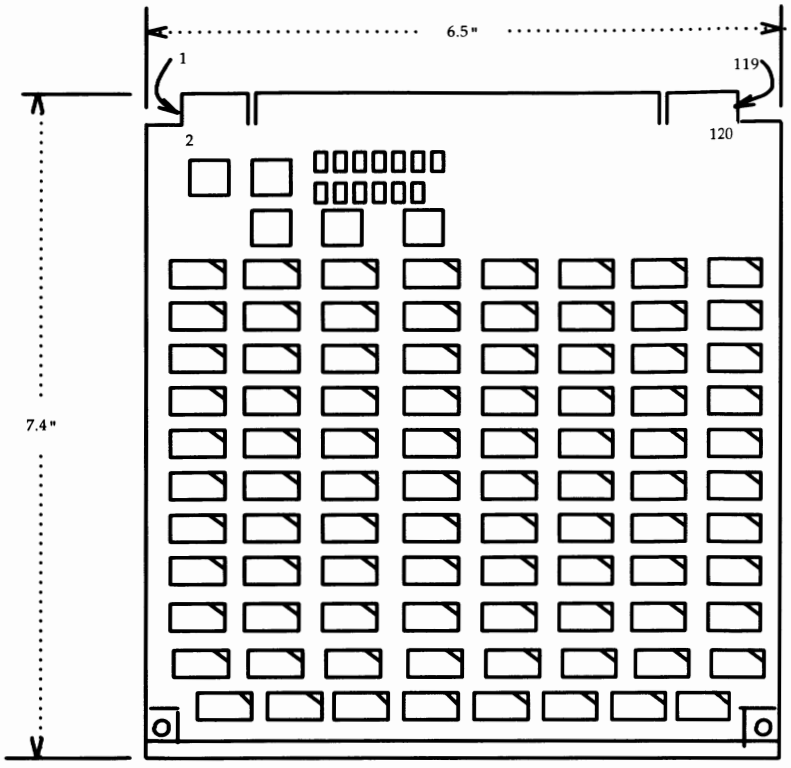


Figure B-11: CM523A 4-Megabyte Memory Card Layout



Conventional Component Side (Top)
(Bottom Side also has Memory Chips)

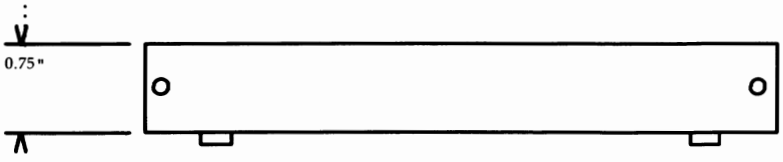
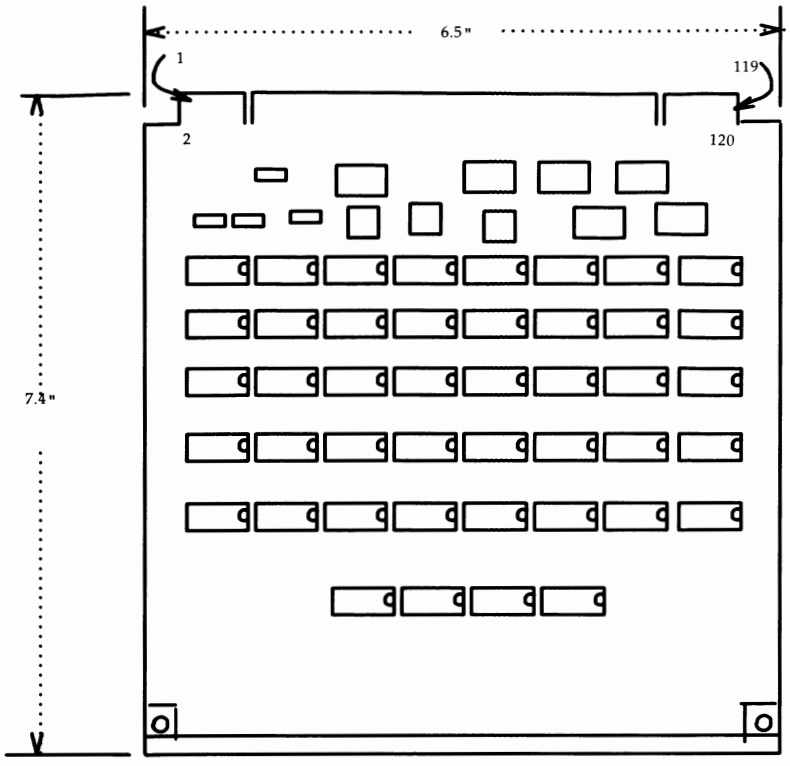


Figure B-11: CM523A 4-Megabyte Memory Card Layout



Conventional Component Side

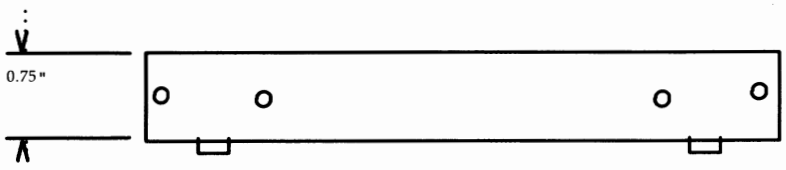
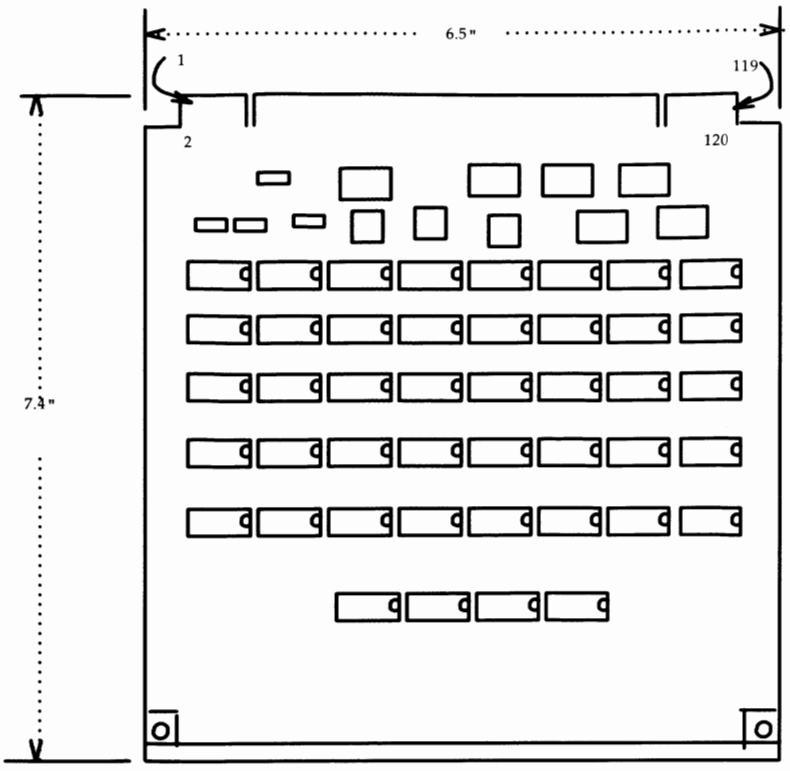


Figure B-12: CM523AA 4-Megabyte Memory Card Layout



Conventional Component Side

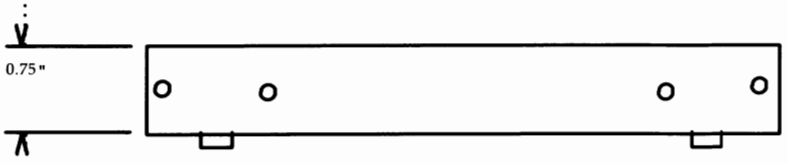
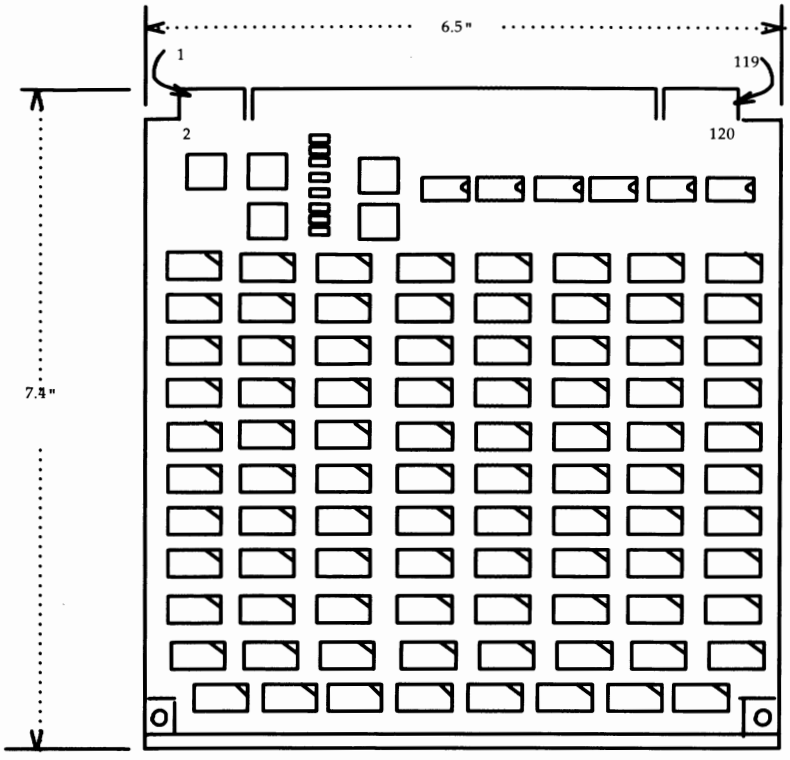


Figure B-12: CM523AA 4-Megabyte Memory Card Layout



Conventional Component Side

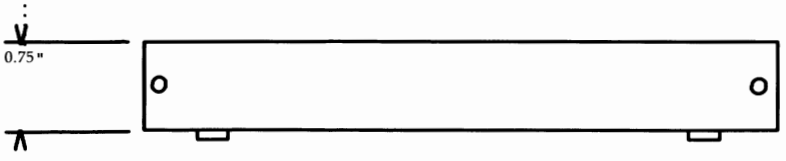
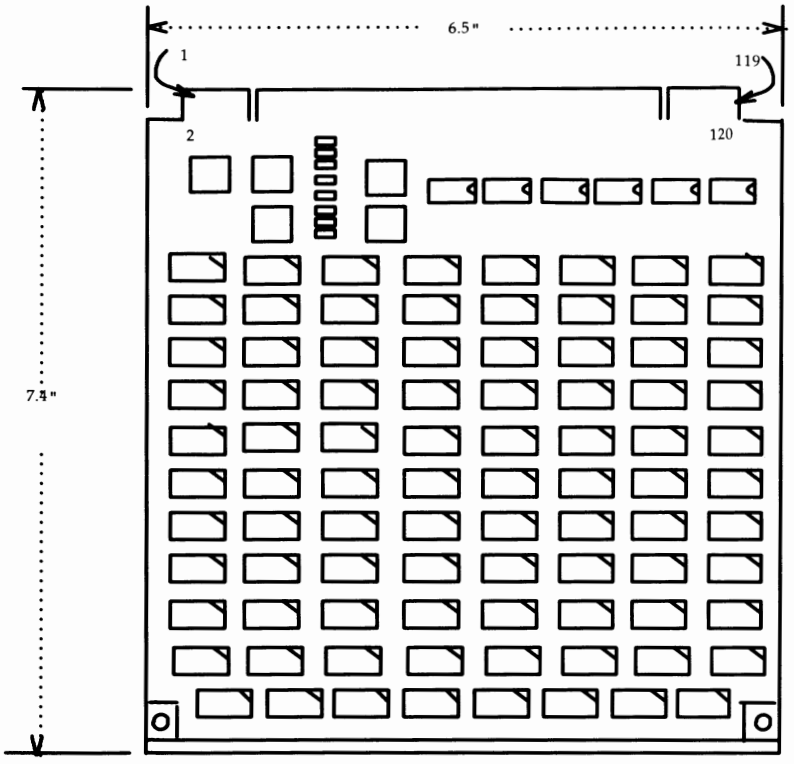


Figure B-13: CM523B 2-Megabyte Memory Card Layout



Conventional Component Side

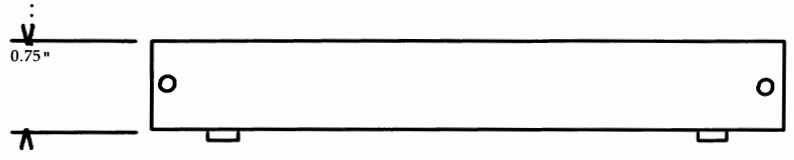
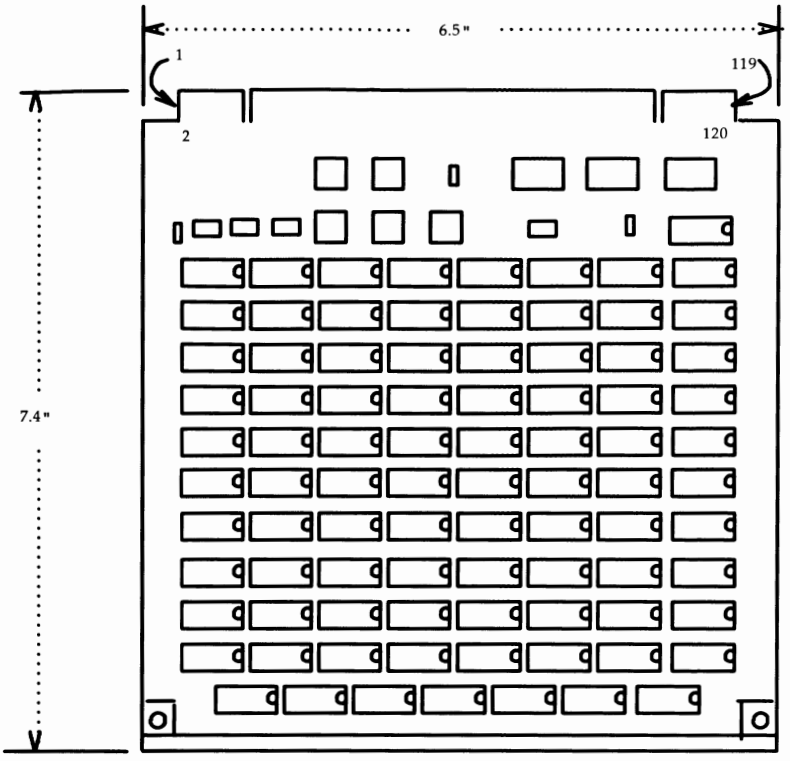


Figure B-13: CM523B 2-Megabyte Memory Card Layout



Conventional Component Side (Top)
(Bottom Side also has Memory Chips)

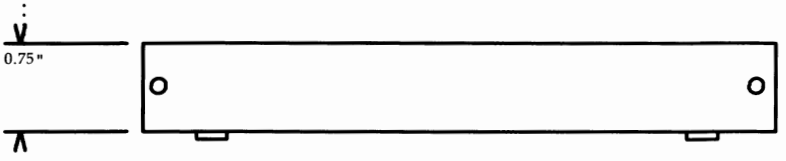
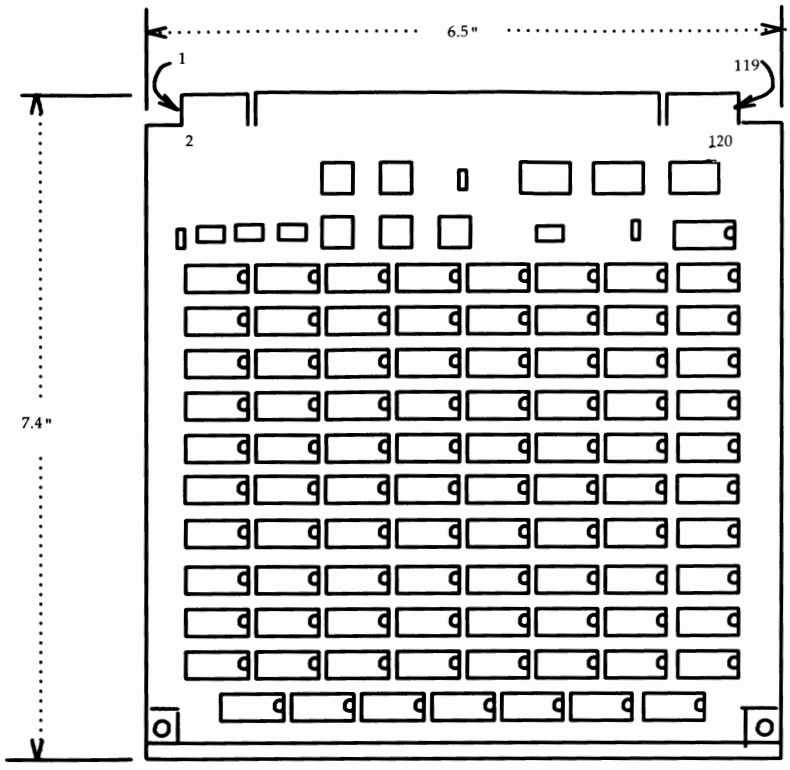


Figure B-14: CM523D 16-Megabyte Memory Card Layout



Conventional Component Side (Top)
(Bottom Side also has Memory Chips)

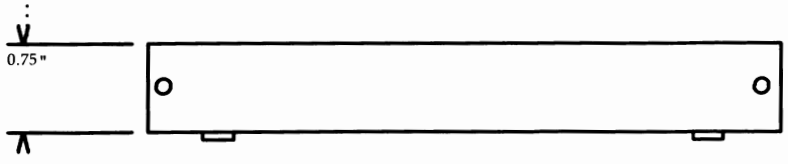


Figure B-14: CM523D 16-Megabyte Memory Card Layout

120-PIN CM523 MEMORY CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	GROUND (GRD)	GROUND
002	+5V (VCC)	POWER
003	NOT USED	NC
004	NOT USED	NC
005	NOT USED	NC
006	NOT USED	NC
007	GROUND (GRD)	GROUND
008	GROUND (GRD)	GROUND
009	ROW ADDRESS STROBE (RAS[0])	INPUT
010	WRITE ENABLE (WE[0])	INPUT
011	GROUND (GRD)	GROUND
012	GROUND (GRD)	GROUND
013	MEMORY CYCLE STATUS G[0]	INPUT
014	BANK ENABLE 1 (BANKEN1[0])	INPUT
015	BANK ENABLE 2 (BANKEN2[0])	INPUT
016	BANK ENABLE 0 (BANKEN0[0])	INPUT
017	GROUND (GRD)	GROUND
018	GROUND (GRD)	GROUND
019	COLUMN ADDRESS STROBE 1 (CAS1[0])	INPUT
020	COLUMN ADDRESS STROBE 3 (CAS3[0])	INPUT
021	COLUMN ADDRESS STROBE 0 (CAS0[0])	INPUT
022	COLUMN ADDRESS STROBE 2 (CAS2[0])	INPUT
023	+5V (VCC)	POWER
024	+5V (VCC)	POWER
025	SIZE BIT 0 (SIZE0[0])	INPUT/OUTPUT
026	NOT USED	NC
027	SIZE BIT 1 (SIZE1[0])	INPUT/OUTPUT
028	SLOT EQUIPPED (ECCEQP[0])	OUTPUT
029	LARGER SIZED MEMORY BOARD (BIGMEM[0])	OUTPUT
030	NOT USED	NC
031	GROUND (GRD)	GROUND
032	GROUND (GRD)	GROUND
033	MULTIPLEXED ADDRESS BIT 00 (MUXA00[1])	INPUT
034	MULTIPLEXED ADDRESS BIT 03 (MUXA03[1])	INPUT
035	GROUND (GRD)	GROUND
036	GROUND (GRD)	GROUND
037	MULTIPLEXED ADDRESS BIT 01 (MUXA01[1])	INPUT
038	MULTIPLEXED ADDRESS BIT 02 (MUXA02[1])	INPUT
039	GROUND (GRD)	GROUND
040	GROUND (GRD)	GROUND
041	MULTIPLEXED ADDRESS BIT 04 (MUXA04[1])	INPUT
042	MULTIPLEXED ADDRESS BIT 07 (MUXA07[1])	INPUT
043	+5V (VCC)	POWER
044	+5V (VCC)	POWER
045	MULTIPLEXED ADDRESS BIT 05 (MUXA05[1])	INPUT
046	MULTIPLEXED ADDRESS BIT 06 (MUXA06[1])	INPUT
047	GROUND (GRD)	GROUND
048	GROUND (GRD)	GROUND
049	MULTIPLEXED ADDRESS BIT 08 (MUXA08[1])	INPUT
050	MULTIPLEXED ADDRESS BIT 11 (MUXA11[1]) (IF USED)	INPUT
051	GROUND (GRD)	GROUND
052	GROUND (GRD)	GROUND
053	MULTIPLEXED ADDRESS BIT 09 (MUXA09[1]) (IF USED)	INPUT
054	MULTIPLEXED ADDRESS BIT 10 (MUXA10[1]) (IF USED)	INPUT
055	GROUND (GRD)	GROUND
056	+5V (VCC)	POWER
057	MULTIPLEXED ADDRESS BIT 12 (MUXA12[1]) (IF USED)	INPUT
058	NOT USED	NC
059	GROUND (GRD)	GROUND
060	GROUND (GRD)	GROUND

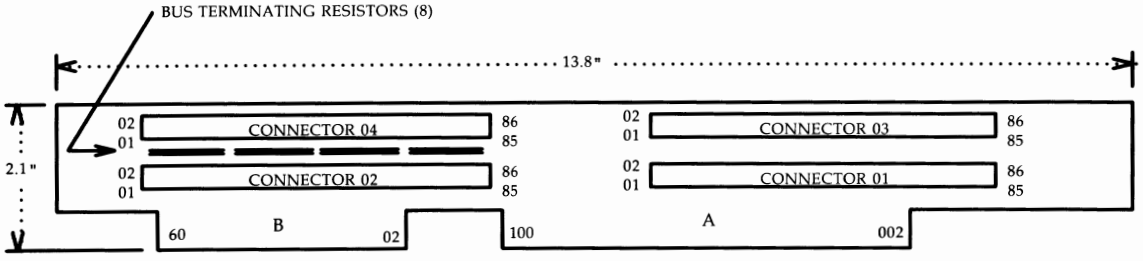
120-PIN CM523 MEMORY CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
061	MEMORY DATA BIT 31 (MD31[1])	INPUT/OUTPUT
062	MEMORY DATA BIT 30 (MD30[1])	INPUT/OUTPUT
063	GROUND (GRD)	GROUND
064	MEMORY DATA BIT 28 (MD28[1])	INPUT/OUTPUT
065	MEMORY DATA BIT 29 (MD29[1])	INPUT/OUTPUT
066	MEMORY DATA BIT 26 (MD26[1])	INPUT/OUTPUT
067	MEMORY DATA BIT 27 (MD27[1])	INPUT/OUTPUT
068	GROUND (GRD)	GROUND
069	MEMORY DATA BIT 25 (MD25[1])	INPUT/OUTPUT
070	MEMORY DATA BIT 24 (MD24[1])	INPUT/OUTPUT
071	GROUND (GRD)	GROUND
072	MEMORY DATA BIT 22 (MD22[1])	INPUT/OUTPUT
073	MEMORY DATA BIT 23 (MD23[1])	INPUT/OUTPUT
074	MEMORY DATA BIT 20 (MD20[1])	INPUT/OUTPUT
075	MEMORY DATA BIT 21 (MD21[1])	INPUT/OUTPUT
076	+5V (VCC)	POWER
077	MEMORY DATA BIT 19 (MD19[1])	INPUT/OUTPUT
078	MEMORY DATA BIT 18 (MD18[1])	INPUT/OUTPUT
079	+5V (VCC)	POWER
080	MEMORY DATA BIT 16 (MD16[1])	INPUT/OUTPUT
081	MEMORY DATA BIT 17 (MD17[1])	INPUT/OUTPUT
082	MEMORY DATA BIT 14 (MD14[1])	INPUT/OUTPUT
083	MEMORY DATA BIT 15 (MD15[1])	INPUT/OUTPUT
084	GROUND (GRD)	GROUND
085	MEMORY DATA BIT 13 (MD13[1])	INPUT/OUTPUT
086	MEMORY DATA BIT 12 (MD12[1])	INPUT/OUTPUT
087	GROUND (GRD)	GROUND
088	MEMORY DATA BIT 10 (MD10[1])	INPUT/OUTPUT
089	MEMORY DATA BIT 11 (MD11[1])	INPUT/OUTPUT
090	MEMORY DATA BIT 08 (MD08[1])	INPUT/OUTPUT
091	MEMORY DATA BIT 09 (MD09[1])	INPUT/OUTPUT
092	GROUND (GRD)	GROUND
093	MEMORY DATA BIT 07 (MD07[1])	INPUT/OUTPUT
094	MEMORY DATA BIT 06 (MD06[1])	INPUT/OUTPUT
095	GROUND (GRD)	GROUND
096	MEMORY DATA BIT 04 (MD04[1])	INPUT/OUTPUT
097	MEMORY DATA BIT 05 (MD05[1])	INPUT/OUTPUT
098	MEMORY DATA BIT 02 (MD02[1])	INPUT/OUTPUT
099	MEMORY DATA BIT 03 (MD03[1])	INPUT/OUTPUT
100	+5V (VCC)	POWER
101	MEMORY DATA BIT 01 (MD01[1]	INPUT/OUTPUT
102	MEMORY DATA BIT 00 (MD00[1]	INPUT/OUTPUT
103	+5V (VCC)	POWER
104	MEMORY CHECK BIT (MCB10[1])	NPUT/OUTPUT
105	MEMORY CHECK BIT (MCB11[1])	NPUT/OUTPUT
106	MEMORY CHECK BIT (MCB08[1])	NPUT/OUTPUT
107	MEMORY CHECK BIT (MCB09[1])	NPUT/OUTPUT
108	GROUND (GRD)	GROUND
109	MEMORY CHECK BIT (MCB07[1])	NPUT/OUTPUT
110	MEMORY CHECK BIT (MCB06[1])	NPUT/OUTPUT
111	GROUND (GRD)	GROUND
112	MEMORY CHECK BIT (MCB04[1])	NPUT/OUTPUT
113	MEMORY CHECK BIT (MCB05[1])	NPUT/OUTPUT
114	MEMORY CHECK BIT (MCB02[1])	NPUT/OUTPUT
115	MEMORY CHECK BIT (MCB03[1])	NPUT/OUTPUT
116	GROUND (GRD)	GROUND
117	MEMORY CHECK BIT (MCB01[1])	NPUT/OUTPUT
118	MEMORY CHECK BIT (MCB00[1])	NPUT/OUTPUT
119	GROUND (GRD)	GROUND
120	+5V (VCC)	POWER

LEGEND:

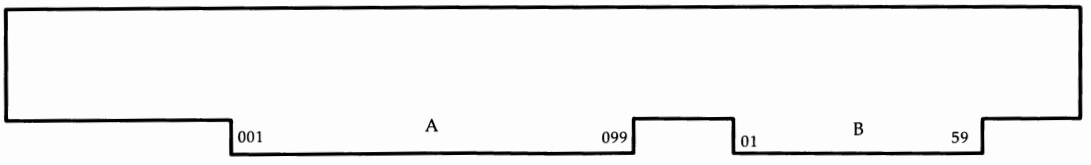
NC No Connection

CM193A/B AND CM194B BACKPLANE INTERCONNECTIONS

Figures B-15 and B-16 show the layout of the CM193A/B and CM194B Backplanes. The CM193A/B Backplane provides four 86-pin edge connectors. The CM194B Backplane provides twelve 86-pin edge connectors. These backplane edge connectors are used to interface feature cards with the system board. The backplane connects to the system board via a 100-pin (Connector A) and a 60-pin (Connector B) card edge connector. Refer to Figures B-15 and B-16 for backplane connector location information. Pin and signal information is provided in tables following the figures for each of the system board connectors. The figures are printed front and back with a blank unit so that the figures can be used in conjunction with the tables.

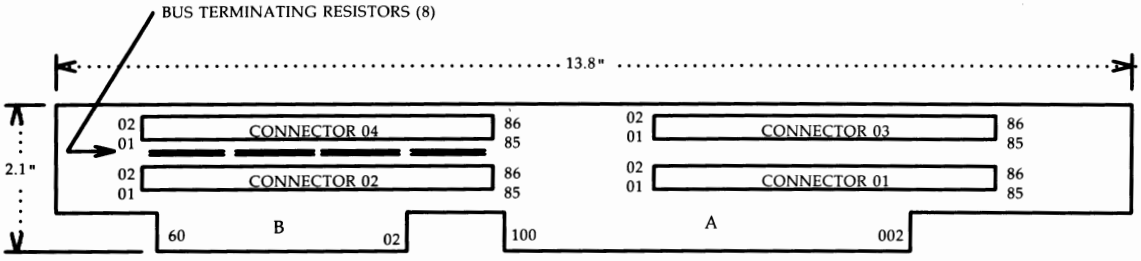


A. Front View

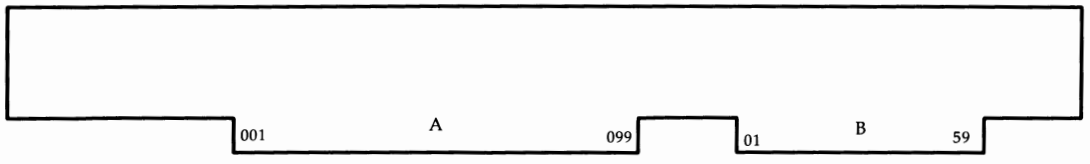


B. Rear View

Figure B-15: CM193A/B Backplane Layout

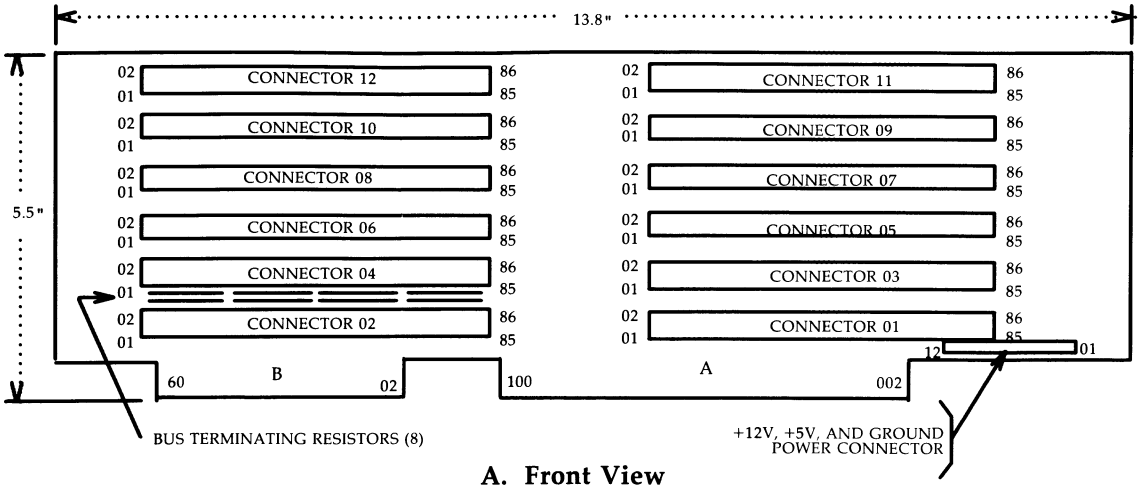


A. Front View

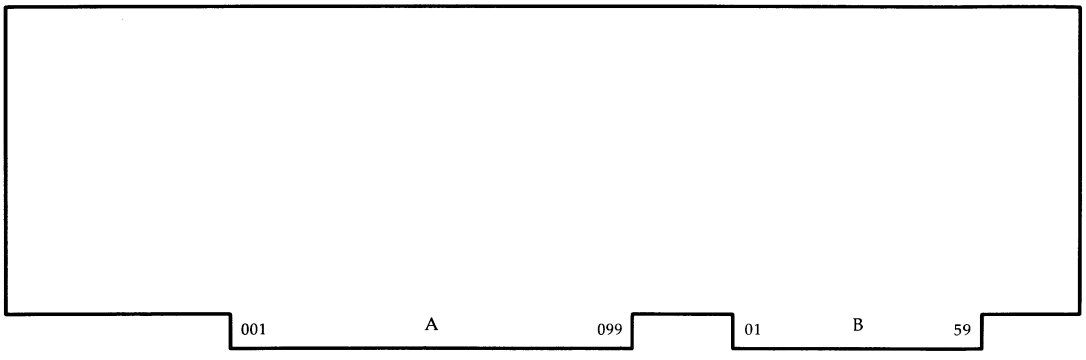


B. Rear View

Figure B-15: CM193A/B Backplane Layout

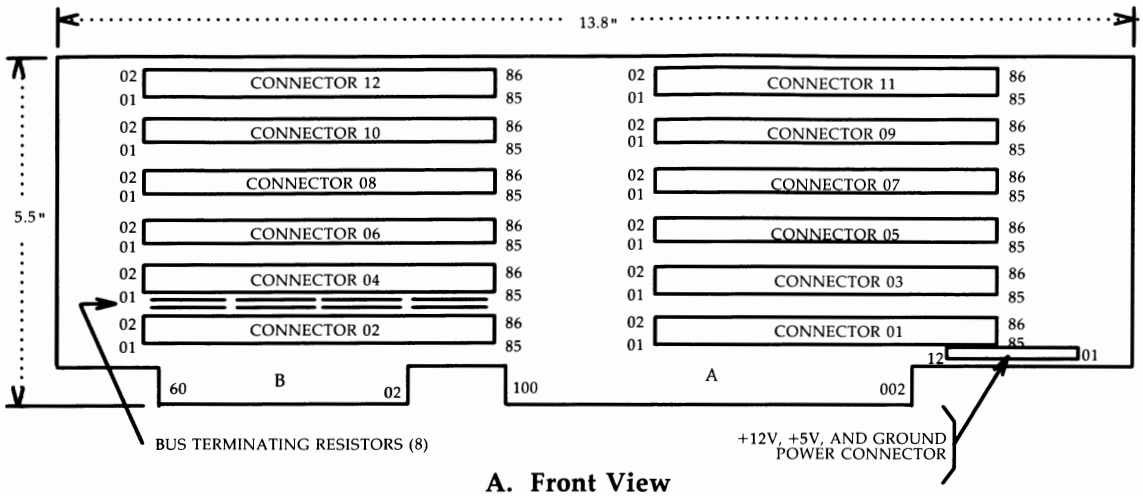


A. Front View

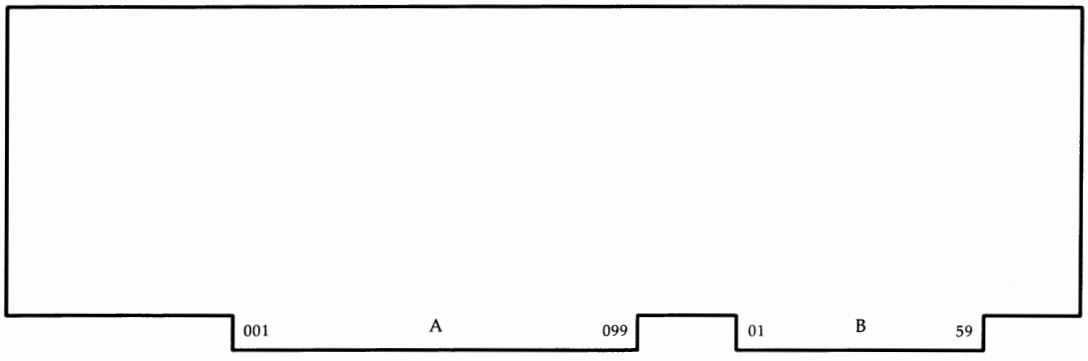


B. Rear View

Figure B-16: CM194B Backplane Layout



A. Front View



B. Rear View

Figure B-16: CM194B Backplane Layout

100-PIN BACKPLANE EDGE (A) CONNECTIONS		
PIN	DESCRIPTION	FUNCTION
A001	+5V (VCC)	POWER
A002	PHYSICAL ADDRESS (PPA23[1])	INPUT/OUTPUT
A003	PHYSICAL ADDRESS (PPA22[1])	INPUT/OUTPUT
A004	GROUND (GRD)	GROUND
A005	PHYSICAL ADDRESS (PPA21[1])	INPUT/OUTPUT
A006	PHYSICAL ADDRESS (PPA20[1])	INPUT/OUTPUT
A007	PHYSICAL ADDRESS (PPA19[1])	INPUT/OUTPUT
A008	GROUND (GRD)	GROUND
A009	PHYSICAL ADDRESS (PPA18[1])	INPUT/OUTPUT
A010	PHYSICAL ADDRESS (PPA17[1])	INPUT/OUTPUT
A011	+5V (VCC)	POWER
A012	GROUND (GRD)	GROUND
A013	PHYSICAL ADDRESS (PPA16[1])	INPUT/OUTPUT
A014	PHYSICAL ADDRESS (PPA15[1])	INPUT/OUTPUT
A015	PHYSICAL ADDRESS (PPA14[1])	INPUT/OUTPUT
A016	GROUND (GRD)	GROUND
A017	PHYSICAL ADDRESS (PPA13[1])	INPUT/OUTPUT
A018	PHYSICAL ADDRESS (PPA12[1])	INPUT/OUTPUT
A019	PHYSICAL ADDRESS (PPA11[1])	INPUT/OUTPUT
A020	PHYSICAL ADDRESS (PPA10[1])	INPUT/OUTPUT
A021	+5V (VCC)	POWER
A022	PHYSICAL ADDRESS (PPA09[1])	INPUT/OUTPUT
A023	PHYSICAL ADDRESS (PPA08[1])	INPUT/OUTPUT
A024	GROUND (GRD)	GROUND
A025	PHYSICAL ADDRESS (PPA07[1])	INPUT/OUTPUT
A026	PHYSICAL ADDRESS (PPA06[1])	INPUT/OUTPUT
A027	PHYSICAL ADDRESS (PPA05[1])	INPUT/OUTPUT
A028	GROUND (GRD)	GROUND
A029	PHYSICAL ADDRESS (PPA04[1])	INPUT/OUTPUT
A030	PHYSICAL ADDRESS (PPA03[1])	INPUT/OUTPUT
A031	+5V (VCC)	POWER
A032	GROUND (GRD)	GROUND
A033	PHYSICAL ADDRESS (PPA02[1])	INPUT/OUTPUT
A034	PHYSICAL ADDRESS (PPA01[1])	INPUT/OUTPUT
A035	PHYSICAL ADDRESS (PPA00[1])	INPUT/OUTPUT
A036	GROUND (GRD)	GROUND
A037	INTERLOCK (PLOCK[0])	INPUT/OUTPUT
A038	READ-WRITE (PR1W[0])	INPUT/OUTPUT
A039	PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
A040	GROUND (GRD)	GROUND
A041	+5V (VCC)	POWER
A042	BUS ACKNOWLEDGE (PBACK[0])	INPUT/OUTPUT
A043	BUS REQUEST (PBRQ[0])	INPUT/OUTPUT
A044	GROUND (GRD)	GROUND
A045	DATA BIT 15 (PD15[1])	INPUT/OUTPUT
A046	DATA BIT 14 (PD14[1])	INPUT/OUTPUT
A047	DATA BIT 13 (PD13[1])	INPUT/OUTPUT
A048	GROUND (GRD)	GROUND
A049	DATA BIT 12 (PD12[1])	INPUT/OUTPUT
A050	DATA BIT 11 (PD11[1])	INPUT/OUTPUT

100-PIN BACKPLANE EDGE (A) CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
A051	+5V (VCC)	POWER
A052	GROUND (GRD)	GROUND
A053	DATA BIT 10 (PD10[1])	INPUT/OUTPUT
A054	DATA BIT 09 (PD09[1])	INPUT/OUTPUT
A055	DATA BIT 08 (PD08[1])	INPUT/OUTPUT
A056	GROUND (GRD)	GROUND
A057	DATA BIT 07 (PD07[1])	INPUT/OUTPUT
A058	DATA BIT 06 (PD06[1])	INPUT/OUTPUT
A059	DATA BIT 05 (PD05[1])	INPUT/OUTPUT
A060	GROUND (GRD)	GROUND
A061	+5V (VCC)	POWER
A062	DATA BIT 04 (PD04[1])	INPUT/OUTPUT
A063	DATA BIT 03 (PD03[1])	INPUT/OUTPUT
A064	GROUND (GRD)	GROUND
A065	DATA BIT 02 (PD02[1])	INPUT/OUTPUT
A066	DATA BIT 01 (PD01[1])	INPUT/OUTPUT
A067	DATA BIT 00 (PD00[1])	INPUT/OUTPUT
A068	GROUND	GROUND
A069	DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
A070	DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
A071	+5V (VCC)	POWER
A072	GROUND (GRD)	GROUND
A073	DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
A074	CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	INPUT/OUTPUT
A075	BUS FAULT (PFLT[0])	INPUT/OUTPUT
A076	GROUND (GRD)	GROUND
A077	INPUT/OUTPUT BOARD FAILURE (PFAIL[0])	INPUT/OUTPUT
A078	BUS BUSY (PBUSY[0])	INPUT/OUTPUT
A079	SYSTEM RESET (SYSRST[0])	INPUT/OUTPUT
A080	GROUND (GRD)	GROUND
A081	+5V (VCC)	POWER
A082	INTERRUPT ACKNOWLEDGE 0 (PIAK0[0])	INPUT/OUTPUT
A083	REQUEST SYSTEM RESET (RQRST[0])	INPUT/OUTPUT
A084	INTERRUPT ACKNOWLEDGE 1 (PIAK1[0])	INPUT/OUTPUT
A085	INTERRUPT REQUEST 0 (PINT0[0])	INPUT/OUTPUT
A086	INTERRUPT ACKNOWLEDGE 2 (PIAK2[0])	INPUT/OUTPUT
A087	INTERRUPT REQUEST 1 (PINT1[0])	INPUT/OUTPUT
A088	GROUND (GRD)	GROUND
A089	INTERRUPT REQUEST 2 (PINT2[0])	INPUT/OUTPUT
A090	BACKUP BATTERY (+3.9V) (VBKUP)	POWER
A091	+5V (VCC)	POWER
A092	GROUND (GRD)	GROUND
A093	CARD SELECT 01 (PCS01[0])	INPUT
A094	-12V (V12N)	POWER
A095	CARD SELECT 02 (PCS02[0])	INPUT
A096	GROUND (GRD)	GROUND
A097	CARD SELECT 03 (PCS03[0])	INPUT
A098	+12V (V12P)	INPUT/OUTPUT
A099	CARD SELECT 04 (PCS04[0])	INPUT
A100	GROUND (GRD)	GROUND

60-PIN BACKPLANE EDGE (B) CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
B001	+5V (VCC)	POWER
B002	CARD SELECT 05 (PCS05[0])	INPUT
B003	+5V (VCC)	POWER
B004	GROUND (GRD)	GROUND
B005	CARD SELECT 06 (PCS06[0])	INPUT
B006	GROUND (GRD)	GROUND
B007	+5V (VCC)	POWER
B008	GROUND (GRD)	GROUND
B009	+5V (VCC)	POWER
B010	GROUND (GRD)	GROUND
B011	CARD SELECT 07 (PCS07[0])	INPUT
B012	GROUND (GRD)	GROUND
B013	+5V (VCC)	POWER
B014	GROUND (GRD)	GROUND
B015	+5V (VCC)	POWER
B016	GROUND (GRD)	GROUND
B017	CARD SELECT 08 (PCS08[0])	INPUT
B018	GROUND (GRD)	GROUND
B019	+5V (VCC)	POWER
B020	GROUND (GRD)	GROUND
B021	+5V (VCC)	POWER
B022	GROUND (GRD)	GROUND
B023	CARD SELECT 09 (PCS09[0])	INPUT
B024	GROUND (GRD)	GROUND
B025	+5V (VCC)	POWER
B026	GROUND (GRD)	GROUND
B027	+5V (VCC)	POWER
B028	GROUND (GRD)	GROUND
B029	CARD SELECT 10 (PCS10[0])	INPUT
B030	GROUND (GRD)	GROUND

60-PIN BACKPLANE EDGE (B) CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
B031	+5V (VCC)	POWER
B032	GROUND (GRD)	GROUND
B033	+5V (VCC)	POWER
B034	GROUND (GRD)	GROUND
B035	CARD SELECT 11 (PCS11[0]	INPUT
B036	GROUND (GRD)	GROUND
B037	+5V (VCC)	POWER
B038	GROUND (GRD)	GROUND
B039	+5V (VCC)	POWER
B040	GROUND (GRD)	GROUND
B041	CARD SELECT 12 (PCS12[0])	INPUT
B042	GROUND (GRD)	GROUND
B043	+5V (VCC)	POWER
B044	GROUND (GRD)	GROUND
B045	+5V (VCC)	POWER
B046	GROUND (GRD)	GROUND
B047	CARD SELECT 13 (PCS13[0])	INPUT
B048	GROUND (GRD)	GROUND
B049	+5V (VCC)	POWER
B050	GROUND (GRD)	GROUND
B051	+5V (VCC)	POWER
B052	GROUND (GRD)	GROUND
B053	CARD SELECT 14 (PCS14[0])	INPUT
B054	GROUND (GRD)	GROUND
B055	+5V (VCC)	POWER
B056	GROUND (GRD)	GROUND
B057	+5V (VCC)	POWER
B058	GROUND (GRD)	GROUND
B059	CARD SELECT 15 (PCS15[0])	INPUT
B060	GROUND (GRD)	GROUND

86-PIN FEATURE CARD CONNECTORS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])	INPUT/OUTPUT
003	-12V (V12N)	POWER
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	INPUT/OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN 1 (PBACKI1[0])	INPUT/OUTPUT
006	PERIPHERAL INTERRUPT REQUEST 1 (PINT0[0])	INPUT/OUTPUT
007	PERIPHERAL CARD SELECT (PCS01[0]—PCS12[0], as applicable)	INPUT
008	PERIPHERAL REQUEST SYSTEM RESET (RQRST[0])	INPUT/OUTPUT
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	+3.9V BACKUP BATTERY (VBKUP)	POWER
012	PERIPHERAL CARD FAILURE (PFAIL[0])	INPUT/OUTPUT
013	PERIPHERAL INTERRUPT ACKNOWLEDGE 2 (PIAK2[0])	INPUT/OUTPUT
014	PERIPHERAL BUS FAULT (PFLT0)	INPUT/OUTPUT
015	PERIPHERAL INTERRUPT ACKNOWLEDGE 2 (PIAK2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE 1 (PIAK1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INTERRUPT ACKNOWLEDGE 1 (PIAK1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INTERRUPT ACKNOWLEDGE 0 (PIAK0[0])	INPUT/OUTPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	INPUT/OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INTERRUPT ACKNOWLEDGE 0 (PIAK0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	INPUT/OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND

86-PIN FEATURE CARD CONNECTORS (Contd)		
PIN	DESCRIPTION	FUNCTION
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	INPUT/OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	INPUT/OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO1[0])	INPUT/OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	INPUT/OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	INPUT/OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	INPUT/OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	INPUT/OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PHYSICAL ADDRESS BIT 07 (PPA07[1])	INPUT/OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	INPUT/OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	INPUT/OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	INPUT/OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	INPUT/OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	INPUT/OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	INPUT/OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	INPUT/OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	INPUT/OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	INPUT/OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	INPUT/OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	INPUT/OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	INPUT/OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	INPUT/OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	INPUT/OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	INPUT/OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	INPUT/OUTPUT

CM194B 12-PIN BACKPLANE POWER CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
01	+5V (VCC)	POWER
02	+5V (VCC)	POWER
03	+5V (VCC)	POWER
04	+5V (VCC)	POWER
05	+5V (VCC)	POWER
06	NC	NC
07	GROUND (GRD)	GROUND
08	GROUND (GRD)	GROUND
09	GROUND (GRD)	GROUND
10	GROUND (GRD)	GROUND
11	GROUND (GRD)	GROUND
12	-12V (N12V)	POWER

LEGEND:

NC No Connection

CM519A/B AND CM520A BACKPLANE INTERCONNECTIONS

Figures B-17, B-18, and B-19 show the layout of the CM519A, CM519B, and CM520A Backplanes. The CM519A Backplane provides twelve 112-pin feature card connectors. There are 12 performance slots underneath the system board consisting of 4 memory, 4 buffered microbus (for MPE cards), 1 VCACHE, and 3 power only connectors.

The CM519B Backplane provides twelve 112-pin feature card connectors. The 12 performance slots underneath the system board consist of 4 memory, 3 buffered microbus (for MPE cards), 3 unbuffered microbus (for PE cards), and 2 power only connectors.

The CM520A Backplane provides seven 112-pin feature card connectors, 2 memory, 2 buffered microbus, and 1 VCACHE.

Refer to these figures for backplane connector location information. Pin and signal information is provided in tables following the figures for each of the backplane connectors. The figures are printed front and back with a blank unit so that the figures can be used in conjunction with the tables.

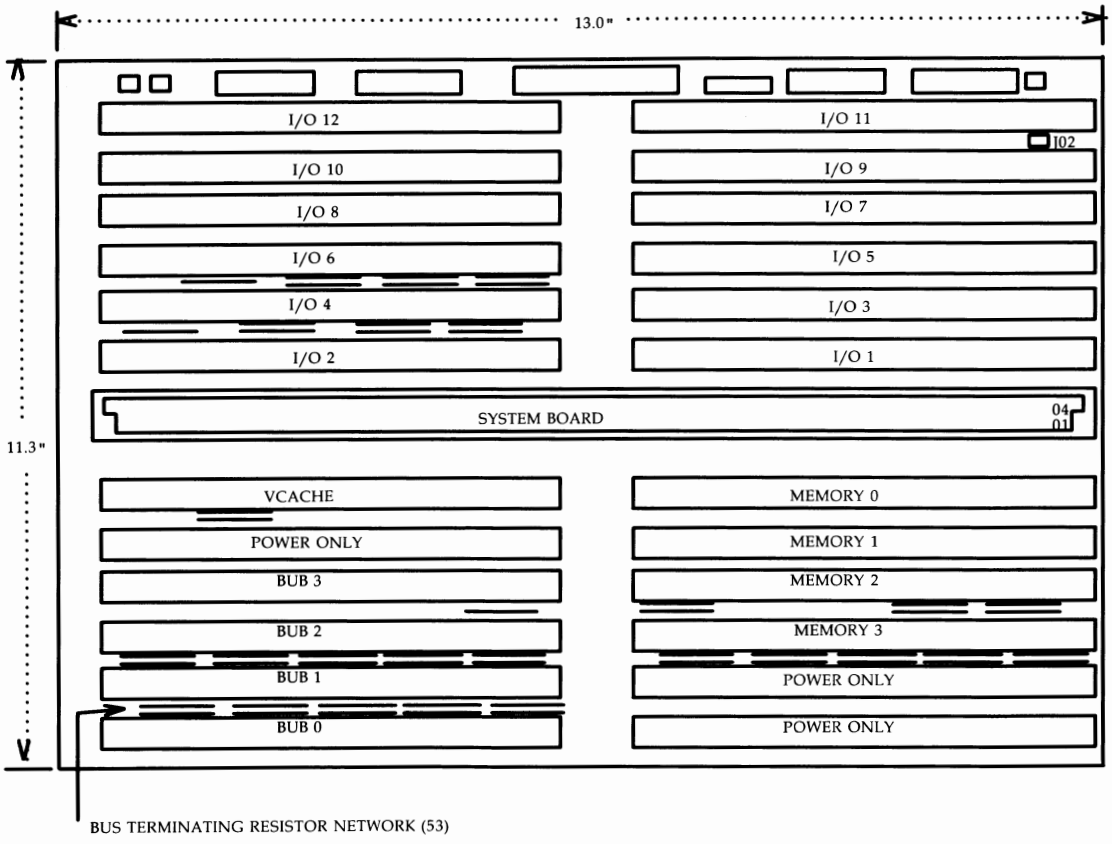


Figure B-17: CM519A Backplane Layout

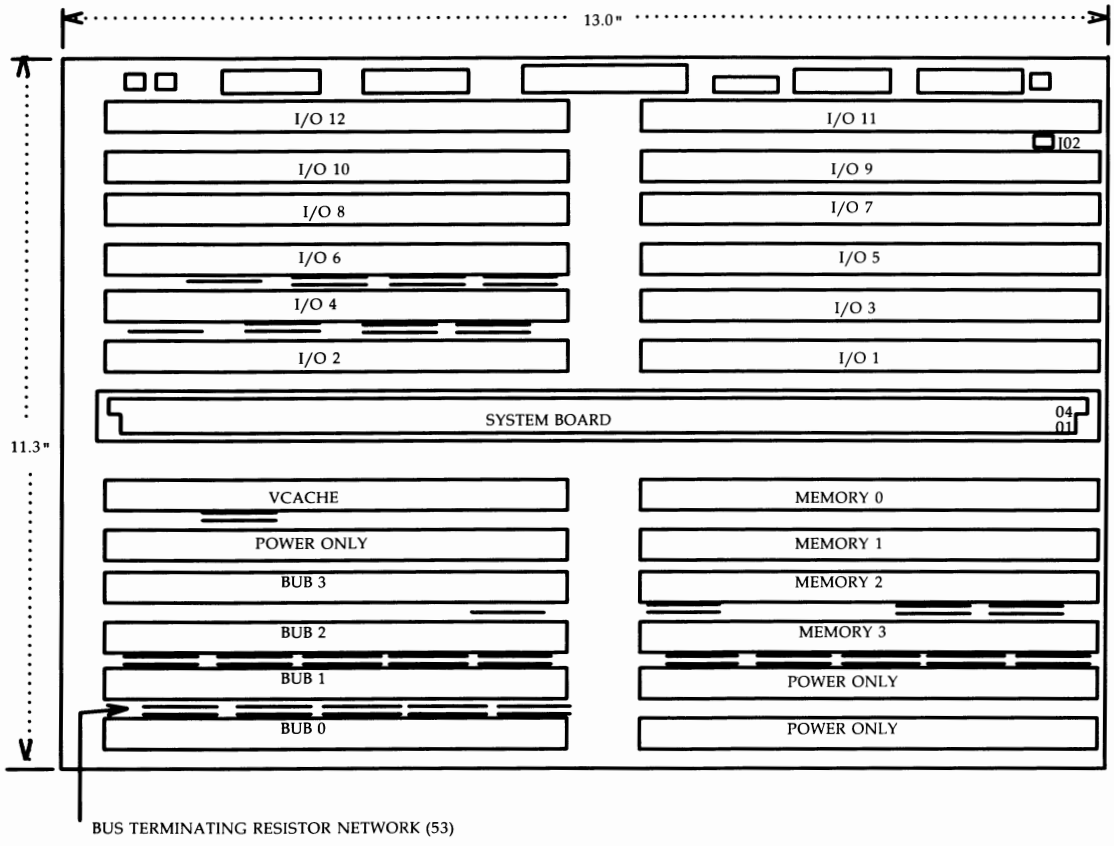


Figure B-17: CM519A Backplane Layout

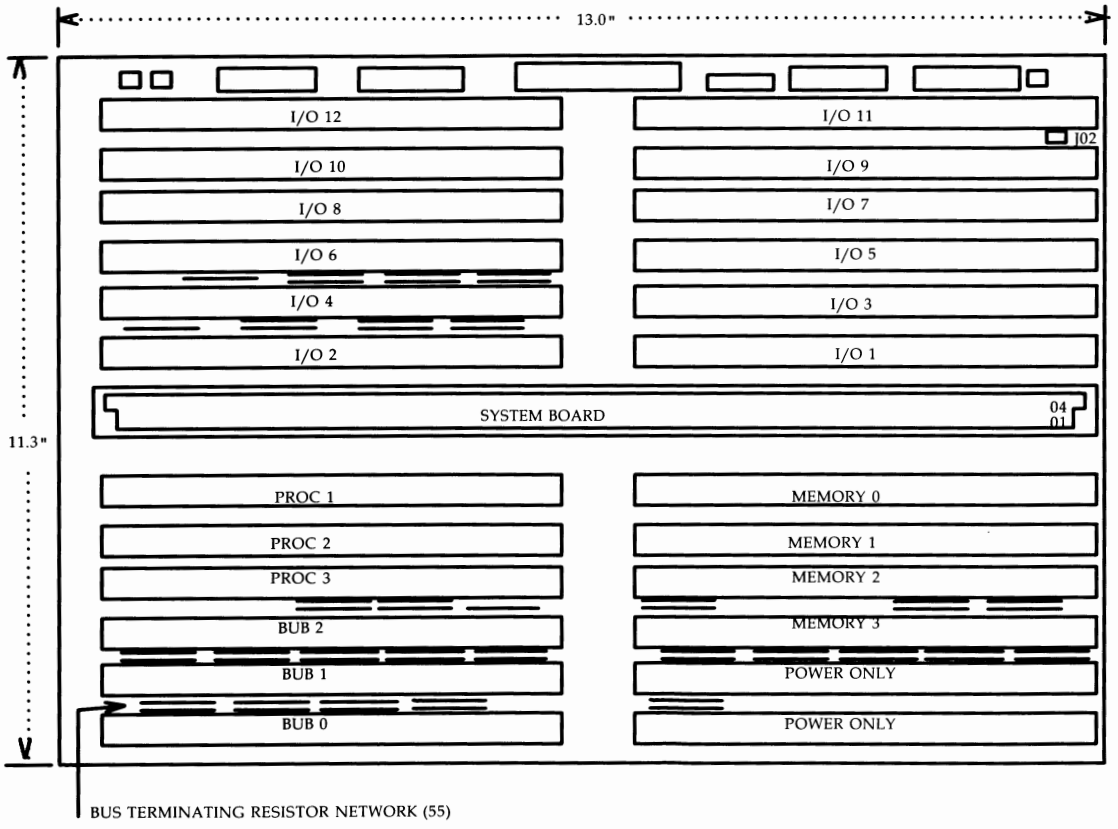


Figure B-18: CM519B Backplane Layout

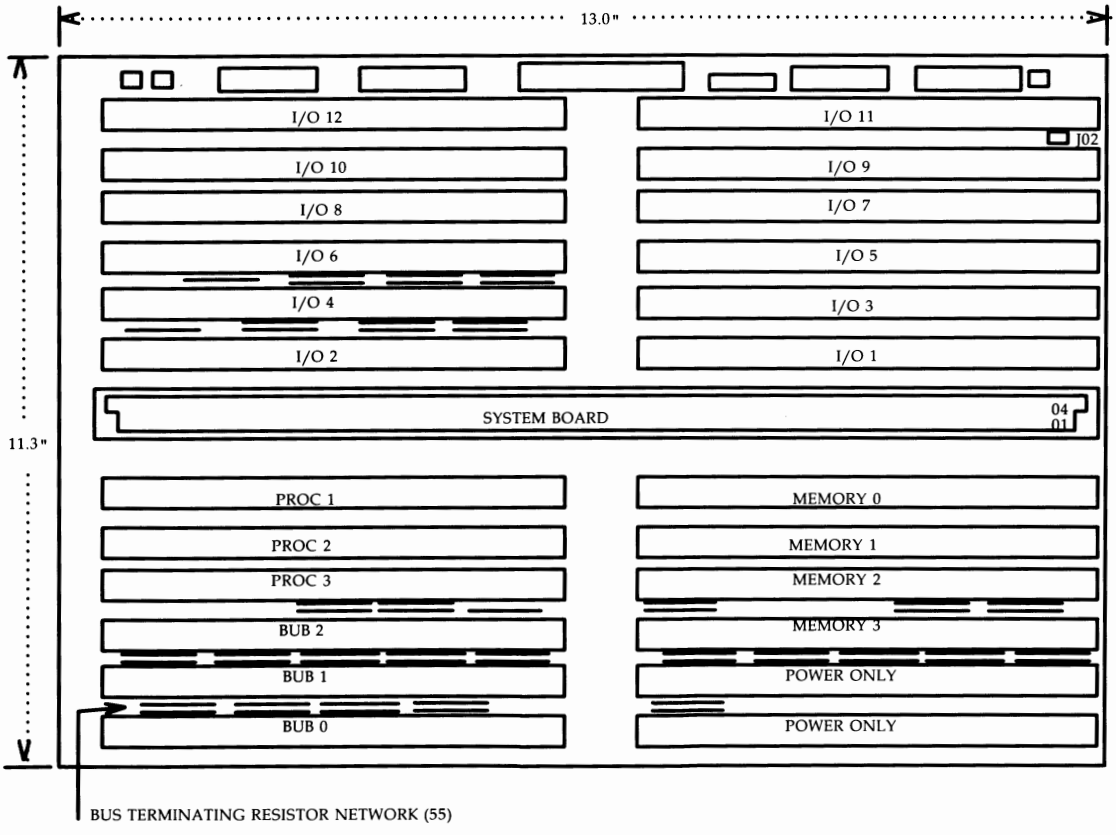


Figure B-18: CM519B Backplane Layout

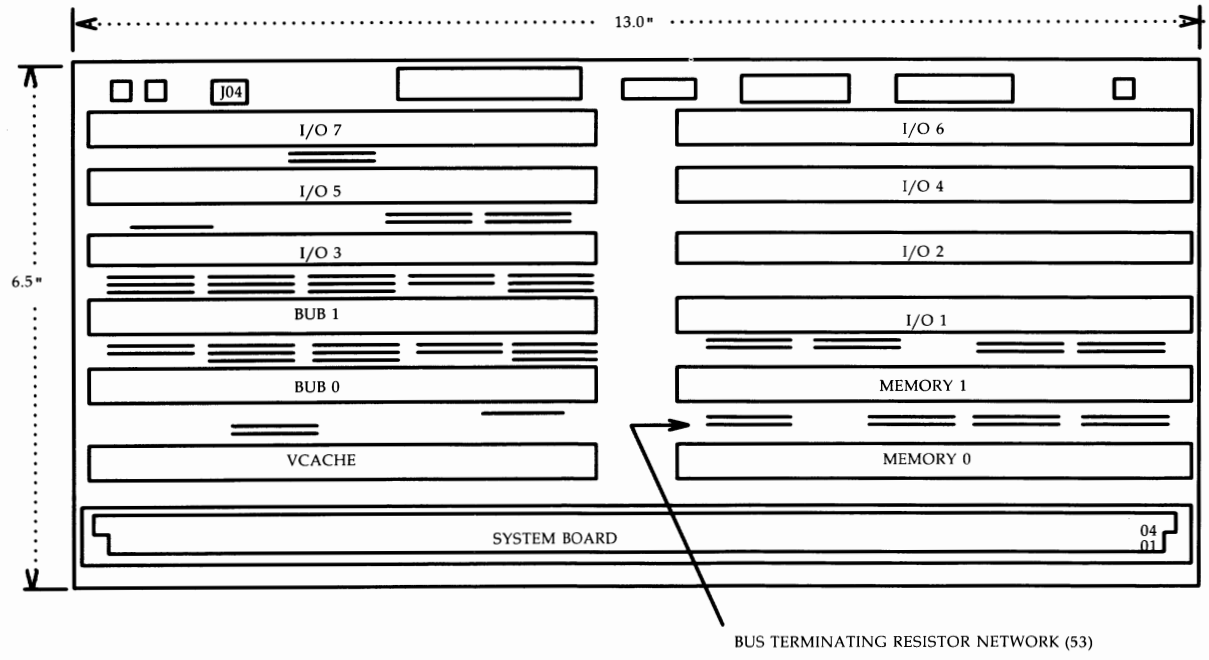


Figure B-19: CM520A Backplane Layout

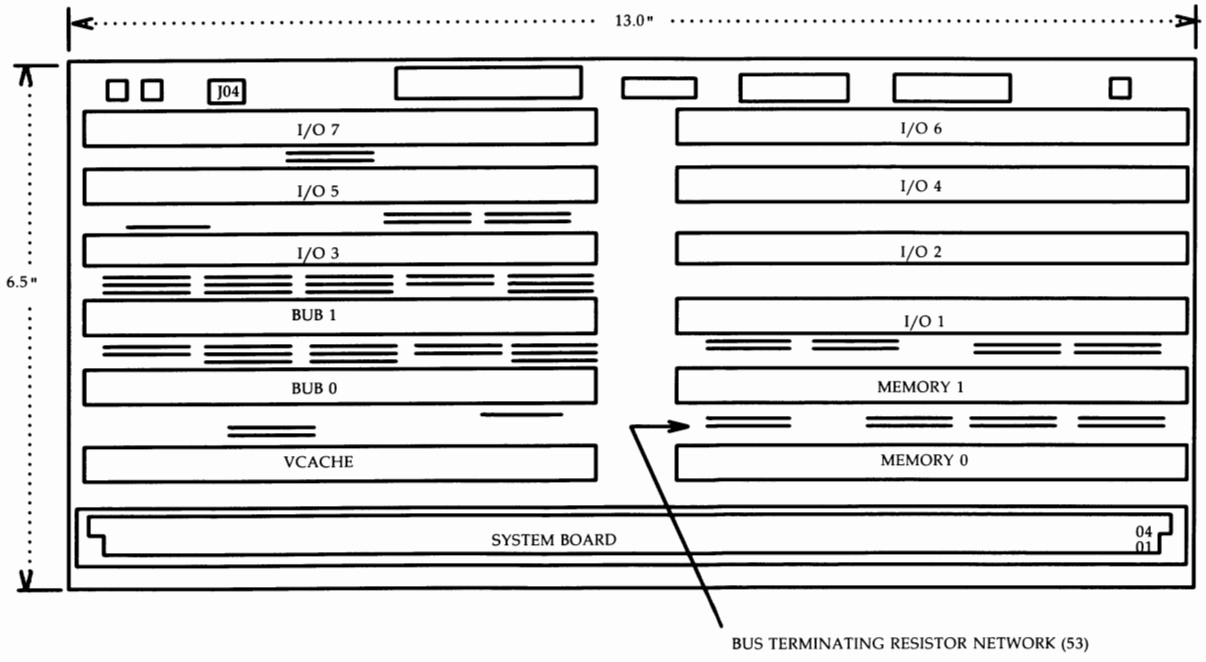


Figure B-19: CM520A Backplane Layout

464-PIN BACKPLANE CONNECTOR, J02		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	+5V (VCC)	POWER
003	FLOPPY READY (FRDY[0])	INPUT
004	FLOPPY SIDE SELECT (FSSEL[0])	OUTPUT
005	-12V (V12N)	POWER
006	FLOPPY READ DATA (FRDATA[0])	INPUT
007	GROUND (GRD)	GROUND
008	FLOPPY WRITE PROTECT (FWRPRT[0])	INPUT
009	FLOPPY TRACK 0 (FTR0[0])	INPUT
010	GROUND (GRD)	GROUND
011	FLOPPY WRITE GATE (FWGATE[0])	OUTPUT
012	FLOPPY WRITE DATA (FWDATA[0])	OUTPUT
013	FLOPPY STEP (FSTEP[0])	OUTPUT
014	FLOPPY DIRECTION SELECT (FDIRC[0])	OUTPUT
015	FLOPPY MOTOR ON (FMOTON[0])	OUTPUT
016	FLOPPY DRIVE SELECT 2 (FDS2[0])	OUTPUT
017	FLOPPY DRIVE SELECT 1 (FDS1[0])	OUTPUT
018	FLOPPY DRIVE SELECT 0 (FDS0[0])	OUTPUT
019	+5V (VCC)	POWER
020	FLOPPY LOW RPM (FLOW[0])	OUTPUT
021	FLOPPY INDEX (FINDEX[0])	INPUT
022	FLOPPY DRIVE SELECT 3 (FDS3[0])	OUTPUT
023	NOT USED (FSPARE[0])	INPUT
024	MEMORY CHECK BIT 00 (MCB00[1])	INPUT/OUTPUT
025	MEMORY CHECK BIT 01 (MCB01[1])	INPUT/OUTPUT
026	GROUND (GRD)	GROUND
027	MEMORY CHECK BIT 03 (MCB03[1])	INPUT/OUTPUT
028	MEMORY CHECK BIT 02 (MCB02[1])	INPUT/OUTPUT
029	MEMORY CHECK BIT 05 (MCB05[1])	INPUT/OUTPUT
030	MEMORY CHECK BIT 04 (MCB04[1])	INPUT/OUTPUT
031	+5V (VCC)	POWER
032	MEMORY CHECK BIT 09 (MCB09[1])	INPUT/OUTPUT
033	MEMORY CHECK BIT 06 (MCB06[1])	INPUT/OUTPUT
034	MEMORY CHECK BIT 07 (MCB07[1])	INPUT/OUTPUT
035	MEMORY CHECK BIT 08 (MCB08[1])	INPUT/OUTPUT
036	MEMORY CHECK BIT 11 (MCB11[1])	INPUT/OUTPUT
037	MEMORY CHECK BIT 10 (MCB10[1])	INPUT/OUTPUT
038	GROUND (GRD)	GROUND
039	MEMORY DATA BIT 00 (MD00[1])	INPUT/OUTPUT
040	MEMORY DATA BIT 01 (MD01[1])	INPUT/OUTPUT
041	MEMORY DATA BIT 02 (MD02[1])	INPUT/OUTPUT
042	MEMORY DATA BIT 03 (MD03[1])	INPUT/OUTPUT
043	GROUND (GRD)	GROUND
044	MEMORY DATA BIT 04 (MD04[1])	INPUT/OUTPUT
045	MEMORY DATA BIT 05 (MDO5[1])	INPUT/OUTPUT
046	+5V (VCC)	POWER
047	MEMORY DATA BIT 06 (MD06[1])	INPUT/OUTPUT
048	MEMORY DATA BIT 07 (MD07[1])	INPUT/OUTPUT
049	MEMORY DATA BIT 08 (MD08[1])	INPUT/OUTPUT
050	MEMORY DATA BIT 09 (MD09[1])	INPUT/OUTPUT
051	MEMORY DATA BIT 10 (MD10[1])	INPUT/OUTPUT
052	MEMORY DATA BIT 11 (MD11[1])	INPUT/OUTPUT
053	MEMORY DATA BIT 12 (MD12[1])	INPUT/OUTPUT
054	MEMORY DATA BIT 13 (MD13[1])	INPUT/OUTPUT
055	GROUND (GRD)	GROUND
056	MEMORY DATA BIT 14 (MD14[1])	INPUT/OUTPUT
057	MEMORY DATA BIT 15 (MD15[1])	INPUT/OUTPUT
058	MEMORY DATA BIT 16 (MD16[1])	INPUT/OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)		
PIN	**DESCRIPTION**	**FUNCTION**
059	MEMORY DATA BIT 17 (MD17[1])	INPUT/OUTPUT
060	MEMORY DATA BIT 18 (MD18[1])	INPUT/OUTPUT
061	MEMORY DATA BIT 19 (MD19[1])	INPUT/OUTPUT
062	GROUND (GRD)	GROUND
063	MEMORY DATA BIT 20 (MD20[1])	INPUT/OUTPUT
064	MEMORY DATA BIT 21 (MD21[1])	INPUT/OUTPUT
065	MEMORY DATA BIT 22 (MD22[1])	INPUT/OUTPUT
066	MEMORY DATA BIT 23 (MD23[1])	INPUT/OUTPUT
067	MEMORY DATA BIT 24 (MD24[1])	INPUT/OUTPUT
068	MEMORY DATA BIT 25 (MD25[1])	INPUT/OUTPUT
069	MEMORY DATA BIT 26 (MD26[1])	INPUT/OUTPUT
070	MEMORY DATA BIT 27 (MD27[1])	INPUT/OUTPUT
071	GROUND (GRD)	GROUND
072	MEMORY DATA BIT 28 (MD28[1])	INPUT/OUTPUT
073	MEMORY DATA BIT 29 (MD29[1])	INPUT/OUTPUT
074	MEMORY DATA BIT 30 (MD30[1])	INPUT/OUTPUT
075	MEMORY DATA BIT 31 (MD31[1])	INPUT/OUTPUT
076	SLOT 3 EQUIPPED (S3EQUIP[0])	INPUT
077	SLOT 3 SIZE 1 (S3SIZ1[1])	INPUT
078	+5V (VCC)	POWER
079	SLOT 3 SIZE 0 (S3SIZ0[1])	INPUT
080	SLOT 2 EQUIPPED (S2EQUIP[0])	INPUT
081	SLOT 2 SIZE 1 (S2SIZ1[1])	INPUT
082	SLOT 2 SIZE 0 (S2SIZ0[1])	INPUT
083	GROUND (GRD)	GROUND
084	SLOT 1 EQUIPPED (S1EQUIP[0])	INPUT
085	SLOT 1 SIZE 1 (S1SIZ1[1])	INPUT
086	SLOT 1 SIZE 0 (S1SIZ0[1])	INPUT
087	SLOT 0 SIZE 1 (S0SIZ1[1])	INPUT
088	SLOT 0 EQUIPPED (S0EQUIP[0])	INPUT
089	SLOT 0 SIZE 0 (S0SIZ0[1])	INPUT
090	GROUND (GRD)	GROUND
091	COLUMN ADDRESS STROBE 1 (CAS1[0])	OUTPUT
092	BANK ENABLE 2 (BANKEN2[0])	OUTPUT
093	COLUMN ADDRESS STROBE 0 (CAS0[0])	OUTPUT
094	COLUMN ADDRESS STROBE 2 (CAS2[0])	OUTPUT
095	COLUMN ADDRESS STROBE 3 (CAS3[0])	OUTPUT
096	SLOT 3 BANK ENABLE 1 (S3BKEN1[0])	OUTPUT
097	SLOT 3 BANK ENABLE 0 (S3BKEN0[0])	OUTPUT
098	SLOT 2 BANK ENABLE 1 (S2BKEN1[0])	OUTPUT
099	GROUND (GRD)	GROUND
100	SLOT 1 BANK ENABLE 1 (S1BKEN1[0])	OUTPUT
101	SLOT 2 BANK ENABLE 0 (S2BKEN0[0])	OUTPUT
102	GROUND (GRD)	GROUND
103	SLOT 1 BANK ENABLE 0 (S1BKEN0[0])	OUTPUT
104	ROW ADDRESS STROBE 1 (RAS1[0])	OUTPUT
105	SLOT 0 BANK ENABLE 0 (S0BKEN0[0])	OUTPUT
106	SLOT 0 BANK ENABLE 1 (S0BKEN1[0])	OUTPUT
107	+5V (VCC)	POWER
108	ROW ADDRESS STROBE 0 (RAS0[0])	OUTPUT
109	WRITE ENABLE 1 (WE1[0])	OUTPUT
110	GROUND (GRD)	GROUND
111	MEMORY CYCLE STATUS (G[0])	OUTPUT
112	NOT USED	NC
113	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	INPUT/OUTPUT
114	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	INPUT/OUTPUT
115	WRITE ENABLE 0 (WE0[0])	OUTPUT
116	BUB CONNECTOR CHIP SELECT 2 (BCCS2[0])	OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)		
PIN	**DESCRIPTION**	**FUNCTION**
117	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	INPUT/OUTPUT
118	GROUND (GRD)	GROUND
119	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	INPUT/OUTPUT
120	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	INPUT/OUTPUT
121	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	INPUT/OUTPUT
122	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	INPUT/OUTPUT
123	+5V (VCC)	POWER
124	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	INPUT/OUTPUT
125	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	INPUT/OUTPUT
126	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	INPUT/OUTPUT
127	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	INPUT/OUTPUT
128	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	INPUT/OUTPUT
129	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	INPUT/OUTPUT
130	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	INPUT/OUTPUT
131	GROUND (GRD)	GROUND
132	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	INPUT/OUTPUT
133	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	INPUT/OUTPUT
134	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	INPUT/OUTPUT
135	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	INPUT/OUTPUT
136	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	INPUT/OUTPUT
137	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
138	+5V (VCC)	POWER
139	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
140	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	INPUT/OUTPUT
141	NOT USED	NC
142	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
143	GROUND (GRD)	GROUND
144	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	INPUT/OUTPUT
145	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
146	GROUND (GRD)	GROUND
147	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
148	PERIPHERAL READ-WRITE (PR1W[0])	INPUT/OUTPUT
149	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
150	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
151	+5V (VCC)	POWER
152	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
153	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
154	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
155	PERIPHERAL BUS REQUEST (PBRQ[0])	INPUT
156	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
157	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
158	GROUND (GRD)	GROUND
159	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
160	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
161	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
162	PERIPHERAL CARD WIDTH (8 OR 16 BITS) (PSIZE16[0])	INPUT
163	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
164	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
165	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
166	+5V (VCC)	POWER
167	PERIPHERAL BUS BUSY (PBUSY[0])	INPUT/OUTPUT
168	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
169	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
170	GROUND (GRD)	GROUND
171	PERIPHERAL INTERRUPT ACKNOWLEDGE 0 (PIAK0[0])	OUTPUT
172	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
173	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
174	PERIPHERAL INTERRUPT ACKNOWLEDGE 1 (PIAK1[0])	OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)			
PIN	DESCRIPTION		FUNCTION
175	GROUND (GRD)		GROUND
176	PERIPHERAL DATA STROBE 1 (PDS1[0])		INPUT/OUTPUT
177	RECEIVED FAILURE (RFAIL[0])		INPUT
178	+5V (VCC)		POWER
179	PERIPHERAL INTERRUPT ACKNOWLEDGE 2 (PIAK2[0])		OUTPUT
180	PERIPHERAL BUS FAULT (PFLT[0])		INPUT/OUTPUT
181	PERIPHERAL CARD SELECT 09 (PCS09[0])		OUTPUT
182	PERIPHERAL CARD SELECT 10 (PCS10[0])		OUTPUT
183	PERIPHERAL CARD SELECT 11 (PCS11[0])		OUTPUT
184	PERIPHERAL CARD SELECT 12 (PCS12[0])		OUTPUT
185	PERIPHERAL CARD SELECT 06 (PCS06[0])		OUTPUT
186	GROUND (GRD)		GROUND
187	PERIPHERAL CARD SELECT 07 (PCS07[0])		OUTPUT
188	PERIPHERAL CARD SELECT 08 (PCS08[0])		OUTPUT
189	PERIPHERAL CARD SELECT 03 (PCS03[0])		OUTPUT
190	PERIPHERAL CARD SELECT 04 (PCS04[0])		OUTPUT
191	GROUND (GRD)		GROUND
192	PERIPHERAL CARD SELECT 05 (PCS05[0])		OUTPUT
193	PERIPHERAL BUS ACKNOWLEDGE (PBACK[0])		OUTPUT
194	BUB GRANTED SLOT 1 (BUBGT1[0])		OUTPUT
195	PERIPHERAL CARD SELECT 01 (PCS01[0])		OUTPUT
196	PERIPHERAL CARD SELECT 02 (PCS02[0])		OUTPUT
197	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])		INPUT
198	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])		INPUT
199	GROUND (GRD)		GROUND
200	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])		INPUT
201	BACKUP BATTERY (VBKUP)		OUTPUT
202	GROUND (GRD)		GROUND
203	PERIPHERAL SEQUENTIAL ACCESS (PSEQACC[0])		OUTPUT
204	BUB BUS REQUEST SLOT 2 (BUBRQ2[0])		INPUT
205	BUB DATA STROBE (BDS[0])		INPUT/OUTPUT
206	BUB ADDRESS STROBE (BAS[0])		INPUT/OUTPUT
207	GROUND (GRD)		GROUND
208	BUB DATA ACKNOWLEDGE (BDTCK[0])		INPUT/OUTPUT
209	BUB GRANTED SLOT 0 (BUBGT0[0])		OUTPUT
210	GROUND (GRD)		GROUND
211	BUB BYPASS MODE ACCESS (BYPASS[0])		OUTPUT
212	BUB DATA FAULT (BFLT[0])		INPUT/OUTPUT
213	NOT USED		NC
214*	BUB BUS REQUEST SLOT 3 (BUBRQ3[0])	*NOT USED*	INPUT *NC*
215	+5V (VCC)		POWER
216	PERIPHERAL PARITY CHECK (PPCHECK[0])		INPUT
217	NOT USED		NC
218	GROUND (GRD)		GROUND
219	BUB BUS REQUEST SLOT 1 (BUBRQ1[0])		INPUT
220	BUB BUS REQUEST SLOT 0 (BUBRQ0[0])		INPUT
221	MULTIPLEXED ADDRESS BIT 02 (MUXA02[1])		OUTPUT
222	MULTIPLEXED ADDRESS BIT 01 (MUXA01[1])		OUTPUT
223	MULTIPLEXED ADDRESS BIT 00 (MUXA00[1])		OUTPUT
224	BUB GRANTED SLOT 2 (BUBGT2[0])		OUTPUT
225	MULTIPLEXED ADDRESS BIT 05 (MUXA05[1])		OUTPUT
226	MULTIPLEXED ADDRESS BIT 04 (MUXA04[1])		OUTPUT
227	GROUND (GRD)		GROUND
228	MULTIPLEXED ADDRESS BIT 03 (MUXA03[1])		OUTPUT
229	MULTIPLEXED ADDRESS BIT 08 (MUXA08[1])		OUTPUT
230	+5V (VCC)		POWER
231	MULTIPLEXED ADDRESS BIT 07 (MUXA07[1])		OUTPUT
232	MULTIPLEXED ADDRESS BIT 06 (MUXA06[1])		OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)		
PIN	**DESCRIPTION**	**FUNCTION**
233	MULTIPLEXED ADDRESS BIT 10 (MUXA10[1])	OUTPUT
234	MULTIPLEXED ADDRESS BIT 09 (MUXA09[1])	OUTPUT
235	BUB GRANTED SLOT 3 (BUBGT3[0])	OUTPUT
236	BUB PERIPHERAL PARITY CHECK (BPCHECK[0])	INPUT/OUTPUT
237	BUB CONNECTOR CHIP SELECT 0 (BCCS0[0])	OUTPUT
238	BUB DATA SIZE BIT 0 (BDSIZE0[1])	INPUT/OUTPUT
239	GROUND (GRD)	GROUND
240	BUB SEQUENTIAL ACCESS (BSEQACC[0])	INPUT/OUTPUT
241	NOT USED	NC
242	NOT USED	NC
243	+5V (VCC)	POWER
244	NOT USED	NC
245	NOT USED	NC
246	GROUND (GRD)	GROUND
247	BUB DATA SIZE BIT 1 (BDSIZE1[1])	INPUT/OUTPUT
248	BUB READ/WRITE (BR1W[0])	INPUT/OUTPUT
249	BUB ADDRESS BIT 02 (BA02[1])	INPUT/OUTPUT
250	BUB ADDRESS BIT 01 (BA01[1])	INPUT/OUTPUT
251	NOT USED	NC
252	NOT USED	NC
253	BUB ADDRESS BIT 05 (BA05[1])	INPUT/OUTPUT
254	BUB ADDRESS BIT 04 (BA04[1])	INPUT/OUTPUT
255	GROUND (GRD)	GROUND
256	NOT USED	NC
257	BUB ADDRESS BIT 08 (BA08[1])	INPUT/OUTPUT
258	+5V (VCC)	POWER
259	BUB ADDRESS BIT 00 (BA00[1])	INPUT/OUTPUT
260	BUB ADDRESS BIT 03 (BA03[1])	INPUT/OUTPUT
261	BUB ADDRESS BIT 11 (BA11[1])	INPUT/OUTPUT
262	BUB ADDRESS BIT 10 (BA10[1])	INPUT/OUTPUT
263	GROUND (GRD)	GROUND
264	BUB ADDRESS BIT 06 (BA06[1])	INPUT/OUTPUT
265	BUB BUSY (BUSY[0])	INPUT/OUTPUT
266	GROUND (GRD)	GROUND
267	BUB CONNECTOR CHIP SELECT 1 (BCCS1[0])	OUTPUT
268	BUB ADDRESS BIT 09 (BA09[1])	INPUT/OUTPUT
269	BUB ADDRESS BIT 12 (BA12[1])	INPUT/OUTPUT
270	BUB ADDRESS BIT 15 (BA15[1])	INPUT/OUTPUT
271	BUB ADDRESS BIT 07 (BA07[1])	INPUT/OUTPUT
272	BUB ADDRESS BIT 13 (BA13[1])	INPUT/OUTPUT
273	BUB ADDRESS BIT 16 (BA16[1])	INPUT/OUTPUT
274	BUB ADDRESS BIT 18 (BA18[1])	INPUT/OUTPUT
275	+5V (VCC)	POWER
276	BUB ADDRESS BIT 17 (BA17[1])	INPUT/OUTPUT
277	BUB ADDRESS BIT 19 (BA19[1])	INPUT/OUTPUT
278	GROUND (GRD)	GROUND
279	BUB ADDRESS BIT 14 (BA14[1])	INPUT/OUTPUT
280	BUB ADDRESS BIT 20 (BA20[1])	INPUT/OUTPUT
281	BUB ADDRESS BIT 22 (BA22[1])	INPUT/OUTPUT
282	BUB ADDRESS BIT 24 (BA24[1])	INPUT/OUTPUT
283	BUB ADDRESS BIT 21 (BA21[1])	INPUT/OUTPUT
284	BUB ADDRESS BIT 23 (BA23[1])	INPUT/OUTPUT
285	BUB ADDRESS BIT 25 (BA25[1])	INPUT/OUTPUT
286	+5V (VCC)	POWER
287	NOT USED	NC
288	NOT USED	NC
289	NOT USED	NC
290	BUB DATA BIT 01 (BD01[1])	INPUT/OUTPUT

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)				
PIN	DESCRIPTION		FUNCTION	
291	BUB DATA BIT 00 (BD00[1])		INPUT/OUTPUT	
292	NOT USED		NC	
293	BUB DATA BIT 02 (BD02[1])		INPUT/OUTPUT	
294	BUB DATA BIT 04 (BD04[1])		INPUT/OUTPUT	
295	GROUND (GRD)		GROUND	
296	BUB DATA BIT 03 (BD03[1])		INPUT/OUTPUT	
297	BUB DATA BIT 05 (BD05[1])		INPUT/OUTPUT	
298	GROUND (GRD)		GROUND	
299	BUB DATA BIT 07 (BD07[1])		INPUT/OUTPUT	
300	BUB DATA BIT 06 (BD06[1])		INPUT/OUTPUT	
301	BUB DATA BIT 08 (BD08[1])		INPUT/OUTPUT	
302	BUB DATA BIT 10 (BD10[1])		INPUT/OUTPUT	
303	+5V (VCC)		POWER	
304	BUB DATA BIT 09 (BD09[1])		INPUT/OUTPUT	
305	BUB DATA BIT 11 (BD11[1])		INPUT/OUTPUT	
306	GROUND (GRD)		GROUND	
307	BUB DATA BIT 13 (BD13[1])		INPUT/OUTPUT	
308	BUB DATA BIT 12 (BD12[1])		INPUT/OUTPUT	
309	BUB DATA BIT 14 (BD14[1])		INPUT/OUTPUT	
310	BUB DATA BIT 17 (BD17[1])		INPUT/OUTPUT	
311	BUB DATA BIT 16 (BD16[1])		INPUT/OUTPUT	
312	BUB DATA BIT 15 (BD15[1])		INPUT/OUTPUT	
313	BUB DATA BIT 18 (BD18[1])		INPUT/OUTPUT	
314	BUB DATA BIT 20 (BD20[1])		INPUT/OUTPUT	
315	GROUND (GRD)		GROUND	
316	BUB DATA BIT 19 (BD19[1])		INPUT/OUTPUT	
317	BUB DATA BIT 21 (BD21[1])		INPUT/OUTPUT	
318	GROUND (GRD)		GROUND	
319	BUB DATA BIT 23 (BD23[1])		INPUT/OUTPUT	
320	BUB DATA BIT 22 (BD22[1])		INPUT/OUTPUT	
321	BUB DATA BIT 24 (BD24[1])		INPUT/OUTPUT	
322	BUB DATA BIT 26 (BD26[1])		INPUT/OUTPUT	
323	GROUND (GRD)		GROUND	
324	BUB DATA BIT 25 (BD25[1])		INPUT/OUTPUT	
325	BUB DATA BIT 27 (BD27[1])		INPUT/OUTPUT	
326	GROUND (GRD)		GROUND	
327	BUB DATA BIT 29 (BD29[1])		INPUT/OUTPUT	
328	BUB DATA BIT 28 (BD28[1])		INPUT/OUTPUT	
329	SYSTEM RESET (SYSRST[0])		OUTPUT	
330	REQUEST SYSTEM RESET (RQRST[0])		INPUT/OUTPUT	
331	NOT USED		NC	
332	THERMAL SHUTDOWN (THSDN[0])		INPUT	
333	BUB DATA BIT 30 (BD30[1])		INPUT/OUTPUT	
334	RECEIVED FAILURE (RFAIL[0])		INPUT	
335	+5V (VCC)		POWER	
336	BUB DATA BIT 31 (BD31[1])		INPUT/OUTPUT	
337	BUB CONNECTOR INHIBIT (BINHIB0[0])		OUTPUT	
338	BUB INTERRUPT LEVEL 10 (BINT010[0])		INPUT	
339	BUB INTERRUPT LEVEL 12 (BINT012[0])		INPUT	
340	BUB INTERRUPT LEVEL 14 (BINT014[0])		INPUT	
341*	UBUS DATA BIT 01 (CD01[1])	*NOT USED*	INPUT/OUTPUT	*NC*
342	GROUND (GRD)		GROUND	
343*	UBUS DATA BIT 00 (CD00[1])	*NOT USED*	INPUT/OUTPUT	*NC*
344*	UBUS SEQUENTIAL ACCESS (CSEQACC[0])	*NOT USED*	INPUT	*NC*
345*	UBUS DATA BIT 05 (CD05[1])	*NOT USED*	INPUT/OUTPUT	*NC*
346*	UBUS DATA BIT 04 (CD04[1])	*NOT USED*	INPUT/OUTPUT	*NC*
347*	UBUS DATA BIT 03 (CD03[1])	*NOT USED*	INPUT/OUTPUT	*NC*
348*	UBUS DATA BIT 02 (CD02[1])	*NOT USED*	INPUT/OUTPUT	*NC*

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)			
PIN	DESCRIPTION		FUNCTION
349*	UBUS DATA BIT 08 (CD08[1])	*NOT USED*	INPUT/OUTPUT *NC*
350*	UBUS DATA BIT 07 (CD07[1])	*NOT USED*	INPUT/OUTPUT *NC*
351	+5V (VCC)		POWER
352*	UBUS DATA BIT 06 (CD06[1])	*NOT USED*	INPUT/OUTPUT *NC*
353*	UBUS DATA BIT 11 (CD11[1])	*NOT USED*	INPUT/OUTPUT *NC*
354	GROUND (GRD)		GROUND
355*	UBUS DATA BIT 10 (CD10[1])	*NOT USED*	INPUT/OUTPUT *NC*
356*	UBUS DATA BIT 09 (CD09[1])	*NOT USED*	INPUT/OUTPUT *NC*
357*	UBUS DATA BIT 14 (CD14[1])	*NOT USED*	INPUT/OUTPUT *NC*
358*	UBUS DATA BIT 13 (CD13[1])	*NOT USED*	INPUT/OUTPUT *NC*
359	GROUND (GRD)		GROUND
360*	UBUS DATA BIT 12 (CD12[1])	*NOT USED*	INPUT/OUTPUT *NC*
361*	UBUS DATA BIT 18 (CD18[1])	*NOT USED*	INPUT/OUTPUT *NC*
362*	UBUS DATA BIT 17 (CD17[1])	*NOT USED*	INPUT/OUTPUT *NC*
363*	UBUS DATA BIT 16 (CD16[1])	*NOT USED*	INPUT/OUTPUT *NC*
364*	UBUS DATA BIT 15 (CD15[1])	*NOT USED*	INPUT/OUTPUT *NC*
365*	UBUS DATA BIT 21 (CD21[1])	*NOT USED*	INPUT/OUTPUT *NC*
366	+5V (VCC)		POWER
367*	UBUS DATA BIT 20 (CD20[1])	*NOT USED*	INPUT/OUTPUT *NC*
368*	UBUS DATA BIT 19 (CD19[1])	*NOT USED*	INPUT/OUTPUT *NC*
369*	UBUS DATA BIT 24 (CD24[1])	*NOT USED*	INPUT/OUTPUT *NC*
370*	UBUS DATA BIT 23 (CD23[1])	*NOT USED*	INPUT/OUTPUT *NC*
371	GROUND (GRD)		GROUND
372*	UBUS DATA BIT 22 (CD22[1])	*NOT USED*	INPUT/OUTPUT *NC*
373*	UBUS DATA BIT 27 (CD27[1])	*NOT USED*	INPUT/OUTPUT *NC*
374	GROUND (GRD)		GROUND
375*	UBUS DATA BIT 26 (CD26[1])	*NOT USED*	INPUT/OUTPUT *NC*
376*	UBUS DATA BIT 25 (CD25[1])	*NOT USED*	INPUT/OUTPUT *NC*
377*	UBUS DATA BIT 31 (CD31[1])	*NOT USED*	INPUT/OUTPUT *NC*
378*	UBUS DATA BIT 30 (CD30[1])	*NOT USED*	INPUT/OUTPUT *NC*
379*	UBUS DATA BIT 29 (CD29[1])	*NOT USED*	INPUT/OUTPUT *NC*
380*	UBUS DATA BIT 28 (CD28[1])	*NOT USED*	INPUT/OUTPUT *NC*
381*	UBUS ADDRESS BIT 02 (CA02[1])	*NOT USED*	INPUT/OUTPUT *NC*
382*	UBUS ADDRESS BIT 01 (CA01[1])	*NOT USED*	INPUT/OUTPUT *NC*
383	+5V (VCC)		POWER
384*	UBUS ADDRESS BIT 00 (CA00[1])	*NOT USED*	INPUT/OUTPUT *NC*
385*	UBUS ADDRESS BIT 05 (CA05[1])	*NOT USED*	INPUT/OUTPUT *NC*
386*	UBUS ADDRESS BIT 06 (CA06[1])	*NOT USED*	INPUT/OUTPUT *NC*
387*	UBUS ADDRESS BIT 04 (CA04[1])	*NOT USED*	INPUT/OUTPUT *NC*
388*	UBUS ADDRESS BIT 03 (CA03[1])	*NOT USED*	INPUT/OUTPUT *NC*
389*	UBUS ADDRESS BIT 08 (CA08[1])	*NOT USED*	INPUT/OUTPUT *NC*
390*	UBUS ADDRESS BIT 07 (CA07[1])	*NOT USED*	INPUT/OUTPUT *NC*
391	GROUND (GRD)		GROUND
392*	UBUS ADDRESS BIT 09 (CA09[1])	*NOT USED*	INPUT/OUTPUT *NC*
393*	UBUS ADDRESS BIT 11 (CA11[1])	*NOT USED*	INPUT/OUTPUT *NC*
394	+5V (VCC)		POWER
395*	UBUS ADDRESS BIT 10 (CA10[1])	*NOT USED*	INPUT/OUTPUT *NC*
396*	UBUS ADDRESS BIT 12 (CA12[1])	*NOT USED*	INPUT/OUTPUT *NC*
397*	UBUS ADDRESS BIT 15 (CA15[1])	*NOT USED*	INPUT/OUTPUT *NC*
398*	UBUS ADDRESS BIT 14 (CA14[1])	*NOT USED*	INPUT/OUTPUT *NC*
399*	UBUS ADDRESS BIT 13 (CA13[1])	*NOT USED*	INPUT/OUTPUT *NC*
400*	UBUS ADDRESS BIT 16 (CA16[1])	*NOT USED*	INPUT/OUTPUT *NC*
401*	UBUS ADDRESS BIT 18 (CA18[1])	*NOT USED*	INPUT/OUTPUT *NC*
402*	UBUS ADDRESS BIT 17 (CA17[1])	*NOT USED*	INPUT/OUTPUT *NC*
403	GROUND (GRD)		GROUND
404*	UBUS ADDRESS BIT 19 (CA19[1])	*NOT USED*	INPUT/OUTPUT *NC*
405*	UBUS ADDRESS BIT 21 (CA21[1])	*NOT USED*	INPUT/OUTPUT *NC*
406	GROUND (GRD)		GROUND

* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)				
PIN	DESCRIPTION		FUNCTION	
407*	UBUS ADDRESS BIT 20 (CA20[1])	*NOT USED*	INPUT/OUTPUT	*NC*
408*	UBUS ADDRESS BIT 22 (CA22[1])	*NOT USED*	INPUT/OUTPUT	*NC*
409*	UBUS ADDRESS BIT 24 (CA24[1])	*NOT USED*	INPUT/OUTPUT	*NC*
410*	UBUS ADDRESS BIT 23 (CA23[1])	*NOT USED*	INPUT/OUTPUT	*NC*
411	+5V (VCC)		POWER	
412*	UBUS ADDRESS BIT 25 (CA25[1])	*NOT USED*	INPUT/OUTPUT	*NC*
413*	UBUS ADDRESS BIT 27 (CA27[1])	*NOT USED*	INPUT/OUTPUT	*NC*
414*	GROUND (GRD)	*PBUS INHIBIT(UINHIB[0])*	GROUND	*OUTPUT*
415*	UBUS ADDRESS BIT 26 (CA26[1])	*NOT USED*	INPUT/OUTPUT	*NC*
416*	UBUS ADDRESS BIT 28 (CA28[1])	*NOT USED*	INPUT/OUTPUT	*NC*
417*	UBUS ADDRESS BIT 31 (CA31[1])	*NOT USED*	INPUT/OUTPUT	*NC*
418*	UBUS ADDRESS BIT 30 (CA30[1])	*NOT USED*	INPUT/OUTPUT	*NC*
419*	UBUS ADDRESS BIT 29 (CA29[1])	*NOT USED*	INPUT/OUTPUT	*NC*
420*	CLOCK 23 (CLK23[1])	*NOT USED*	OUTPUT	*NC*
421	HOLD REMOTE POWERON (PWRON[1])		OUTPUT	
422	REMOTE POWER DOWN REQUEST (PDWNRQ[0])		INPUT	
423	GROUND (GRD)		GROUND	
424*	CLOCK 34 (CLK34[1])	*NOT USED*	OUTPUT	*NC*
425*	UBUS GRANTED (BUSGT[0])	*CPU LATCH ADDRESS (CPULTCH[1])*	OUTPUT	*OUTPUT*
426	SANITY TIMER TIMEOUT (SANTO[0])		INPUT/OUTPUT	
427	OPERATIONAL INTERRUPT LEVEL 15 (OPINT15[0])		INPUT	
428*	VIRTUAL CACHE HIT (VCHIT[0])	*SLOT 3 VIRTUAL ADDRESS STROBE (C3VAS[0])*	INPUT	*INPUT/OUTPUT*
429*	UBUS EXECUTION MODE 1 (XMD1[1])	*NOT USED*	OUTPUT	*NC*
430	+5V (VCC)		POWER	
431*	UBUS BUS REQUEST (BUSRQ[0])	*SLOT 2 VIRTUAL ADDRESS STROBE (C2VAS[0])*	INPUT	*INPUT*
432*	UBUS COPROCESSOR DONE (DONE[0])	*SLOT 1 VIRTUAL ADDRESS STROBE (C1VAS[0])*	INPUT	*INPUT*
433*	UBUS VIRTUAL ADDRESS (BY CPU) (VAD[0])	*PBUS INTERLOCK (UINTLK[0])*	OUTPUT	*INPUT*
434*	UBUS ACCESS STATUS BIT 3 (SAS3[1])	*PBUS CARD SELECT SLOT 3 (UPCS3[0]*	OUTPUT	*OUTPUT*
435	GROUND (GRD)		GROUND	
436*	UBUS ACCESS STATUS BIT 2 (SAS2[1])	*PBUS CARD SELECT SLOT 2 (UPCS2[0])*	OUTPUT	*OUTPUT*
437*	UBUS DATA ACKNOWLEDGE (DTACK[0])	*PBUS SLOT 3 MEMORY REQUEST (CPU3MEM[0]*	INPUT	*INPUT*
438	GROUND (GRD)		GROUND	
439*	UBUS ABORT ACTIVATED (ABORT[0])	*NOT USED*	OUTPUT	*NC*

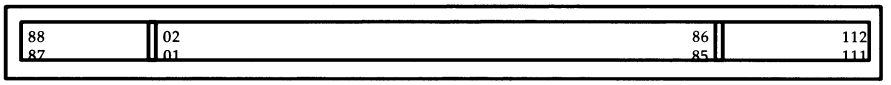
* CM518C System Board signal description shown in *italics*.

464-PIN BACKPLANE CONNECTOR, J02 (Contd)				
PIN	**DESCRIPTION**		**FUNCTION**	
440*	UBUS CACHE ABLE (CABLE[0])	*PBUS DATA ACKNOWLEDGE (UDTACK[0])*	INPUT/OUTPUT	*OUTPUT*
441*	UBUS EARLY PHYSICAL ADDRESS STROBE (EPAS[0])	*PBUS PHYSICAL ADDRESS STROBE (UPAS[0])*	OUTPUT	*INPUT*
442*	UBUS VIRTUAL ADDRESS STROBE (VAS[0])	*NOT USED*	OUTPUT	*NC*
443*	UBUS ACCESS STATUS BIT 1 (SAS1[1])	*PBUS CARD SELECT SLOT 1 (UPCS1[0])*	OUTPUT	*OUTPUT*
444*	UBUS ACCESS STATUS BIT 0 (SAS0[1])	*PBUS SLOT 3 OUTPUT ENABLE (C3ALOE[0])*	OUTPUT	*OUTPUT*
445*	UBUS DATA SIZE BIT 0 (CDSIZE0[1])	*PBUS DATA SIZE BIT 0 (UDSIZE0[1])*	OUTPUT	*INPUT*
446*	UBUS SYNCHRONOUS READY (SRDY[0])	*PBUS SLOT 2 MEMORY REQUEST (CPU2MEM[0])*	INPUT	*INPUT*
447	+5V (VCC)		POWER	
448*	UBUS CYCLE INITIATE (CYCLEI[0])	*PBUS SLOT 2 OUTPUT ENABLE (C2ALOE[0])*	OUTPUT	*OUTPUT*
449*	BUB CONNECTOR CHIP SELECT 3 (BCCS3[0])	*PBUS SLOT 1 OUTPUT ENABLE (C1ALOE[0])*	OUTPUT	*OUTPUT*
450	GROUND (GRD)		GROUND	
451*	UBUS DATA READY (DRDY[0])	*NOT USED*	OUTPUT	*NC*
452*	RECEIVED FAILURE (RFAIL[0])	*PBUS SLOT 1 MEMORY REQUEST (CPU1MEM[0])*	INPUT	*INPUT*
453	UBUS CHIP SELECT (CS1[0])	*PULLED UP*	OUTPUT	*OUTPUT*
454*	UBUS FAULT (FLT[0])	*PBUS FAULT (UFLT[0])*	INPUT	*OUTPUT*
455	ABORT PUSH BUTTON (ABUTTN[0])		INPUT	
456*	UBUS DATA SIZE BIT 1 (CDSIZE1[1])	*PBUS DATA SIZE BIT 1 (UDSIZE1[1])*	OUTPUT	*INPUT*
457*	UBUS DATA SHADOW (DSHAD[0])	*NOT USED*	OUTPUT	*NC*
458	GROUND (GRD)		GROUND	
459*	UBUS READ/WRITE (CR1W[0])	*PBUS READ/WRITE (UR1W[0])*	OUTPUT	*INPUT*
460*	UBUS DATA STROBE (DS[0])	*NOT USED*	OUTPUT	*NC*
461	POWER LED (GLED[0])		OUTPUT	
462	+5V (VCC)		POWER	
463	DIAGNOSTIC LED (ERLED[0])		OUTPUT	
464	+3.6V (VBAT)		INPUT	

* CM518C System Board signal description shown in *italics*.

LEGEND:

NC No Connection

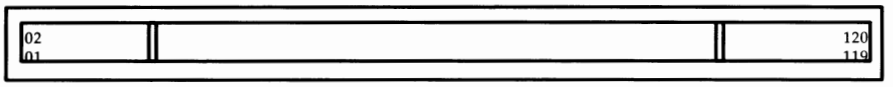


112-PIN FEATURE CARD CONNECTORS		
PIN	**DESCRIPTION**	**FUNCTION** (From Feature Card)
001	+12V (V12P)	POWER
002	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])	OUTPUT
003	-12V (V12N)	POWER
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	OUTPUT
007	PERIPHERAL CARD SELECT (PCS01[0]—PCS12[0], as applicable)	INPUT
008	PERIPHERAL REQUEST SYSTEM RESET (RQRST[0])	OUTPUT
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	+3.6V BACKUP BATTERY (VBKUP)	POWER
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	PERIPHERAL INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	OUTPUT
014	PERIPHERAL BUS FAULT (PFLT0)	INPUT/OUTPUT
015	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INTERRUPT ACKNOWLEDGE OUT 1 (PIAKO1[0])	OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUTT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	INPUT/OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INTERRUPT ACKNOWLEDGE OUT 0 (PIAKO0[0])	OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	INPUT/OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	INPUT/OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	READ-WRITE (PR[1]W[0])	INPUT/OUTPUT

112-PIN FEATURE CARD CONNECTORS (Contd)		
PIN	DESCRIPTION	FUNCTION (From Feature Card)
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	INPUT/OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	INPUT/OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	INPUT/OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	INPUT/OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	INPUT/OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	INPUT/OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	INPUT/OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	INPUT/OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	INPUT/OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	INPUT/OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	INPUT/OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	INPUT/OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	INPUT/OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	INPUT/OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	INPUT/OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	INPUT/OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	INPUT/OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	INPUT/OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	INPUT/OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	INPUT/OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	INPUT/OUTPUT
087	+5V (VCC)	POWER
088	PERIPHERAL SEQUENTIAL ACCESS (PSEQACC[0])	INPUT/OUTPUT
089	PERIPHERAL SYSTEMS SUPPORT ACCESS (PSSSA[0])	INPUT/OUTPUT
090	+5V (VCC)	POWER
091	GROUND	GROUND
092	GROUND	GROUND
093	SPARE	NC
094	SPARE	NC
095	SPARE	NC
096	SPARE	NC
097	SPARE	NC
098	SPARE	NC
099	GROUND	GROUND
100	RESERVED	NC
101	RESERVED	NC
102	GROUND	GROUND
103	RESERVED	NC
104	RESERVED	NC
105	RESERVED	NC
106	RESERVED	NC
107	+5V (VCC)	POWER
108	RESERVED	NC
109	RESERVED	NC
110	+5V (VCC)	POWER
111	RESERVED	NC
112	RESERVED	NC

LEGEND:

NC No Connection

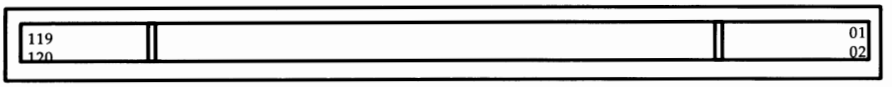


120-PIN CM523 MEMORY CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	GROUND (GRD)	GROUND
002	+5V (VCC)	POWER
003	NOT USED	NC
004	NOT USED	NC
005	NOT USED	NC
006	NOT USED	NC
007	GROUND (GRD)	GROUND
008	GROUND (GRD)	GROUND
009	ROW ADDRESS STROBE (RAS[0])	OUTPUT
010	WRITE ENABLE (WE[0])	OUTPUT
011	GROUND (GRD)	GROUND
012	GROUND (GRD)	GROUND
013	MEMORY CYCLE STATUS G[0]	OUTPUT
014	BANK ENABLE 1 (BANKEN1[0])	OUTPUT
015	BANK ENABLE 2 (BANKEN2[0])	OUTPUT
016	BANK ENABLE 0 (BANKEN0[0])	OUTPUT
017	GROUND (GRD)	GROUND
018	GROUND (GRD)	GROUND
019	COLUMN ADDRESS STROBE 1 (CAS1[0])	OUTPUT
020	COLUMN ADDRESS STROBE 3 (CAS3[0])	OUTPUT
021	COLUMN ADDRESS STROBE 0 (CAS0[0])	OUTPUT
022	COLUMN ADDRESS STROBE 2 (CAS2[0])	OUTPUT
023	+5V (VCC)	POWER
024	+5V (VCC)	POWER
025	SIZE BIT 0 (SIZE0[0])	INPUT/OUTPUT
026	NOT USED	NC
027	SIZE BIT 1 (SIZE1[0])	INPUT/OUTPUT
028	SLOT EQUIPPED (ECCEQP[0])	OUTPUT
029	LARGER SIZED MEMORY BOARD (BIGMEM[0])	OUTPUT
030	NOT USED	NC
031	GROUND (GRD)	GROUND
032	GROUND (GRD)	GROUND
033	MULTIPLEXED ADDRESS BIT 00 (MUXA00[1])	OUTPUT
034	MULTIPLEXED ADDRESS BIT 03 (MUXA03[1])	OUTPUT
035	GROUND (GRD)	GROUND
036	GROUND (GRD)	GROUND
037	MULTIPLEXED ADDRESS BIT 01 (MUXA01[1])	OUTPUT
038	MULTIPLEXED ADDRESS BIT 02 (MUXA02[1])	OUTPUT
039	GROUND (GRD)	GROUND
040	GROUND (GRD)	GROUND
041	MULTIPLEXED ADDRESS BIT 04 (MUXA04[1])	OUTPUT
042	MULTIPLEXED ADDRESS BIT 07 (MUXA07[1])	OUTPUT
043	+5V (VCC)	POWER
044	+5V (VCC)	POWER
045	MULTIPLEXED ADDRESS BIT 05 (MUXA05[1])	OUTPUT
046	MULTIPLEXED ADDRESS BIT 06 (MUXA06[1])	OUTPUT
047	GROUND (GRD)	GROUND
048	GROUND (GRD)	GROUND
049	MULTIPLEXED ADDRESS BIT 08 (MUXA08[1])	OUTPUT
050	MULTIPLEXED ADDRESS BIT 11 (MUXA11[1]) (IF USED)	OUTPUT
051	GROUND (GRD)	GROUND
052	GROUND (GRD)	GROUND
053	MULTIPLEXED ADDRESS BIT 09 (MUXA09[1]) (IF USED)	OUTPUT
054	MULTIPLEXED ADDRESS BIT 10 (MUXA10[1]) (IF USED)	OUTPUT
055	GROUND (GRD)	GROUND
056	+5V (VCC)	POWER
057	MULTIPLEXED ADDRESS BIT 12 (MUXA12[1]) (IF USED)	OUTPUT
058	NOT USED	NC

120-PIN CM523 MEMORY CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
059	GROUND (GRD)	GROUND
060	GROUND (GRD)	GROUND
061	MEMORY DATA BIT 31 (MD31[1])	INPUT/OUTPUT
062	MEMORY DATA BIT 30 (MD30[1])	INPUT/OUTPUT
063	GROUND (GRD)	GROUND
064	MEMORY DATA BIT 28 (MD28[1])	INPUT/OUTPUT
065	MEMORY DATA BIT 29 (MD29[1])	INPUT/OUTPUT
066	MEMORY DATA BIT 26 (MD26[1])	INPUT/OUTPUT
067	MEMORY DATA BIT 27 (MD27[1])	INPUT/OUTPUT
068	GROUND (GRD)	GROUND
069	MEMORY DATA BIT 25 (MD25[1])	INPUT/OUTPUT
070	MEMORY DATA BIT 24 (MD24[1])	INPUT/OUTPUT
071	GROUND (GRD)	GROUND
072	MEMORY DATA BIT 22 (MD22[1])	INPUT/OUTPUT
073	MEMORY DATA BIT 23 (MD23[1])	INPUT/OUTPUT
074	MEMORY DATA BIT 20 (MD20[1])	INPUT/OUTPUT
075	MEMORY DATA BIT 21 (MD21[1])	INPUT/OUTPUT
076	+5V (VCC)	POWER
077	MEMORY DATA BIT 19 (MD19[1])	INPUT/OUTPUT
078	MEMORY DATA BIT 18 (MD18[1])	INPUT/OUTPUT
079	+5V (VCC)	POWER
080	MEMORY DATA BIT 16 (MD16[1])	INPUT/OUTPUT
081	MEMORY DATA BIT 17 (MD17[1])	INPUT/OUTPUT
082	MEMORY DATA BIT 14 (MD14[1])	INPUT/OUTPUT
083	MEMORY DATA BIT 15 (MD15[1])	INPUT/OUTPUT
084	GROUND (GRD)	GROUND
085	MEMORY DATA BIT 13 (MD13[1])	INPUT/OUTPUT
086	MEMORY DATA BIT 12 (MD12[1])	INPUT/OUTPUT
087	GROUND (GRD)	GROUND
088	MEMORY DATA BIT 10 (MD10[1])	INPUT/OUTPUT
089	MEMORY DATA BIT 11 (MD11[1])	INPUT/OUTPUT
090	MEMORY DATA BIT 08 (MD08[1])	INPUT/OUTPUT
091	MEMORY DATA BIT 09 (MD09[1])	INPUT/OUTPUT
092	GROUND (GRD)	GROUND
093	MEMORY DATA BIT 07 (MD07[1])	INPUT/OUTPUT
094	MEMORY DATA BIT 06 (MD06[1])	INPUT/OUTPUT
095	GROUND (GRD)	GROUND
096	MEMORY DATA BIT 04 (MD04[1])	INPUT/OUTPUT
097	MEMORY DATA BIT 05 (MD05[1])	INPUT/OUTPUT
098	MEMORY DATA BIT 02 (MD02[1])	INPUT/OUTPUT
099	MEMORY DATA BIT 03 (MD03[1])	INPUT/OUTPUT
100	+5V (VCC)	POWER
101	MEMORY DATA BIT 01 (MD01[1]	INPUT/OUTPUT
102	MEMORY DATA BIT 00 (MD00[1]	INPUT/OUTPUT
103	+5V (VCC)	POWER
104	MEMORY CHECK BIT (MCB10[1])	NPUT/OUTPUT
105	MEMORY CHECK BIT (MCB11[1])	NPUT/OUTPUT
106	MEMORY CHECK BIT (MCB08[1])	NPUT/OUTPUT
107	MEMORY CHECK BIT (MCB09[1])	NPUT/OUTPUT
108	GROUND (GRD)	GROUND
109	MEMORY CHECK BIT (MCB07[1])	NPUT/OUTPUT
110	MEMORY CHECK BIT (MCB06[1])	NPUT/OUTPUT
111	GROUND (GRD)	GROUND
112	MEMORY CHECK BIT (MCB04[1])	NPUT/OUTPUT
113	MEMORY CHECK BIT (MCB05[1])	NPUT/OUTPUT
114	MEMORY CHECK BIT (MCB02[1])	NPUT/OUTPUT
115	MEMORY CHECK BIT (MCB03[1])	NPUT/OUTPUT
116	GROUND (GRD)	GROUND
117	MEMORY CHECK BIT (MCB01[1])	NPUT/OUTPUT
118	MEMORY CHECK BIT (MCB00[1])	NPUT/OUTPUT
119	GROUND (GRD)	GROUND
120	+5V (VCC)	POWER

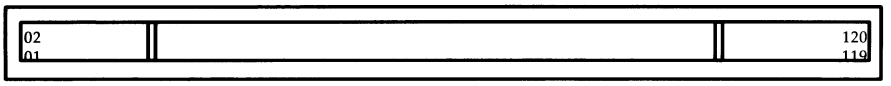
LEGEND:

NC No Connection



120-PIN BUFFERED MICROBUS (BUB) EDGE CONNECTIONS		
PIN	DESCRIPTION	FUNCTION (From System Board)
001	BUB CONNECTOR INHIBIT SLOT 0 (BINHIB0[0])	OUTPUT
002	GROUND (GRD)	GROUND
003	OPERATIONAL INTERRUPT LEVEL 15 (OPINT15[0])	INPUT
004	BUB INTERRUPT LEVEL 10 (BINT010[0])	INPUT
005	BUB INTERRUPT LEVEL 12 (BINT012[0])	INPUT
006	+5V (VCC)	POWER
007	BUB INTERRUPT LEVEL 14 (BINT014[0])	INPUT
008	GROUND (GRD)	GROUND
009	BUB FAILURE (BFAIL[0])	INPUT
010	BUB DATA BIT 31 (BD31[1])	INPUT/OUTPUT
011	BUB DATA BIT 30 (BD30[1])	INPUT/OUTPUT
012	BUB DATA BIT 29 (BD29[1])	INPUT/OUTPUT
013	BUB DATA BIT 28 (BD28[1])	INPUT/OUTPUT
014	GROUND (GRD)	GROUND
015	+5V (VCC)	POWER
016	BUB DATA BIT 26 (BD26[1])	INPUT/OUTPUT
017	BUB DATA BIT 27 (BD27[1])	INPUT/OUTPUT
018	BUB DATA BIT 25 (BD25[1])	INPUT/OUTPUT
019	BUB DATA BIT 24 (BD24[1])	INPUT/OUTPUT
020	GROUND (GRD)	GROUND
021	BUB DATA BIT 22 (BD22[1])	INPUT/OUTPUT
022	BUB DATA BIT 23 (BD23[1])	INPUT/OUTPUT
023	BUB DATA BIT 21 (BD21[1])	INPUT/OUTPUT
024	BUB DATA BIT 20 (BD20[1])	INPUT/OUTPUT
025	BUB DATA BIT 18 (BD18[1])	INPUT/OUTPUT
026	BUB DATA BIT 19 (BD19[1])	INPUT/OUTPUT
027	GROUND (GRD)	GROUND
028	BUB DATA BIT 17 (BD17[1])	INPUT/OUTPUT
029	BUB DATA BIT 16 (BD16[1])	INPUT/OUTPUT
030	BUB DATA BIT 14 (BD14[1])	INPUT/OUTPUT
031	BUB DATA BIT 15 (BD15[1])	INPUT/OUTPUT
032	+5V (VCC)	POWER
033	BUB DATA BIT 12 (BD12[1])	INPUT/OUTPUT
034	BUB DATA BIT 13 (BD13[1])	INPUT/OUTPUT
035	+12V (V12P)	POWER
036	BUB DATA BIT 11 (BD11[1])	INPUT/OUTPUT
037	BUB DATA BIT 10 (BD10[1])	INPUT/OUTPUT
038	-12V (V12N)	POWER
039	GROUND (GRD)	GROUND
040	BUB DATA BIT 08 (BD08[1])	INPUT/OUTPUT
041	BUB DATA BIT 09 (BD09[1])	INPUT/OUTPUT
042	BUB DATA BIT 07 (BD07[1])	INPUT/OUTPUT
043	BUB DATA BIT 06 (BD06[1])	INPUT/OUTPUT
044	BUB DATA BIT 05 (BD05[1])	INPUT/OUTPUT
045	BUB DATA BIT 04 (BD04[1])	INPUT/OUTPUT
046	GROUND (GRD)	GROUND
047	BUB DATA BIT 03 (BD03[1])	INPUT/OUTPUT
048	BUB DATA BIT 02 (BD02[1])	INPUT/OUTPUT
049	BUB DATA BIT 00 (BD00[1])	INPUT/OUTPUT
050	BUB DATA BIT 01 (BD01[1])	INPUT/OUTPUT
051	GROUND (GRD)	GROUND
052	BUB DATA PARITY BIT 0 (BDP0[1])	INPUT/OUTPUT
053	BUB DATA PARITY BIT 1 (BDP1[1])	INPUT/OUTPUT
054	BUB DATA PARITY BIT 3 (BDP3[1])	INPUT/OUTPUT
055	BUB DATA PARITY BIT 2 (BDP2[1])	INPUT/OUTPUT
056	+5V (VCC)	POWER

120-PIN BUFFERED MICROBUS (BUB) EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION (From System Board)
057	BUB ADDRESS BIT 26 (BA26[1])	INPUT/OUTPUT
058	BUB ADDRESS BIT 25 (BA25[1])	INPUT/OUTPUT
059	BUB ADDRESS BIT 24 (BA24[1])	INPUT/OUTPUT
060	BUB ADDRESS BIT 23 (BA23[1])	INPUT/OUTPUT
061	BUB ADDRESS BIT 22 (BA22[1])	INPUT/OUTPUT
062	BUB ADDRESS BIT 21 (BA21[1])	INPUT/OUTPUT
063	GROUND (GRD)	GROUND
064	BUB ADDRESS BIT 20 (BA20[1])	INPUT/OUTPUT
065	BUB ADDRESS BIT 12 (BA12[1])	INPUT/OUTPUT
066	BUB ADDRESS BIT 19 (BA19[1])	INPUT/OUTPUT
067	BUB ADDRESS BIT 18 (BA18[1])	INPUT/OUTPUT
068	BUB ADDRESS BIT 17 (BA17[1])	INPUT/OUTPUT
069	BUB ADDRESS BIT 16 (BA16[1])	INPUT/OUTPUT
070	GROUND (GRD)	GROUND
071	BUB ADDRESS BIT 15 (BA15[1])	INPUT/OUTPUT
072	BUB ADDRESS BIT 14 (BA14[1])	INPUT/OUTPUT
073	GROUND (GRD)	GROUND
074	BUB ADDRESS BIT 13 (BA13[1])	INPUT/OUTPUT
075	+5V (VCC)	POWER
076	SYSTEM RESET (SYSRST[0])	OUTPUT
077	REQUEST SYSTEM RESET (RQRST[0])	INPUT
078	BUB ADDRESS BIT 27 (BA27[1])	INPUT/OUTPUT
079	BUB BUSY (BUSY[0])	INPUT/OUTPUT
080	GROUND (GRD)	GROUND
081	BUB ADDRESS BIT 11 (BA11[1])	INPUT/OUTPUT
082	BUB ADDRESS BIT 10 (BA10[1])	INPUT/OUTPUT
083	BUB ADDRESS BIT 09 (BA09[1])	INPUT/OUTPUT
084	BUB ADDRESS BIT 08 (BA08[1])	INPUT/OUTPUT
085	BUB ADDRESS BIT 07 (BA07[1])	INPUT/OUTPUT
086	BUB ADDRESS BIT 06 (BA06[1])	INPUT/OUTPUT
087	GROUND (GRD)	GROUND
088	BUB ADDRESS BIT 05 (BA05[1])	INPUT/OUTPUT
089	GROUND (GRD)	GROUND
090	BUB ADDRESS BIT 04 (BA04[1])	INPUT/OUTPUT
091	BUB ADDRESS BIT 03 (BA03[1])	INPUT/OUTPUT
092	BUB ADDRESS BIT 02 (BA02[1])	INPUT/OUTPUT
093	BUB ADDRESS BIT 01 (BA01[1])	INPUT/OUTPUT
094	+5V (VCC)	POWER
095	BUB ADDRESS BIT 00 (BA00[1])	INPUT/OUTPUT
096	BUB ADDRESS PARITY BIT 0 (BAP0[1])	INPUT/OUTPUT
097	BUB ADDRESS PARITY BIT 2 (BAP2[1])	INPUT/OUTPUT
098	BUB ADDRESS PARITY BIT 1 (BAP1[1])	INPUT/OUTPUT
099	GROUND (GRD)	GROUND
100	BUB ADDRESS PARITY BIT 3 (BAP3[1])	INPUT/OUTPUT
101	BUB READ/WRITE (BR1W0)	INPUT/OUTPUT
102	+5V (VCC)	POWER
103	BUB CONNECTOR CHIP SELECT 0 (BCCS0[0])	OUTPUT
104	GROUND (GRD)	GROUND
105	BUB DATA SIZE BIT 0 (BDSIZE0[1])	INPUT/OUTPUT
106	BUB DATA SIZE BIT 1 (BDSIZE1[1])	INPUT/OUTPUT
107	BUB SEQUENTIAL ACCESS (BSEQACC[0])	INPUT
108	BUB PERIPHERAL PARITY (BPCHECK[0])	INPUT
109	BUB BUS REQUEST (BUBRQ[0])	INPUT
110	SANITY TIMER TIMEOUT (SANT[0])	OUTPUT
111	+5V (VCC)	POWER
112	BUB FAULT (BFLT[0])	INPUT/OUTPUT
113	BUB GRANTED SLOT (BUBGT[0])	OUTPUT
114	BUB BYPASS MODE ACCESS (BYPASS[0])	OUTPUT
115	BUB DATA STROBE (BDS[0])	INPUT/OUTPUT
116	BUB ADDRESS STROBE (BAS[0])	INPUT/OUTPUT
117	BUB DATA ACKNOWLEDGE (BDTCK[0])	INPUT/OUTPUT
118	GROUND (GRD)	GROUND
119	NOT USED (BSPARE1)	INPUT/OUTPUT
120	NOT USED (BSPARE2)	INPUT/OUTPUT

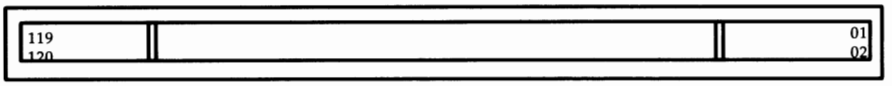


120-PIN VCACHE EDGE CONNECTIONS		
PIN	DESCRIPTION	FUNCTION (From VCACHE)
001	UBUS DATA STROBE (DS[0])	INPUT
002	UBUS READ/WRITE (CR1W0)	INPUT
003	GROUND (GRD)	GROUND
004	UBUS DATA SHADOW (DSHAD[0])	INPUT
005	UBUS DATA SIZE BIT 1 (CDSIZE1[1])	INPUT
006	UBUS FAULT (FLT[0])	OUTPUT
007	UBUS CARD SELECT (CS1[0])	INPUT
008	GROUND (GRD)	GROUND
009	UBUS FAILURE (FAIL[0])	OUTPUT
010	UBUS DATA READY (DRDY[0])	OUTPUT
011	UBUS CYCLE INITIATE (CYCLEI[0])	INPUT
012	UBUS SYNCHRONOUS READY (SRDY[0])	OUTPUT
013	UBUS DATA SIZE BIT 0 (CDSIZE0[1])	INPUT
014	UBUS ACCESS STATUS BIT 0 (SAS0[1])	INPUT
015	+5V (VCC)	POWER
016	ACCESS STATUS BIT 1 (SAS1[1])	INPUT
017	UBUS VIRTUAL ADDRESS STROBE (VAS[0])	INPUT
018	UBUS EARLY PHYSICAL ADDRESS STROBE (EPAS[0])	INPUT
019	UBUS CACHE ABLE (CABLE[0])	INPUT
020	GROUND (GRD)	GROUND
021	UBUS ABORT ACTIVATED (ABORT[0])	INPUT
022	UBUS DATA ACKNOWLEDGE (DTACK[0])	OUTPUT
023	UBUS ACCESS STATUS BIT 2 (SAS2[1])	INPUT
024	UBUS ACCESS STATUS BIT 3 (SAS3[1])	INPUT
025	UBUS VIRTUAL ADDRESS (BY CPU) (VAD[0])	INPUT
026	UBUS COPROCESSOR DONE (DONE[0])	OUTPUT
027	GROUND (GRD)	GROUND
028	UBUS BUS REQUEST (BUSRQ[0])	OUTPUT
029	UBUS EXECUTION MODE 1 (XMD1[1])	INPUT
030	UBUS VIRTUAL CACHE HIT (VCHIT[0])	OUTPUT
031	OPERATIONAL INTERRUPT LEVEL 15 (OPINT15[0])	OUTPUT
032	+5V (VCC)	POWER
033	SANITY TIMER TIMEOUT (SANT[0])	INPUT
034	UBUS GRANTED (BUSGT[0])	INPUT
035	+12V (V12P)	POWER
036	NOT USED	NC
037	CLOCK 34 (CLK34[1])	INPUT
038	-12V (V12N)	POWER
039	GROUND (GRD)	GROUND
040	UBUS SEQUENTIAL ACCESS (CSEQACC[0])	OUTPUT
041	CLOCK 23 (CLK23[1])	INPUT
042	SYSTEM RESET (SYSRST[0])	INPUT
043	NOT USED	NC
044	REQUEST SYSTEM RESET (RQRST[0])	OUTPUT
045	UBUS ADDRESS BIT 31 (CA31[1])	INPUT
046	UBUS ADDRESS BIT 30 (CA30[1])	INPUT
047	UBUS ADDRESS BIT 29 (CA29[1])	INPUT
048	UBUS ADDRESS BIT 28 (CA28[1])	INPUT
049	UBUS ADDRESS BIT 27 (CA27[1])	INPUT
050	UBUS ADDRESS BIT 26 (CA26[1])	INPUT
051	GROUND (GRD)	GROUND
052	UBUS ADDRESS BIT 25 (CA25[1])	INPUT
053	UBUS ADDRESS BIT 24 (CA24[1])	INPUT
054	UBUS ADDRESS BIT 23 (CA23[1])	INPUT
055	UBUS ADDRESS BIT 22 (CA22[1])	INPUT
056	+5V (VCC)	POWER
057	UBUS ADDRESS BIT 21 (CA21[1])	INPUT
058	UBUS ADDRESS BIT 20 (CA20[1])	INPUT

120-PIN VCACHE EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION (From VCACHE)
059	UBUS ADDRESS BIT 19 (CA19[1])	INPUT
060	UBUS ADDRESS BIT 18 (CA18[1])	INPUT
061	UBUS ADDRESS BIT 17 (CA17[1])	INPUT
062	UBUS ADDRESS BIT 16 (CA16[1])	INPUT
063	GROUND (GRD)	GROUND
064	UBUS ADDRESS BIT 15 (CA15[1])	INPUT
065	UBUS ADDRESS BIT 14 (CA14[1])	INPUT
066	UBUS ADDRESS BIT 13 (CA13[1])	INPUT
067	UBUS ADDRESS BIT 12 (CA12[1])	INPUT
068	UBUS ADDRESS BIT 11 (CA11[1])	INPUT
069	UBUS ADDRESS BIT 10 (CA10[1])	INPUT
070	GROUND (GRD)	GROUND
071	UBUS ADDRESS BIT 09 (CA09[1])	INPUT
072	UBUS ADDRESS BIT 08 (CA08[1])	INPUT
073	UBUS ADDRESS BIT 07 (CA07[1])	INPUT
074	UBUS ADDRESS BIT 06 (CA06[1])	INPUT
075	+5V (VCC)	POWER
076	UBUS ADDRESS BIT 05 (CA05[1])	INPUT
077	UBUS ADDRESS BIT 04 (CA04[1])	INPUT
078	UBUS ADDRESS BIT 03 (CA03[1])	INPUT
079	UBUS ADDRESS BIT 02 (CA02[1])	INPUT
080	UBUS ADDRESS BIT 01 (CA01[1])	INPUT
081	UBUS ADDRESS BIT 00 (CA00[1])	INPUT
082	GROUND (GRD)	GROUND
083	UBUS DATA BIT 31 (CD31[1])	INPUT/OUTPUT
084	UBUS DATA BIT 30 (CD30[1])	INPUT/OUTPUT
085	UBUS DATA BIT 29 (CD29[1])	INPUT/OUTPUT
086	UBUS DATA BIT 28 (CD28[1])	INPUT/OUTPUT
087	GROUND (GRD)	GROUND
088	UBUS DATA BIT 27 (CD27[1])	INPUT/OUTPUT
089	UBUS DATA BIT 26 (CD26[1])	INPUT/OUTPUT
090	UBUS DATA BIT 25 (CD25[1])	INPUT/OUTPUT
091	UBUS DATA BIT 24 (CD24[1])	INPUT/OUTPUT
092	UBUS DATA BIT 23 (CD23[1])	INPUT/OUTPUT
093	UBUS DATA BIT 22 (CD22[1])	INPUT/OUTPUT
094	+5V (VCC)	POWER
095	UBUS DATA BIT 21 (CD21[1])	INPUT/OUTPUT
096	UBUS DATA BIT 20 (CD20[1])	INPUT/OUTPUT
097	UBUS DATA BIT 19 (CD19[1])	INPUT/OUTPUT
098	UBUS DATA BIT 18 (CD18[1])	INPUT/OUTPUT
099	GROUND (GRD)	GROUND
100	UBUS DATA BIT 17 (CD17[1])	INPUT/OUTPUT
101	UBUS DATA BIT 16 (CD16[1])	INPUT/OUTPUT
102	UBUS DATA BIT 15 (CD15[1])	INPUT/OUTPUT
103	UBUS DATA BIT 14 (CD14[1])	INPUT/OUTPUT
104	UBUS DATA BIT 13 (CD13[1])	INPUT/OUTPUT
105	UBUS DATA BIT 12 (CD12[1])	INPUT/OUTPUT
106	GROUND (GRD)	GROUND
107	UBUS DATA BIT 11 (CD11[1])	INPUT/OUTPUT
108	UBUS DATA BIT 10 (CD10[1])	INPUT/OUTPUT
109	UBUS DATA BIT 09 (CD09[1])	INPUT/OUTPUT
110	UBUS DATA BIT 08 (CD08[1])	INPUT/OUTPUT
111	+5V (VCC)	POWER
112	UBUS DATA BIT 07 (CD07[1])	INPUT/OUTPUT
113	UBUS DATA BIT 06 (CD06[1])	INPUT/OUTPUT
114	UBUS DATA BIT 05 (CD05[1])	INPUT/OUTPUT
115	UBUS DATA BIT 04 (CD04[1])	INPUT/OUTPUT
116	UBUS DATA BIT 03 (CD03[1])	INPUT/OUTPUT
117	UBUS DATA BIT 02 (CD02[1])	INPUT/OUTPUT
118	GROUND (GRD)	GROUND
119	UBUS DATA BIT 01 (CD01[1])	INPUT/OUTPUT
120	UBUS DATA BIT 00 (CD00[1])	INPUT/OUTPUT

LEGEND:

NC No Connection



120-PIN PROCESSING BUS (PBUS) EDGE CONNECTIONS		
PIN	DESCRIPTION	FUNCTION (From System Board)
001	BUB CONNECTOR INHIBIT SLOT 0 (BINHIB0[0])	OUTPUT
002	GROUND (GRD)	GROUND
003	OPERATIONAL INTERRUPT LEVEL 15 (OPINT15[0])	INPUT
004	BUB INTERRUPT LEVEL 10 (UINT10[0])	INPUT
005	BUB INTERRUPT LEVEL 12 (UINT12[0])	INPUT
006	+5V (VCC)	POWER
007	BUB INTERRUPT LEVEL 14 (UINT14[0])	INPUT
008	GROUND (GRD)	GROUND
009	BUB PHYSICAL ADDRESS STROBE (UPAS[0])	INPUT
010	BUB DATA BIT 31 (BD31[1])	INPUT/OUTPUT
011	BUB DATA BIT 30 (BD30[1])	INPUT/OUTPUT
012	BUB DATA BIT 29 (BD29[1])	INPUT/OUTPUT
013	BUB DATA BIT 28 (BD28[1])	INPUT/OUTPUT
014	GROUND (GRD)	GROUND
015	+5V (VCC)	POWER
016	BUB DATA BIT 26 (BD26[1])	INPUT/OUTPUT
017	BUB DATA BIT 27 (BD27[1])	INPUT/OUTPUT
018	BUB DATA BIT 25 (BD25[1])	INPUT/OUTPUT
019	BUB DATA BIT 24 (BD24[1])	INPUT/OUTPUT
020	GROUND (GRD)	GROUND
021	BUB DATA BIT 22 (BD22[1])	INPUT/OUTPUT
022	BUB DATA BIT 23 (BD23[1])	INPUT/OUTPUT
023	BUB DATA BIT 21 (BD21[1])	INPUT/OUTPUT
024	BUB DATA BIT 20 (BD20[1])	INPUT/OUTPUT
025	BUB DATA BIT 18 (BD18[1])	INPUT/OUTPUT
026	BUB DATA BIT 19 (BD19[1])	INPUT/OUTPUT
027	GROUND (GRD)	GROUND
028	BUB DATA BIT 17 (BD17[1])	INPUT/OUTPUT
029	BUB DATA BIT 16 (BD16[1])	INPUT/OUTPUT
030	BUB DATA BIT 14 (BD14[1])	INPUT/OUTPUT
031	BUB DATA BIT 15 (BD15[1])	INPUT/OUTPUT
032	+5V (VCC)	POWER
033	BUB DATA BIT 12 (BD12[1])	INPUT/OUTPUT
034	BUB DATA BIT 13 (BD13[1])	INPUT/OUTPUT
035	+12V (V12P)	POWER
036	BUB DATA BIT 11 (BD11[1])	INPUT/OUTPUT
037	BUB DATA BIT 10 (BD10[1])	INPUT/OUTPUT
038	-12V (V12N)	POWER
039	GROUND (GRD)	GROUND
040	BUB DATA BIT 08 (BD08[1])	INPUT/OUTPUT
041	BUB DATA BIT 09 (BD09[1])	INPUT/OUTPUT
042	BUB DATA BIT 07 (BD07[1])	INPUT/OUTPUT
043	BUB DATA BIT 06 (BD06[1])	INPUT/OUTPUT
044	BUB DATA BIT 05 (BD05[1])	INPUT/OUTPUT
045	BUB DATA BIT 04 (BD04[1])	INPUT/OUTPUT
046	GROUND (GRD)	GROUND
047	BUB DATA BIT 03 (BD03[1])	INPUT/OUTPUT
048	BUB DATA BIT 02 (BD02[1])	INPUT/OUTPUT
049	BUB DATA BIT 00 (BD00[1])	INPUT/OUTPUT
050	BUB DATA BIT 01 (BD01[1])	INPUT/OUTPUT
051	GROUND (GRD)	GROUND
052	NOT USED	NC
053	NOT USED	NC
054	NOT USED	NC
055	NOT USED	NC
056	+5V (VCC)	POWER
057	BUB ADDRESS BIT 26 (BA26[1])	INPUT/OUTPUT
058	BUB ADDRESS BIT 25 (BA25[1])	INPUT/OUTPUT

120-PIN PROCESSING BUS (PBUS) EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION (From System Board)
059	BUB ADDRESS BIT 24 (BA24[1])	INPUT/OUTPUT
060	BUB ADDRESS BIT 23 (BA23[1])	INPUT/OUTPUT
061	BUB ADDRESS BIT 22 (BA22[1])	INPUT/OUTPUT
062	BUB ADDRESS BIT 21 (BA21[1])	INPUT/OUTPUT
063	GROUND (GRD)	GROUND
064	BUB ADDRESS BIT 20 (BA20[1])	INPUT/OUTPUT
065	BUB ADDRESS BIT 12 (BA12[1])	INPUT/OUTPUT
066	BUB ADDRESS BIT 19 (BA19[1])	INPUT/OUTPUT
067	BUB ADDRESS BIT 18 (BA18[1])	INPUT/OUTPUT
068	BUB ADDRESS BIT 17 (BA17[1])	INPUT/OUTPUT
069	BUB ADDRESS BIT 16 (BA16[1])	INPUT/OUTPUT
070	GROUND (GRD)	GROUND
071	BUB ADDRESS BIT 15 (BA15[1])	INPUT/OUTPUT
072	BUB ADDRESS BIT 14 (BA14[1])	INPUT/OUTPUT
073	GROUND (GRD)	GROUND
074	BUB ADDRESS BIT 13 (BA13[1])	INPUT/OUTPUT
075	+5V (VCC)	POWER
076	SYSTEM RESET (SYSRST[0])	OUTPUT
077	REQUEST SYSTEM RESET (RQRST[0])	INPUT
078	BUB ADDRESS BIT 27 (BA27[1])	INPUT/OUTPUT
079	PBUS INTERLOCK (UINTLK[0])	INPUT
080	GROUND (GRD)	GROUND
081	BUB ADDRESS BIT 11 (BA11[1])	INPUT/OUTPUT
082	BUB ADDRESS BIT 10 (BA10[1])	INPUT/OUTPUT
083	BUB ADDRESS BIT 09 (BA09[1])	INPUT/OUTPUT
084	BUB ADDRESS BIT 08 (BA08[1])	INPUT/OUTPUT
085	BUB ADDRESS BIT 07 (BA07[1])	INPUT/OUTPUT
086	BUB ADDRESS BIT 06 (BA06[1])	INPUT/OUTPUT
087	GROUND (GRD)	GROUND
088	BUB ADDRESS BIT 05 (BA05[1])	INPUT/OUTPUT
089	GROUND (GRD)	GROUND
090	BUB ADDRESS BIT 04 (BA04[1])	INPUT/OUTPUT
091	BUB ADDRESS BIT 03 (BA03[1])	INPUT/OUTPUT
092	BUB ADDRESS BIT 02 (BA02[1])	INPUT/OUTPUT
093	BUB ADDRESS BIT 01 (BA01[1])	INPUT/OUTPUT
094	+5V (VCC)	POWER
095	BUB ADDRESS BIT 00 (BA00[1])	INPUT/OUTPUT
096	NOT USED	NC
097	NOT USED	NC
098	NOT USED	NC
099	GROUND (GRD)	GROUND
100	NOT USED	NC
101	PBUS READ/WRITE (UR1W0)	INPUT
102	+5V (VCC)	POWER
103	PBUS CONNECTOR CHIP SELECT (UPCS[0])	OUTPUT
104	GROUND (GRD)	GROUND
105	PBUS DATA SIZE BIT 0 (UDSIZE0[1])	INPUT/OUTPUT
106	PBUS DATA SIZE BIT 1 (UDSIZE1[1])	INPUT/OUTPUT
107	PBUS ADDRESS STROBE (UAS[0])	INPUT
108	BUB PERIPHERAL PARITY (BPCHECK[0])	INPUT
109	PBUS MEMORY ACCESS (CPUMEM[0])	INPUT
110	CPU LATCH (CPULTCH[1])	OUTPUT
111	+5V (VCC)	POWER
112	PBUS FAULT (UFLT[0])	OUTPUT
113	PBUS OUTPUT ENABLE (CBALOE[0])	OUTPUT
114	PBUS DATA ACKNOWLEDGE (UDTCK[0])	OUTPUT
115	PBUS DATA STROBE (BDS[0])	INPUT/OUTPUT
116	BUB ADDRESS STROBE (BAS[0])	OUTPUT
117	BUB DATA ACKNOWLEDGE (BDTCK[0])	INPUT
118	GROUND (GRD)	GROUND
119	NOT USED	NC
120	NOT USED	NC

LEGEND:

NC No Connection

34-PIN FLOPPY DISK CONNECTOR, J10		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND	GROUND
2	FLOPPY LOW RPM (FLOW)	OUTPUT
3	GROUND	GROUND
4	NOT USED (FSPARE)	NC
5	GROUND	GROUND
6	FLOPPY DRIVE SELECT 3 (FDS3[0])	OUTPUT
7	GROUND	GROUND
8	INDEX (FINDEX[0])	INPUT
9	GROUND	GROUND
10	FLOPPY DRIVE SELECT 0 (FDS0[0])	OUTPUT
11	GROUND	GROUND
12	FLOPPY DRIVE SELECT 1 (FDS1[0])	OUTPUT
13	GROUND	GROUND
14	FLOPPY DRIVE SELECT 2 (FDS2[0])	OUTPUT
15	GROUND	GROUND
16	MOTOR ON (FMOTON[0])	OUTPUT
17	GROUND	GROUND
18	FLOPPY DIRECTION SELECT (FDIRC[0])	OUTPUT
19	GROUND	GROUND
20	FLOPPY STEP (FSTEP[0])	OUTPUT
21	GROUND	GROUND
22	WRITE DATA (FWDATA[0])	OUTPUT
23	GROUND	GROUND
24	FLOPPY WRITE GATE (FWGATE[0])	OUTPUT
25	GROUND	GROUND
26	FLOPPY TRACK 0 (FTR0[0])	INPUT
27	GROUND	GROUND
28	FLOPPY WRITE PROTECT (FWRTPRT[0])	INPUT
29	GROUND	GROUND
30	READ DATA (FRDATA[0])	INPUT
31	GROUND	GROUND
32	FLOPPY SIDE SELECT (FSSEL[0])	OUTPUT
33	GROUND	GROUND
34	FLOPPY READY (FRDY[0])	INPUT

LEGEND:

NC No Connection

4-PLUG POWER CONNECTORS		
PIN	DESCRIPTION	FUNCTION
1,2,3,4	+5 V (VCC)	POWER

5-PLUG GROUND CONNECTORS		
PIN	DESCRIPTION	FUNCTION
1,2,3,4,5	GROUND (GRD)	GROUND

10-PIN POWER CONTROL CONNECTOR		
PIN	DESCRIPTION	FUNCTION
1,2	+12V RS-232C SUPPLY (V12P)	POWER
3,4	GROUND	GROUND
5	-12V RS-232C SUPPLY (V12N)	POWER
6	SYSTEM RESET REQUEST (RQRST[0])	CONTROL
7	POWER ON HOLD (PWRON[1])	CONTROL
8	EXTERNAL POWER HOLD (EXTPWR[1]) (SOFT POWER CONTROL)	CONTROL
9	THERMAL SHUTDOWN REQUEST (THSDN[0])	CONTROL
10	POWER DOWN REQUEST (PDWNRQ[0])	CONTROL

3-PIN BATTERY CONNECTOR, J11	
PIN	DESCRIPTION
1	+3.9V (VBAT)
2	NOT USED
3	GROUND

2-PIN DIAGNOSTIC INDICATOR CONNECTOR, J12	
PIN	DESCRIPTION
1	D1PU1 (+)
2	ERLED0 (-)

2-PIN POWER INDICATOR CONNECTOR, J13	
PIN	DESCRIPTION
1	D2PU2 (+)
2	GLEDON0 (-)

CM195A NETWORK INTERFACE CARD INTERCONNECTIONS

The CM195A Network Interface (NI) Card interconnections include the following:

- 86-pin card edge connections
- 15-transceiver drop connector.

Figure B-20 shows the layout of the CM195A NI Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

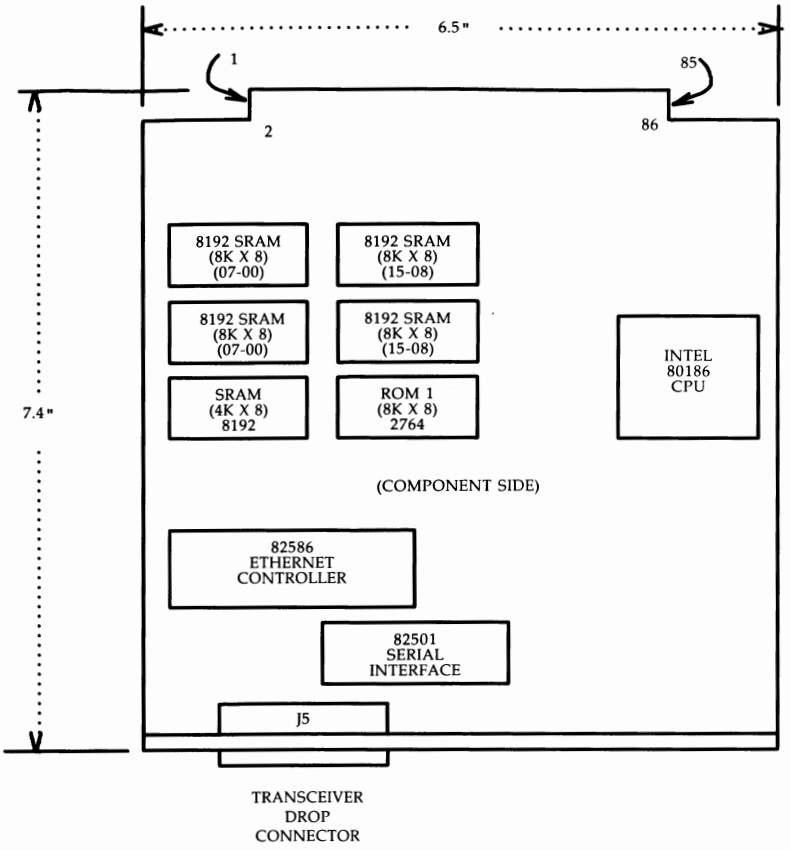
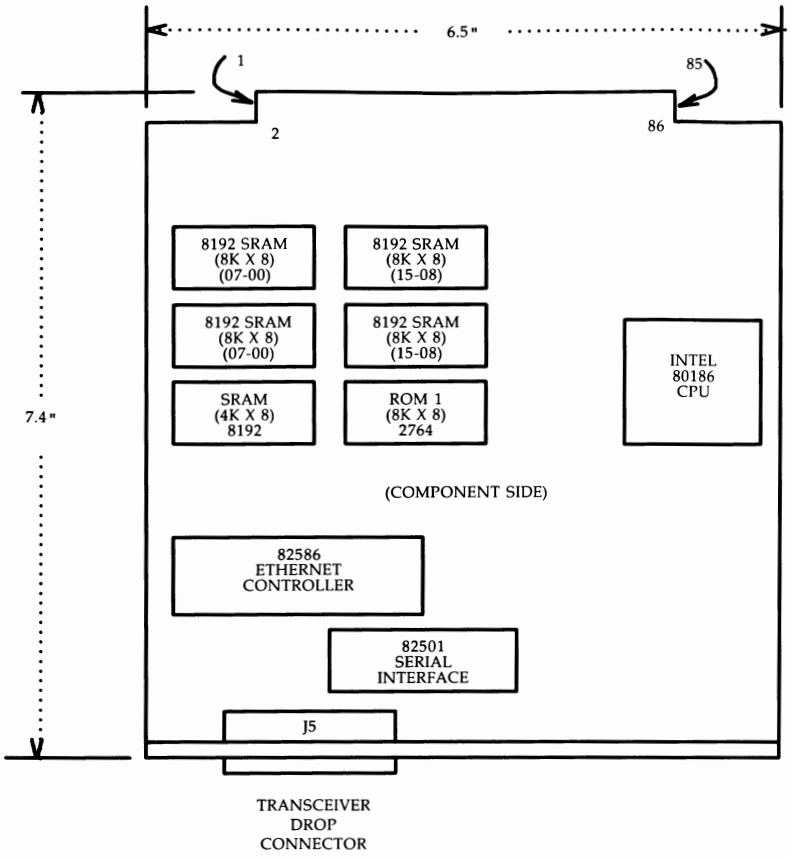


Figure B-20: CM195A NI Card Layout



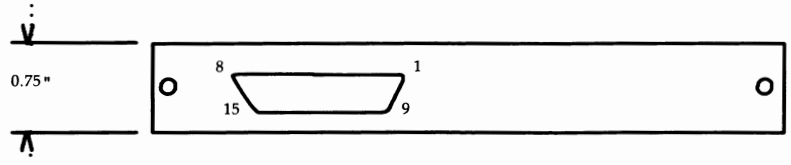


Figure B-20: CM195A NI Card Layout

86-PIN CM195A NI CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	-12V (V12N)	POWER
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN 1 (PBACKI1[0])	INPUT/OUTPUT
006	NOT USED	NC
007	PERIPHERAL CARD SELECT (PCS01[0]—PCS12[0], as applicable)	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT/OUTPUT
014	BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT/OUTPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	INPUT/OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195A NI CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	INPUT/OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR1W0)	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

LEGEND:

NC No Connection

15-PIN CM195A NI CARD TRANSCEIVER DROP CONNECTOR		
PIN	**DESCRIPTION**	**FUNCTION**
01	GROUND	GROUND
02	COLLISION DETECTED (CDS1)(COIL+)	INPUT
03	TRANSMITTED DATA (TDS1)(TX+)	OUTPUT
04	NOT USED	NC
05	RECEIVE DATA (RDS1)(RX+)	INPUT
06	TRANSCEIVER POWER RETURN (VXCR)	GROUND
07	NOT USED	NC
08	NOT USED	NC
09	COLLISION DETECTED RETURN (RDR0)	INPUT
10	TRANSMITTED DATA RETURN (TDR0)(TX-)	OUTPUT
11	NOT USED	NC
12	RECEIVED DATA RETURN (RDR0)(RX-)	INPUT
13	+12V TRANSCEIVER POWER (VXCS)(V12P)	POWER
14	NOT USED	NC
15	NOT USED	NC

LEGEND:

NC No Connection

CM195AA ALARM INTERFACE CIRCUIT CARD INTERCONNECTIONS

The CM195AA Alarm Interface Circuit (AIC) Card interconnections include the following:

- 86-pin card edge connections
- Three 8-pin modular jacks
- Four 4-pin modular jacks.

Figure B-21 shows the layout of the CM195AA AIC Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

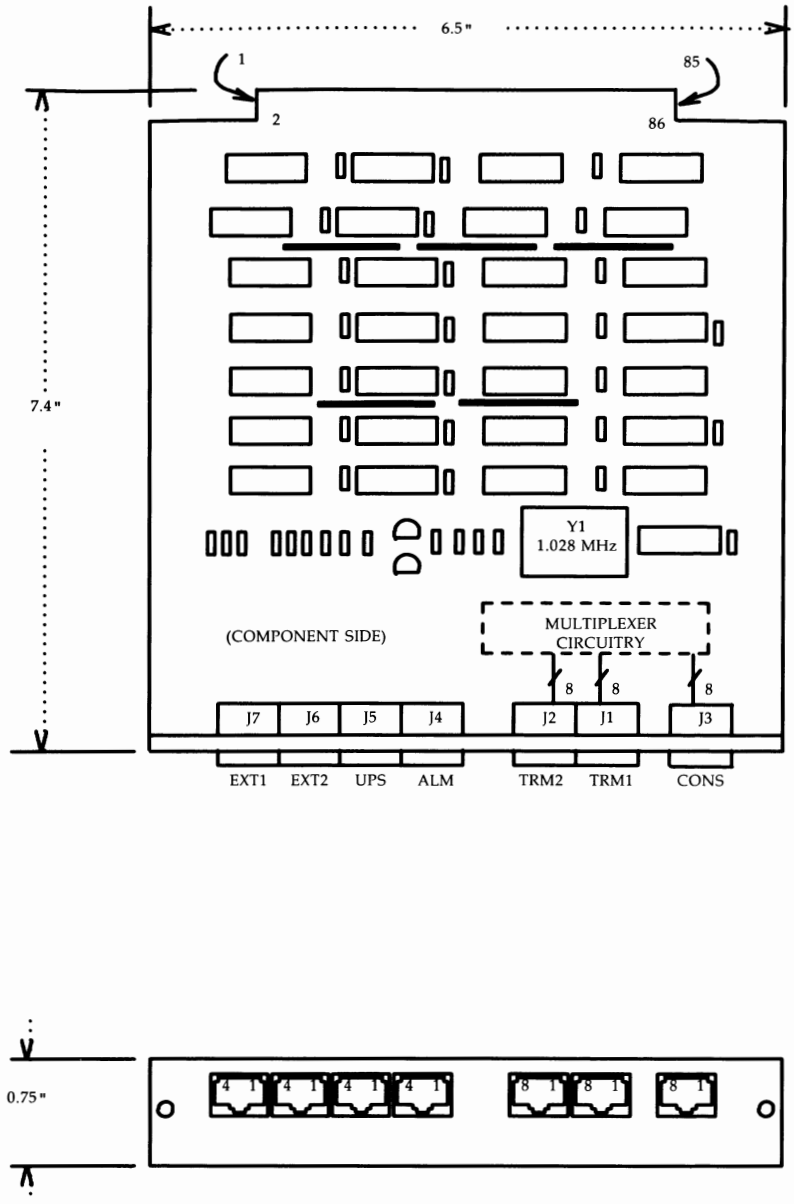
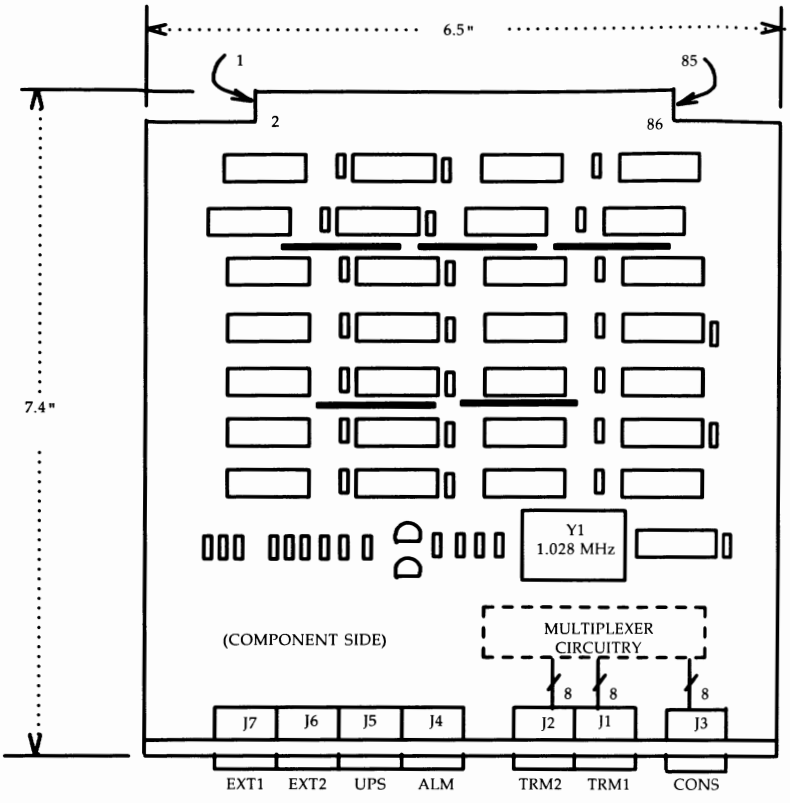


Figure B-21: CM195AA AIC Card Layout



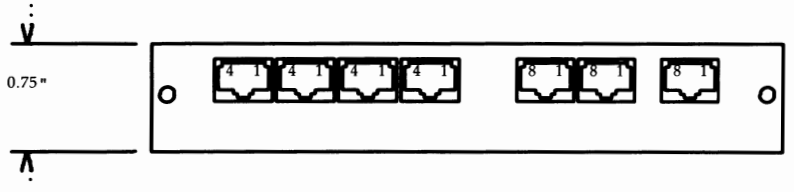


Figure B-21: CM195AA AIC Card Layout

86-PIN CM195AA AIC CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])	OUTPUT
003	-12V (V12N)	POWER
004	NOT USED	NC
005	PERIPHERAL BUS ACKNOWLEDGE IN 1 (PBACKI1[0])	INPUT/OUTPUT
006	NOT USED	NC
007	PERIPHERAL CARD SELECT (PCS0[0])	INPUT
008	RESET REQUEST (RQRST[0])	OUTPUT
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	NOT USED	NC
013	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT/OUTPUT
014	NOT USED	NC
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	NOT USED	NC
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	NOT USED	NC
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195AA AIC CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	NOT USED	NC
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	NOT USED	NC
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	INPUT/OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT
055	PERIPHERAL READ-WRITE (PR1W0)	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	INPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	NOT USED	NC
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	NOT USED	NC
067	NOT USED	NC
068	NOT USED	NC
069	NOT USED	NC
070	NOT USED	NC
071	NOT USED	NC
072	GROUND	GROUND
073	GROUND	GROUND
074	NOT USED	NC
075	NOT USED	NC
076	NOT USED	NC
077	NOT USED	NC
078	NOT USED	NC
079	NOT USED	NC
080	GROUND	GROUND
081	GROUND	GROUND
082	NOT USED	NC
083	NOT USED	NC
084	NOT USED	NC
085	NOT USED	NC
086	NOT USED	NC

LEGEND:

NC No Connection

8-PIN AIC CARD CONS CONNECTOR, J3		
PIN	**DESCRIPTION**	**FUNCTION**
1	REQUEST TO SEND (RTS)	OUTPUT
2	GROUND	GROUND
3	DATA CARRIER DETECT (DCD)	OUTPUT
4	RECEIVE DATA (RXD)	OUTPUT
5	DATA TERMINAL READY (DTR)	INPUT
6	TRANSMIT DATA (TXD)	INPUT
7	CLEAR TO SEND (CTS)	OUTPUT
8	GROUND	GROUND

8-PIN AIC CARD TRM CONNECTORS, J1 and J2		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND	GROUND
2	CLEAR TO SEND (CTS)	OUTPUT
3	TRANSMIT DATA (TXD)	INPUT
4	DATA TERMINAL READY (DTR)	INPUT
5	RECEIVE DATA (RXD)	OUTPUT
6	DATA CARRIER DETECT (DCD)	OUTPUT
7	GROUND	GROUND
8	REQUEST TO SEND (RTS)	OUTPUT

PIN*	ALM	UPS	EXT2	EXT1
1	Darlington Emitter† (MJOUT1)	Ground	Ground‡	Ground§
2	Darlington Collector† (MAJORIN1)	AC FAILURE (ACFSET0)	EXTERNAL TTL‡ (EXT2IN0)	EXTERNAL TTL§ (EXT1IN0)
3	Darlington Emitter¶ (MINOUT1)	Ground	Ground	Ground
4	Darlington Collector¶ (MININ1)	LOWBAT (LOWBSET0)	NC	NC

LEGEND:

NC — No Connection
* — P1 is on the right and P4 is on the left of each modular jack, referenced with the component side up and the face plate toward you.
† — Major Alarm outputs (intended for activating an External Alarm Processing Unit).
‡ — Closure across these pins results in major alarm (accepts either TTL or Closure).
§ — Closure across these pins results in minor alarm (accepts either TTL or Closure).
¶ — Minor Alarm outputs (intended for activating an External Alarm Processing Unit).

CM195AC/CM195AD "DATAKIT" VCS INTERFACE CARD INTERCONNECTIONS

The CM195AC/CM195AD Datakit Virtual Circuit Switch (VCS) Interface Card consists of two circuit cards. The interconnections for the two cards include the following:

- Two 86-pin card edge connections
- Two 40-conductor ribbon cables
- Fiber optic receiver
- Fiber optic transceiver.

Figure B-22 shows the layout of the Datakit VCS Interface Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

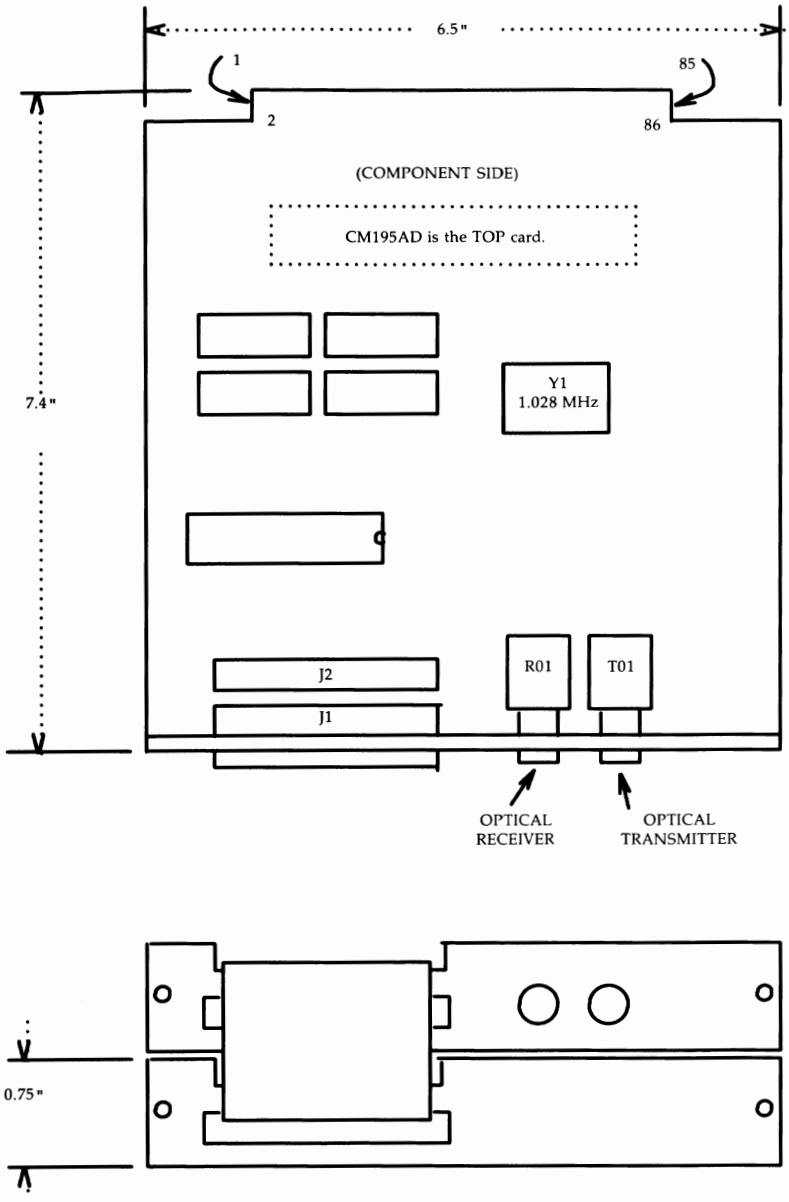


Figure B-22: CM195AC/CM195AD Datakit VCS Interface Card Layout

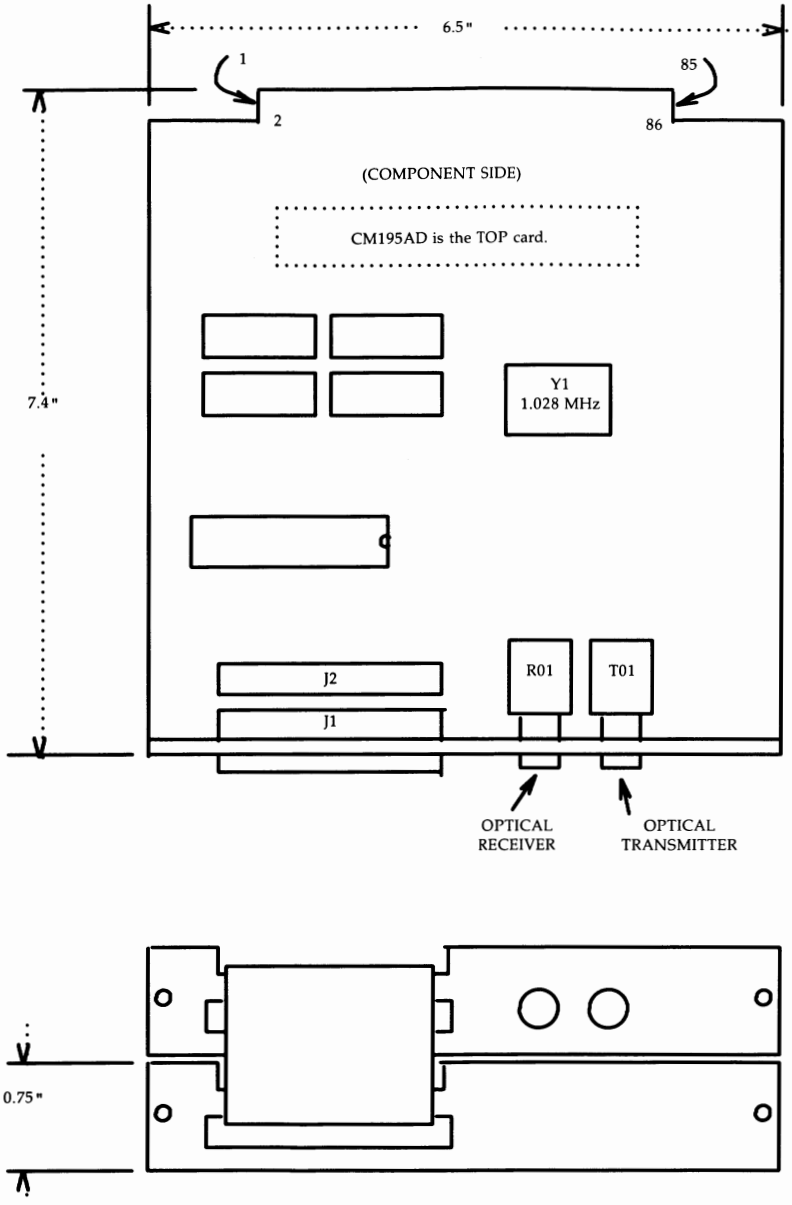


Figure B-22: CM195A/CM195AD Datakit VCS Interface Card Layout

86-PIN CM195AC DATAKIT VCS CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])	OUTPUT
003	-12V (V12N)	POWER
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN 1 (PBACKI1[0])	INPUT/OUTPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	OUTPUT
007	PERIPHERAL CARD SELECT (PCS0[0])	INPUT
008	REQUEST RESET (RQRST[0])	OUTPUT
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	+3.9V BACKUP BATTERY (VBKUP)	POWER
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT/OUTPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	INPUT/OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195AC DATAKIT VCS CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	INPUT/OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR1W0)	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

86-PIN CM195AD FIBER INTERFACE CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	-12V (V12N)	POWER
004	NOT USED	NC
005	PERIPHERAL BUS ACKNOWLEDGE IN 1 (PBACKI1[0])	INPUT/OUTPUT
006	NOT USED	NC
007	NOT USED	NC
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	NOT USED	NC
011	+3.9V BACKUP BATTERY (VBKUP)	POWER
012	NOT USED	NC
013	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT
014	NOT USED	NC
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	NOT USED	NC
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT
020	NOT USED	NC
021	PERIPHERAL INPUT ACKNOWLEDGE IN 1 (PIAKI1[0])	OUTPUT
022	NOT USED	NC
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT
024	NOT USED	NC
025	GROUND (GRD)	GROUND
026	NOT USED	NC
027	NOT USED	NC
028	NOT USED	NC
029	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	OUTPUT
030	NOT USED	NC
031	NOT USED	NC
032	GROUND (GRD)	GROUND
033	NOT USED	NC
034	NOT USED	NC
035	NOT USED	NC
036	NOT USED	NC
037	GROUND (GRD)	GROUND
038	NOT USED	NC
039	NOT USED	NC
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND

86-PIN CM195AD FIBER INTERFACE CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
042	NOT USED	NC
043	NOT USED	NC
044	NOT USED	NC
045	NOT USED	NC
046	NOT USED	NC
047	NOT USED	NC
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	NOT USED	NC
051	NOT USED	NC
052	NOT USED	NC
053	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	OUTPUT
054	NOT USED	NC
055	NOT USED	NC
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	NOT USED	NC
059	NOT USED	NC
060	NOT USED	NC
061	NOT USED	NC
062	NOT USED	NC
063	NOT USED	NC
064	+5V (VCC)	POWER
065	GROUND (GRD)	GROUND
066	NOT USED	NC
067	NOT USED	NC
068	NOT USED	NC
069	NOT USED	NC
070	NOT USED	NC
071	NOT USED	NC
072	GROUND (GRD)	GROUND
073	GROUND (GRD)	GROUND
074	NOT USED	NC
075	NOT USED	NC
076	NOT USED	NC
077	NOT USED	NC
078	NOT USED	NC
079	NOT USED	NC
080	GROUND (GRD)	GROUND
081	GROUND (GRD)	GROUND
082	NOT USED	NC
083	NOT USED	NC
084	NOT USED	NC
085	NOT USED	NC
086	NOT USED	NC

LEGEND:

NC No Connection

40-CONDUCTOR RIBBON CABLE CONNECTIONS, INNER CABLE		
PIN	**CM195AC SIGNAL**	**CM195AD SIGNAL**
01	GROUND	GROUND
02	PIBD00[1]	PIADR00[1]
03	PIBD01[1]	PIADR01[1]
04	PIBD02[1]	PIADR02[1]
05	PIBD03[1]	PIADR03[1]
06	PIBD04[1]	PIADR04[1]
07	PIBD05[1]	PIADR05[1]
08	PIBD06[1]	PIADR06[1]
09	PIBD07[1]	PIADR07[1]
10	PIBD08[1]	PIADR08[1]
11	GROUND	GROUND
12	PIBD09[1]	PIADR09[1]
13	PIBD10[1]	PIADR10[1]
14	PIBD11[1]	PIADR11[1]
15	PIBD12[1]	PIADR12[1]
16	PIBD13[1]	PIADR13[1]
17	PIBD14[1]	PIADR14[1]
18	PIBD15[1]	PIADR15[1]
19	PIBD16[1]	PIADR17[1]
20	PIBD18[1]	PIADR19[1]
21	GROUND	GROUND
22	PITMR0[0]	PITMRIN[0]
23	PITMR1[0]	PITMRIN[1]
24	PILOCK[0]	PIDRQ1[1]
25	PIHLDA[1]	PIHOLD[1]
26	PIPCS4[0]	PIURDY[1]
27	PIPCS5[0]	PINMI[1]
28	PIRAMACK[0]	PIS0[0]
29	PIMCS2[0]	PITEST[1]
30	PICLKOUT[1]	PIBHE[0]
31	GROUND	PIS1[0]
32	PIRST[1]	PIALE[1]
33	PIPCS3[0]	PR1W0
34	PIPCS2[0]	PIRD[0]
35	PIMCS3[0]	PIDT1R0
36	GROUND	GROUND
37	PIINTRA[1]	PIINTRB[1]
38	SPARE	PIDEN[0]
39	BRDPRES[0]	PIS2[0]
40	GROUND	GROUND

40-CONDUCTOR RIBBON CABLE CONNECTIONS, OUTER CABLE		
PIN	CM195AD SIGNAL	CM195AC SIGNAL
01	GROUND	GROUND
02	PED00[1]	NC
03	PED01[1]	ADR01[1]
04	PED02[1]	ADR02[1]
05	PED03[1]	NC
06	PED04[1]	NC
07	PED05[1]	NC
08	PED06[1]	NC
09	PED07[1]	NC
10	PED08[1]	NC
11	GROUND	GROUND
12	PED09[1]	NC
13	PED10[1]	NC
14	PED11[1]	NC
15	PED12[1]	NC
16	PED13[1]	NC
17	PED14[1]	NC
18	PED15[1]	NC
19	PIADR16[1]	NC
20	PIADR18[1]	NC
21	GROUND	GROUND
22	NC	NC
23	NC	NC
24	NC	DRQ1[1]
25	NC	NC
26	PCS4[0]	URDY[1]
27	PCS5[0]	NC
28	NC	NC
29	MCS2[0]	NC
30	NC	NC
31	GROUND	NC
32	PRST[1]	NC
33	PCS3[0]	WR[0]
34	NC	RD[0]
35	NC	NC
36	GROUND	GROUND
37	INTRA[1]	INTRB[1]
38	NC	NC
39	BRDPRES[0]	NC
40	GROUND	GROUND

LEGEND:

NC No Connection

CM195AE GPSC CARD INTERCONNECTIONS

The CM195AE General Purpose Synchronous Controller (GPSC) Card interconnections include the following:

- 86-pin card edge connections
- Two 50-pin synchronous interface connections.

Figure B-23 shows the layout of the CM195AE GPSC Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

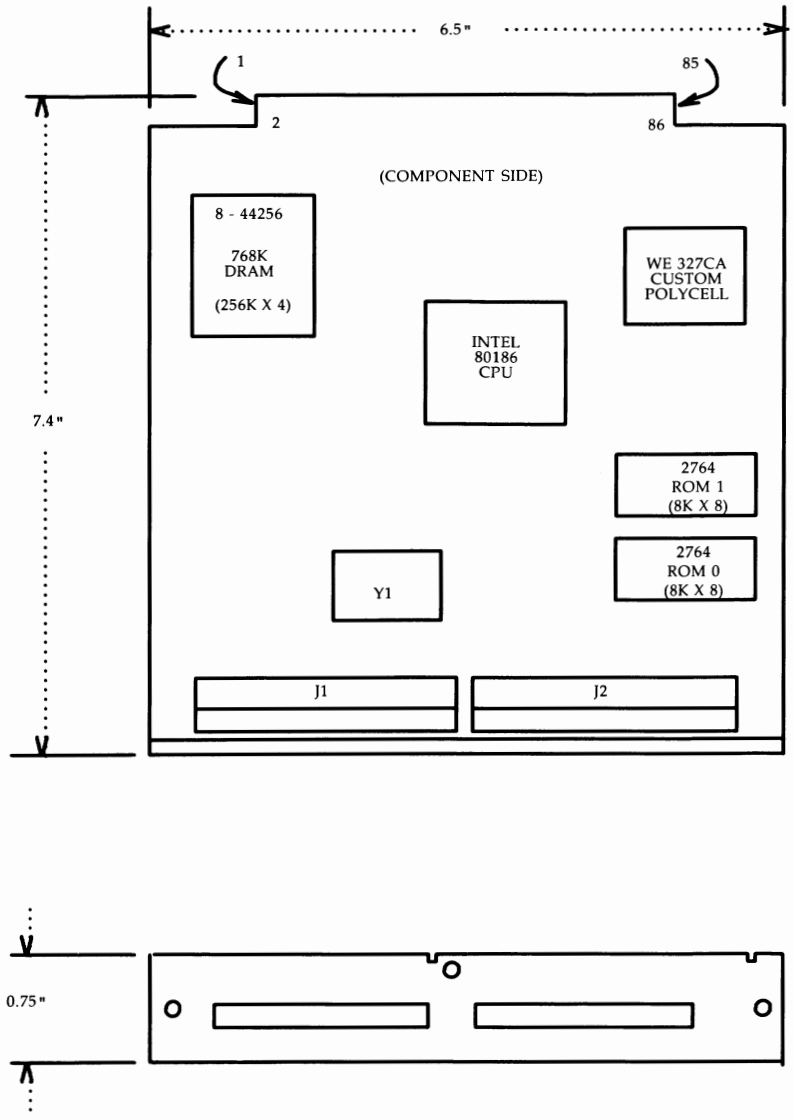


Figure B-23: CM195AE GPSC Card Layout

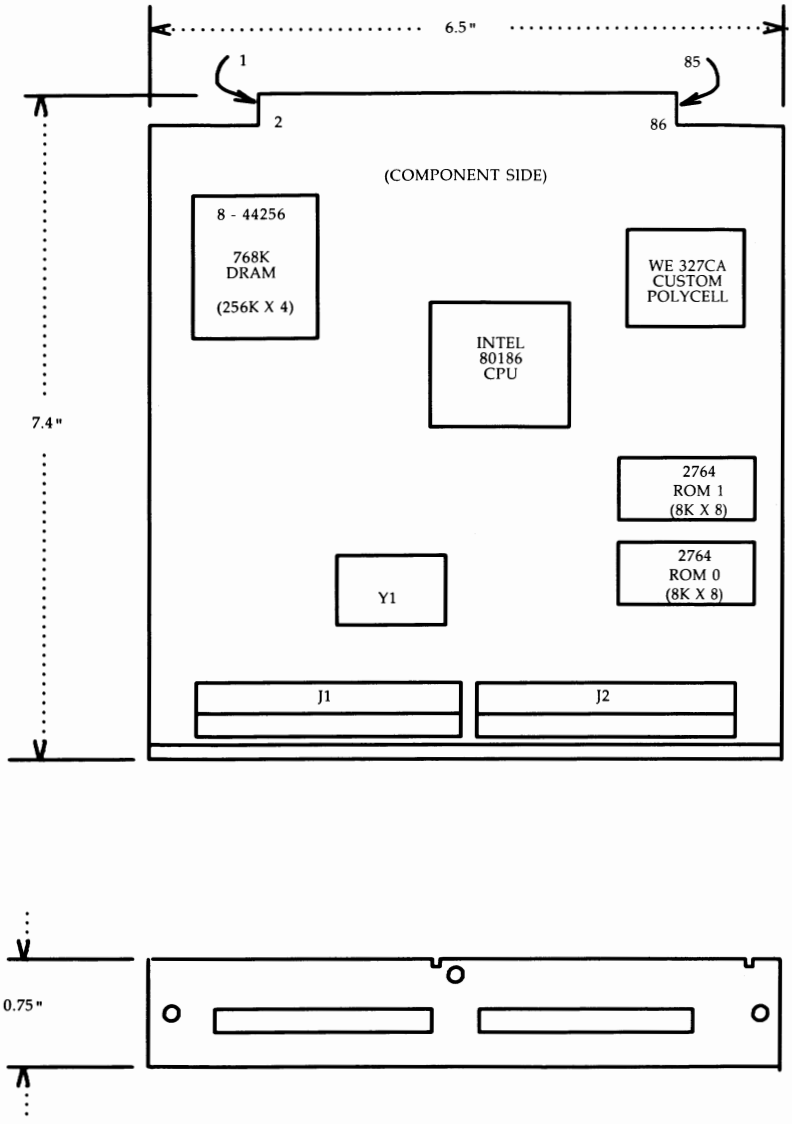


Figure B-23: CM195AE GPSC Card Layout

86-PIN CM195E GPSC CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	-12V (V12N)	POWER
004	NOT USED	NC
005	PERIPHERAL BUS ACKNOWLEDGE IN 1 (PBACKI1[0])	INPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	OUTPUT
007	PERIPHERAL CARD SELECT (PCS0[0])	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT/OUTPUT
014	BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	INPUT/OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195AE GPSC CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	INPUT/OUTPUT
054	NOT USED	NC
055	PERIPHERAL READ-WRITE (PR1W0)	INPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

LEGEND:

NC No Connection

50-PIN CM195AE GPSC INTERFACE CONNECTORS, J1 and J2		
PIN	**DESCRIPTION**	**FUNCTION**
01	TRANSMIT DATA BALANCED (TXDB[1])	OUTPUT
02	TRANSMIT DATA BALANCED (TXDB[0])	OUTPUT
03	TRANSMIT DATA UNBALANCED (TXDU[0])	OUTPUT
04	READY TO SEND UNBALANCED (RTSU[1])	OUTPUT
05	READY TO SEND BALANCED (RTSB[1])	OUTPUT
06	READY TO SEND BALANCED (RTSB[0])	OUTPUT
07	DATA TERMINAL READY UNBALANCED (DTRU[1])	OUTPUT
08	INTERFACE CLOCK UNBALANCED (ICKU[0])	INPUT
09	DATA TERMINAL READY BALANCED (DTRB[1])	OUTPUT
10	DATA TERMINAL READY BALANCED (DTRB[0])	OUTPUT
11	INTERFACE CLOCK BALANCED (ICKB[1])	INPUT
12	INTERFACE CLOCK BALANCED (ICKB[0])	INPUT
13	RATE SELECT UNBALANCED (RASU[1])	INPUT
14	LOCAL LOOP BACK UNBALANCED (LLBU[1])	INPUT/OUTPUT
15	RECEIVE DATA UNBALANCED (RXDU[0])	INPUT
16	CLEAR TO SEND UNBALANCED (CTSU[1])	INPUT
17	RECEIVE DATA BALANCED (RXDB[1])	INPUT
18	RECEIVE DATA BALANCED (RXDB[0])	INPUT
19	CLEAR TO SEND BALANCED (CTSB[1])	INPUT
20	CLEAR TO SEND BALANCED (CTSB[0])	INPUT
21	DATA SET READY UNBALANCED (DSRU[1])	OUTPUT
22	DATA CARRIER DETECT UNBALANCED (DCDU[1])	INPUT
23	DATA SET READY BALANCED (DSRB[1])	OUTPUT
24	DATA SET READY BALANCED (DSRB[0])	OUTPUT
25	TRANSMIT SIGNAL UNBALANCED (XTCU[0])	OUTPUT
26	GROUND	GROUND
27	DATA CARRIER DETECT BALANCED (DCDB[1])	INPUT
28	DATA CARRIER DETECT BALANCED (DCDB[0])	INPUT
29	TRANSMIT SIGNAL BALANCED (XTCB[1])	OUTPUT
30	TRANSMIT SIGNAL BALANCED (XTCB[0])	OUTPUT
31	RECEIVE SIGNAL BALANCED (XRCB[1])	INPUT
32	RECEIVE SIGNAL BALANCED (XRCB[0])	INPUT
33	RING INDICATOR UNBALANCED (RINU[1])	NPUT
34	TIMEOUT (TMOU[1])	INPUT
35	RECEIVE SIGNAL UNBALANCED (XRCU[0])	INPUT
36	GROUND	GROUND
37	GENERAL PURPOSE BIT 1 UNBALANCED/BALANCED (GP1U1B0)	INPUT/OUTPUT
38	GENERAL PURPOSE BIT 2 UNBALANCED/BALANCED (GP2U1B0)	INPUT/OUTPUT
39	+12V (POS12V)	POWER
40	POSITIVE DRIVE POWER (PDRVP)	POWER
41	NEGATIVE DRIVE POWER (NDRVP)	POWER
42	-12V (NEG12V)	POWER
43	+5V VCC	POWER
44	NEW SIGNAL (NSUN[1])	NC
45	NOT USED	NC
46	NOT USED	NC
47	NOT USED	NC
48	NOT USED	NC
49	NOT USED	NC
50	NOT USED	NC

LEGEND:

NC No Connection

GPSC Interface Cables

There are three different cables available for connection to several industry-standard interfaces. The following table lists the GPSC connector pins and the associated industry-standard connector pin.

GPSC INTERFACE CABLE PIN TRANSLATION

GPSC PIN NO.	RS-232C (25-PIN)	RS-449 (37-PIN)	V-35 (34-PIN)
01	NC	4	P (Note)
02	NC	22	S (Note)
03	2	NC	NC
04	4	NC	C
05	NC	7	NC
06	NC	25	NC
07	20	NC	H
08	24	NC	NC
09	NC	12	NC
10	NC	30	NC
11	NC	17	U (Note)
12	NC	12	W (Note)
13	23	16	NC
14	18	10	K
15	3	NC	NC
16	5	NC	D
17	NC	6	R (Note)
18	NC	24	T (Note)
19	NC	9	NC
20	NC	27	NC
21	6	NC	E
22	8	NC	F
23	NC	11	NC
24	NC	29	NC
25	15	NC	NC
26	7	19,20,37	B
27	NC	13	NC
28	NC	31	NC
29	NC	5	Y (Note)
30	NC	23	AA (Note)
31	NC	8	V (Note)
32	NC	26	X (Note)
33	22	15	J
34	25	18	NC
35	17	NC	NC
36	7	19,20,37	B
37	NC	GRD	GRD
38	NC	GRD	NC
39	PDRVxP	NC	PDRVxP
40	V12P	NC	V12P
41	V12N	NC	V12N
42	NDRVxP	NC	NDRVxP
43	NC	NC	NC
44	NC	NC	NC
45	NC	NC	NC
46	NC	NC	NC
47	NC	NC	NC
48	NC	NC	NC
49	NC	NC	NC
50	NC	NC	NC

NOTE: For these signals, the cable assembly will provide a passive network required to convert to/from EIA RS-422 signal levels and CCITT V.35 signal levels.

LEGEND:

GRD	Ground
NC	No Connection

CM195AY/CM195Y EPORTS CARD INTERCONNECTIONS

The CM195AY/CM195Y Enhanced Peripheral Port Controller (EPORTS) Card interconnections include the following:

- 86-pin card edge connections
- Eight 8-pin RS-232C modular connectors.

Figure B-24 shows the layout of the CM195AY/CM195Y EPORTS Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

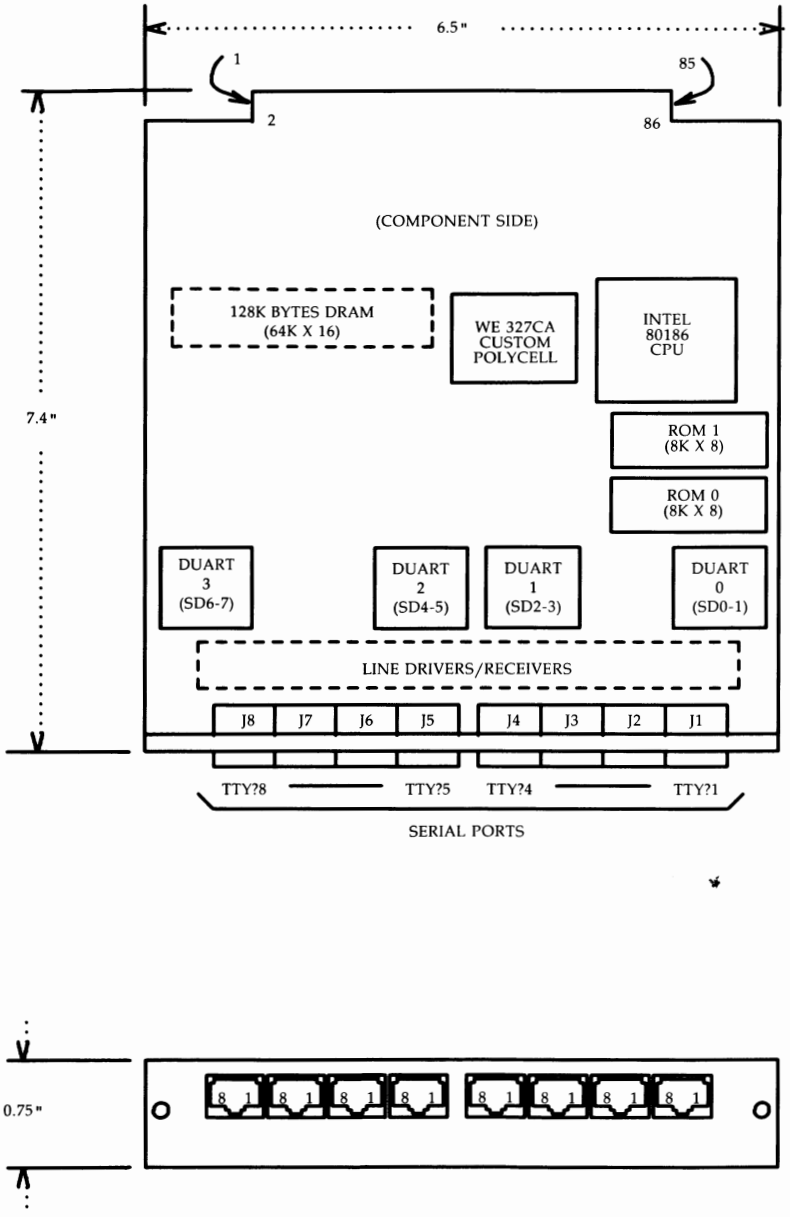


Figure B-24: CM195AY/CM195Y EPORTS Card Layout

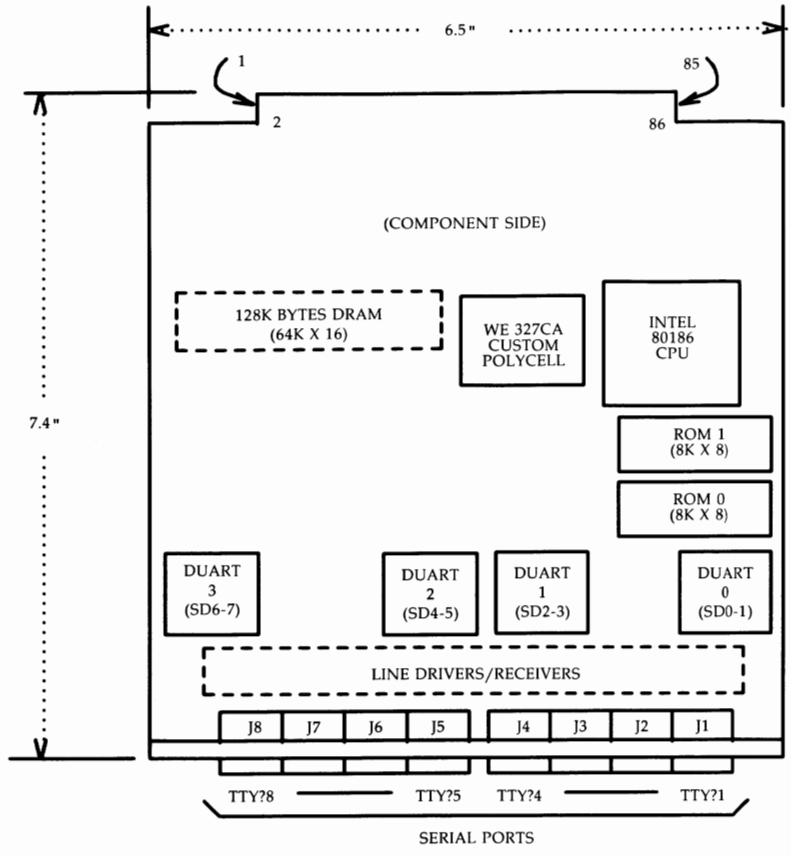


Figure B-24: CM195AY/CM195Y EPORTS Card Layout

86-PIN CM195AY/CM195Y EPORTS CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	-12V (V12N)	POWER
004	NOT USED	NC
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI0)	INPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	OUTPUT
007	PERIPHERAL CARD SELECT (PCS01[0]—PCS12[0], as applicable)	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195AY/CM195Y EPORTS CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

LEGEND:

NC No Connection

8-PIN CM195AY/CM195Y EPORTS CARD MODULAR CONNECTORS, J1 through J8		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND	GROUND
2	CLEAR TO SEND (CTS)	INPUT
3	TRANSMIT DATA (TXD)	INPUT
4	DATA TERMINAL READY (DTR)	INPUT
5	RECEIVE DATA (RXD)	OUTPUT
6	DATA CARRIER DETECT (DCD)	OUTPUT
7	GROUND	GROUND
8	REQUEST TO SEND (RTS)	OUTPUT

CM195B/CM195BA PORTS CARD INTERCONNECTIONS

The CM195B/CM195BA Peripheral Port Controller (PORTS) Card interconnections include the following:

- 86-pin card edge connections
- Four 8-pin RS-232C modular connectors
- One 36-pin CENTRONICS parallel connector.

Figure B-25 shows the layout of the CM195B/CM195BA PORTS Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

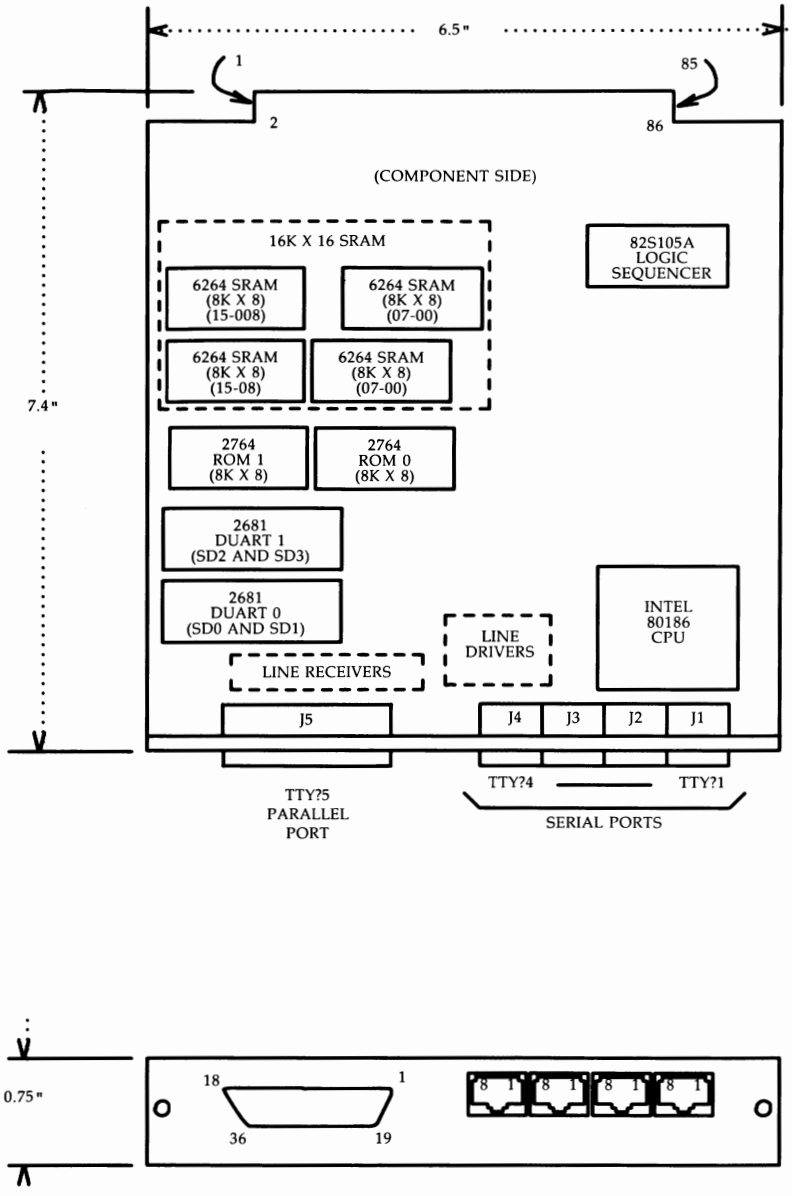
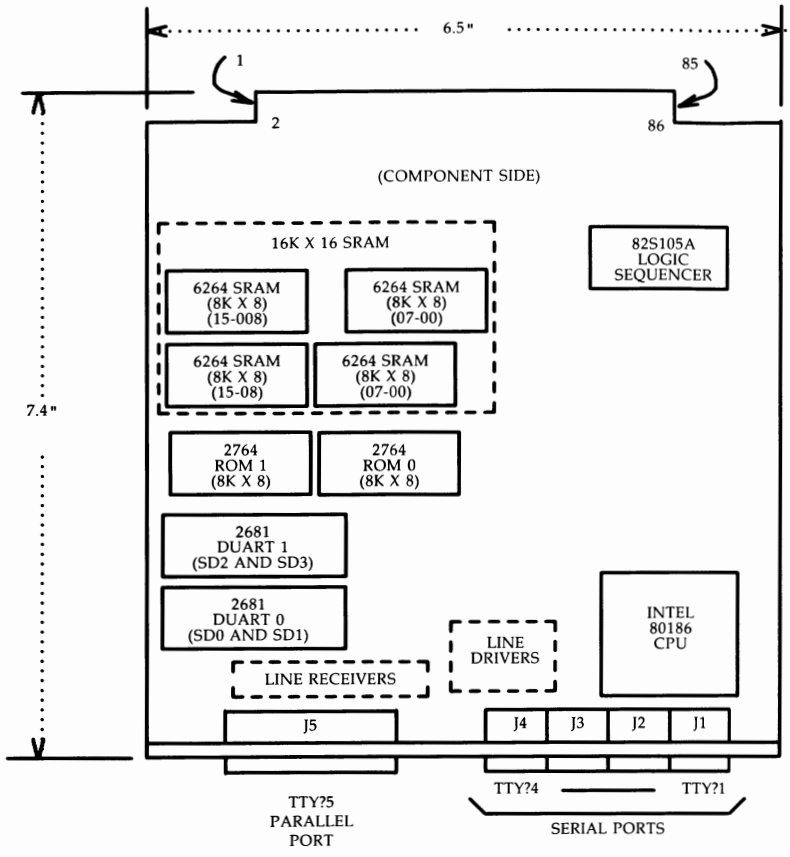


Figure B-25: CM195B/CM195BA PORTS Card Layout



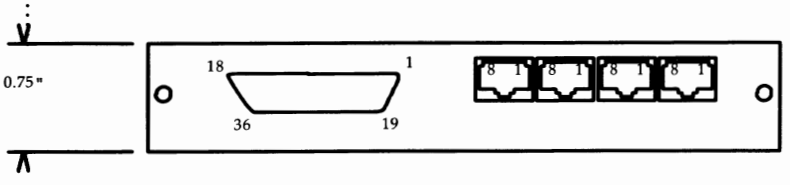


Figure B-25: CM195B/CM195BA PORTS Card Layout

86-PIN CM195B/CM195BA PORTS CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	-12V (V12N)	POWER
004	NOT USED	NC
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	OUTPUT
007	PERIPHERAL CARD SELECT (PCS01[0]—PCS12[0], as applicable)	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	BUS FAULT (PFLT0)	INPUT
015	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	OUTPUT
028	PERIPHERAL DATA BIT 05 (PD051)	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195B/CM195BA PORTS CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO0)	OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

LEGEND:

NC No Connection

8-PIN CM195B/CM195BA PORTS CARD MODULAR CONNECTORS, J1 through J4		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND	GROUND
2	NOT USED	NC
3	TRANSMIT DATA (TXD)	INPUT
4	DATA TERMINAL READY (DTR)	INPUT
5	RECEIVE DATA (RXD)	OUTPUT
6	DATA CARRIER DETECT (DCD)	OUTPUT
7	GROUND	GROUND
8	NOT USED	NC

LEGEND:

NC No Connection

36-PIN CM195B/CM195BA PORTS CARD PARALLEL CONNECTOR, J5		
PIN	**DESCRIPTION**	**FUNCTION**
01	(PRSTRB[0])	INPUT/OUTPUT
02	(PRPA0[1])	OUTPUT
03	(PRPA1[1])	OUTPUT
04	(PRPA2[1])	OUTPUT
05	(PRPA3[1])	OUTPUT
06	(PRPA4[1])	OUTPUT
07	(PRPA5[1])	OUTPUT
08	(PRPA6[1])	OUTPUT
09	(PRPA7[1])	OUTPUT
10	NOT USED	NC
11	PERIPHERAL BUS BUSY (PRBUSY[1])	INPUT
12	PERIPHERAL PARITY ERROR (PRPE[1])	INPUT
13	PERIPHERAL CARD SELECT (PRSEL[1])	INPUT
14	GROUND	GROUND
15	NOT USED	NC
16	GROUND	GROUND
17	GROUND	GROUND
18	NOT USED	NC
19	GROUND	GROUND
20	GROUND	GROUND
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	GROUND	GROUND
26	GROUND	GROUND
27	GROUND	GROUND
28	GROUND	GROUND
29	GROUND	GROUND
30	GROUND	GROUND
31	PERIPHERAL REQUEST SYSTEM RESET (PRREST[0])	INPUT/OUTPUT
32	PERIPHERAL BUS FAULT (PRFAILT[0])	INPUT/OUTPUT
33	GROUND	GROUND
34	NOT USED	NC
35	NOT USED	NC
36	NOT USED	NC

LEGEND:

NC No Connection

CM195H CARTRIDGE TAPE CONTROLLER CARD INTERCONNECTIONS

The CM195H Cartridge Tape Controller (CTC) Card interconnections include the following:

- 86-pin card edge connections
- 34-pin device connector.

Figure B-26 shows the layout of the CM195H CTC Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

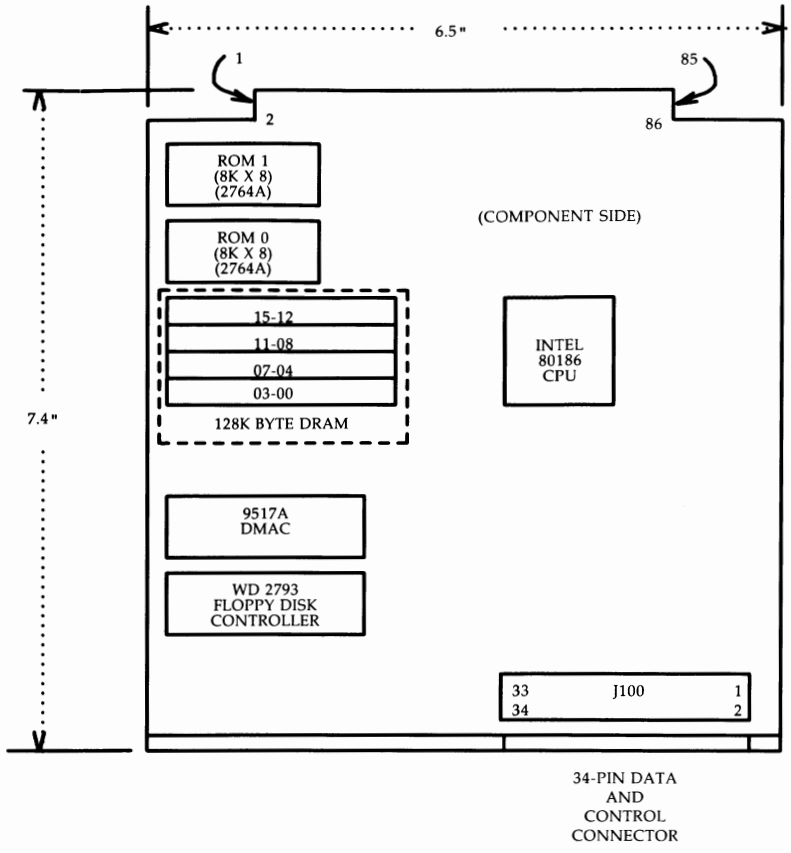
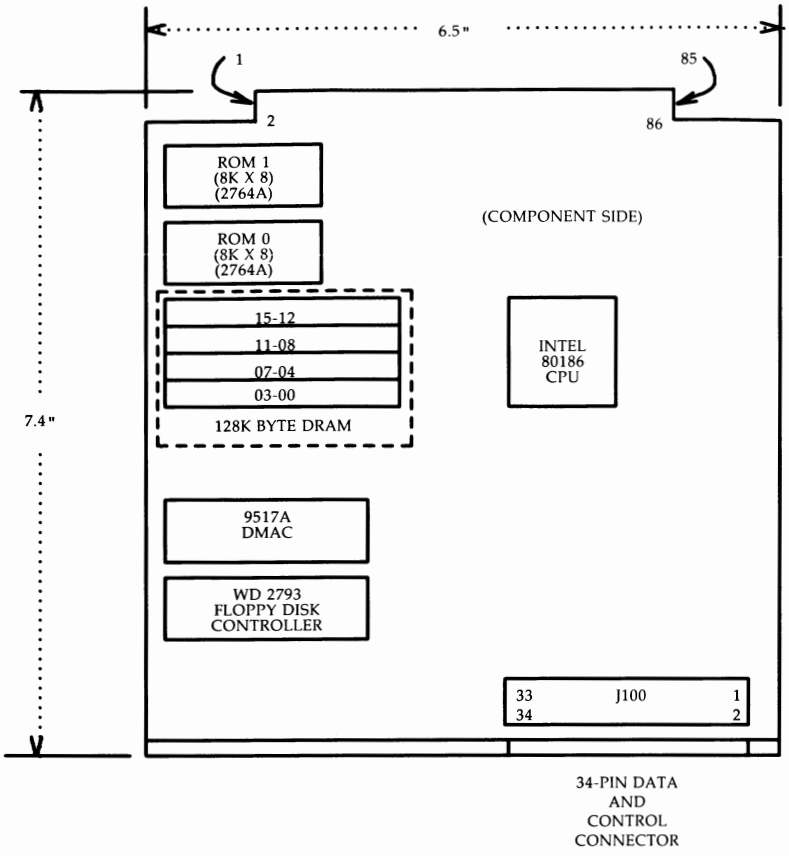


Figure B-26: CM195H CTC Card Layout



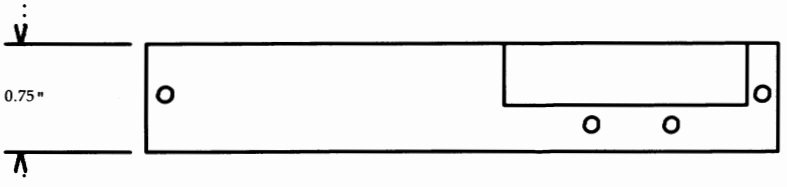


Figure B-26: CM195H CTC Card Layout

86-PIN CM195H CTC CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	NOT USED	NC
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	NOT USED	NC
007	PERIPHERAL CARD SELECT (PCS01[0]—PCS12[0], as applicable)	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	PERIPHERAL BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195H CTC CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA001)	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

LEGEND:

NC No Connection

34-PIN DEVICE CONNECTOR, J100		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND	GROUND
2	NOT USED	NC
3	GROUND	GROUND
4	NOT USED	NC
5	GROUND	GROUND
6	NOT USED	NC
7	GROUND	GROUND
8	INDEX (FINDEX[0])	INPUT
9	GROUND	GROUND
10	FLOPPY DRIVE SELECT 0 (FDSEL[0])	OUTPUT
11	GROUND	GROUND
12	NOT USED	NC
13	GROUND	GROUND
14	NOT USED	NC
15	GROUND	GROUND
16	MOTOR ON (MON[0])	OUTPUT
17	GROUND	GROUND
18	FLOPPY DIRECTION SELECT (FDIRC[0])	OUTPUT
19	GROUND	GROUND
20	FLOPPY STEP (FSTEP[0])	OUTPUT
21	GROUND	GROUND
22	WRITE DATA (FWDATA[0])	OUTPUT
23	GROUND	GROUND
24	FLOPPY WRITE GATE (FWGATE[0])	OUTPUT
25	GROUND	GROUND
26	FLOPPY TRACK 0 (FTR0[0]	INPUT)
27	GROUND	GROUND
28	FLOPPY WRITE PROTECT (FWRTPRT[0])	INPUT
29	GROUND	GROUND
30	READ DATA (FRDATA[0])	INPUT
31	GROUND	GROUND
32	FLOPPY SIDE SELECT (FSSEL[0])	OUTPUT
33	GROUND	GROUND
34	FLOPPY READY (FRDY[0])	INPUT

LEGEND:

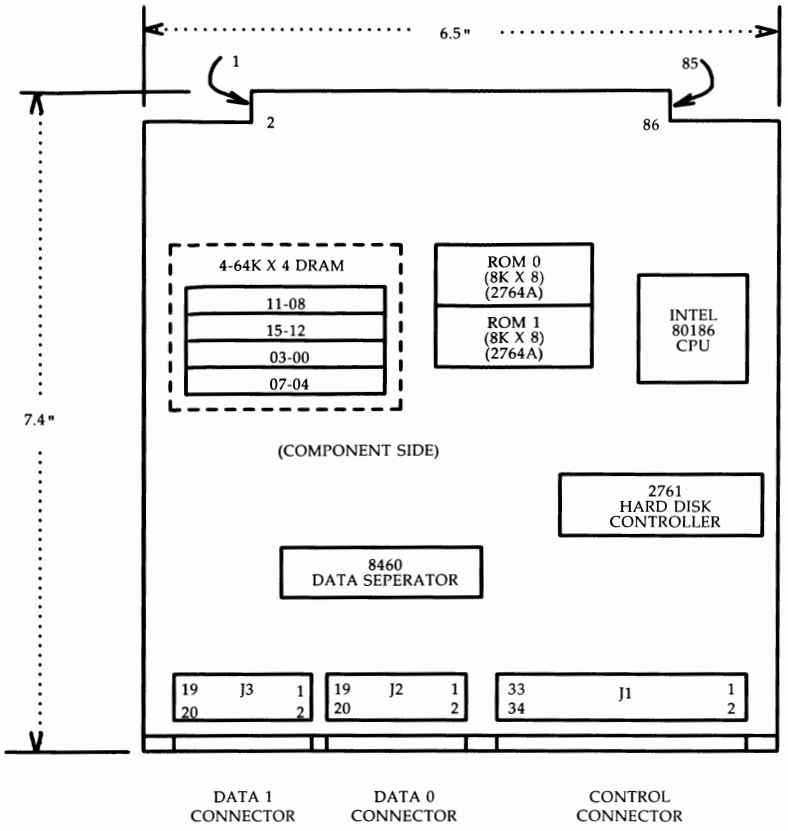
NC No Connection

CM195K EXPANSION DISK CONTROLLER CARD INTERCONNECTIONS

The CM195K Expansion Disk Controller (XDC) Card interconnections include the following:

- 86-pin card edge connections
- 34-pin control connector (J1)
- 20-pin data 0 connector (J2)
- 20-pin data 1 connector (J3).

Figure B-27 shows the layout of the CM195K XDC Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.



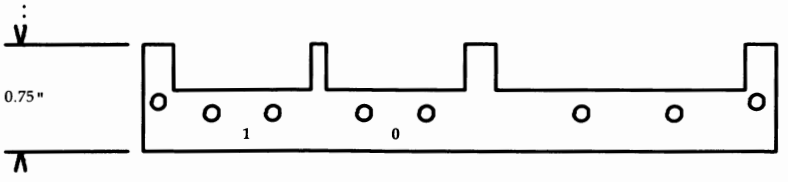
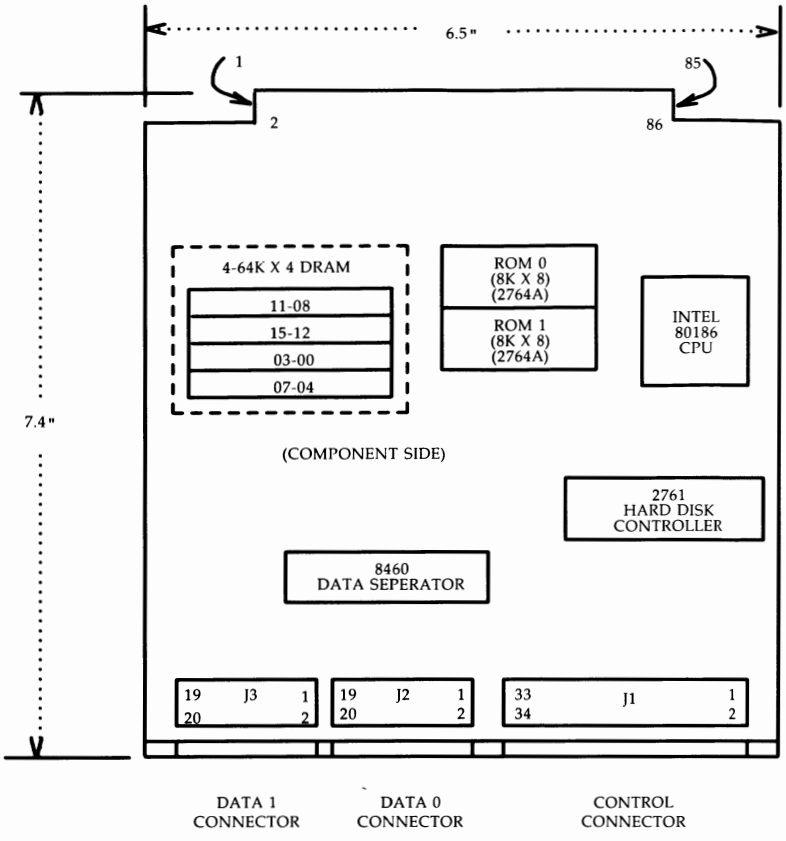


Figure B-27: CM195K XDC Card Layout



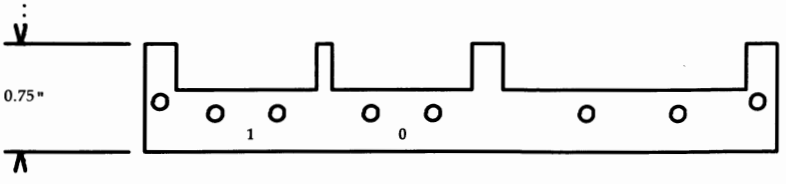


Figure B-27: CM195K XDC Card Layout

86-PIN CM195K XDC CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	NOT USED	NC
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	NOT USED	NC
007	PERIPHERAL CARD SELECT (PCS[0])	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	PERIPHERAL BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195K XDC CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD141)	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	INPUT/OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	NC
055	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

LEGEND:

NC No Connection

34-PIN CONTROL CONNECTOR, J1		
PIN	**DESCRIPTION**	**FUNCTION**
1	GROUND	GROUND
2	HEAD SELECT 3 (HS3[0])	OUTPUT
	REDUCED WRITE CURRENT (RWC[0])	OUTPUT
3	GROUND	GROUND
4	HEAD SELECT 2 (HS2[0])	OUTPUT
5	GROUND	GROUND
6	WRITE GATE (WGATE[0])	OUTPUT
7	GROUND	GROUND
8	SEEK COMPLETE (SKC[0])	INPUT
9	GROUND	GROUND
10	TRACK 0 (TRK0[0])	INPUT
11	GROUND	GROUND
12	WRITE FAULT (WRTFLT[0])	INPUT
13	GROUND	GROUND
14	HEAD SELECT 0 (HS0[0])	OUTPUT
15	GROUND	GROUND
16	CONNECTOR COMMON (J2P7)(J3P7)	GROUND
17	GROUND	GROUND
18	HEAD SELECT 1 (HS1[0])	OUTPUT
19	GROUND	GROUND
20	INDEX (INDEX[0])	INPUT
21	GROUND	GROUND
22	READY (RDY[0])	INPUT
23	GROUND	GROUND
24	STEP (XSTEP[0])	OUTPUT
25	GROUND	GROUND
26	DRIVE SELECT 0 (DSEL0[0])	OUTPUT
27	GROUND	GROUND
28	DRIVE SELECT 1 (DSEL1[0])	OUTPUT
29	GROUND	GROUND
30	NOT USED	NC
31	GROUND	GROUND
32	NOT USED	NC
33	GROUND	GROUND
34	DIRECTION IN (DIR[0])	OUTPUT

LEGEND:

NC No Connection

20-PIN DATA 0 CONNECTOR, J2		
PIN	DESCRIPTION	FUNCTION
1	DRIVE SELECTED (DSD[0])	INPUT
2	GROUND	GROUND
3	NOT USED	NC
4	GROUND	GROUND
5	NOT USED	NC
6	GROUND	GROUND
7	CONNECTOR COMMON (J1P16)(J3P7)	
8	GROUND	GROUND
9	NOT USED	NC
10	GROUND	GROUND
11	GROUND	GROUND
12	GROUND	GROUND
13	+MFM WRITE DATA (MFMOP0)	OUTPUT
14	-MFM WRITE DATA (MFMON0)	OUTPUT
15	GROUND	
16	GROUND	GROUND
17	+MFM READ DATA (MFMIP0)	INPUT
18	-MFM READ DATA (MFMIN0)	INPUT
19	GROUND	GROUND
20	NOT USED	NC

LEGEND:

MFM	Modified Frequency Modulation
NC	No Connection

20-PIN DATA 1 CONNECTOR, J3		
PIN	**DESCRIPTION**	**FUNCTION**
1	DRIVE SELECTED (DSD[0])	INPUT
2	GROUND	GROUND
3	NOT USED	NC
4	GROUND	GROUND
5	NOT USED	NC
6	GROUND	GROUND
7	CONNECTOR COMMON (J1P16)(J2P7)	
8	GROUND	GROUND
9	NOT USED	NC
10	GROUND	GROUND
11	GROUND	GROUND
12	GROUND	GROUND
13	+MFM WRITE DATA (MFMOP1)	OUTPUT
14	-MFM WRITE DATA (MFMON1)	OUTPUT
15	GROUND	GROUND
16	GROUND	GROUND
17	+MFM READ DATA (MFMIP1)	INPUT
18	-MFM READ DATA (MFMIN1)	INPUT
19	GROUND	GROUND
20	NOT USED	NC

LEGEND:

MFM	Modified Frequency Modulation
NC	No Connection

CM195T INTELLIGENT SERIAL CONTROLLER CARD INTERCONNECTIONS

The CM195T Intelligent Serial Controller (ISC) Card interconnections include the following:

- 86-pin card edge connections
- 37-pin serial port connector (J01)
- 25-pin serial port Channel A connector (J02)
- 25-pin serial port Channel B connector (J03).

Figure B-28 shows the layout of the CM195T ISC Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

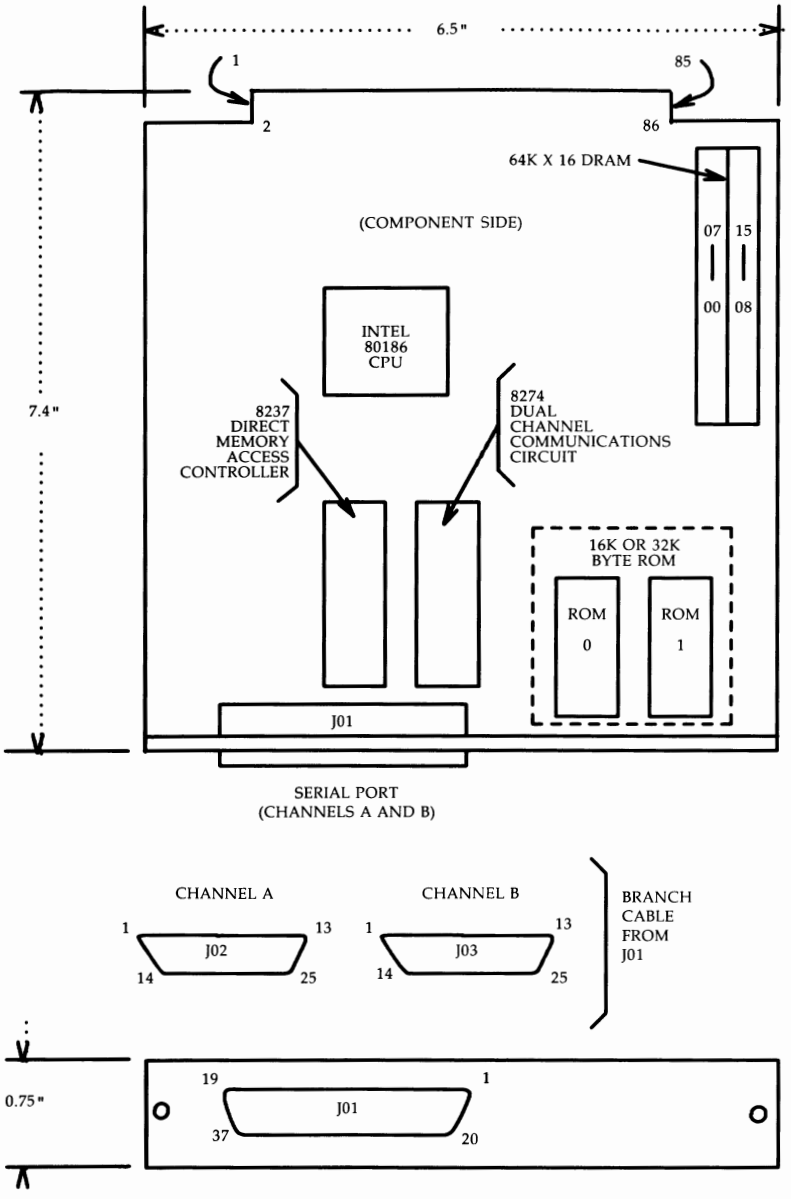


Figure B-28: CM195T ISC Card Layout

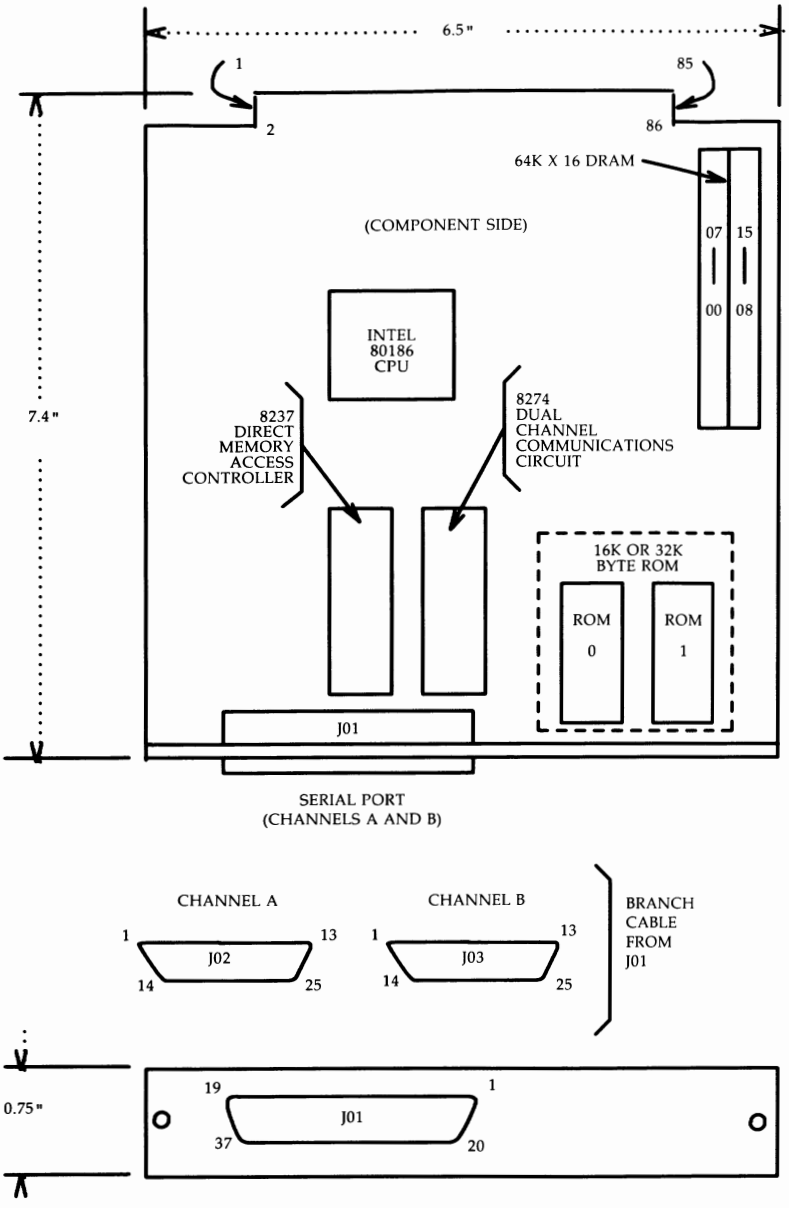


Figure B-28: CM195T ISC Card Layout

86-PIN CM195T ISC CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])	OUTPUT
003	-12V (V12N)	POWER
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	OUTPUT
007	PERIPHERAL CARD SELECT (PCS[0])	INPUT
008	PERIPHERAL REQUEST SYSTEM RESET (RQRST[0])	INPUT/OUTPUT
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	+3.9V BACKUP BATTERY (VBKUP)	POWER
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	PERIPHERAL BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKO2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKO0[0])	INPUT/OUTPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND

86-PIN CM195T ISC CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	INPUT/OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR1W0)	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

37-PIN CM195T ISC CARD SERIAL PORT CONNECTOR, J01		
PIN	**DESCRIPTION**	**FUNCTION**
01	SIGNAL GROUND (J2P1)	GROUND
02	A CHANNEL RECEIVE CLOCK (ARXC)(J2P17)	INPUT
03	A CHANNEL TRANSMIT DATA (ATXD)(J2P2)	OUTPUT
04	A CHANNEL TRANSMIT CLOCK INPUT (ATXCI)(J2P15)	INPUT
05	A CHANNEL RECEIVE DATA (ARXD)(J2P3)	INPUT
06	NOT USED	NC
07	A CHANNEL REQUEST TO SEND (ARTS)(J2P4)	OUTPUT
08	NOT USED	NC
09	A CHANNEL CLEAR TO SEND (ACTS)(J2P5)	INPUT
10	NOT USED	NC
11	SIGNAL GROUND (J2P7)	GROUND
12	NOT USED	NC
13	A CHANNEL DATA CARRIER DETECT (ADCD)(J2P8)	INPUT
14	NOT USED	NC
15	A CHANNEL DATA TERMINAL READY (ADTR)(J2P20)	OUTPUT
16	A CHANNEL RING INDICATOR (ARI)(J2P22)	INPUT
17	A CHANNEL DATA SET READY (ADSR)(J2P6)	INPUT
18	A CHANNEL TRANSMIT CLOCK OUTPUT (ATXCO)(J2P24)	OUTPUT
19	NOT USED	NC
20	NOT USED	NC
21	B CHANNEL TRANSMIT DATA (BTXD)(J3P2)	OUTPUT
22	B CHANNEL RECEIVE CLOCK (BRXC)(J3P17)	INPUT
23	B CHANNEL RECEIVE DATA (BRXD)(J3P3)	INPUT
24	B CHANNEL TRANSMIT CLOCK INPUT(BTXCI)(J3P15)	INPUT
25	B CHANNEL REQUEST TO SEND (BRTS)(J3P4)	OUTPUT
26	NOT USED	NC
27	B CHANNEL CLEAR TO SEND (BCTS)(J3P5)	INPUT
28	SIGNAL GROUND (J3P1)	GROUND
29	SIGNAL GROUND	GROUND
30	NOT USED	NC
31	B CHANNEL DATA CARRIER DETECT (BDCD)(J3P8)	INPUT
32	NOT USED	NC
33	B CHANNEL DATA TERMINAL READY (BDTR)(J3P20)	OUTPUT
34	NOT USED	NC
35	B CHANNEL DATA SET READY (BDSR)(J3P6)	INPUT
36	B CHANNEL TRANSMIT CLOCK OUTPUT (BTXCO)(J3P24)	OUTPUT
37	B CHANNEL RING INDICATOR (BRI)(J3P22	INPUT

LEGEND:

NC No Connection

25-PIN CM195T ISC CARD SERIAL PORT CONNECTOR, J02 OR J03 (CHANNEL A IS J02, CHANNEL B IS J03)		
PIN	**DESCRIPTION**	**FUNCTION**
01	SIGNAL GROUND	GROUND
02	TRANSMIT DATA (TXD)	OUTPUT
03	RECEIVE DATA (RXD)	INPUT
04	REQUEST TO SEND (RTS)	OUTPUT
05	CLEAR TO SEND (CTS)	INPUT
06	DATA SET READY (DSR)	INPUT
07	SIGNAL GROUND	GROUND
08	DATA CARRIER DETECT (DCD)	INPUT
09	NOT USED	NC
10	NOT USED	NC
11	NOT USED	NC
12	NOT USED	NC
13	NOT USED	NC
14	NOT USED	NC
15	TRANSMIT CLOCK INPUT(BTXCI)	INPUT
16	NOT USED	NC
17	RECEIVE CLOCK (RXC)	INPUT
18	NOT USED	NC
19	NOT USED	NC
20	DATA TERMINAL READY (DTR)	OUTPUT
21	NOT USED	NC
22	RING INDICATOR (RI)	INPUT
23	NOT USED	NC
24	TRANSMIT CLOCK OUTPUT (TXCO)	OUTPUT
25	NOT USED	NC

LEGEND:

MFM	Modified Frequency Modulation
NC	No Connection

CM195U STARLAN INTERFACE CARD INTERCONNECTIONS

The CM195U STARLAN Interface Card interconnections include the following:

- 86-pin card edge connections
- 14-pin IN connector (J1)
- 14-pin OUT connector (J2)
- 8-pin TELEPHONE connector (J3).

Figure B-29 shows the layout of the CM195U STARLAN Interface Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

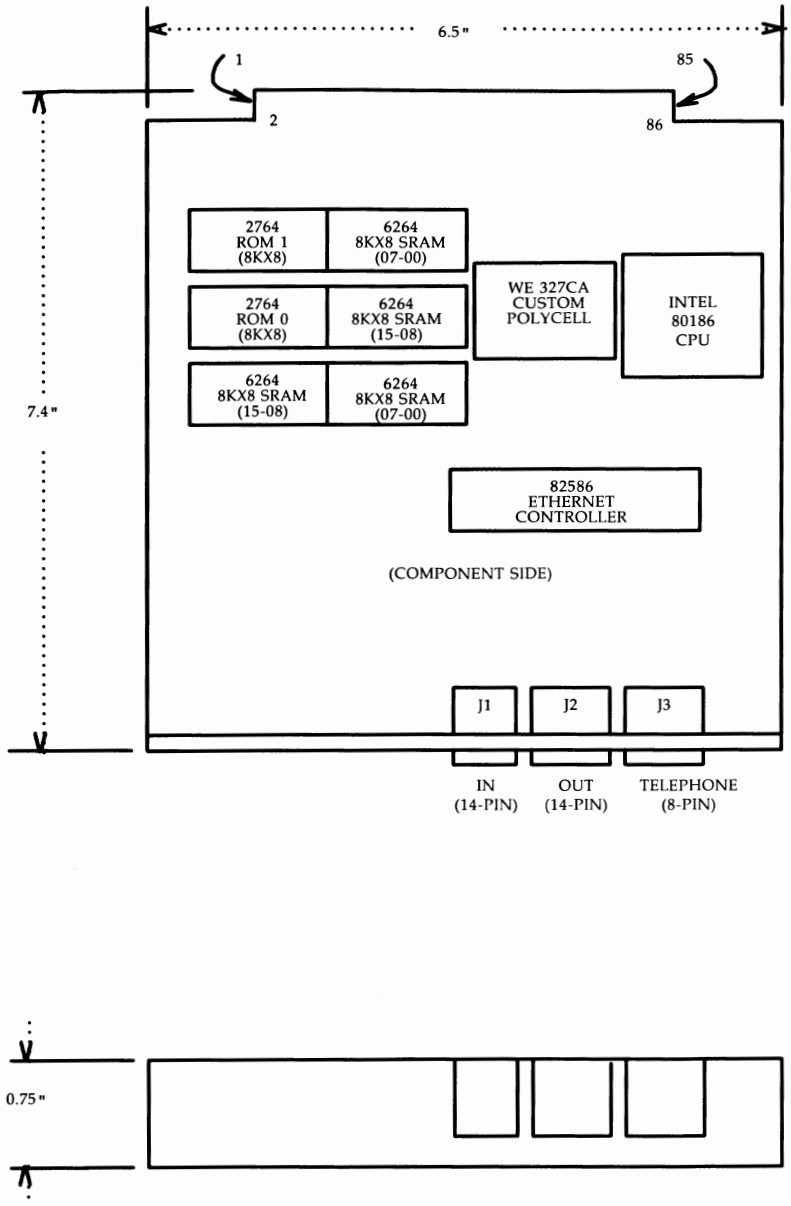


Figure B-29: CM195U STARLAN Interface Card Layout

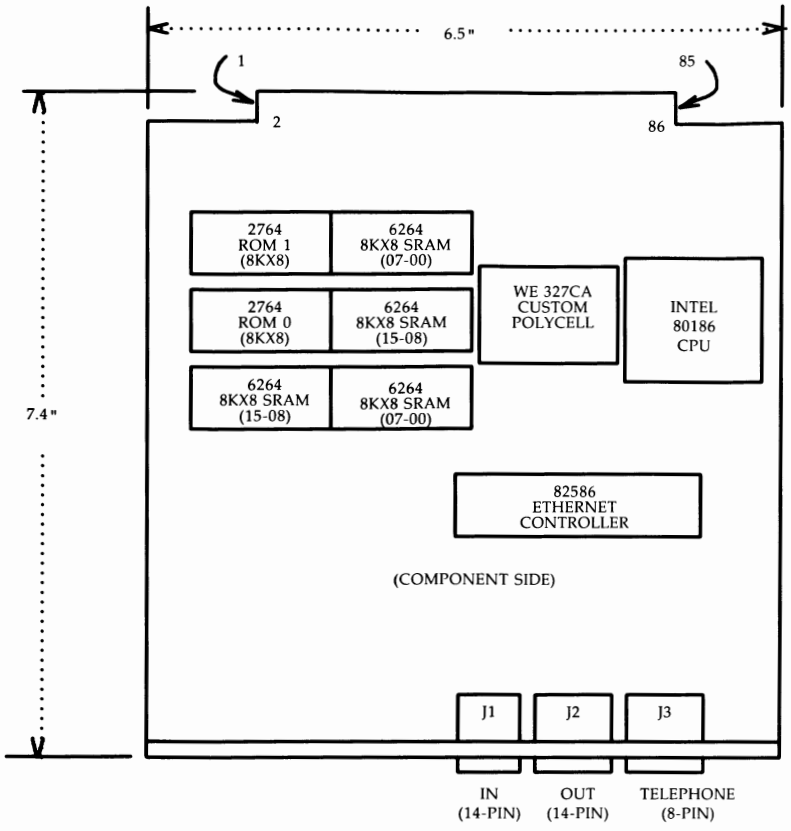


Figure B-29: CM195U STARLAN Interface Card Layout

86-PIN CM195U STARLAN INTERFACE CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	PERIPHERAL INTERRUPT REQUEST 2 (PINT2[0])	OUTPUT
003	-12V (V12N)	POWER
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	OUTPUT
007	PERIPHERAL CARD SELECT (PCS[0])	INPUT
008	PERIPHERAL REQUEST SYSTEM RESET (RQRST[0])	INPUT/OUTPUT
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	+3.9V BACKUP BATTERY (VBKUP)	POWER
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	PERIPHERAL BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKO2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKO0[0])	INPUT/OUTPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND

86-PIN CM195U STARLAN INTERFACE CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	INPUT/OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

14-PIN CM195U STARLAN INTERFACE CARD "IN" CONNECTOR, J1		
PIN	**DESCRIPTION**	**FUNCTION**
001	OUT2	TRANSMIT
002	OUT1	TRANSMIT
003	OUT1	TRANSMIT
004	OUT2	TRANSMIT
005	IN1	RECEIVE
006	NOT USED	NC
007	NOT USED	NC
008	IN2	RECEIVE
009	NOT USED	NC
010	NOT USED	NC
011	IN1	RECEIVE
012	NOT USED	NC
013	NOT USED	NC
014	IN2	RECEIVE

14-PIN CM195U STARLAN INTERFACE CARD "OUT" CONNECTOR, J2		
PIN	**DESCRIPTION**	**FUNCTION**
001	IN1	RECEIVE
002	OUT1	TRANSMIT
003	OUT1	TRANSMIT
004	OUT2	
005	IN1	RECEIVE
006		
007		
008	IN2	RECEIVE
009		
010		
011	OUT2	TRANSMIT
012	NOT USED	NC
013	NOT USED	NC
014	IN2	RECEIVE

8-PIN CM195U STARLAN INTERFACE CARD "TELEPHONE" CONNECTOR, J3		
PIN	**DESCRIPTION**	**FUNCTION**
001	NOT USED	NC
002	NOT USED	NC
003	NOT USED	NC
004		
005		
006	NOT USED	NC
007		
008		

LEGEND:

NC No Connection

CM195W SCSI HOST ADAPTER CARD INTERCONNECTIONS

The CM195W Small Computer System Interface (SCSI) Host Adapter Card interconnections include the following:

- 86-pin card edge connections
- 50-pin SCSI Bus 0 connections
- 50-pin SCSI Bus 1 connections.

Figure B-30 shows the layout of the CM195W SCSI Host Adapter Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

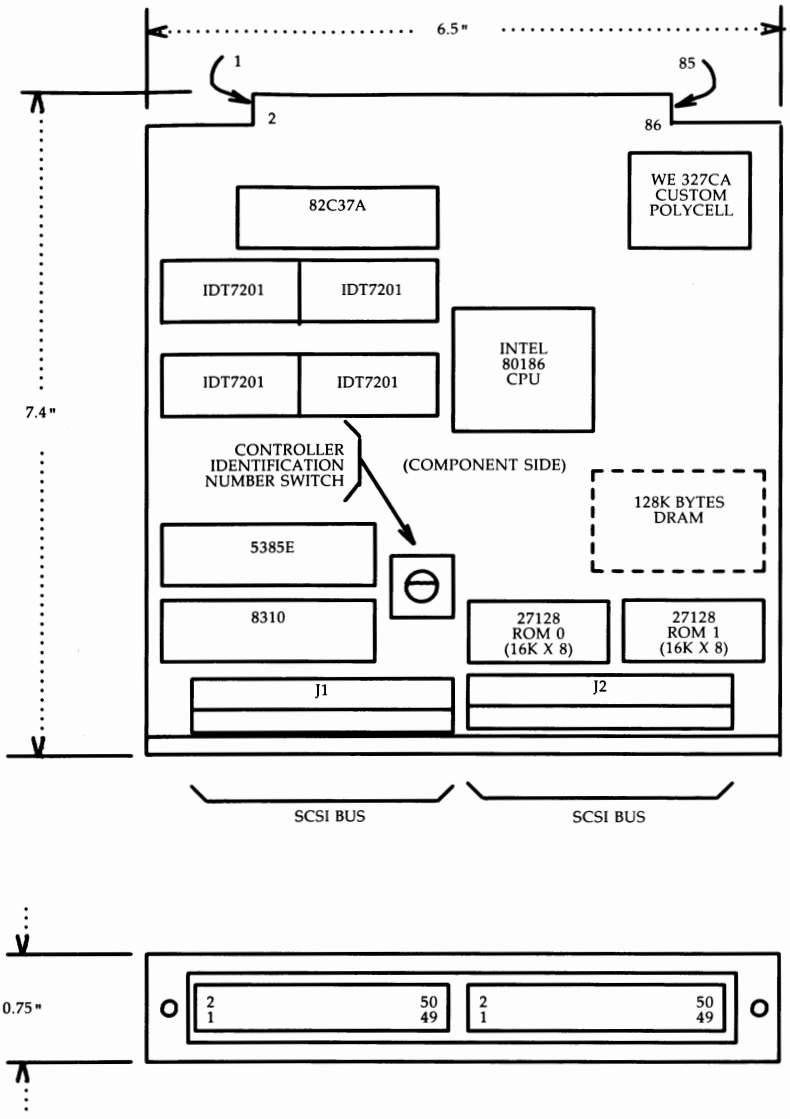


Figure B-30: CM195W SCSI Host Adapter Card Layout

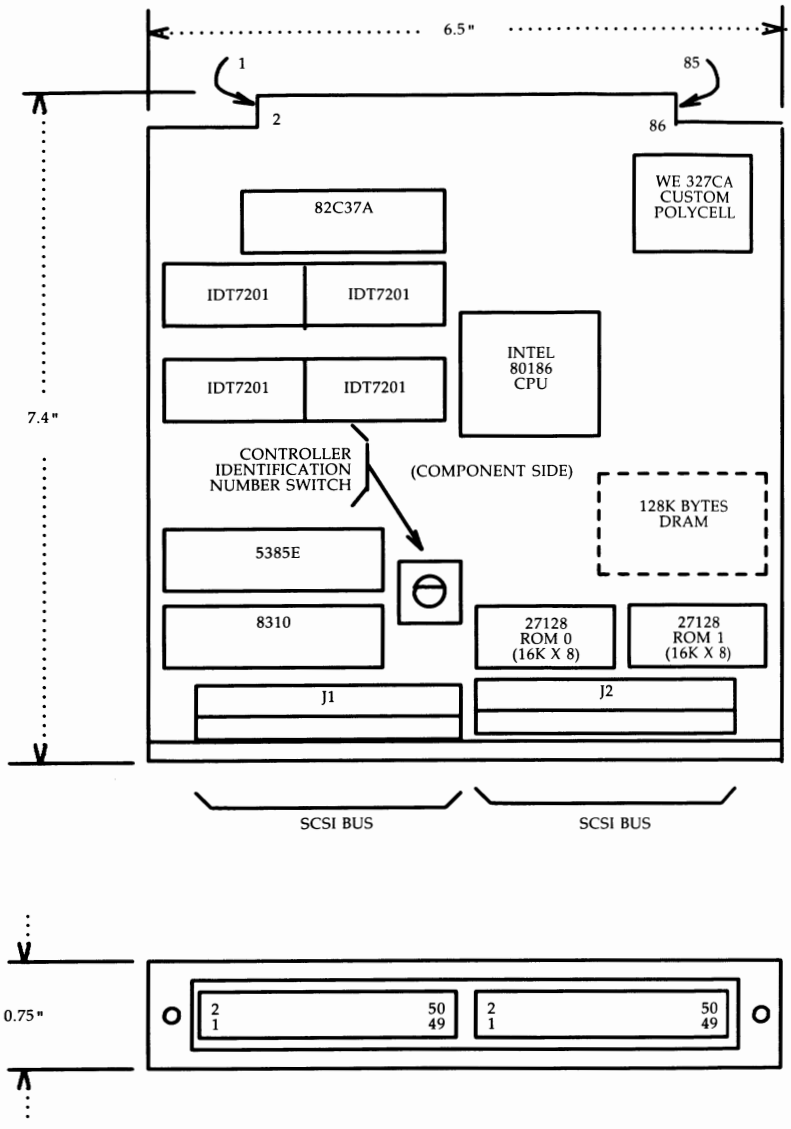


Figure B-30: CM195W SCSI Host Adapter Card Layout

86-PIN CM195W SCSI HOST ADAPTER CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	+12V (V12P)	POWER
002	NOT USED	NC
003	-12V (V12N)	POWER
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	PERIPHERAL INTERRUPT REQUEST 0 (PINT0[0])	NC
007	PERIPHERAL CARD SELECT (PCS01[0]—PCS12[0], as applicable)	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
014	BUS FAULT (PFLT[0])	INPUT
015	INTERRUPT ACKNOWLEDGE OUT 2 (PIAKO2[0])	INPUT/OUTPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIAKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE OUT 0 (PIAKO0[0])	INPUT/OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT

86-PIN CM195W SCSI HOST ADAPTER CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT

LEGEND:

NC No Connection

50-PIN CM195W SCSI HOST ADAPTER CARD BUS 0 AND 1 CONNECTORS, J1 and J2		
PIN	**DESCRIPTION**	**FUNCTION**
01	GROUND	GROUND
02	-DATA BUS BIT 0 (-DB0)	INPUT/OUTPUT
03	GROUND	GROUND
04	-DATA BUS BIT 1 (-DB1)	INPUT/OUTPUT
05	GROUND	GROUND
06	-DATA BUS BIT 2 (-DB2)	INPUT/OUTPUT
07	GROUND	GROUND
08	-DATA BUS BIT 3 (-DB3)	INPUT/OUTPUT
09	GROUND	GROUND
10	-DATA BUS BIT 4 (-DB4)	INPUT/OUTPUT
11	GROUND	GROUND
12	-DATA BUS BIT 5 (-DB5)	INPUT/OUTPUT
13	GROUND	GROUND
14	-DATA BUS BIT 6 (-DB6)	INPUT/OUTPUT
15	GROUND	GROUND
16	-DATA BUS BIT 7 (-DB7)	INPUT/OUTPUT
17	GROUND	GROUND
18	-DATA BUS PARITY BIT (-DBP)	INPUT/OUTPUT
19	GROUND	GROUND
20	GROUND	GROUND
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	OPEN	—
26	TERMINATOR POWER	POWER
27	GROUND	GROUND
28	GROUND	GROUND
29	GROUND	GROUND
30	GROUND	GROUND
31	GROUND	GROUND
32	-ATTENTION	INPUT/OUTPUT
33	GROUND	GROUND
34	GROUND	GROUND
35	GROUND	GROUND
36	-BUSY	INPUT/OUTPUT
37	GROUND	GROUND
38	-ACKNOWLEDGE	INPUT/OUTPUT
39	GROUND	GROUND
40	-RESET	OUTPUT
41	GROUND	GROUND
42	-MESSAGE	INPUT/OUTPUT
43	GROUND	GROUND
44	-SELECT	INPUT/OUTPUT
45	GROUND	GROUND
46	-CONTROL/DATA	INPUT/OUTPUT
47	GROUND	GROUND
48	-REQUEST	INPUT/OUTPUT
49	GROUND	GROUND
50	-INPUT/OUTPUT	INPUT/OUTPUT

CM521A DIFFERENTIAL SCSI HOST ADAPTER CARD INTERCONNECTIONS

The CM521A Differential SCSI Host Adapter Card interconnections include the following:

- 112-pin card edge connections
- 50-pin SCSI Bus 0 connections
- 50-pin SCSI Bus 1 connections.

Figure B-31 shows the layout of the CM521A Differential SCSI Host Adapter Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

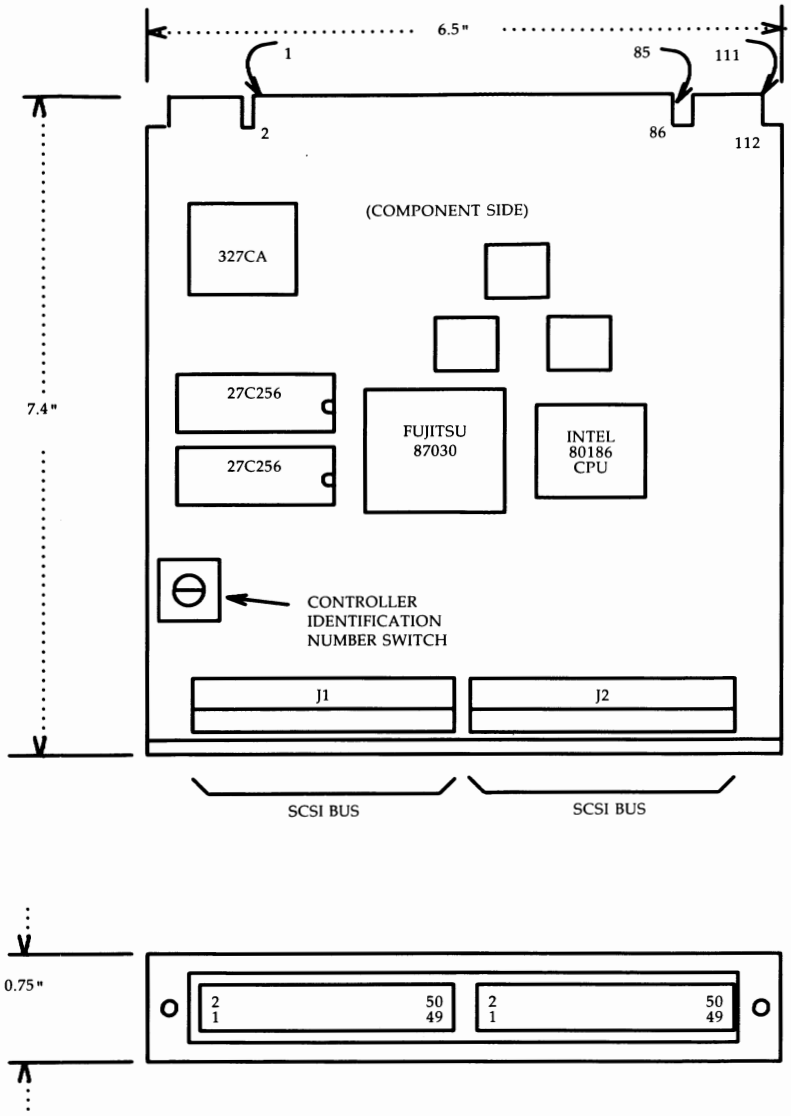


Figure B-31: CM521A Differential SCSI Host Adapter Card Layout

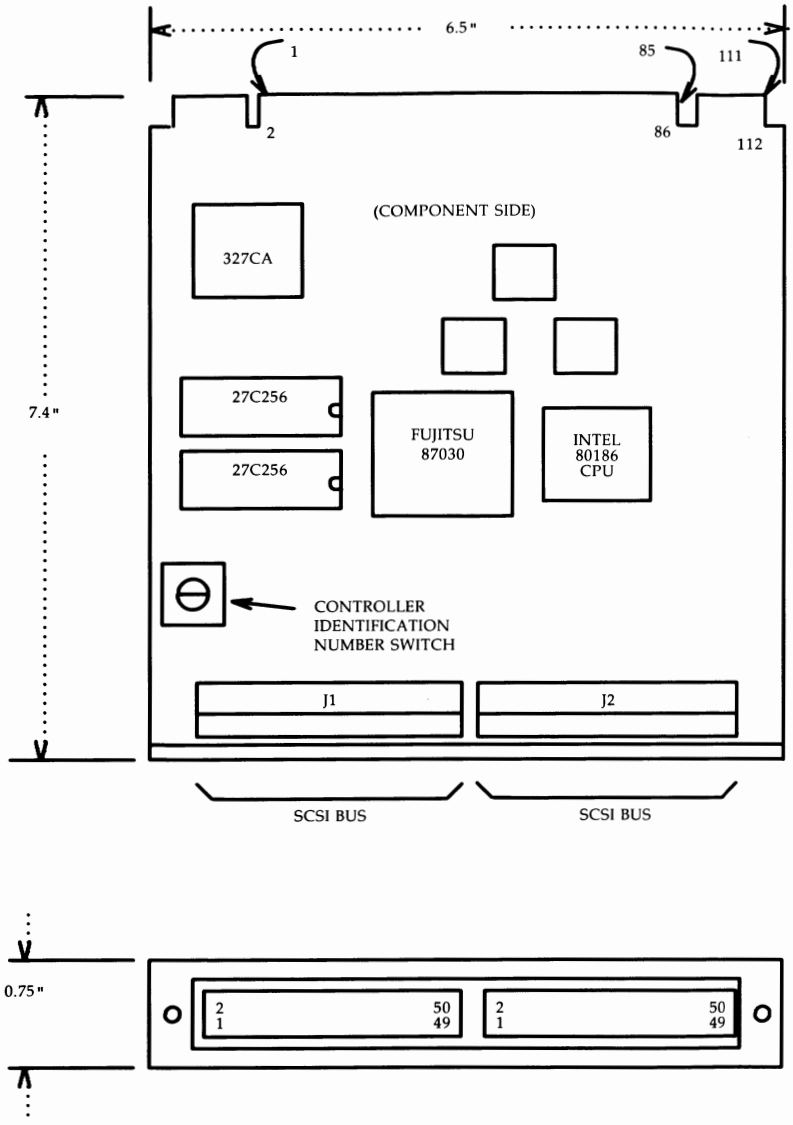


Figure B-31: CM521A Differential SCSI Host Adapter Card Layout

112-PIN CM521A DIFFERENTIAL SCSI HOST ADAPTER CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
001	NOT USED	NC
002	NOT USED	NC
003	NOT USED	NC
004	PERIPHERAL INTERRUPT REQUEST 1 (PINT1[0])	OUTPUT
005	PERIPHERAL BUS ACKNOWLEDGE IN (PBACKI[0])	INPUT
006	NOT USED	NC
007	PERIPHERAL CARD SELECT (PCS[0])	INPUT
008	NOT USED	NC
009	GROUND (GRD)	GROUND
010	SYSTEM RESET (SYSRST[0])	INPUT
011	NOT USED	NC
012	PERIPHERAL CARD FAILURE (PFAIL[0])	OUTPUT
013	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	OUTPUT
014	BUS FAULT (PFLT[0])	INPUT/OUTPUT
015	INTERRUPT ACKNOWLEDGE IN 2 (PIAKI2[0])	INPUT
016	GROUND (GRD)	GROUND
017	+5V (VCC)	POWER
018	PERIPHERAL DATA ACKNOWLEDGE (PDTACK[0])	INPUT/OUTPUT
019	PERIPHERAL INTERRUPT ACKNOWLEDGE IN 1 (PIAKI1[0])	INPUT
020	PERIPHERAL DATA STROBE 1 (PDS1[0])	INPUT/OUTPUT
021	PERIPHERAL INPUT ACKNOWLEDGE OUT 1 (PIACKO1[0])	INPUT/OUTPUT
022	PERIPHERAL DATA BIT 00 (PD00[1])	INPUT/OUTPUT
023	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	INPUT
024	PERIPHERAL DATA BIT 02 (PD02[1])	INPUT/OUTPUT
025	GROUND (GRD)	GROUND
026	PERIPHERAL DATA BIT 03 (PD03[1])	INPUT/OUTPUT
027	PERIPHERAL BUSY (PBUSY[0])	INOUT/OUTPUT
028	PERIPHERAL DATA BIT 05 (PD05[1])	INPUT/OUTPUT
029	PERIPHERAL INPUT ACKNOWLEDGE IN 0 (PIAKI0[0])	OUTPUT
030	PERIPHERAL DATA BIT 07 (PD07[1])	INPUT/OUTPUT
031	PERIPHERAL CARD WIDTH (8 OR 16 BITS)(PSIZE16[0])	OUTPUT
032	GROUND (GRD)	GROUND
033	PERIPHERAL DATA STROBE 0 (PDS0[0])	INPUT/OUTPUT
034	PERIPHERAL DATA BIT 08 (PD08[1])	INPUT/OUTPUT
035	PERIPHERAL DATA BIT 01 (PD01[1])	INPUT/OUTPUT
036	PERIPHERAL DATA BIT 10 (PD10[1])	INPUT/OUTPUT
037	GROUND (GRD)	GROUND
038	PERIPHERAL DATA BIT 12 (PD12[1])	INPUT/OUTPUT
039	PERIPHERAL DATA BIT 04 (PD04[1])	INPUT/OUTPUT
040	+5V (VCC)	POWER
041	GROUND (GRD)	GROUND
042	PERIPHERAL DATA BIT 13 (PD13[1])	INPUT/OUTPUT
043	PERIPHERAL DATA BIT 06 (PD06[1])	INPUT/OUTPUT
044	PERIPHERAL DATA BIT 15 (PD15[1])	INPUT/OUTPUT
045	PERIPHERAL DATA BIT 09 (PD09[1])	INPUT/OUTPUT
046	PERIPHERAL BUS REQUEST (PBRQ[0])	INPUT/OUTPUT
047	PERIPHERAL DATA BIT 11 (PD11[1])	INPUT/OUTPUT
048	GROUND (GRD)	GROUND
049	GROUND (GRD)	GROUND
050	PERIPHERAL PHYSICAL ADDRESS STROBE (PPAS[0])	INPUT/OUTPUT
051	PERIPHERAL DATA BIT 14 (PD14[1])	INPUT/OUTPUT
052	PERIPHERAL INTERLOCK OPERATION (PLOCK[0])	OUTPUT
053	PERIPHERAL BUS ACKNOWLEDGE OUT (PBACKO[0])	OUTPUT
054	PERIPHERAL PHYSICAL ADDRESS BIT 00 (PPA00[1])	INPUT/OUTPUT
055	PERIPHERAL READ-WRITE (PR[1]W[0])	INPUT/OUTPUT
056	GROUND (GRD)	GROUND

112-PIN CM521A DIFFERENTIAL SCSI HOST ADAPTER CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
057	GROUND (GRD)	GROUND
058	PERIPHERAL PHYSICAL ADDRESS BIT 02 (PPA02[1])	INPUT/OUTPUT
059	PERIPHERAL PHYSICAL ADDRESS BIT 01 (PPA01[1])	INPUT/OUTPUT
060	PERIPHERAL PHYSICAL ADDRESS BIT 04 (PPA04[1])	INPUT/OUTPUT
061	PERIPHERAL PHYSICAL ADDRESS BIT 03 (PPA03[1])	INPUT/OUTPUT
062	PERIPHERAL PHYSICAL ADDRESS BIT 05 (PPA05[1])	INPUT/OUTPUT
063	PERIPHERAL PHYSICAL ADDRESS BIT 06 (PPA06[1])	INPUT/OUTPUT
064	+5V (VCC)	POWER
065	GROUND	GROUND
066	PERIPHERAL PHYSICAL ADDRESS BIT 07 (PPA07[1])	INPUT/OUTPUT
067	PERIPHERAL PHYSICAL ADDRESS BIT 09 (PPA09[1])	INPUT/OUTPUT
068	PERIPHERAL PHYSICAL ADDRESS BIT 08 (PPA08[1])	INPUT/OUTPUT
069	PERIPHERAL PHYSICAL ADDRESS BIT 10 (PPA10[1])	INPUT/OUTPUT
070	PERIPHERAL PHYSICAL ADDRESS BIT 11 (PPA11[1])	INPUT/OUTPUT
071	PERIPHERAL PHYSICAL ADDRESS BIT 12 (PPA12[1])	INPUT/OUTPUT
072	GROUND	GROUND
073	GROUND	GROUND
074	PERIPHERAL PHYSICAL ADDRESS BIT 13 (PPA13[1])	INPUT/OUTPUT
075	PERIPHERAL PHYSICAL ADDRESS BIT 15 (PPA15[1])	INPUT/OUTPUT
076	PERIPHERAL PHYSICAL ADDRESS BIT 14 (PPA14[1])	INPUT/OUTPUT
077	PERIPHERAL PHYSICAL ADDRESS BIT 17 (PPA17[1])	OUTPUT
078	PERIPHERAL PHYSICAL ADDRESS BIT 16 (PPA16[1])	INPUT/OUTPUT
079	PERIPHERAL PHYSICAL ADDRESS BIT 20 (PPA20[1])	OUTPUT
080	GROUND	GROUND
081	GROUND	GROUND
082	PERIPHERAL PHYSICAL ADDRESS BIT 18 (PPA18[1])	OUTPUT
083	PERIPHERAL PHYSICAL ADDRESS BIT 23 (PPA23[1])	OUTPUT
084	PERIPHERAL PHYSICAL ADDRESS BIT 19 (PPA19[1])	OUTPUT
085	PERIPHERAL PHYSICAL ADDRESS BIT 21 (PPA21[1])	OUTPUT
086	PERIPHERAL PHYSICAL ADDRESS BIT 22 (PPA22[1])	OUTPUT
087	+5V (VCC)	POWER
088	PERIPHERAL SEQUENTIAL ACCESS (PSEQACC[0])	OUTPUT
089	PERIPHERAL SYSTEMS SUPPORT ACCESS (PSSSA[0])	INPUT
090	+5V (VCC)	POWER
091	GROUND	GROUND
092	GROUND	GROUND
093	PERIPHERAL PHYSICAL ADDRESS BIT 31 (PPA31[1])	OUTPUT
094	PERIPHERAL PHYSICAL ADDRESS BIT 30 (PPA30[1])	OUTPUT
095	PERIPHERAL PHYSICAL ADDRESS BIT 29 (PPA29[1])	OUTPUT
096	PERIPHERAL PHYSICAL ADDRESS BIT 28 (PPA28[1])	OUTPUT
097	PERIPHERAL PHYSICAL ADDRESS BIT 27 (PPA27[1])	OUTPUT
098	PERIPHERAL PHYSICAL ADDRESS BIT 26 (PPA26[1])	OUTPUT
099	GROUND	GROUND
100	PERIPHERAL ADDRESS PARITY BIT 0 (PAP0[1])	INPUT/OUTPUT
101	PERIPHERAL ADDRESS PARITY BIT 1 (PAP1[1])	INPUT/OUTPUT
102	GROUND	GROUND
103	PERIPHERAL PHYSICAL ADDRESS BIT 24 (PPA24[1])	OUTPUT
104	PERIPHERAL PHYSICAL ADDRESS BIT 25 (PPA25[1])	OUTPUT
105	PERIPHERAL ADDRESS PARITY BIT 2 (PAP2[1])	INPUT/OUTPUT
106	PERIPHERAL ADDRESS PARITY BIT 3 (PAP3[1])	INPUT/OUTPUT
107	+5V (VCC)	POWER
108	PERIPHERAL DATA PARITY BIT 0 (PDP0[1])	INPUT/OUTPUT
109	PERIPHERAL DATA PARITY BIT 1 (PDP1[1])	INPUT/OUTPUT
110	+5V (VCC)	POWER
111	PERIPHERAL PARITY CHECK (PPCHEK[0])	OUTPUT
112	PERIPHERAL SUPPORT OF PARITY (PSSSPOE[0])	INPUT

LEGEND:

NC No Connection

50-PIN CM521A DIFFERENTIAL SCSI HOST ADAPTER CARD BUS 0 AND 1 CONNECTORS		
PIN	**DESCRIPTION**	**FUNCTION**
01	GROUND	GROUND
02	GROUND	GROUND
03	+DATA BUS BIT 0 (+DB0)	INPUT/OUTPUT
04	-DATA BUS BIT 0 (-DB0)	INPUT/OUTPUT
05	+DATA BUS BIT 1 (+DB1)	INPUT/OUTPUT
06	-DATA BUS BIT 1 (-DB1)	INPUT/OUTPUT
07	+DATA BUS BIT 2 (+DB2)	INPUT/OUTPUT
08	-DATA BUS BIT 2 (-DB2)	INPUT/OUTPUT
09	+DATA BUS BIT 3 (+DB3)	INPUT/OUTPUT
10	-DATA BUS BIT 3 (-DB3)	INPUT/OUTPUT
11	+DATA BUS BIT 4 (+DB4)	INPUT/OUTPUT
12	-DATA BUS BIT 4 (-DB4)	INPUT/OUTPUT
13	+DATA BUS BIT 5 (+DB5)	INPUT/OUTPUT
14	-DATA BUS BIT 5 (-DB5)	INPUT/OUTPUT
15	+DATA BUS BIT 6 (+DB6)	INPUT/OUTPUT
16	-DATA BUS BIT 6 (-DB6)	INPUT/OUTPUT
17	+DATA BUS BIT 7 (+DB7)	INPUT/OUTPUT
18	-DATA BUS BIT 7 (-DB7)	INPUT/OUTPUT
19	+DATA BUS PARITY BIT (+DBP)	INPUT/OUTPUT
20	-DATA BUS PARITY BIT (-DBP)	INPUT/OUTPUT
21	DIFFERENTIAL SENSE	INPUT/OUTPUT
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	TERMINATOR POWER	POWER
26	TERMINATOR POWER	POWER
27	GROUND	GROUND
28	GROUND	GROUND
29	+ATTENTION	INPUT/OUTPUT
30	-ATTENTION	INPUT/OUTPUT
31	GROUND	GROUND
32	GROUND	GROUND
33	+BUSY	INPUT/OUTPUT
34	-BUSY	INPUT/OUTPUT
35	+ACKNOWLEDGE	INPUT/OUTPUT
36	-ACKNOWLEDGE	INPUT/OUTPUT
37	+RESET	OUTPUT
38	-RESET	OUTPUT
39	+MESSAGE	INPUT/OUTPUT
40	-MESSAGE	INPUT/OUTPUT
41	+SELECT	INPUT/OUTPUT
42	-SELECT	INPUT/OUTPUT
43	+CONTROL/DATA	INPUT/OUTPUT
44	-CONTROL/DATA	INPUT/OUTPUT
45	+REQUEST	INPUT/OUTPUT
46	-REQUEST	INPUT/OUTPUT
47	+INPUT/OUTPUT	INPUT/OUTPUT
48	-INPUT/OUTPUT	INPUT/OUTPUT
49	GROUND	GROUND
50	GROUND	GROUND

CM522A VCACHE CARD INTERCONNECTIONS

The CM522A Virtual Cache (VCACHE) Card interconnection consists of a 120-pin card edge connection. Figure B-32 shows the layout of the CM522A VCACHE Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

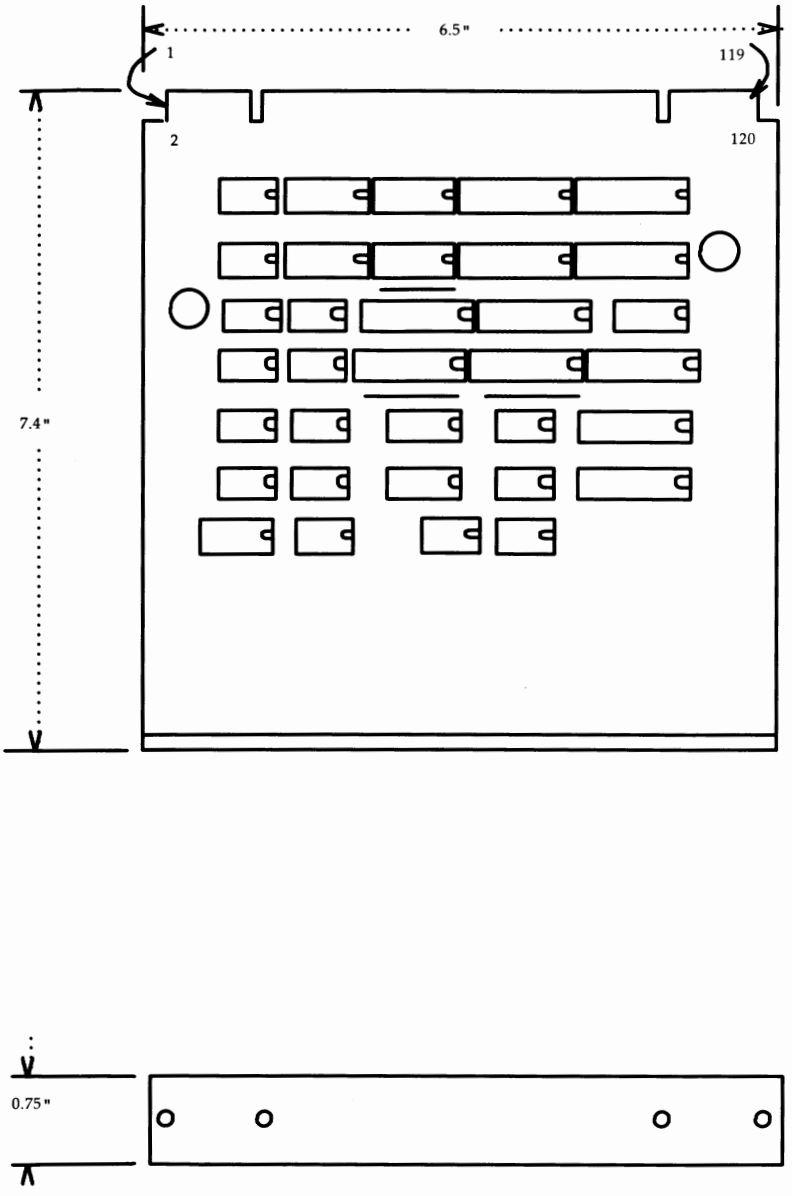


Figure B-32: CM522A VCACHE Card Layout

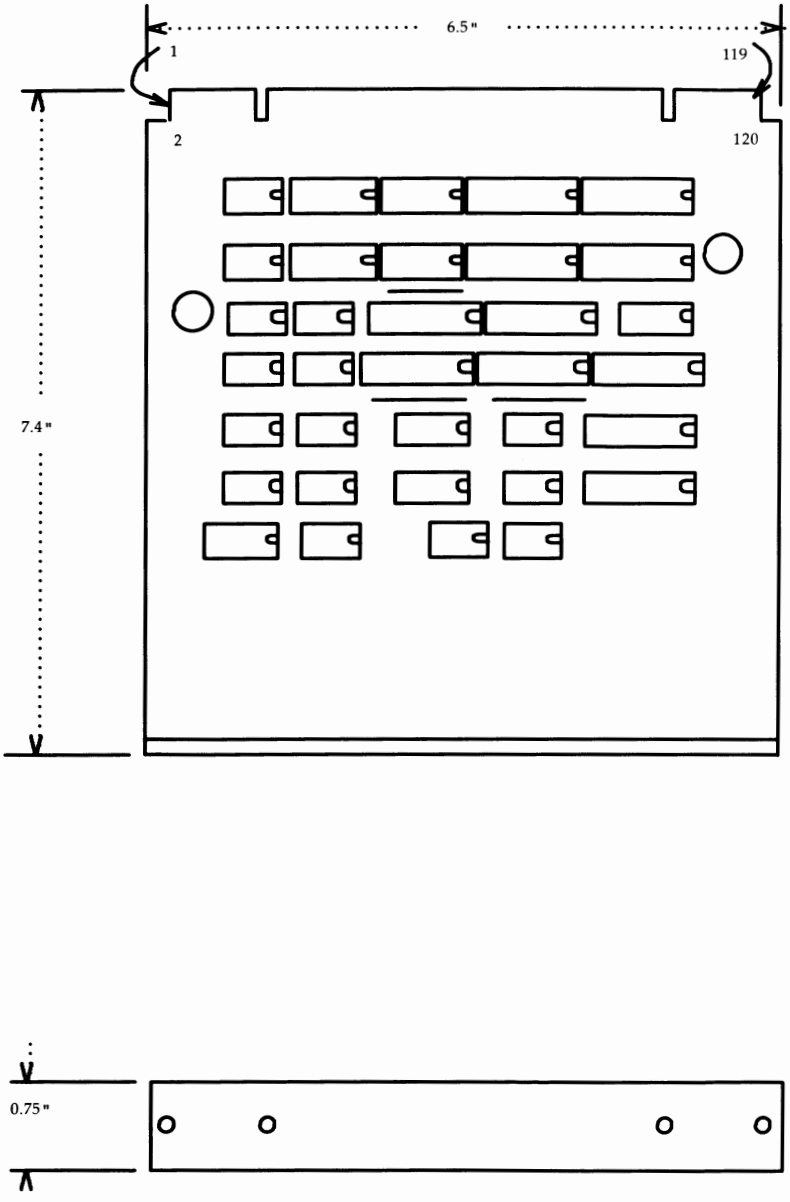


Figure B-32: CM522A VCACHE Card Layout

120-PIN VCACHE CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
1	UBUS DATA STROBE (DS[0])	INPUT
2	NOT USED	NC
3	GROUND (GRD)	GROUND
4	UBUS DATA SHADOW (DSHAD[0])	INPUT
5	UBUS DATA SIZE BIT 1 (CDSIZE1[1])	INPUT
6	UBUS FAULT (FLT[0])	OUTPUT
7	UBUS CARD SELECT (CS1[0])	INPUT
8	GROUND (GRD)	GROUND
9	NOT USED	NC
10	NOT USED	NC
11	NOT USED	NC
12	UBUS SYNCHRONOUS READY (SRDY[0])	OUTPUT
13	UBUS DATA SIZE BIT 0 (CDSIZE0[1])	INPUT
14	UBUS ACCESS STATUS BIT 0 (SAS0[1])	INPUT
15	+5V (VCC)	POWER
16	ACCESS STATUS BIT 1 (SAS1[1])	INPUT
17	UBUS VIRTUAL ADDRESS STROBE (VAS[0])	INPUT
18	NOT USED	NC
19	UBUS CACHE ABLE (CABLE[0])	INPUT
20	GROUND (GRD)	GROUND
21	UBUS ABORT ACTIVATED (ABORT[0])	INPUT
22	UBUS DATA ACKNOWLEDGE (DTACK[0])	OUTPUT
23	UBUS ACCESS STATUS BIT 2 (SAS2[1])	INPUT
24	UBUS ACCESS STATUS BIT 3 (SAS3[1])	INPUT
25	NOT USED	NC
26	NOT USED	NC
27	GROUND (GRD)	GROUND
28	NOT USED	NC
29	UBUS EXECUTION MODE 1 (XMD1[1])	INPUT
30	UBUS VIRTUAL CACHE HIT (VCHIT[0])	OUTPUT
31	NOT USED	NC
32	+5V (VCC)	POWER
33	NOT USED	NC
34	NOT USED	NC
35	NOT USED	NC
36	NOT USED	NC
37	CLOCK 34 (CLK34[1])	INPUT
38	NOT USED	NC
39	GROUND (GRD)	GROUND
40	NOT USED	NC
41	CLOCK 23 (CLK23[1])	INPUT
42	SYSTEM RESET (SYSRST[0])	INPUT
43	NOT USED	NC
44	NOT USED	NC
45	UBUS ADDRESS BIT 31 (CA31[1])	INPUT
46	UBUS ADDRESS BIT 30 (CA30[1])	INPUT
47	UBUS ADDRESS BIT 29 (CA29[1])	INPUT
48	UBUS ADDRESS BIT 28 (CA28[1])	INPUT
49	UBUS ADDRESS BIT 27 (CA27[1])	INPUT
50	UBUS ADDRESS BIT 26 (CA26[1])	INPUT
51	GROUND (GRD)	GROUND
52	UBUS ADDRESS BIT 25 (CA25[1])	INPUT
53	UBUS ADDRESS BIT 24 (CA24[1])	INPUT
54	UBUS ADDRESS BIT 23 (CA23[1])	INPUT
55	UBUS ADDRESS BIT 22 (CA22[1])	INPUT
56	+5V (VCC)	POWER
57	UBUS ADDRESS BIT 21 (CA21[1])	INPUT
58	UBUS ADDRESS BIT 20 (CA20[1])	INPUT
59	UBUS ADDRESS BIT 19 (CA19[1])	INPUT
60	UBUS ADDRESS BIT 18 (CA18[1])	INPUT

120-PIN VCACHE CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
61	UBUS ADDRESS BIT 17 (CA17[1])	INPUT
62	UBUS ADDRESS BIT 16 (CA16[1])	INPUT
63	GROUND (GRD)	GROUND
64	UBUS ADDRESS BIT 15 (CA15[1])	INPUT
65	UBUS ADDRESS BIT 14 (CA14[1])	INPUT
66	UBUS ADDRESS BIT 13 (CA13[1])	INPUT
67	UBUS ADDRESS BIT 12 (CA12[1])	INPUT
68	UBUS ADDRESS BIT 11 (CA11[1])	INPUT
69	UBUS ADDRESS BIT 10 (CA10[1])	INPUT
70	GROUND (GRD)	GROUND
71	UBUS ADDRESS BIT 09 (CA09[1])	INPUT
72	UBUS ADDRESS BIT 08 (CA08[1])	INPUT
73	UBUS ADDRESS BIT 07 (CA07[1])	INPUT
74	UBUS ADDRESS BIT 06 (CA06[1])	INPUT
75	+5V (VCC)	POWER
76	UBUS ADDRESS BIT 05 (CA05[1])	INPUT
77	UBUS ADDRESS BIT 04 (CA04[1])	INPUT
78	UBUS ADDRESS BIT 03 (CA03[1])	INPUT
79	UBUS ADDRESS BIT 02 (CA02[1])	INPUT
80	UBUS ADDRESS BIT 01 (CA01[1])	INPUT
81	UBUS ADDRESS BIT 00 (CA00[1])	INPUT
82	GROUND (GRD)	GROUND
83	UBUS DATA BIT 31 (CD31[1])	INPUT/OUTPUT
84	UBUS DATA BIT 30 (CD30[1])	INPUT/OUTPUT
85	UBUS DATA BIT 29 (CD29[1])	INPUT/OUTPUT
86	UBUS DATA BIT 28 (CD28[1])	INPUT/OUTPUT
87	GROUND (GRD)	GROUND
88	UBUS DATA BIT 27 (CD27[1])	INPUT/OUTPUT
89	UBUS DATA BIT 26 (CD26[1])	INPUT/OUTPUT
90	UBUS DATA BIT 25 (CD25[1])	INPUT/OUTPUT
91	UBUS DATA BIT 24 (CD24[1])	INPUT/OUTPUT
92	UBUS DATA BIT 23 (CD23[1])	INPUT/OUTPUT
93	UBUS DATA BIT 22 (CD22[1])	INPUT/OUTPUT
94	+5V (VCC)	POWER
95	UBUS DATA BIT 21 (CD21[1])	INPUT/OUTPUT
96	UBUS DATA BIT 20 (CD20[1])	INPUT/OUTPUT
97	UBUS DATA BIT 19 (CD19[1])	INPUT/OUTPUT
98	UBUS DATA BIT 18 (CD18[1])	INPUT/OUTPUT
99	GROUND (GRD)	GROUND
100	UBUS DATA BIT 17 (CD17[1])	INPUT/OUTPUT
101	UBUS DATA BIT 16 (CD16[1])	INPUT/OUTPUT
102	UBUS DATA BIT 15 (CD15[1])	INPUT/OUTPUT
103	UBUS DATA BIT 14 (CD14[1])	INPUT/OUTPUT
104	UBUS DATA BIT 13 (CD13[1])	INPUT/OUTPUT
105	UBUS DATA BIT 12 (CD12[1])	INPUT/OUTPUT
106	GROUND (GRD)	GROUND
107	UBUS DATA BIT 11 (CD11[1])	INPUT/OUTPUT
108	UBUS DATA BIT 10 (CD10[1])	INPUT/OUTPUT
109	UBUS DATA BIT 09 (CD09[1])	INPUT/OUTPUT
110	UBUS DATA BIT 08 (CD08[1])	INPUT/OUTPUT
111	+5V (VCC)	POWER
112	UBUS DATA BIT 07 (CD07[1])	INPUT/OUTPUT
113	UBUS DATA BIT 06 (CD06[1])	INPUT/OUTPUT
114	UBUS DATA BIT 05 (CD05[1])	INPUT/OUTPUT
115	UBUS DATA BIT 04 (CD04[1])	INPUT/OUTPUT
116	UBUS DATA BIT 03 (CD03[1])	INPUT/OUTPUT
117	UBUS DATA BIT 02 (CD02[1])	INPUT/OUTPUT
118	GROUND (GRD)	GROUND
119	UBUS DATA BIT 01 (CD01[1])	INPUT/OUTPUT
120	UBUS DATA BIT 00 (CD00[1])	INPUT/OUTPUT

LEGEND:

NC No Connection

CM524A PROCESSING ELEMENT CARD INTERCONNECTIONS

The CM524A Processing Element (PE) Card interconnection consists of a 120-pin card edge connection. Figure B-33 shows the layout of the CM524A PE Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

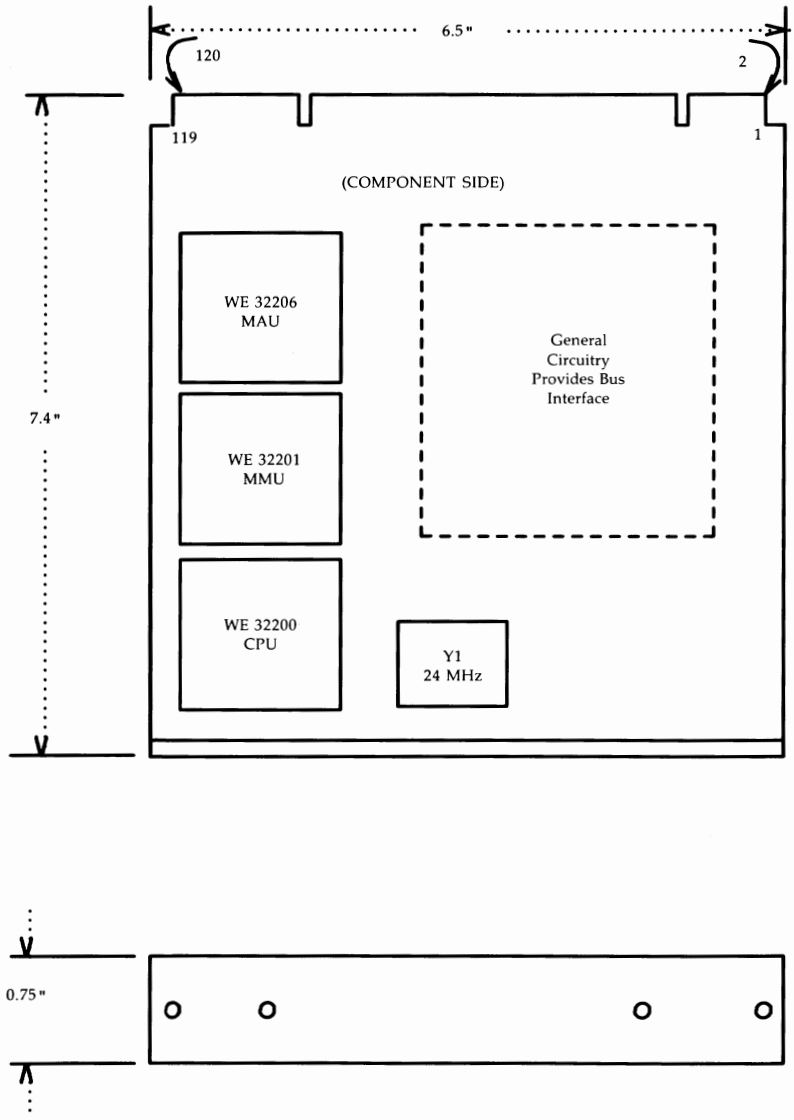


Figure B-33: CM524A PE Card Layout

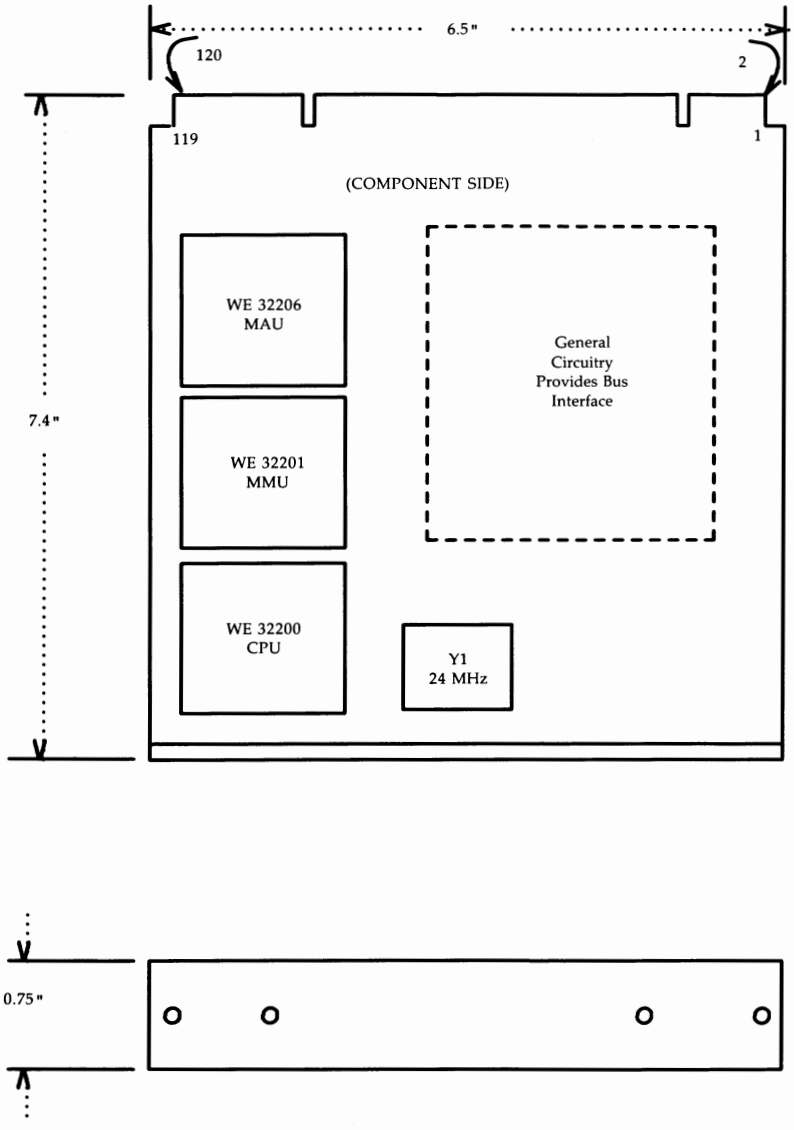


Figure B-33: CM524A PE Card Layout

120-PIN PE CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
1	BUB CONNECTOR INHIBIT SLOT 0 (BINHIB0[0])	INPUT
2	GROUND (GRD)	GROUND
3	OPERATIONAL INTERRUPT LEVEL 15 (OPINT15[0])	OUTPUT
4	NOT USED	NC
5	NOT USED	NC
6	+5V (VCC)	POWER
7	NOT USED	NC
8	GROUND (GRD)	GROUND
9	BUB PHYSICAL ADDRESS STROBE (UPAS[0])	OUTPUT
10	BUB DATA BIT 31 (BD31[1])	INPUT/OUTPUT
11	BUB DATA BIT 30 (BD30[1])	INPUT/OUTPUT
12	BUB DATA BIT 29 (BD29[1])	INPUT/OUTPUT
13	BUB DATA BIT 28 (BD28[1])	INPUT/OUTPUT
14	GROUND (GRD)	GROUND
15	+5V (VCC)	POWER
16	BUB DATA BIT 26 (BD26[1])	INPUT/OUTPUT
17	BUB DATA BIT 27 (BD27[1])	INPUT/OUTPUT
18	BUB DATA BIT 25 (BD25[1])	INPUT/OUTPUT
19	BUB DATA BIT 24 (BD24[1])	INPUT/OUTPUT
20	GROUND (GRD)	GROUND
21	BUB DATA BIT 22 (BD22[1])	INPUT/OUTPUT
22	BUB DATA BIT 23 (BD23[1])	INPUT/OUTPUT
23	BUB DATA BIT 21 (BD21[1])	INPUT/OUTPUT
24	BUB DATA BIT 20 (BD20[1])	INPUT/OUTPUT
25	BUB DATA BIT 18 (BD18[1])	INPUT/OUTPUT
26	BUB DATA BIT 19 (BD19[1])	INPUT/OUTPUT
27	GROUND (GRD)	GROUND
28	BUB DATA BIT 17 (BD17[1])	INPUT/OUTPUT
29	BUB DATA BIT 16 (BD16[1])	INPUT/OUTPUT
30	BUB DATA BIT 14 (BD14[1])	INPUT/OUTPUT
31	BUB DATA BIT 15 (BD15[1])	INPUT/OUTPUT
32	+5V (VCC)	POWER
33	BUB DATA BIT 12 (BD12[1])	INPUT/OUTPUT
34	BUB DATA BIT 13 (BD13[1])	INPUT/OUTPUT
35	NOT USED	NC
36	BUB DATA BIT 11 (BD11[1])	INPUT/OUTPUT
37	BUB DATA BIT 10 (BD10[1])	INPUT/OUTPUT
38	NOT USED	NC
39	GROUND (GRD)	GROUND
40	BUB DATA BIT 08 (BD08[1])	INPUT/OUTPUT
41	BUB DATA BIT 09 (BD09[1])	INPUT/OUTPUT
42	BUB DATA BIT 07 (BD07[1])	INPUT/OUTPUT
43	BUB DATA BIT 06 (BD06[1])	INPUT/OUTPUT
44	BUB DATA BIT 05 (BD05[1])	INPUT/OUTPUT
45	BUB DATA BIT 04 (BD04[1])	INPUT/OUTPUT
46	GROUND (GRD)	GROUND
47	BUB DATA BIT 03 (BD03[1])	INPUT/OUTPUT
48	BUB DATA BIT 02 (BD02[1])	INPUT/OUTPUT
49	BUB DATA BIT 00 (BD00[1])	INPUT/OUTPUT
50	BUB DATA BIT 01 (BD01[1])	INPUT/OUTPUT
51	GROUND (GRD)	GROUND
52	NOT USED	NC
53	NOT USED	NC
54	NOT USED	NC
55	NOT USED	NC
56	+5V (VCC)	POWER
57	BUB ADDRESS BIT 26 (BA26[1])	INPUT/OUTPUT
58	BUB ADDRESS BIT 25 (BA25[1])	INPUT/OUTPUT
59	BUB ADDRESS BIT 24 (BA24[1])	INPUT/OUTPUT
60	BUB ADDRESS BIT 23 (BA23[1])	INPUT/OUTPUT

120-PIN PE CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
61	BUB ADDRESS BIT 22 (BA22[1])	INPUT/OUTPUT
62	BUB ADDRESS BIT 21 (BA21[1])	INPUT/OUTPUT
63	GROUND (GRD)	GROUND
64	BUB ADDRESS BIT 20 (BA20[1])	INPUT/OUTPUT
65	BUB ADDRESS BIT 12 (BA12[1])	INPUT/OUTPUT
66	BUB ADDRESS BIT 19 (BA19[1])	INPUT/OUTPUT
67	BUB ADDRESS BIT 18 (BA18[1])	INPUT/OUTPUT
68	BUB ADDRESS BIT 17 (BA17[1])	INPUT/OUTPUT
69	BUB ADDRESS BIT 16 (BA16[1])	INPUT/OUTPUT
70	GROUND (GRD)	GROUND
71	BUB ADDRESS BIT 15 (BA15[1])	INPUT/OUTPUT
72	BUB ADDRESS BIT 14 (BA14[1])	INPUT/OUTPUT
73	GROUND (GRD)	GROUND
74	BUB ADDRESS BIT 13 (BA13[1])	INPUT/OUTPUT
75	+5V (VCC)	POWER
76	SYSTEM RESET (SYSRST[0])	INPUT
77	NOT USED	NC
78	BUB ADDRESS BIT 27 (BA27[1])	INPUT/OUTPUT
79	PBUS INTERLOCK (UINTLK[0])	OUTPUT
80	GROUND (GRD)	GROUND
81	BUB ADDRESS BIT 11 (BA11[1])	INPUT/OUTPUT
82	BUB ADDRESS BIT 10 (BA10[1])	INPUT/OUTPUT
83	BUB ADDRESS BIT 09 (BA09[1])	INPUT/OUTPUT
84	BUB ADDRESS BIT 08 (BA08[1])	INPUT/OUTPUT
85	BUB ADDRESS BIT 07 (BA07[1])	INPUT/OUTPUT
86	BUB ADDRESS BIT 06 (BA06[1])	INPUT/OUTPUT
87	GROUND (GRD)	GROUND
88	BUB ADDRESS BIT 05 (BA05[1])	INPUT/OUTPUT
89	GROUND (GRD)	GROUND
90	BUB ADDRESS BIT 04 (BA04[1])	INPUT/OUTPUT
91	BUB ADDRESS BIT 03 (BA03[1])	INPUT/OUTPUT
92	BUB ADDRESS BIT 02 (BA02[1])	INPUT/OUTPUT
93	BUB ADDRESS BIT 01 (BA01[1])	INPUT/OUTPUT
94	+5V (VCC)	POWER
95	BUB ADDRESS BIT 00 (BA00[1])	INPUT/OUTPUT
96	NOT USED	NC
97	NOT USED	NC
98	NOT USED	NC
99	GROUND (GRD)	GROUND
100	NOT USED	NC
101	PBUS READ/WRITE (UR1W0)	OUTPUT
102	+5V (VCC)	POWER
103	PBUS CONNECTOR CHIP SELECT (UPCS[0])	INPUT
104	GROUND (GRD)	GROUND
105	PBUS DATA SIZE BIT 0 (UDSIZE0[1])	INPUT/OUTPUT
106	PBUS DATA SIZE BIT 1 (UDSIZE1[1])	INPUT/OUTPUT
107	PBUS ADDRESS STROBE (UAS[0])	OUTPUT
108	NOT USED	NC
109	PBUS MEMORY ACCESS (CPUMEM[0])	OUTPUT
110	CPU LATCH (CPULTCH[1])	INPUT
111	+5V (VCC)	POWER
112	PBUS FAULT (UFLT[0])	INPUT
113	PBUS OUTPUT ENABLE (CBALOE[0])	INPUT
114	PBUS DATA ACKNOWLEDGE (UDTCK[0])	INPUT
115	PBUS DATA STROBE (BDS[0])	INPUT/OUTPUT
116	BUB ADDRESS STROBE (BAS[0])	INPUT
117	BUB DATA ACKNOWLEDGE (BDTCK[0])	OUTPUT
118	GROUND (GRD)	GROUND
119	NOT USED	NC
120	NOT USED	NC

LEGEND:

NC No Connection

CM525B VMEbus CARD INTERCONNECTIONS

The CM525B Versa Modula Europa bus (VMEbus) Card interconnections include the following:

- Two 120-pin card edge connections
- Four 37n miniature D-type connectors.

Figure B-34 shows the layout of the CM525B VMEbus Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

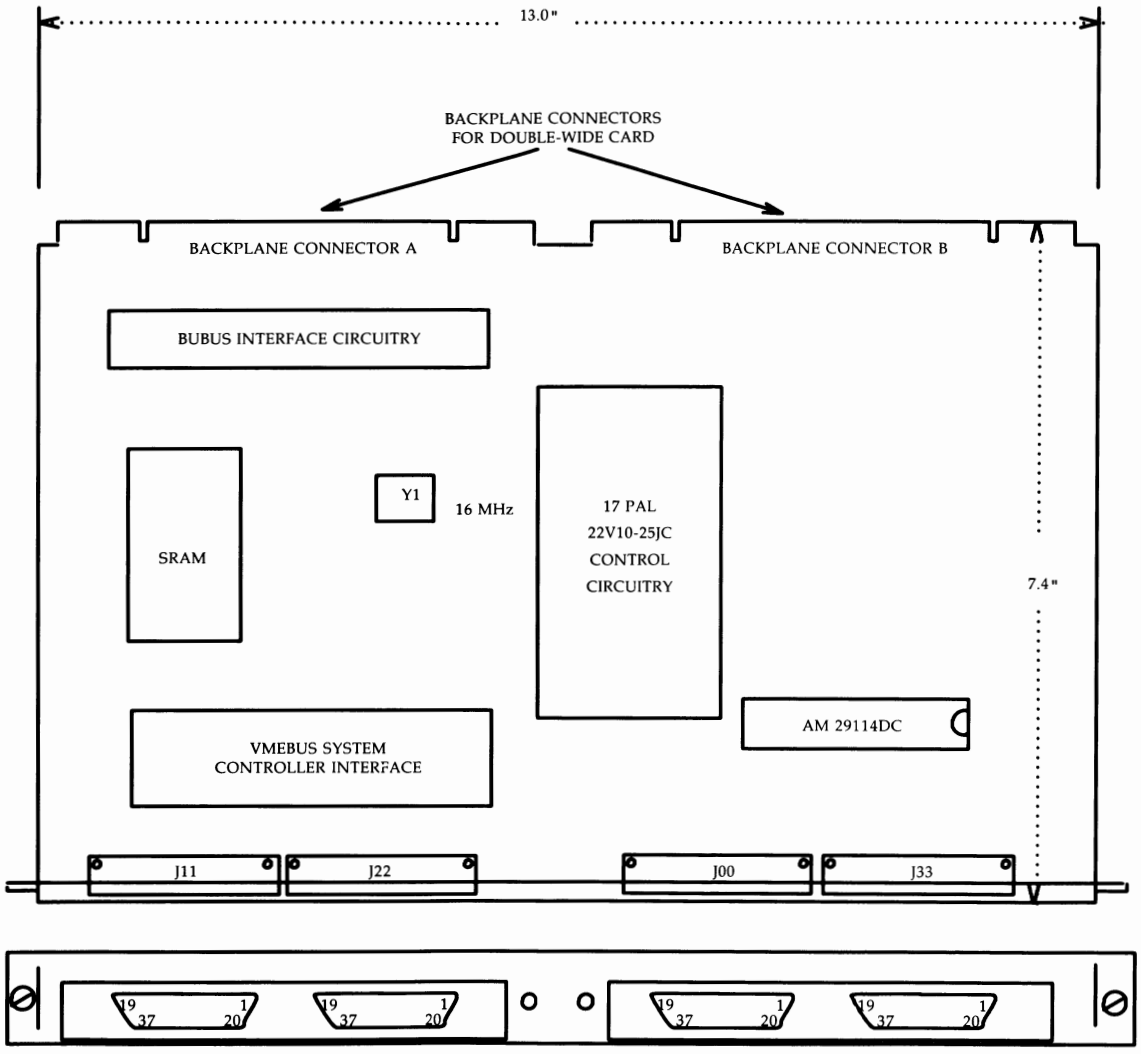


Figure B-34: CM525B VMEbus Card Layout

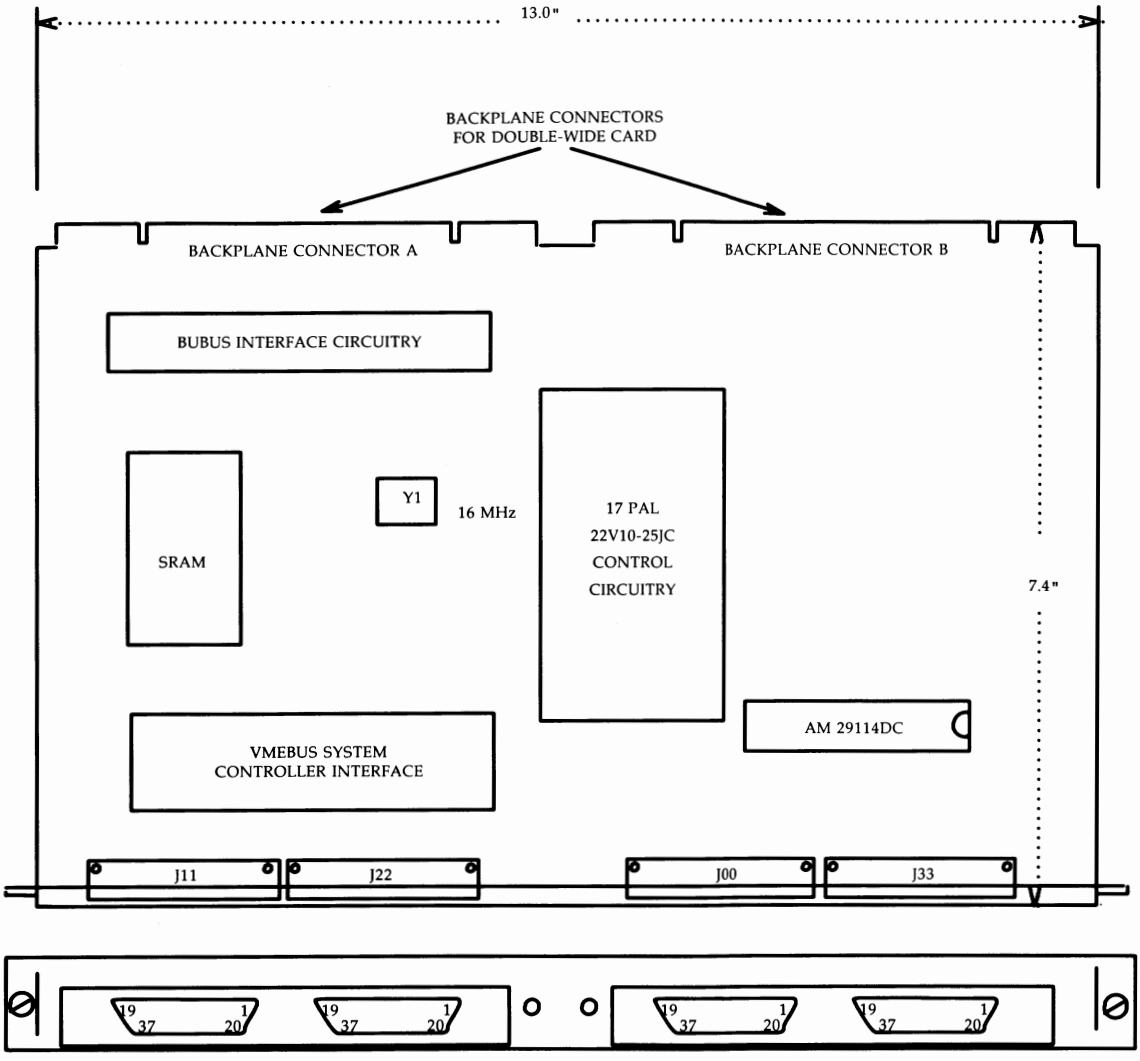


Figure B-34: CM525B VMEbus Card Layout

120-PIN VMEbus CARD EDGE CONNECTIONS, CONNECTOR A		
PIN	**DESCRIPTION**	**FUNCTION**
1	BUB CONNECTOR INHIBIT SLOT 0 (BINHIB0[0])	INPUT
2	GROUND (GRD)	GROUND
3	NOT USED	NC
4	NOT USED	NC
5	NOT USED	NC
6	+5V (VCC)	POWER
7	BUB INTERRUPT LEVEL 14 (BINT14[0])	OUTPUT
8	GROUND (GRD)	GROUND
9	BUB FAILURE (BFAIL[0])	OUTPUT
10	BUB DATA BIT 31 (BD31[1])	INPUT/OUTPUT
11	BUB DATA BIT 30 (BD30[1])	INPUT/OUTPUT
12	BUB DATA BIT 29 (BD29[1])	INPUT/OUTPUT
13	BUB DATA BIT 28 (BD28[1])	INPUT/OUTPUT
14	GROUND (GRD)	GROUND
15	+5V (VCC)	POWER
16	BUB DATA BIT 26 (BD26[1])	INPUT/OUTPUT
17	BUB DATA BIT 27 (BD27[1])	INPUT/OUTPUT
18	BUB DATA BIT 25 (BD25[1])	INPUT/OUTPUT
19	BUB DATA BIT 24 (BD24[1])	INPUT/OUTPUT
20	GROUND (GRD)	GROUND
21	BUB DATA BIT 22 (BD22[1])	INPUT/OUTPUT
22	BUB DATA BIT 23 (BD23[1])	INPUT/OUTPUT
23	BUB DATA BIT 21 (BD21[1])	INPUT/OUTPUT
24	BUB DATA BIT 20 (BD20[1])	INPUT/OUTPUT
25	BUB DATA BIT 18 (BD18[1])	INPUT/OUTPUT
26	BUB DATA BIT 19 (BD19[1])	INPUT/OUTPUT
27	GROUND (GRD)	GROUND
28	BUB DATA BIT 17 (BD17[1])	INPUT/OUTPUT
29	BUB DATA BIT 16 (BD16[1])	INPUT/OUTPUT
30	BUB DATA BIT 14 (BD14[1])	INPUT/OUTPUT
31	BUB DATA BIT 15 (BD15[1])	INPUT/OUTPUT
32	+5V (VCC)	POWER
33	BUB DATA BIT 12 (BD12[1])	INPUT/OUTPUT
34	BUB DATA BIT 13 (BD13[1])	INPUT/OUTPUT
35	NOT USED	NC
36	BUB DATA BIT 11 (BD11[1])	INPUT/OUTPUT
37	BUB DATA BIT 10 (BD10[1])	INPUT/OUTPUT
38	NOT USED	NC
39	GROUND (GRD)	GROUND
40	BUB DATA BIT 08 (BD08[1])	INPUT/OUTPUT
41	BUB DATA BIT 09 (BD09[1])	INPUT/OUTPUT
42	BUB DATA BIT 07 (BD07[1])	INPUT/OUTPUT
43	BUB DATA BIT 06 (BD06[1])	INPUT/OUTPUT
44	BUB DATA BIT 05 (BD05[1])	INPUT/OUTPUT
45	BUB DATA BIT 04 (BD04[1])	INPUT/OUTPUT
46	GROUND (GRD)	GROUND
47	BUB DATA BIT 03 (BD03[1])	INPUT/OUTPUT
48	BUB DATA BIT 02 (BD02[1])	INPUT/OUTPUT
49	BUB DATA BIT 00 (BD00[1])	INPUT/OUTPUT
50	BUB DATA BIT 01 (BD01[1])	INPUT/OUTPUT
51	GROUND (GRD)	GROUND
52	BUB DATA PARITY BIT 0 (BDP0[1])	INPUT/OUTPUT
53	BUB DATA PARITY BIT 1 (BDP1[1])	INPUT/OUTPUT
54	BUB DATA PARITY BIT 3 (BDP3[1])	INPUT/OUTPUT
55	BUB DATA PARITY BIT 2 (BDP2[1])	INPUT/OUTPUT
56	+5V (VCC)	POWER
57	BUB ADDRESS BIT 26 (BA26[1])	INPUT/OUTPUT
58	BUB ADDRESS BIT 25 (BA25[1])	INPUT/OUTPUT
59	BUB ADDRESS BIT 24 (BA24[1])	INPUT/OUTPUT
60	BUB ADDRESS BIT 23 (BA23[1])	INPUT/OUTPUT

120-PIN VMEbus CARD EDGE CONNECTIONS, CONNECTOR A (Contd)		
PIN	DESCRIPTION	FUNCTION
61	BUB ADDRESS BIT 22 (BA22[1])	INPUT/OUTPUT
62	BUB ADDRESS BIT 21 (BA21[1])	INPUT/OUTPUT
63	GROUND (GRD)	GROUND
64	BUB ADDRESS BIT 20 (BA20[1])	INPUT/OUTPUT
65	BUB ADDRESS BIT 12 (BA12[1])	INPUT/OUTPUT
66	BUB ADDRESS BIT 19 (BA19[1])	INPUT/OUTPUT
67	BUB ADDRESS BIT 18 (BA18[1])	INPUT/OUTPUT
68	BUB ADDRESS BIT 17 (BA17[1])	INPUT/OUTPUT
69	BUB ADDRESS BIT 16 (BA16[1])	INPUT/OUTPUT
70	GROUND (GRD)	GROUND
71	BUB ADDRESS BIT 15 (BA15[1])	INPUT/OUTPUT
72	BUB ADDRESS BIT 14 (BA14[1])	INPUT/OUTPUT
73	GROUND (GRD)	GROUND
74	BUB ADDRESS BIT 13 (BA13[1])	INPUT/OUTPUT
75	+5V (VCC)	POWER
76	SYSTEM RESET (SYSRST[0])	INPUT
77	NOT USED	NC
78	BUB ADDRESS BIT 27 (BA27[1])	INPUT/OUTPUT
79	NOT USED	NC
80	GROUND (GRD)	GROUND
81	BUB ADDRESS BIT 11 (BA11[1])	INPUT/OUTPUT
82	BUB ADDRESS BIT 10 (BA10[1])	INPUT/OUTPUT
83	BUB ADDRESS BIT 09 (BA09[1])	INPUT/OUTPUT
84	BUB ADDRESS BIT 08 (BA08[1])	INPUT/OUTPUT
85	BUB ADDRESS BIT 07 (BA07[1])	INPUT/OUTPUT
86	BUB ADDRESS BIT 06 (BA06[1])	INPUT/OUTPUT
87	GROUND (GRD)	GROUND
88	BUB ADDRESS BIT 05 (BA05[1])	INPUT/OUTPUT
89	GROUND (GRD)	GROUND
90	BUB ADDRESS BIT 04 (BA04[1])	INPUT/OUTPUT
91	BUB ADDRESS BIT 03 (BA03[1])	INPUT/OUTPUT
92	BUB ADDRESS BIT 02 (BA02[1])	INPUT/OUTPUT
93	BUB ADDRESS BIT 01 (BA01[1])	INPUT/OUTPUT
94	+5V (VCC)	POWER
95	BUB ADDRESS BIT 00 (BA00[1])	INPUT/OUTPUT
96	BUB ADDRESS PARITY BIT 0 (BAP0[1])	INPUT/OUTPUT
97	BUB ADDRESS PARITY BIT 2 (BAP2[1])	INPUT/OUTPUT
98	BUB ADDRESS PARITY BIT 1 (BAP1[1])	INPUT/OUTPUT
99	GROUND (GRD)	GROUND
100	BUB ADDRESS PARITY BIT 3 (BAP3[1])	INPUT/OUTPUT
101	BUB READ/WRITE (BR1W0)	INPUT/OUTPUT
102	+5V (VCC)	POWER
103	BUB CONNECTOR CHIP SELECT (BCCS[0])	INPUT
104	GROUND (GRD)	GROUND
105	BUB DATA SIZE BIT 0 (BDSIZE0[1])	INPUT/OUTPUT
106	BUB DATA SIZE BIT 1 (BDSIZE1[1])	INPUT/OUTPUT
107	BUB SEQUENTIAL ACCESS (BSEQACC[0])	OUTPUT
108	BUB PARITY CHECK (BPCHECK[0])	OUTPUT
109	BUB REQUEST (BUBRQ[0])	OUTPUT
110	NOT USED	NC
111	+5V (VCC)	POWER
112	BUB FAULT (BFLT[0])	INPUT/OUTPUT
113	BUB GRANTED (BUBGT[0])	INPUT
114	NOT USED	NC
115	BUB DATA STROBE (BDS[0])	INPUT/OUTPUT
116	BUB ADDRESS STROBE (BAS[0])	INPUT
117	BUB DATA ACKNOWLEDGE (BDTCK[0])	INPUT/OUTPUT
118	GROUND (GRD)	GROUND
119	NOT USED	NC
120	NOT USED	NC

LEGEND:

NC No Connection

Backplane Connector B is used to supply VCC and Ground. Any pins that are not listed in the following table are NOT USED.

VMEbus BACKPLANE CONNECTOR B	
VCC	GROUND
002	001
023	007
024	008
043	011
044	012
056	017
076	018
079	031
100	032
103	035
120	036
	039
	040
	047
	048
	051
	052
	055
	059
	060
	063
	068
	071
	084
	087
	092
	095
	108
	111
	116
	119

37-PIN VME XBUS CONNECTIONS, J00		
PIN	**DESCRIPTION**	**FUNCTION**
01	GROUND	GROUND
02	XBUS RESET (XRESET[1])	INPUT
03	XBUS DATA STROBE 0 (XDS0[1])	INPUT
04	XBUS FAIL (XSFAIL[1])	INPUT
05	XBUS DATA ACKNOWLEDGE (XDTACK[1])	INPUT
06	XBUS READ/WRITE (XR0W1)	INPUT/OUTPUT
07	XBUS INTERRUPT REQUEST BIT 4 (XIRQ4[1])	INPUT
08	XBUS INTERRUPT REQUEST BIT 3 (XIRQ3[1])	INPUT
09	XBUS ADDRESS PARITY BIT 1 (XADP1[0])	INPUT/OUTPUT
10	XBUS ADDRESS PARITY BIT 2 (XADP2[0])	INPUT/OUTPUT
11	XBUS ADDRESS PARITY BIT 3 (XADP3[0])	INPUT/OUTPUT
12	XBUS ADDRESS ACKNOWLEDGE (XAACK[1])	OUTPUT
13	XBUS ADDRESS PARITY BIT 0 (XADP0[0])	INPUT/OUTPUT
14	XBUS INTERRUPT REQUEST BIT 2 (XIRQ2[1])	INPUT
15	XBUS ADDRESS STROBE (XAS[1])	INPUT
16	XBUS ERROR (XBERR[1])	INPUT
17	XBUS INTERRUPT REQUEST BIT 1 (XIRQ1[1])	INPUT
18	NOT USED	NC
19	NOT USED	NC
20	GROUND	GROUND
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	GROUND	GROUND
26	GROUND	GROUND
27	GROUND	GROUND
28	GROUND	GROUND
29	GROUND	GROUND
30	GROUND	GROUND
31	GROUND	GROUND
32	GROUND	GROUND
33	GROUND	GROUND
34	GROUND	GROUND
35	GROUND	GROUND
36	GROUND	GROUND
37	NOT USED	NC

LEGEND:

NC No Connection

37-PIN VME XBUS CONNECTIONS, J11		
PIN	**DESCRIPTION**	**FUNCTION**
01	GROUND	GROUND
02	XBUS ADDRESS 30 (XAD30[0])	INPUT/OUTPUT
03	XBUS ADDRESS 25 (XAD25[0])	INPUT/OUTPUT
04	XBUS ADDRESS 31 (XAD31[0])	INPUT/OUTPUT
05	XBUS ADDRESS 26 (XAD26[0])	INPUT/OUTPUT
06	XBUS ADDRESS 27 (XAD27[0])	INPUT/OUTPUT
07	XBUS ADDRESS 28 (XAD28[0])	INPUT/OUTPUT
08	XBUS ADDRESS 29 (XAD29[0])	INPUT/OUTPUT
09	XBUS ADDRESS 22 (XAD22[0])	INPUT/OUTPUT
10	XBUS ADDRESS 23 (XAD23[0])	INPUT/OUTPUT
11	XBUS ADDRESS 24 (XAD24[0])	INPUT/OUTPUT
12	XBUS ADDRESS 20 (XAD20[0])	INPUT/OUTPUT
13	XBUS ADDRESS 21 (XAD21[0])	INPUT/OUTPUT
14	XBUS ADDRESS 18 (XAD18[0])	INPUT/OUTPUT
15	XBUS ADDRESS 19 (XAD19[0])	INPUT/OUTPUT
16	XBUS ADDRESS 16 (XAD16[0])	INPUT/OUTPUT
17	XBUS ADDRESS 17 (XAD17[0])	INPUT/OUTPUT
18	NOT USED	NC
19	NOT USED	NC
20	GROUND	GROUND
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	GROUND	GROUND
26	GROUND	GROUND
27	GROUND	GROUND
28	GROUND	GROUND
29	GROUND	GROUND
30	GROUND	GROUND
31	GROUND	GROUND
32	GROUND	GROUND
33	GROUND	GROUND
34	GROUND	GROUND
35	GROUND	GROUND
36	GROUND	GROUND
37	NOT USED	NC

LEGEND:

NC No Connection

37-PIN VME XBUS CONNECTIONS, J22		
PIN	DESCRIPTION	FUNCTION
01	GROUND	GROUND
02	XBUS ADDRESS 14 (XAD14[0])	INPUT/OUTPUT
03	XBUS ADDRESS 09 (XAD09[0])	INPUT/OUTPUT
04	XBUS ADDRESS 15 (XAD15[0])	INPUT/OUTPUT
05	XBUS ADDRESS 10 (XAD10[0])	INPUT/OUTPUT
06	XBUS ADDRESS 11 (XAD11[0])	INPUT/OUTPUT
07	XBUS ADDRESS 12 (XAD12[0])	INPUT/OUTPUT
08	XBUS ADDRESS 13 (XAD13[0])	INPUT/OUTPUT
09	XBUS ADDRESS 06 (XAD06[0])	INPUT/OUTPUT
10	XBUS ADDRESS 07 (XAD07[0])	INPUT/OUTPUT
11	XBUS ADDRESS 08 (XAD08[0])	INPUT/OUTPUT
12	XBUS ADDRESS 04 (XAD04[0])	INPUT/OUTPUT
13	XBUS ADDRESS 05 (XAD05[0])	INPUT/OUTPUT
14	XBUS ADDRESS 02 (XAD02[0])	INPUT/OUTPUT
15	XBUS ADDRESS 03 (XAD03[0])	INPUT/OUTPUT
16	XBUS ADDRESS 00 (XAD00[0])	INPUT/OUTPUT
17	XBUS ADDRESS 01 (XAD01[0])	INPUT/OUTPUT
18	NOT USED	NC
19	NOT USED	NC
20	GROUND	GROUND
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	GROUND	GROUND
26	GROUND	GROUND
27	GROUND	GROUND
28	GROUND	GROUND
29	GROUND	GROUND
30	GROUND	GROUND
31	GROUND	GROUND
32	GROUND	GROUND
33	GROUND	GROUND
34	GROUND	GROUND
35	GROUND	GROUND
36	GROUND	GROUND
37	NOT USED	NC

LEGEND:

NC No Connection

37-PIN VME XBUS CONNECTIONS, J33		
PIN	**DESCRIPTION**	**FUNCTION**
01	GROUND	GROUND
02	GROUND	GROUND
03	NOT USED	NC
04	GROUND	GROUND
05	XBUS INTERRUPT REQUEST BIT 7 (XIRQ7[1])	INPUT
06	XBUS INTERRUPT REQUEST BIT 6 (XIRQ6[1])	INPUT
07	XBUS INTERRUPT REQUEST BIT 5 (XIRQ5[1])	INPUT
08	GROUND	GROUND
09	XBUS DATA STROBE 1 (XDS1[1])	INPUT
10	XBUS DATA STROBE 2 (XDS2[1])	INPUT
11	GROUND	GROUND
12	XBUS SEQUENCE (XSEQ[1])	INPUT
13	XBUS INTERRUPT ACKNOWLEDGE (XIACK[1])	OUTPUT
14	XBUS LOCK (XLOCK[1])	INPUT
15	XBUS DATA STROBE 3 (XDS3[1])	INPUT
16	XBUS REQUEST (XBREQ[1])	OUTPUT
17	XBUS GRANTED (XBUSGRT[1])	OUTPUT
18	NOT USED	NC
19	NOT USED	NC
20	GROUND	GROUND
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	GROUND	GROUND
26	GROUND	GROUND
27	GROUND	GROUND
28	GROUND	GROUND
29	GROUND	GROUND
30	GROUND	GROUND
31	GROUND	GROUND
32	GROUND	GROUND
33	GROUND	GROUND
34	GROUND	GROUND
35	GROUND	GROUND
36	GROUND	GROUND
37	NOT USED	NC

LEGEND:

NC No Connection

CM527A MULTIPROCESSOR ENHANCEMENT CARD INTERCONNECTIONS

The CM527A Multiprocessor Enhancement (MPE) Card interconnection consists of a 120-pin card edge connection. Figure B-35 shows the layout of the CM527A MPE Card. Refer to this figure for card connector location information. Pin and signal information is provided in tables following the figure for each of the card connectors. The figure is printed front and back with a blank unit so that the figure can be used in conjunction with any table.

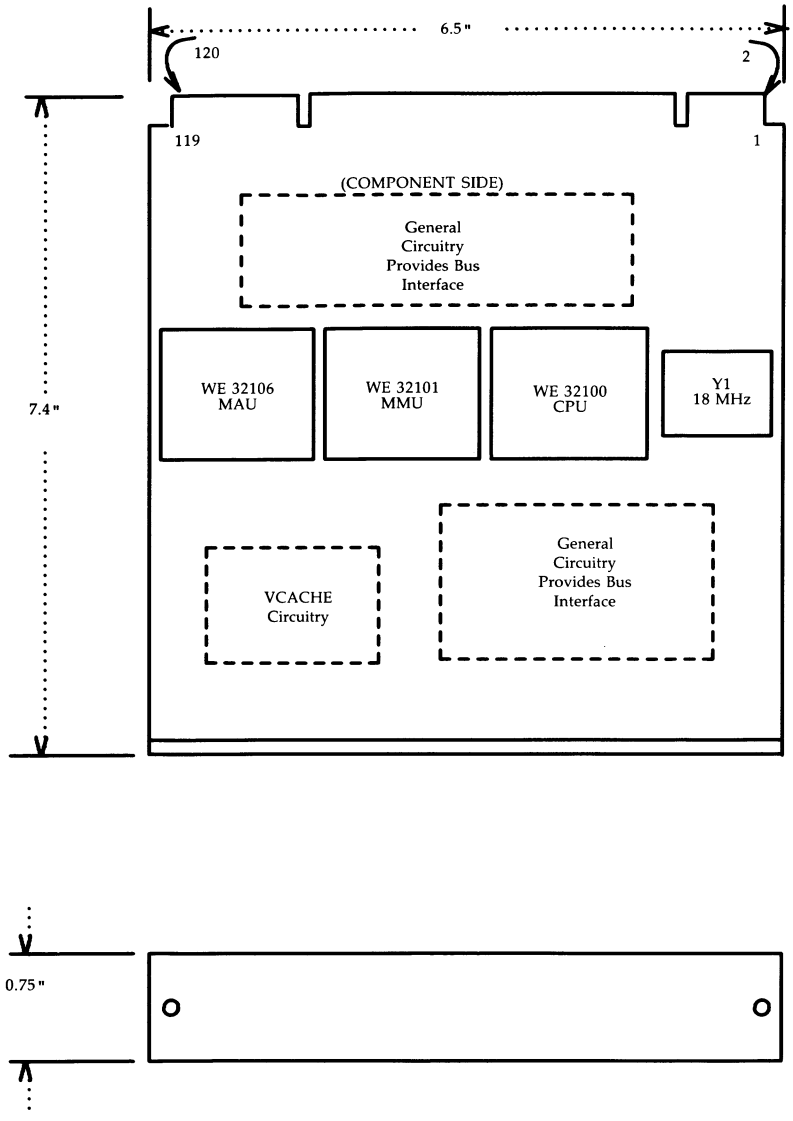


Figure B-35: CM527A MPE Card Layout

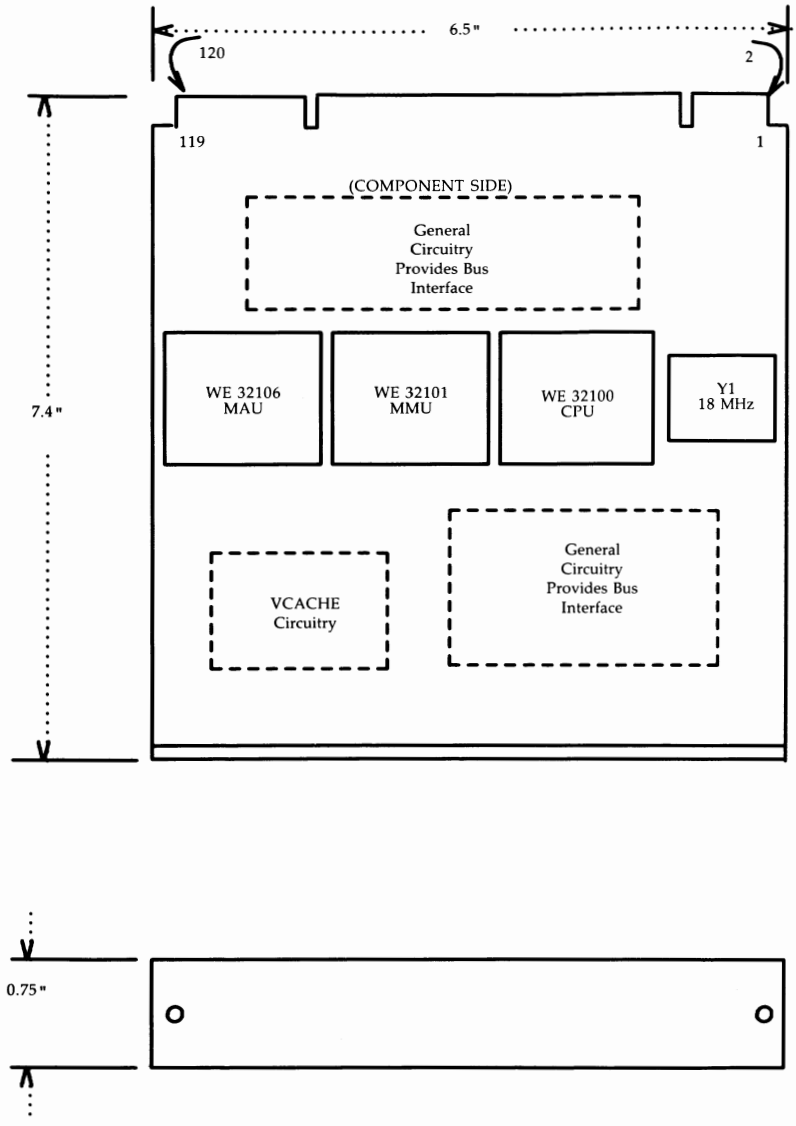


Figure B-35: CM527A MPE Card Layout

120-PIN MPE CARD EDGE CONNECTIONS		
PIN	**DESCRIPTION**	**FUNCTION**
1	BUB CONNECTOR INHIBIT SLOT 0 (BINHIB0[0])	INPUT
2	GROUND (GRD)	GROUND
3	OPERATIONAL INTERRUPT LEVEL 15 (OPINT15[0])	OUTPUT
4	NOT USED	NC
5	NOT USED	NC
6	+5V (VCC)	POWER
7	NOT USED	NC
8	GROUND (GRD)	GROUND
9	NOT USED	NC
10	BUB DATA BIT 31 (BD31[1])	INPUT/OUTPUT
11	BUB DATA BIT 30 (BD30[1])	INPUT/OUTPUT
12	BUB DATA BIT 29 (BD29[1])	INPUT/OUTPUT
13	BUB DATA BIT 28 (BD28[1])	INPUT/OUTPUT
14	GROUND (GRD)	GROUND
15	+5V (VCC)	POWER
16	BUB DATA BIT 26 (BD26[1])	INPUT/OUTPUT
17	BUB DATA BIT 27 (BD27[1])	INPUT/OUTPUT
18	BUB DATA BIT 25 (BD25[1])	INPUT/OUTPUT
19	BUB DATA BIT 24 (BD24[1])	INPUT/OUTPUT
20	GROUND (GRD)	GROUND
21	BUB DATA BIT 22 (BD22[1])	INPUT/OUTPUT
22	BUB DATA BIT 23 (BD23[1])	INPUT/OUTPUT
23	BUB DATA BIT 21 (BD21[1])	INPUT/OUTPUT
24	BUB DATA BIT 20 (BD20[1])	INPUT/OUTPUT
25	BUB DATA BIT 18 (BD18[1])	INPUT/OUTPUT
26	BUB DATA BIT 19 (BD19[1])	INPUT/OUTPUT
27	GROUND (GRD)	GROUND
28	BUB DATA BIT 17 (BD17[1])	INPUT/OUTPUT
29	BUB DATA BIT 16 (BD16[1])	INPUT/OUTPUT
30	BUB DATA BIT 14 (BD14[1])	INPUT/OUTPUT
31	BUB DATA BIT 15 (BD15[1])	INPUT/OUTPUT
32	+5V (VCC)	POWER
33	BUB DATA BIT 12 (BD12[1])	INPUT/OUTPUT
34	BUB DATA BIT 13 (BD13[1])	INPUT/OUTPUT
35	NOT USED	NC
36	BUB DATA BIT 11 (BD11[1])	INPUT/OUTPUT
37	BUB DATA BIT 10 (BD10[1])	INPUT/OUTPUT
38	NOT USED	NC
39	GROUND (GRD)	GROUND
40	BUB DATA BIT 08 (BD08[1])	INPUT/OUTPUT
41	BUB DATA BIT 09 (BD09[1])	INPUT/OUTPUT
42	BUB DATA BIT 07 (BD07[1])	INPUT/OUTPUT
43	BUB DATA BIT 06 (BD06[1])	INPUT/OUTPUT
44	BUB DATA BIT 05 (BD05[1])	INPUT/OUTPUT
45	BUB DATA BIT 04 (BD04[1])	INPUT/OUTPUT
46	GROUND (GRD)	GROUND
47	BUB DATA BIT 03 (BD03[1])	INPUT/OUTPUT
48	BUB DATA BIT 02 (BD02[1])	INPUT/OUTPUT
49	BUB DATA BIT 00 (BD00[1])	INPUT/OUTPUT
50	BUB DATA BIT 01 (BD01[1])	INPUT/OUTPUT
51	GROUND (GRD)	GROUND
52	NOT USED	NC
53	NOT USED	NC
54	NOT USED	NC
55	NOT USED	NC
56	+5V (VCC)	POWER
57	BUB ADDRESS BIT 26 (BA26[1])	INPUT/OUTPUT
58	BUB ADDRESS BIT 25 (BA25[1])	INPUT/OUTPUT
59	BUB ADDRESS BIT 24 (BA24[1])	INPUT/OUTPUT
60	BUB ADDRESS BIT 23 (BA23[1])	INPUT/OUTPUT

120-PIN MPE CARD EDGE CONNECTIONS (Contd)		
PIN	DESCRIPTION	FUNCTION
61	BUB ADDRESS BIT 22 (BA22[1])	INPUT/OUTPUT
62	BUB ADDRESS BIT 21 (BA21[1])	INPUT/OUTPUT
63	GROUND (GRD)	GROUND
64	BUB ADDRESS BIT 20 (BA20[1])	INPUT/OUTPUT
65	BUB ADDRESS BIT 12 (BA12[1])	INPUT/OUTPUT
66	BUB ADDRESS BIT 19 (BA19[1])	INPUT/OUTPUT
67	BUB ADDRESS BIT 18 (BA18[1])	INPUT/OUTPUT
68	BUB ADDRESS BIT 17 (BA17[1])	INPUT/OUTPUT
69	BUB ADDRESS BIT 16 (BA16[1])	INPUT/OUTPUT
70	GROUND (GRD)	GROUND
71	BUB ADDRESS BIT 15 (BA15[1])	INPUT/OUTPUT
72	BUB ADDRESS BIT 14 (BA14[1])	INPUT/OUTPUT
73	GROUND (GRD)	GROUND
74	BUB ADDRESS BIT 13 (BA13[1])	INPUT/OUTPUT
75	+5V (VCC)	POWER
76	SYSTEM RESET (SYSRST[0])	INPUT
77	NOT USED	NC
78	BUB ADDRESS BIT 27 (BA27[1])	INPUT/OUTPUT
79	BUB BUSY (BUSY[0])	OUTPUT
80	GROUND (GRD)	GROUND
81	BUB ADDRESS BIT 11 (BA11[1])	INPUT/OUTPUT
82	BUB ADDRESS BIT 10 (BA10[1])	INPUT/OUTPUT
83	BUB ADDRESS BIT 09 (BA09[1])	INPUT/OUTPUT
84	BUB ADDRESS BIT 08 (BA08[1])	INPUT/OUTPUT
85	BUB ADDRESS BIT 07 (BA07[1])	INPUT/OUTPUT
86	BUB ADDRESS BIT 06 (BA06[1])	INPUT/OUTPUT
87	GROUND (GRD)	GROUND
88	BUB ADDRESS BIT 05 (BA05[1])	INPUT/OUTPUT
89	GROUND (GRD)	GROUND
90	BUB ADDRESS BIT 04 (BA04[1])	INPUT/OUTPUT
91	BUB ADDRESS BIT 03 (BA03[1])	INPUT/OUTPUT
92	BUB ADDRESS BIT 02 (BA02[1])	INPUT/OUTPUT
93	BUB ADDRESS BIT 01 (BA01[1])	INPUT/OUTPUT
94	+5V (VCC)	POWER
95	BUB ADDRESS BIT 00 (BA00[1])	INPUT/OUTPUT
96	NOT USED	NC
97	NOT USED	NC
98	NOT USED	NC
99	GROUND (GRD)	GROUND
100	NOT USED	NC
101	BUB READ/WRITE (BR1W0)	INPUT/OUTPUT
102	+5V (VCC)	POWER
103	BUB CONNECTOR CHIP SELECT (BCCS[0])	INPUT
104	GROUND (GRD)	GROUND
105	BUB DATA SIZE BIT 0 (BDSIZE0[1])	INPUT/OUTPUT
106	BUB DATA SIZE BIT 1 (BDSIZE1[1])	INPUT/OUTPUT
107	BUB SEQUENTIAL ACCESS (BSEQACC[0])	OUTPUT
108	NOT USED	NC
109	BUB REQUEST (BUBRQ[0])	OUTPUT
110	NOT USED	NC
111	+5V (VCC)	POWER
112	BUB FAULT (BFLT[0])	INPUT/OUTPUT
113	BUB GRANTED (BUBGT[0])	INPUT
114	NOT USED	NC
115	BUB DATA STROBE (BDS[0])	INPUT/OUTPUT
116	BUB ADDRESS STROBE (BAS[0])	INPUT
117	BUB DATA ACKNOWLEDGE (BDTCK[0])	INPUT/OUTPUT
118	GROUND (GRD)	GROUND
119	NOT USED	NC
120	NOT USED	NC

LEGEND:

NC No Connection

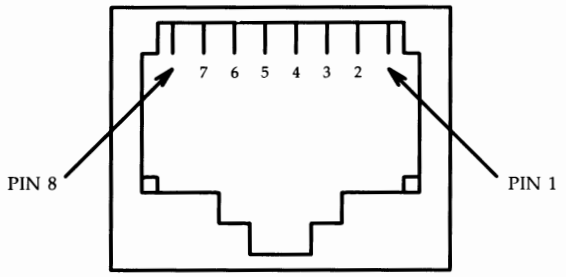
MISCELLANEOUS CONNECTORS AND CABLES

General

The miscellaneous connectors and cables are used to do the following:

- Interface the serial and parallel Input/Output (I/O) ports on the Peripheral Port Controller Card (PORTS) with various peripheral devices
- Interface serial I/O CONSOLE and CONTTY ports with various peripheral devices.

Figure B-36 identifies the CONSOLE, CONTTY, and PORTS 8-pin modular jacks.



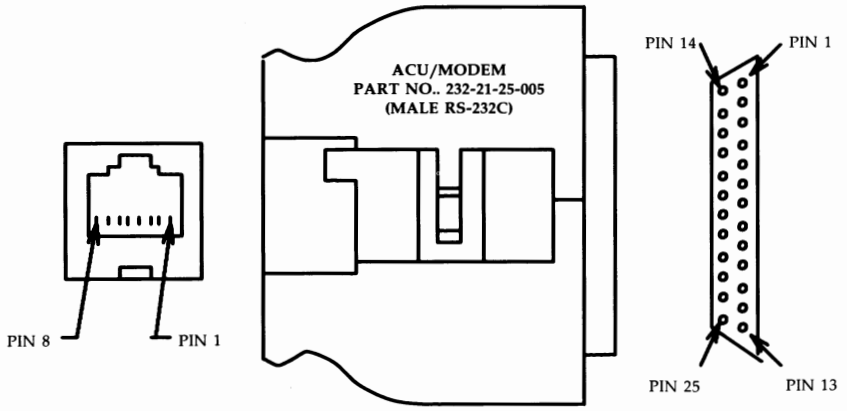
PIN	SIGNAL NAME
8	RESERVED
7	SIGNAL GROUND (SG)
6	DATA CARRIER DETECT (DCD)
5	RECEIVE DATA (RXD)
4	DATA TERMINAL READY (DTR)
3	TRANSMIT DATA (TXD)
2	RESERVED
1	FRAME GROUND (FG)

Figure B-36: CONSOLE, CONTTY, and PORTS 8-Pin Modular Jacks Pin Identification

8-Pin Module to 25-Pin Connectors

ACU/MODEM Connector, 232-21-25-005

Figure B-37 identifies the Automatic Calling Unit (ACU)/MODEM Connector pins. This connector is used to interface an 8-pin modular, RS-232C, serial port to a female, 25-pin, connector on a MODEM configured as Data Communication Equipment (DCE).



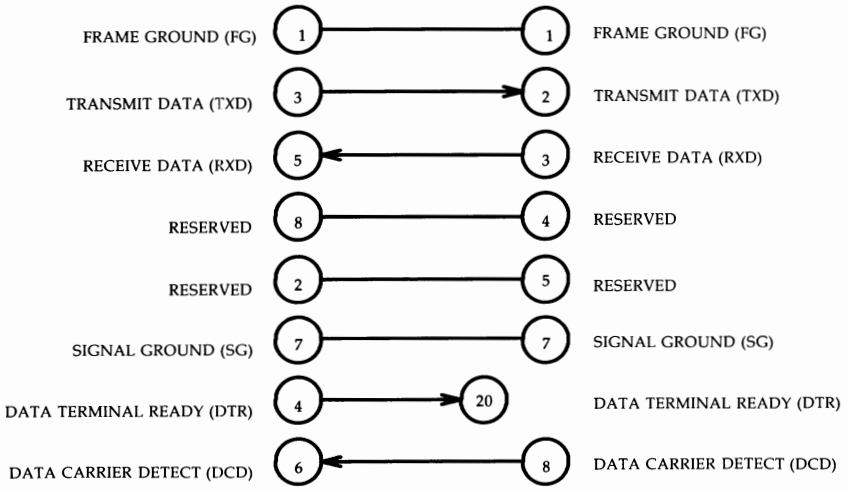


Figure B-37: ACU/MODEM Connector (232-21-25-005) Pin Identification

Terminal/Printer Female Connector, 232-22-25-006

Figure B-38 identifies the Terminal/Printer Female Connector pins. This connector is used to interface the 8-pin modular, RS-232C, serial port to a male 25-pin connector on a terminal or printer connector configured as Data Communication Equipment (DCE).

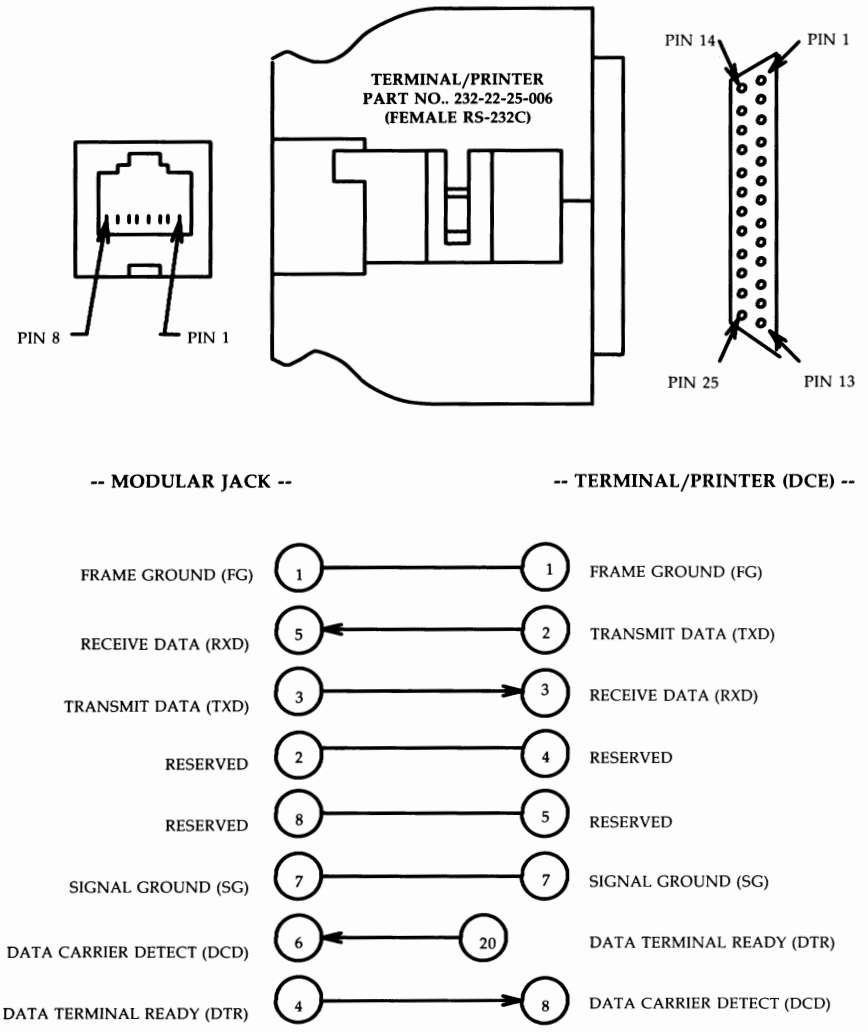


Figure B-38: Terminal/Printer Female Connector (232-22-25-006) Pin Identification

Terminal/Printer Male Connector, 232-21-25-010

Figure B-39 identifies the Terminal/Printer Male Connector pins. This connector is used to interface the 8-pin modular, RS-232C, serial port to a female 25-pin connector on a terminal or printer connector configured as Data Terminal Equipment (DTE).

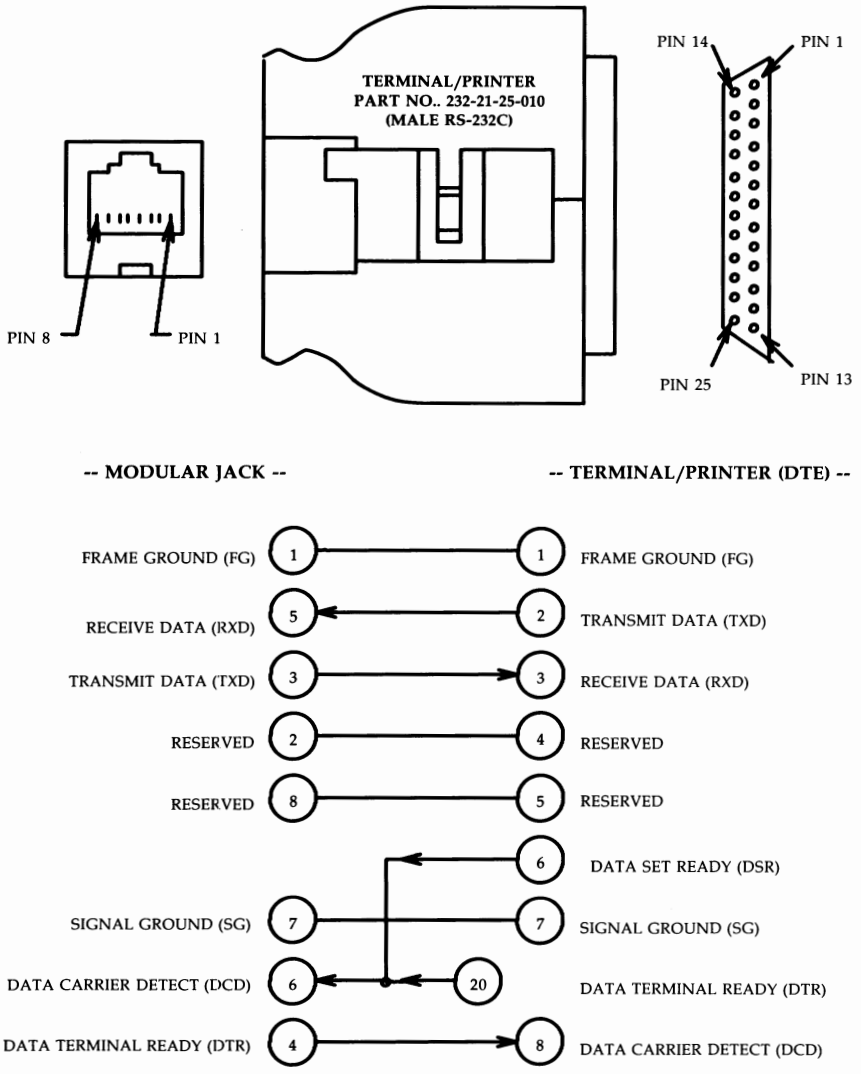


Figure B-39: Terminal/Printer Male Connector (232-21-25-010) Pin Identification

Remote Console Male Connector, 232-21-25-008

Figure B-40 identifies the Remote Console Male Connector pins. This connector is used to interface the 8-pin modular, RS-232C, serial port to a female 25-pin connector on a console terminal configured as Data Communication Equipment (DCE). This connector is also called a dumb MODEM connector.

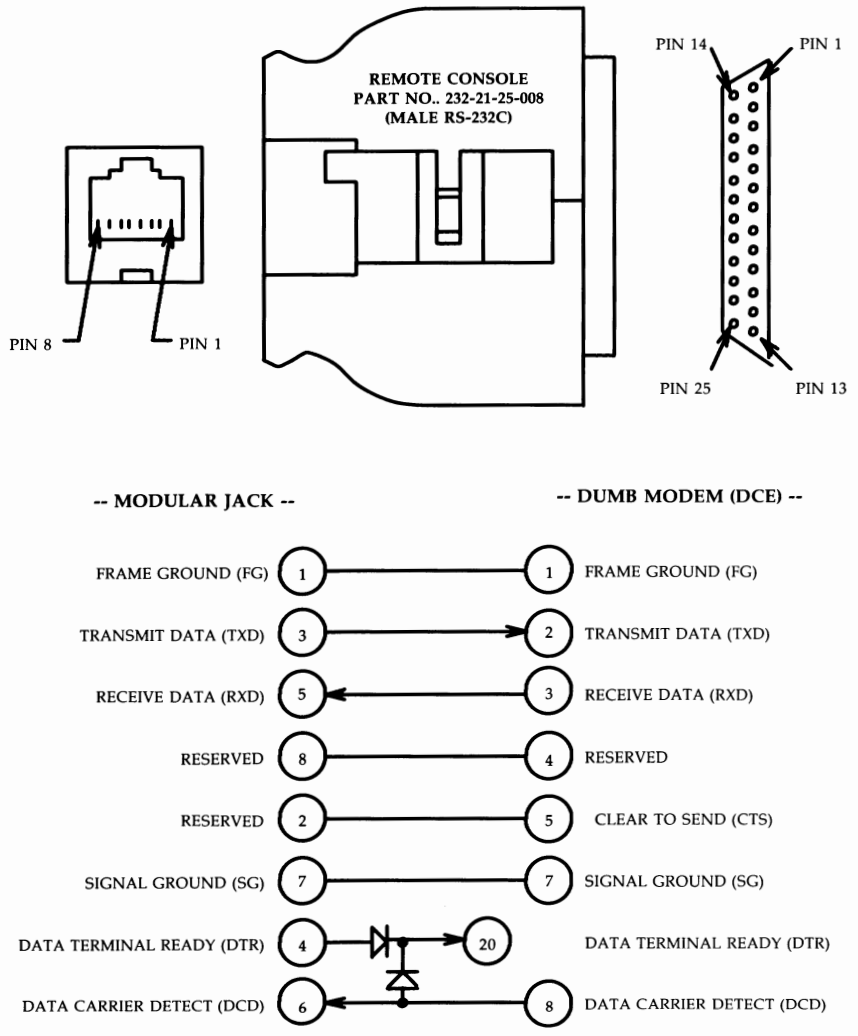


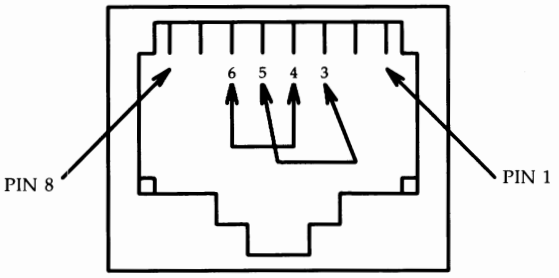
Figure B-40: Remote Console Male Connector (232-21-25-008) Pin Identification

PORTS Loop Around Connections

A minimum of two PORTS Loop Around connectors are required to run certain PORTS interactive diagnostic phases. A PORTS Loop Around connector is an 8-pin modular plug with the following pins tied together:

- Transmit Data (pin 3) tied to Receive Data (pin 5)
- Data Terminal Ready (pin 4) tied to Data Carrier Detect (pin 6).

Figure B-41 shows the PORTS modular jack and plug arrangement.



PIN	SIGNAL NAME
8	RESERVED
7	SIGNAL GROUND (SG)
6	DATA CARRIER DETECT (DCD)
5	RECEIVE DATA (RXD)
4	DATA TERMINAL READY (DTR)
3	TRANSMIT DATA (TXD)
2	RESERVED
1	FRAME GROUND (FG)

Figure B-41: PORTS Loop Around Connections

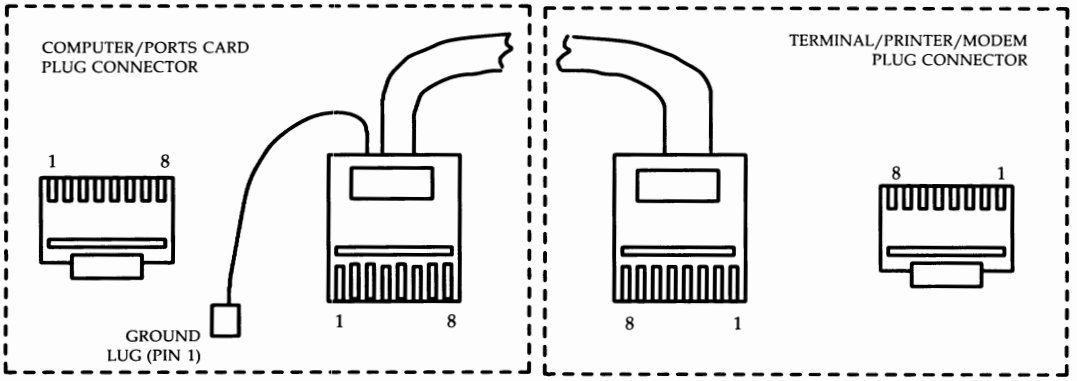
EPORTS Loop Around Connections

The CM195AY EPORTS Card can use the same connections with some modifications. The ground signals (pins 1 and 7) are tied together and pin 8 is tied to Transmit Data (pin 3) before the connection to Receive Data (pin 5).

Terminal/Printer/Peripheral Device Cables

8-Conductor Modular Cables

The 8-conductor modular cables are available in 7-, 14-, 25-, and 50-foot lengths. The pinouts for these connectorized cables are shown in Figure B-42.



PIN	SIGNAL NAME
8	RESERVED (REQUEST TO SEND)
7	SIGNAL GROUND (SG)
6	DATA CARRIER DETECT (DCD)
5	RECEIVE DATA (RXD)
4	DATA TERMINAL READY (DTR)
3	TRANSMIT DATA (TXD)
2	RESERVED (CLEAR TO SEND)
1	FRAME GROUND (FG)

Figure B-42: 8-Conductor Modular Cable Connector Pin Identification

36-Conductor CENTRONICS Connectorized Cable

The 36-conductor CENTRONICS cable is used to connect the parallel port of a Peripheral Controller (PORTS) card to a female CENTRONICS connector of a peripheral device. Figure B-43 shows the pinout for this connectorized cable. The following table identifies the signals carried on this cable. The FUNCTION column is with respect to the PORTS card connection for I/O definitions.

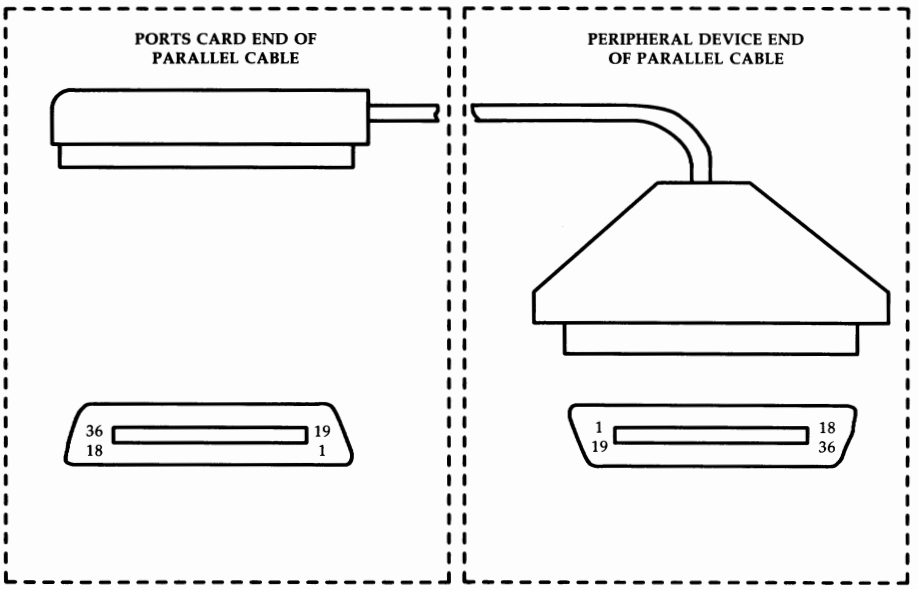


Figure B-43: CENTRONICS Connectorized Cable Pin Identification

36-PIN CENTRONICS CONNECTORIZED CABLE		
PIN	**DESCRIPTION**	**FUNCTION**
01	(PRSTRB[0])	INPUT/OUTPUT
02	(PRPA0[1])	OUTPUT
03	(PRPA1[1])	OUTPUT
04	(PRPA2[1])	OUTPUT
05	(PRPA3[1])	OUTPUT
06	(PRPA4[1])	OUTPUT
07	(PRPA5[1])	OUTPUT
08	(PRPA6[1])	OUTPUT
09	(PRPA7[1])	OUTPUT
10	NOT USED	NC
11	PERIPHERAL BUS BUSY (PRBUSY[1])	INPUT
12	PERIPHERAL PARITY ERROR (PRPE[1])	INPUT
13	PERIPHERAL CARD SELECT (PRSEL[1])	INPUT
14	GROUND	GROUND
15	NOT USED	NC
16	GROUND	GROUND
17	GROUND	GROUND
18	NOT USED	NC
19	GROUND	GROUND
20	GROUND	GROUND
21	GROUND	GROUND
22	GROUND	GROUND
23	GROUND	GROUND
24	GROUND	GROUND
25	GROUND	GROUND
26	GROUND	GROUND
27	GROUND	GROUND
28	GROUND	GROUND
29	GROUND	GROUND
30	GROUND	GROUND
31	PERIPHERAL REQUEST SYSTEM RESET (PRREST[0])	INPUT/OUTPUT
32	PERIPHERAL BUS FAULT (PRFAILT[0])	INPUT/OUTPUT
33	GROUND	GROUND
34	NOT USED	NC
35	NOT USED	NC
36	NOT USED	NC

LEGEND:

NC No Connection

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