Commodore 900 Computer System

System Hardware Specification

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1. Introduction

This document describes the features and specifications of the Commodore 900 computer. The Commodore 900 is a 16 bit computer utilizing a Z8001 CPU running at 6 MHz. The following features are supplied with the unit:

1. 32k bytes of ROM which includes diagnostics and boot code.
2. 512k bytes of RAM standard, with sockets for additional 512k.
3. Video display options:
   A. High resolution 1024 x 800 pixel monochrome bitmap display.
   B. 80 character x 25 line character mode display - monochrome.
   C. 80 character x 25 line character/medium res. graphics - color.
4. 99-key, full ASCII keyboard with numeric keypad.
5. IEEE-488 interface for use with existing Commodore peripherals.
6. Centronics-type parallel port for use with high speed printers.
7. Two RS-232 serial ports in standard HiRes system. Four ports in character mode system.
8. High speed (DMA) hard disk - 20MB standard, up to two 67MB drives possible.
9. Up to two high speed (DMA), 1.1 Mbyte double sided floppy disk drives.
10. Coherent (UNIX-compatabile) operating system.
11. Real time clock with battery backup.

2. General Specifications

CPU type	:	Zilog Z8001 (16 bit)
Clock speed	:	6 Mhz CPU 24 Mhz APU optional (available early 86)
Address space	:	16M bytes total ROM & RAM 32k bytes ROM standard 512k bytes RAM standard 512k bytes additional expansion possible in standard system.
Display	:	On separate PCB. Options available are: (1) 1024 x 800 bitmap monochrome display. (2) 80 x 25 character mode display - mono. (3) 80 x 25 character mode/medium res. graphics - color.
Keyboard	:	99-key, full ASCII detachable keyboard 10 function keys Numeric keypad
Sound	:	Simple tone generator standard
Standard interfaces	:	IEEE-488 Centronics parallel interface RS-232 50 - 19.2k Baud Two ports standard in HiRes systems, Four ports in Character mode systems.
Mass storage	:	High speed floppy drive standard 20Mb Winchester hard disk drive standard.
Expansion	:	All important signals are brought out on a bus to allow the addition of RAM, ROM and/or I/O devices.

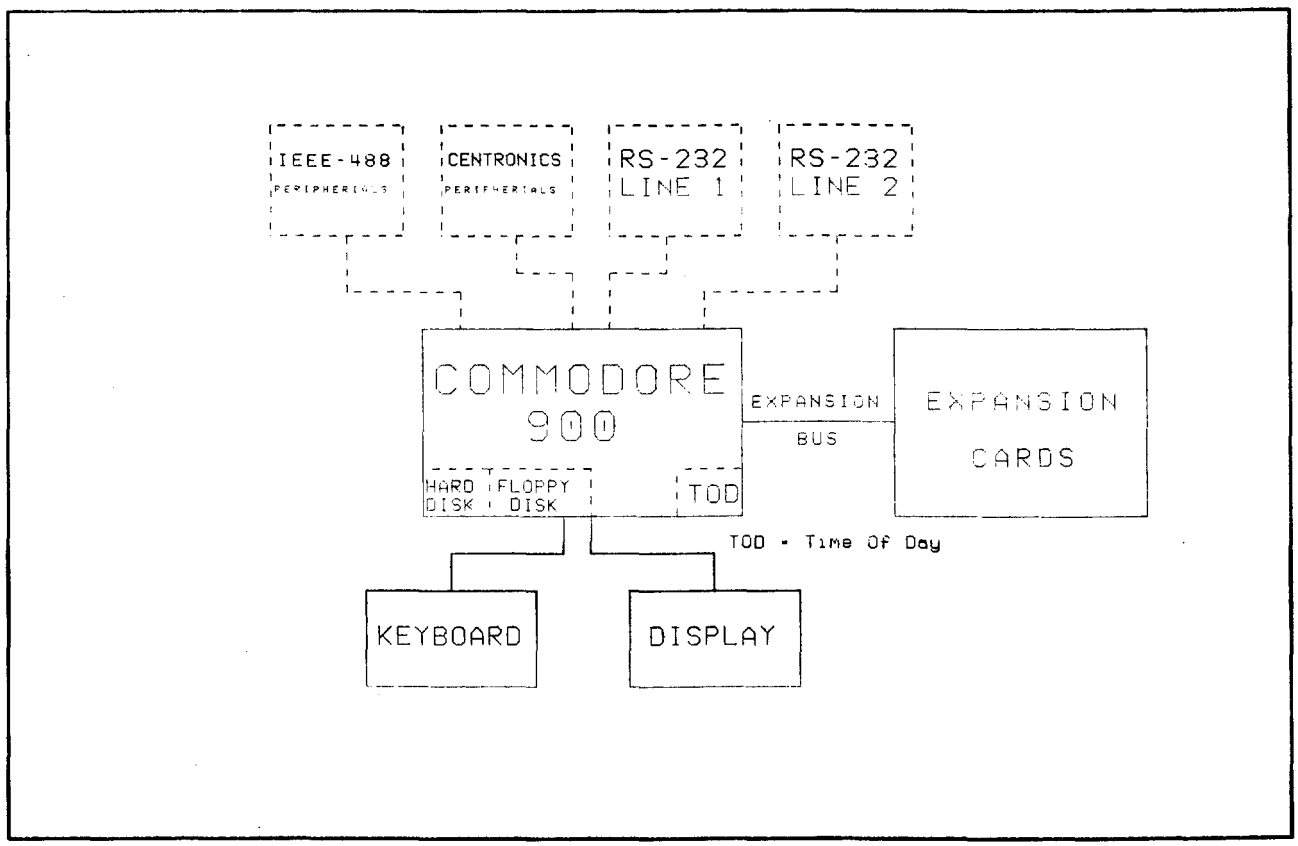


Figure 2-1. Commodore 900 Block Diagram

2.1 System Architecture

This section is designed to give a general description of system utilization and expandability. The following discussion refers to the block diagram in figure 2-1.

2.1.1 Overview

This computer is based on Zilog's Z8001 16 bit segmented CPU running at 6 MHz. All connections to this processor are made through Zilog's Z-Bus. One Z8010 MMU is used to translate the upper six address lines and the seven segment number lines supplied by the CPU into 15 linear address lines. These lines, in conjunction with the lower nine untranslated address lines, are used to address all memory. All CPU memory transactions, excluding DMA transfers, take place through the MMU. In a 'standard' configuration, the MMU would use A8-A15 in the translation process. In order to reduce the hardware required for dynamic RAM support only the upper six are used in this system (i.e. A8 & A9 are not passed through the MMU). This reduction has the effect of altering the segment granularity from 256 to 1024 bytes. Untranslated address lines are available strictly for use in the I/O space. All peripherals are addressed over the Z-Bus through this I/O space.

2.1.2 Memory Expansion

This unit can support up to 16M bytes combined total of ROM and RAM. The addition of ROM or RAM requires simply decoding some region of the linear address space and connecting it to the Z-BUS. The standard unit contains 512k of RAM with sockets for an additional 512k. Further expansion is possible through the use of an expansion card.

2.1.3 Keyboard Interface

The keyboard for this unit is scanned using a single chip microprocessor. This microprocessor, which resides in the keyboard and passes data serially to a shift register in the CPU box, is accessed through a Z8036 parallel I/O interface chip (See technical section for specific connections). This Z8036 is located at address 0x00-0x7F in the normal I/O space. An IBM PC compatible interface is utilized.

2.1.4 Video Display

The video display for the Commodore 900 is on a separate PC board from the main CPU logic. This allows for flexibility in the selection of the type of display on the unit.

2.1.4.1 Bit Map High Resolution Display

This display consists of a 1024 x 800 pixel bitmapped monochrome screen. Each pixel corresponds to a bit in memory in segments 3E and 3F. The upper left most pixel is bit 15 (msb) of the word at segment 0x3E offset 0000, the next pixel in that row is bit 14, etc. The lower right most pixel is bit 0 (lsb) of the word at segment 0x3F offset 0x8FFE.

2.1.4.2 Monochrome Character Display

This is an IBM PC compatabile 80 character by 25 line monochrome display. All attributes (flash, underline, etc.) are supported. A standard IBM PC type monochrome monitor may be used.

2.1.4.3 Low Cost Color Display

A low cost color display supporting both character and medium resolution graphics modes is designed utilizing Commodore's 8563 custom display chip. In a character mode, an 80 character by 25 line screen with programmable fonts is displayed. Graphics modes up to 640 x 400 are supported. A standard digital RGBI monitor is used.

2.1.5 Sound Generation

Sound is produced by one of the counters in a Z8036 parallel I/O interface. This Z8036 is located address 80-FF in the normal I/O space.

2.1.6 Serial I/O

Serial I/O for this unit is achieved through a Z8030 serial communications controller (SCC). This device provides two channels which can be configured as RS-232 compatible ports. The SCC is located at address 0x100-0x17F in the normal I/O space. The inputs and outputs of this chip are connected through standard RS-232 buffers to two DB-25S connectors, designated Line 1 and Line 2. Additional RS232 ports are possible through the use of an optional expansion board.

2.1.7 IEEE-488 Interface

The IEEE interface is provided by a Z8036 parallel I/O interface which is conditioned by standard IEEE-488 line drivers and receivers. The Z8036 is located at address 0x80-0xFF in the normal I/O space.

2.1.8 Centronics Interface

The Centronics interface uses the remaining lines on the keyboard and IEEE Z8036's. These lines are buffered by open collector TTL gates. The Z8036's are located at addresses 0x00-0x7F and 0x80-0xFF in the normal I/O space (See the technical section for specific pin connections).

2.1.9 Single Step

The ability to single step through programs is provided through the use of the non-vectored interrupt. This function is controlled by a latch at address 201 in the normal I/O space. When enabled, a NVI will be generated during every second instruction following the one which enabled it. If non-vectored interrupts are enabled, the interrupt will be processed at the end of the instruction during which the interrupt was generated.

2.1.10 Disk/Tape Interface

The internal hard disk, floppy disk, and tape controllers are accessed through a custom DMA chip. Commands are passed to the disk/tape controllers through the DMA device. Both controllers use the same DMA chip.

2.1.11 Hard Disk Size Limitations

The Commodore 900's operating system itself does not place a limt on the maximum size of the hard disk drive that may be attached. The limit of 67 Mbytes is the maximum that the current hard disk controller can handle. The controller uses the ST506 interface to communicate to the hard disk drive. This interface sets the limit on the number of heads to 8. With current drive technology, the largest 8 head 5.25" disk drive available is 67 Mbytes in size. Note that the controller could be upgraded at a later date to accomodate larger drives as disk technology advances.

2.2 Software Overview

Software presently supplied with the Commodore 900 is the Coherent operating system. Coherent is a UNIX compatible, multi-tasking, multi-user operating system. The unit itself (ROM based software) will only contain simple diagnostics and boot code. The boot ROM's will boot a secondary bootstrap program from a known location on the disk. This secondary program is operating system dependent. The secondary bootstrap loads the Coherent OS, advanced diagnostics, or another operating system and then transfers control to the appropriate environment.

3. Technical Specification

This section provides the details for issues discussed in previous sections, as well as technical issues not yet mentioned. A diagram of the system busses is in figure 3-1.

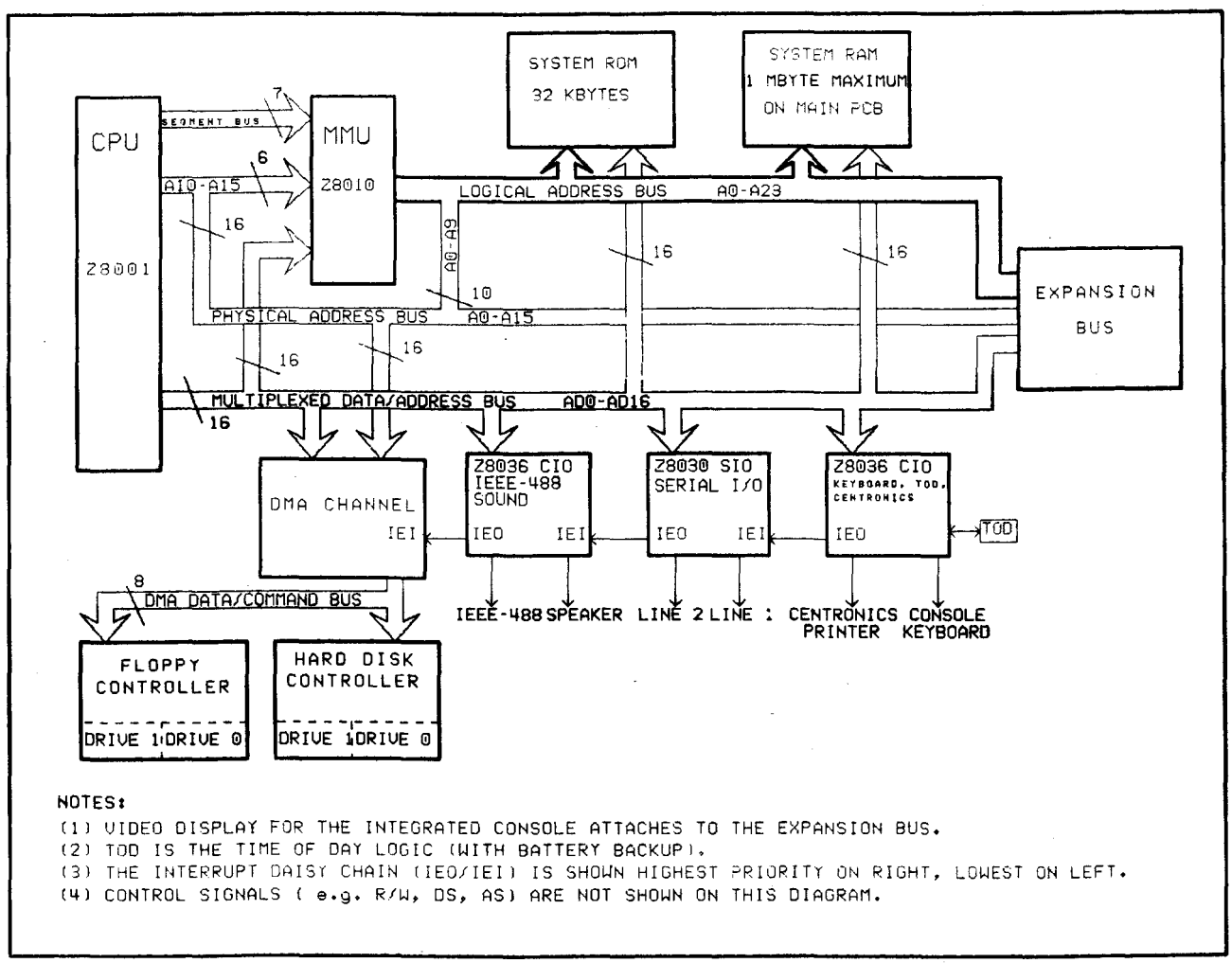


Figure 3-1. Commodore 900 Bus Logic

3.1 Memory Configuration

The large memory space is controlled by a Zilog Z8010 MMU. All memory accesses (excluding DMA) pass through the MMU. A8 & A9 are always passed untranslated. This changes the segment granularity to 1024 bytes instead of the usual 256 bytes. At power up, the MMU will pass addresses untranslated (MSEN bit of the mode register is set & TRANS bit is cleared). The control registers of the MMU are part of the Z8000's special I/O address space (address 0x00FC).

The physical memory map of the Commodore 900 computer is shown below in figure 3-2. Abbreviations used are:

HDR - High resolution Display Ram.
CDR - Character mode Display Ram.
ROM - System ROM.
RAM - System RAM.
RESERVED - Reserved for use by CBM.

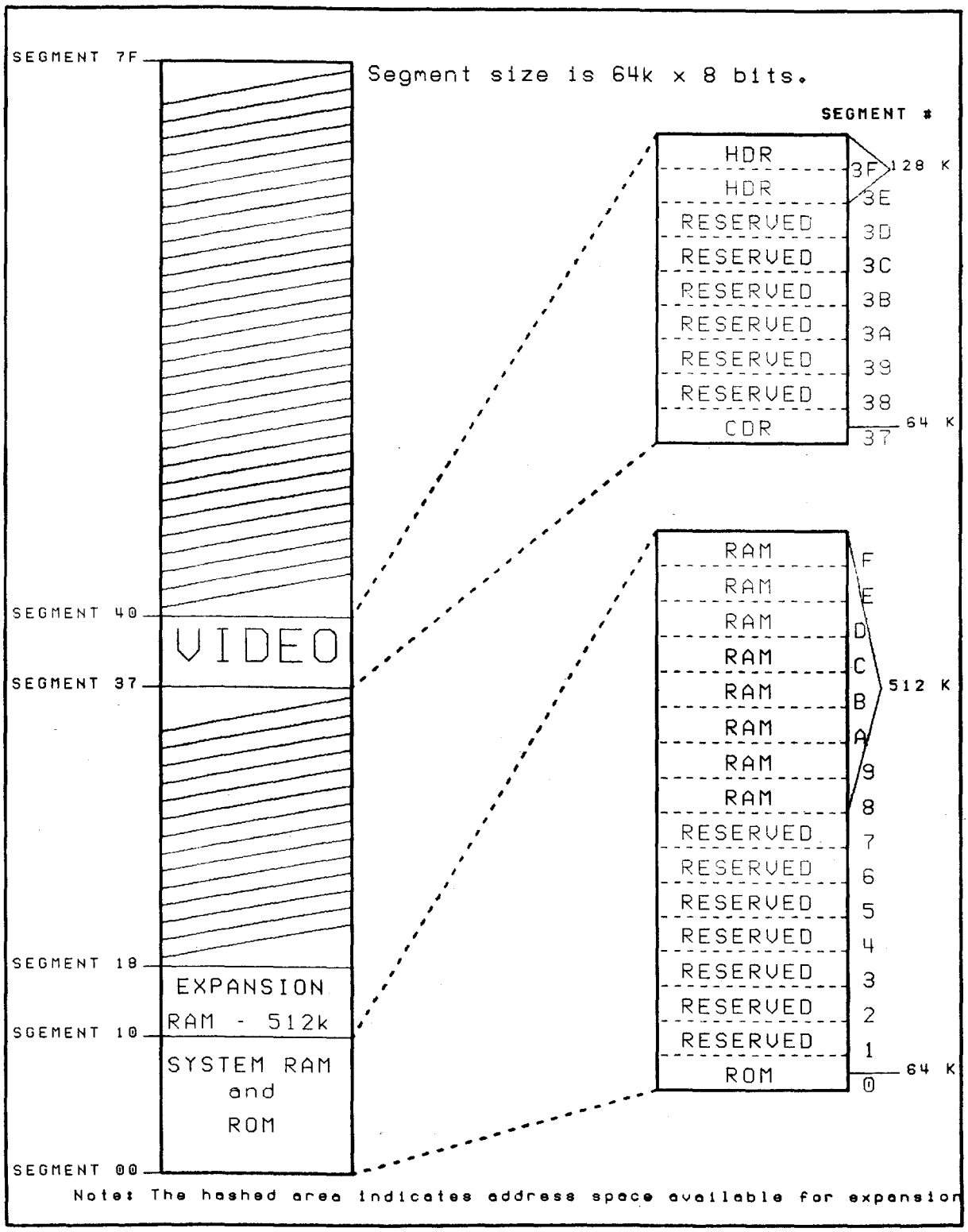


Figure 3-2. Commodore 900 Memory Map

3.2 Keyboard

The keyboard for this device supports the full ASCII character set (i.e. must have all alphanumeric characters and a control key). The keyboard can be broken up into five groups of keys: alphanumeric, keypad, cursor control, function and special function. These groups contain the following keys:

Alphanumeric

26	A-Z
10	0-9
1	Space
11	Symbols
3	Shift keys (2 shift, 1 lock)
2	Control (cntrl, alt)
1	Return
1	Tab
1	Escape
1	Backspace
1	Delete

Keypad

10	0-9
1	Decimal point
1	00
1	Enter
5	Symbols (?+-*/)
1	CE

Cursor control

4	Direction keys

Function

10	F0-F9
3	Mouse function keys

Special function

1	Help
1	Stop
1	Insert
1	Home/Clr
1	Screen print

3.2.1 Keyboard Interface

Keyboard scanning is accomplished by a single chip microprocessor which resides in the keyboard unit. The microprocessor passes data serially to the host CPU. Nine bits are transmitted from the keyboard and assembled in a TTL shift register at the host CPU. The shift register is read by a Z8036 CIO. The ninth data bit (key up/down detect) is used to cause a pattern match interupt on Z8036 I/O line PA7. One interrupt will be generated for each keystroke. The keyboard is disabled by a write of 0 to bit #1 of I/O location 0x0205. A one written to this bit enables the keyboard. Care must be taken not to disturb bit 0, used for the IEEE REN function. The table below shows the I/O connections to the Z8036.

Z8036 (0x0000-0x007F)

Port A :	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
Keyboard data :	KD0	KD1	KD2	KD3	KD4	KD5	KD6	KD8

Port C :	PC0	PC1	PC2	PC3
Kbd handshake :	CBSY	TODSEL	KD7	KBDCLR

KD0-KD8, & KBDCLR are keyboard data lines from shift register.
CBSY is a Centronics line

3.3 Video Display

The video display for the Commodore 900 is a separate PCB from the main CPU PC board. This approach allows for many possible display schemes and for easy upgrade of the display at a later date.

3.3.1 High Resolution Display

The high resolution display for consists of a 1024 x 800 pixel bitmapped screen. Each pixel corresponds to a bit in memory in segments 0x3E and 0x3F. (Bit = 1 = illuminated) The upper left most pixel is bit 15 (msb) of the word at segment 0x3E offset 0000, the next pixel in that row is bit 14, etc. The lower right most pixel is bit 0 (lsb) of the word at segment 0x3F offset 0x8FFE. Timing for the video section is derived through custom logic. The video scan rates are 53 kHz for the horizontal and 60 Hz for vertical. The required video bandwidth of the monitor is 72 MHz. These rates make the use of a special custom monitor necessary.

3.3.2 Character Mode Display

A character mode display option is also available (it is a lower cost alternative to the bitmap display). This option provides an 80 character by 25 line display. The IBM PC attributes - reverse video, flash, underline, and half brightness - are supported. The video RAM is part of the system's address space in physical segment 0x37. The video signal is IBM PC monochrome compatible.

3.3.3 Color Character Mode Display

Commodore's 8563 display chip can be used to pruduce a *very* low cost display option. Only four integrated circuits and a clock are required for this display section - the 8563, 2 RAM's and one TTL IC. This display is capable of a color 80 character by 25 line display and color graphics modes up to a 640 x 400 resolution. The display RAM is isolated from the system bus by the 8563. The effective display update speed is about 50k 'baud'.

3.4 Sound Generation

Sound is generated by counter/timer #2 of the Z8036 at address 0x80-0xFF. This Z8036 is clocked at 750kHz giving a minimum frequency of about 5Hz. Counter #2 should be programmed to provide an external output (PB0). To generate more complex sounds it can be internally linked to counter/timer #1. This counter can be used to give a tone of a certain duration or used to modulate the output with another square wave. The diagram below illustrates the particular bit connections.

Z8036 (0x0080-0x00FF)

Port B :	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
	SND	#	#	#	#	#	#	#

SND - Sound output
\# - IEEE control

3.5 RS-232 Interface

Two RS-232 ports are provided on the main CPU board through the use of the Z8030 SCC (Serial Communications Controller). This is located in the normal I/O space at address 0x100-0x17F. This chip must be programmed to use the asynchronous RS-232 compatible protocol. The receive and transmit clocks provided to the Z8030 are 6MHz, the following table gives the values which must be programmed into the chip to provide the standard RS-232 baud rates.

Z8030A with 6MHz clock (x16 clock mode in all cases)

Desired baud rate	Time constant (hex)	Actual baud rate
50	0EA4	50.0
75	09C3	75.0
110	09A8	110.0
134.5	0971	134.5
150	04E1	150.0
300	026F	300.3
600	0137	599.6
1200	009A	1203.0
1800	0066	1804.6
2000	005C	1996.5
2400	004C	2406.1
3600	0032	3609.1
4800	0025	4809.0
7200	0018	7218.2
9600	0012	9383.0
19200	0008	19248.0

A total of eight RS-232 ports are allowed by the system architecture for login purposes. The six ports in addition to those on the main board are provided on various expansion boards. The six lines are contained on three Zilog SCC devices, designated Aux1, Aux2, and Aux3. A fourth SCC, Aux4, is available in the architecture for synchronous communication, modems, printers, and other devices. The I/O location for all these devices is fixed in section 3.12.

The RS232 connectors are female DB25 connectors pinned out as follows:

SIGNAL NAME	CONNECTOR PIN #
TxD	2
RxD	3
RTS	4
CTS	5
DSR	6
DCD	8
DTR	20
SIGNAL GROUND	7
CHASSIS GROUND	1

3.6 Centronics Interface

A Centronics parallel port is provided by buffering a Z8036 port with open collector TTL drivers. Eight data lines and three control lines are supported. They are distributed over two Z8036's as follows:

Z8036 (0x0000-0x007F)

Port B	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
Centronics Data:	CD0	CD1	CD2	CD3	CD4	CD5	CD6	CD7

Port C	PC0	PC1	PC2	PC3
Centronics :	CBSY	TODSEL	*	*

Z8036 (0x0080-0x00FF)

Port B	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
Cent. Control :	$	_CACK	#	#	#	#	#	#

Port C	PC0	PC1	PC2	PC3
Cent. Control :	#	#	#	_CDS

* - Keyboard control
\# - IEEE-488 control
$ - Sound output

The pinout of the printer connector is like that of the IBM PC. The pinout is shown below. The connector used is a male DB25 connector.

Signal Name	Connector Pin #
CD0	2
CD1	3
CD2	4
CD3	5
CD4	6
CD5	7
CD6	8
CD7	9
CBSY	11
_CACK	10
_CDS	1
GROUND	18-25

3.7 Time of Day Clock

A time of day clock chip is used to provide the correct time. A battery back up is utilized for at least a 3 month backup period before losing data. The clock data and control lines are 'multiplexed' with the printer lines. This can be done without conflict as both the Centronics interface and the clock chip have separate select lines. Both devices ignore transistions on data lines when not selected. When selecting the clock with the TODSEL line, care should be taken to not disturb any other port C lines. The clock chip is connected to the Z8036 as follows.

Z8036 (0x0000-0x007F)

Port B	: PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
Data/Control	: D0	D1	D2	D3	READ	WRITE	ADWRITE	STOP

Port C	: PC0	PC1	PC2	PC3
Centronics	: -	TODSEL	-	-

3.8 IEEE-488 Interface

The IEEE-488 interface is provided in the form of buffered port lines of a Z8036. The conditioning is done by 75160 and 75161 line drivers and receivers. The table below shows the connections to the ports of the Z8036. The connector and pinout for the IEEE-488 interface is the industry standard.

Z8036 (0x0080-0x00FF)

Port A	: PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
IEEE-488 data	: D1	D2	D3	D4	D5	D6	D7	D8
Port B	: PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
IEEE Control	: $	*	SRQ	ATN	DAV	EOI	NDAC	NRFD

Port C	: PC0	PC1	PC2	PC3
IEEE Control	: IFC	TE	DC	*

The remote enable signal, REN, is controlled by bit 0 of a latch at 203 in the normal I/O space. This latch is set to zero on powerup.

* - Centronics control lines
$ - Sound output
DC,TE - Control lines for 75160 and 75161 (IEEE-488)

3.9 Software I/O Techniques

It should be noted that many of the I/O ports on the Zilog devices are shared by different I/O functions. To write to a port that is shared the port ***must always*** be first read, then the data byte ANDed or ORed to reset or set appropriate bits, and then written back to the port. This will insure that the integrity of all I/O devices is maintained. It should be noted that in some special cases interrupts must be disabled during the read/write cycle for a port. The software specification will identify where this is needed.

Programming for the IEEE-488, RS232C, and Centronics ports is defined in the Software Specification or industry standard publications.

The time of day chip is a chip device intended to reside on a memory bus. However, the access time of the device is exceedingly long, and to avoid unnecessary logic for wait state generation, the device resides on an I/O port and memory transactions are simulated in software. The TOD device has a 4 bit multiplexed address/data bus (D0-D3), read, write, address write, stop, and chip select (TODSEL) lines. To begin a transaction, the device is first selected by lowering the TODSEL input. Next, the STOP line should be raised to temporarily stop the device from counting. This is done to prevent registers changing during the read/write process.

To read or write a given register, the register address is placed on D0-D3 and ADWRITE is raised and then lowered (specific timing for the device signals

are available from the MSM52831 specification). After this, data is either read or written from the selected register. To read, the READ line is raised and data is read from D0-D3 after the access time has passed and READ is lowered. To write, the data is placed on D0-D3 and write is lowered and then raised after the access time has passed. After all registers have been read or written, the STOP line is lowered and TODSEL is raised. This completes a read/write transaction with the TOD circuit.

3.10 Single Step Control

The control of the single stepper is accomplished through bit 0 of a latch located at address 0x201 in the normal I/O space. On powerup this line is forced low. Any I/O access to address 0x201 will set bit 0 low and enable the single step logic. The NVI line to the Z8000 will be asserted during the second instruction following the one which sets bit 0 and will be cleared before the execution of the third instruction. The Z8000 will enter the NVI processing routine at the completion of the instruction during which NVI was asserted if NVI interrupts are enabled. This function is intended for use by a high level language debugger such as the Coherent package's DB.

3.11 DMA Interface

The custom DMA controller is used to access controllers for the floppy drive, hard drive, and a tape drive. Commands are passed to the various controllers through separate 16 byte command blocks at pre-defined addresses. The controllers report errors in their respective command block area. Data may be read from or written to any area of RAM memory. It should be noted that DMA addresses *do not* pass through the MMU and as such represent *physical, not logical* addresses. The command block address are at the following physical locations in RAM.

Hard disk drive controller	:	Segment 8, offset 0x0000
Floppy disk controller	:	Segment 8, offset 0x0010
Tape controller	:	Segment 8, offset 0x0020

3.11.1 Command Structure

Both data and controller commands pass through the DMA channel. The command block is similiar in structure to the SASI command block. The basic structure is in figure 3-3. The various controllers check for a 0xFF in byte 12 to determine if the command is valid. The first controller in line blocks the interrupt from other controllers attached to the 8716. If no 0xFF is found in the command block, the first controller will disconnect from the 8716 bus and allow the interrupt to pass on to the other controllers. This allows several devices to share a single DMA controller. For a detailed discussion of the command block, see the hard disk or floppy disk specification.

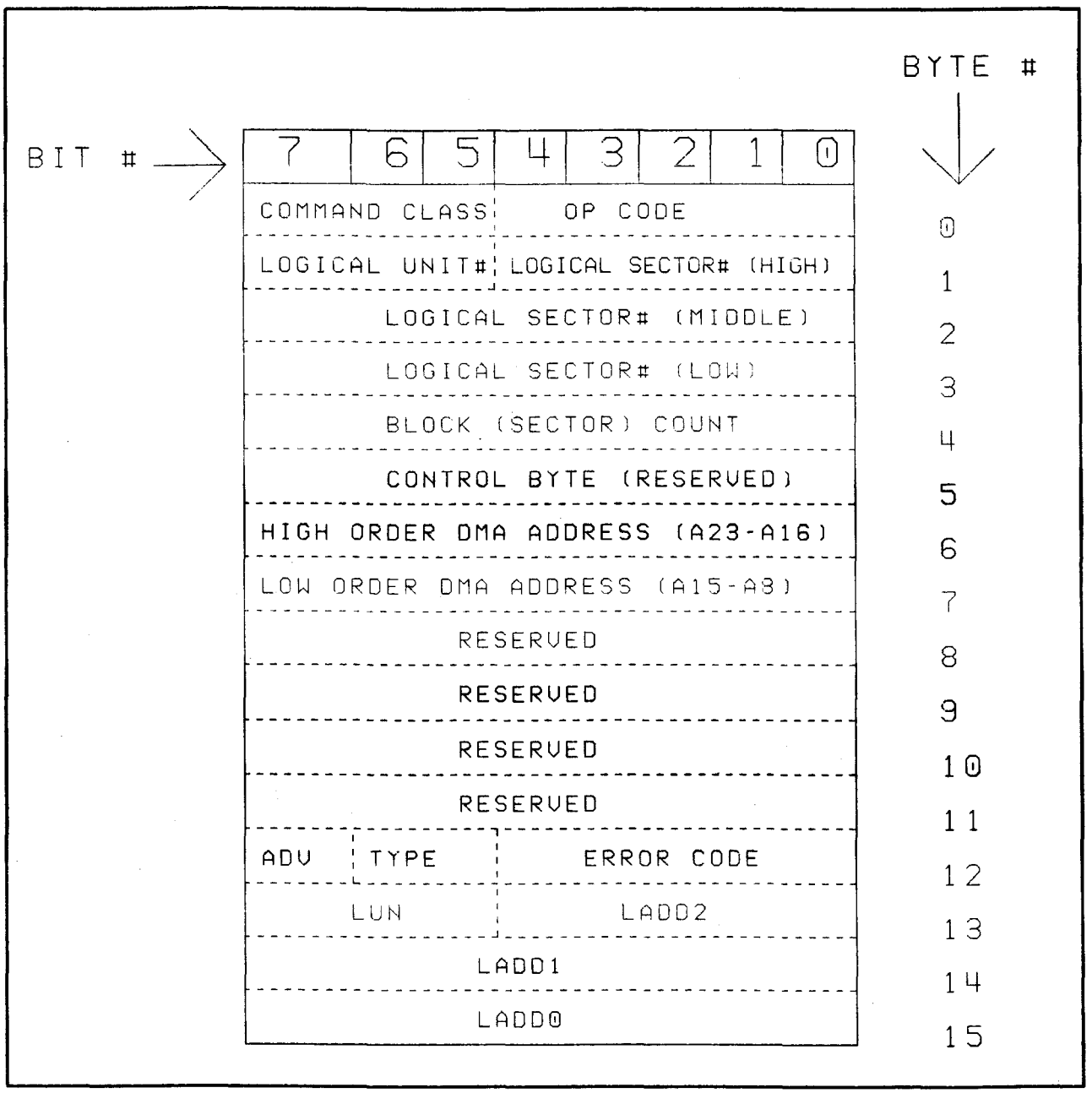


Figure 3-3. Disk Command Block

3.12 I/O Map

The following table lists the used and reserved addresses in the normal I/O space (addresses in hex).

0000-007F	Z8036 - Keyboard/TOD/Centronics
0080-00FF	Z8036 - IEEE-488/Centronics/Sound
0100-017F	Z8030 - Serial I/O Line1/Line2
0180-01FF	Color Character Mode display (8563)
0200-02FF	Single step/IEEE REN
0300-037F	Z8030 - Aux1
0380-03FF	Z8030 - Aux2
0400-04FF	Mouse/Video Configuration Registers
0500-05FF	DMA device for disk/tape
0600-067F	Z8030 - Aux3
0680-06FF	Z8030 - Aux4
0700-07FF	LAN Controller
0800-0FFF	** RESERVED **
1000-FFFF	** UNUSED **

3.13 Vectored Interrupt Priority

In accordance with the Z-Bus, vectored interrupts are prioritized using a daisy chain. Both ends of the chain are supplied to the expansion connector to allow peripherals to have either the highest or the lowest priority in the chain. On the CPU board the peripherals are prioritized in the following order.

1. APU when installed. (Highest)
2. Keyboard - Z8036, also used for time of day.
3. RS-232 - Z8030.
4. IEEE - Z8036.
5. DMA device (for disk/tape controllers). (Lowest)

3.14 Arithmetic Co-processor

A 60 pin dual in-line header will be provided on the circuit board to connect to an added circuit board which will contain the Z8070 arithmetic coprocessor.

3.15 Power Supply

The power supply for this unit is of the switching type. The following table shows the maximum current requirements for the individual voltages.

+5V @9.00A
+12V @2.50A
-12V @0.05A
-5V @0.50A

4. Packaging Considerations

This section provides the requirements for housing the Commodore 900 computer and its associated peripherals.

4.1 Internal Space Requirements

4.1.1 Display

This unit utilizes a 15' high resolution black and white picture tube and associated driving electronics in a separate enclosure. A five pin connector is provided on the monitor and the CPU enclosures for interconnection.

4.1.2 PC Board

The PC board for the main CPU contains about 92 integrated circuits. This represents all the logic except for the video display and hard disk controller (both are separate PC boards).

4.1.3 Power Supply

The power supply dissipates a maximum of 110 Watts. It is compatible with the Commodore PC power supply.

4.1.4 Storage Devices

Space is provided the CPU enclosure for two 5 1/4" half height devices and one full height 5 1/4" device.

4.2 Switches

Only two switches are provided in addition to the keyboard. These are a power switch and a reset button.

4.3 External Connections

The following connectors are mounted on the rear panel of the unit:

1. Two video connectors for HiRes display, one for others
2. Two RS-232 connectors

3. One IEEE-488 connector
4. One Centronics connector
5. One AC power line connector
6. One mouse connector
7. Keyboard connector on the front of the unit

4.4 Expansion

Expansion of the Commodore 900 is possible through the use of various expansion cards that will be defined at a later date. The CPU case for this unit will allow expansion cards to be mounted internally.

5. Software

The software provided with this machine has a multilayered organization. The following sections describe the function of each of these layers.

5.1 ROM Based Software

The unit contains a small amount of ROM which, on power-up, will perform the following functions.

1. Execute system diagnostics. This will perform verification of the unit's hardware (ROM, RAM, MMU, etc.) and report any errors.

2. Initialize I/O parts. This will assure that the interface parts (Z8030 and Z8036s) are in some normal operating state.

3. Describe RAM configuration. A memory map will be created at a designated place in memory which will describe the current RAM configuration.

4. Describe peripheral configuration. A description of the Commodore peripherals currently attached to the unit will placed at a predetermined place in memory.

5. Boot a system from disk. A system will be booted in from either a floppy or the hard disk. See the boot ROM specification for operation details.

Also contained in the ROM is the default character set which is used at power-up.

5.2 Coherent Operating System

Supplied on a floppy disk with the unit will be the Coherent Operating System. Coherent is a UNIX-like, multi-tasking, multi-user operating system which takes full advantage of the segmented operation of the Z8001 CPU and Z8010 MMU. In addition, Coherent will provide support for the following devices:

1. Up to 2 floppy disk drives.
2. Up to 2 hard disk drives.
   (limited to 67 M bytes each by current hard disk technology).
3. The console device which consists of the keyboard and high resolution bitmap or character mode display.
4. Eight RS-232C ports which may be used as user ports or for device I/O. These ports are full duplex only with programmable baud rate (0-19.2k) and modem/CTS handshaking.
5. An IEEE-488 interface. Supports printers only. Disks can be used with a special utility program.
6. Centronics parallel printer port.

Coherent comes with the standard Coherent shell and over 50 utilities. This does not include the assembler, text editor or formatter, or the language C.

5.3 Commodore Shell

Commodore will supply a menu driven shell with window management that provides access to system utilities, application programs, and console parameters. This shell will be invoked at system boot to provide the unsophistocated user with a friendly environment. For a detailed description of this and other software details, please see the Software Specification.