

FAIRLIGHT

COMPUTER MUSICAL INSTRUMENT

All about Fairlight



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Warning this **Service Manual** is only for

Fairlight Computer **M**usical **I**nstrument Model **IIx**

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CMI SYSTEM SERVICE MANUAL

FAIRLIGHT INSTRUMENTS, FEBRUARY 1985

Revision 2.1

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1. INTRODUCTION

The Fairlight Computer Musical Instrument is a complete music production and performance instrument. It is a special purpose computer system incorporating a custom dual M6809 central processor interfaced to special input-output devices optimised for the rather unusual requirements of music production.

The information presented in this manual is intended as a guide to give the reader an appreciation of the general operating principles of the C.M.I. In the event of a malfunction, it should be used to isolate which of the four main C.M.I. sub-systems is at fault, then for detailed functional information refer to the service manual for the item concerned.

Related documents are:
C.M.I. MAINFRAME SERVICE MANUAL
GRAPHICS TERMINAL SERVICE MANUAL
ALPHA-NUMERIC KEYBOARD SERVICE MANUAL
MUSIC KEYBOARD SERVICE MANUAL
FLOPPY-DISK DRIVE SERVICE MANUAL

1.1 SYSTEM OVERVIEW

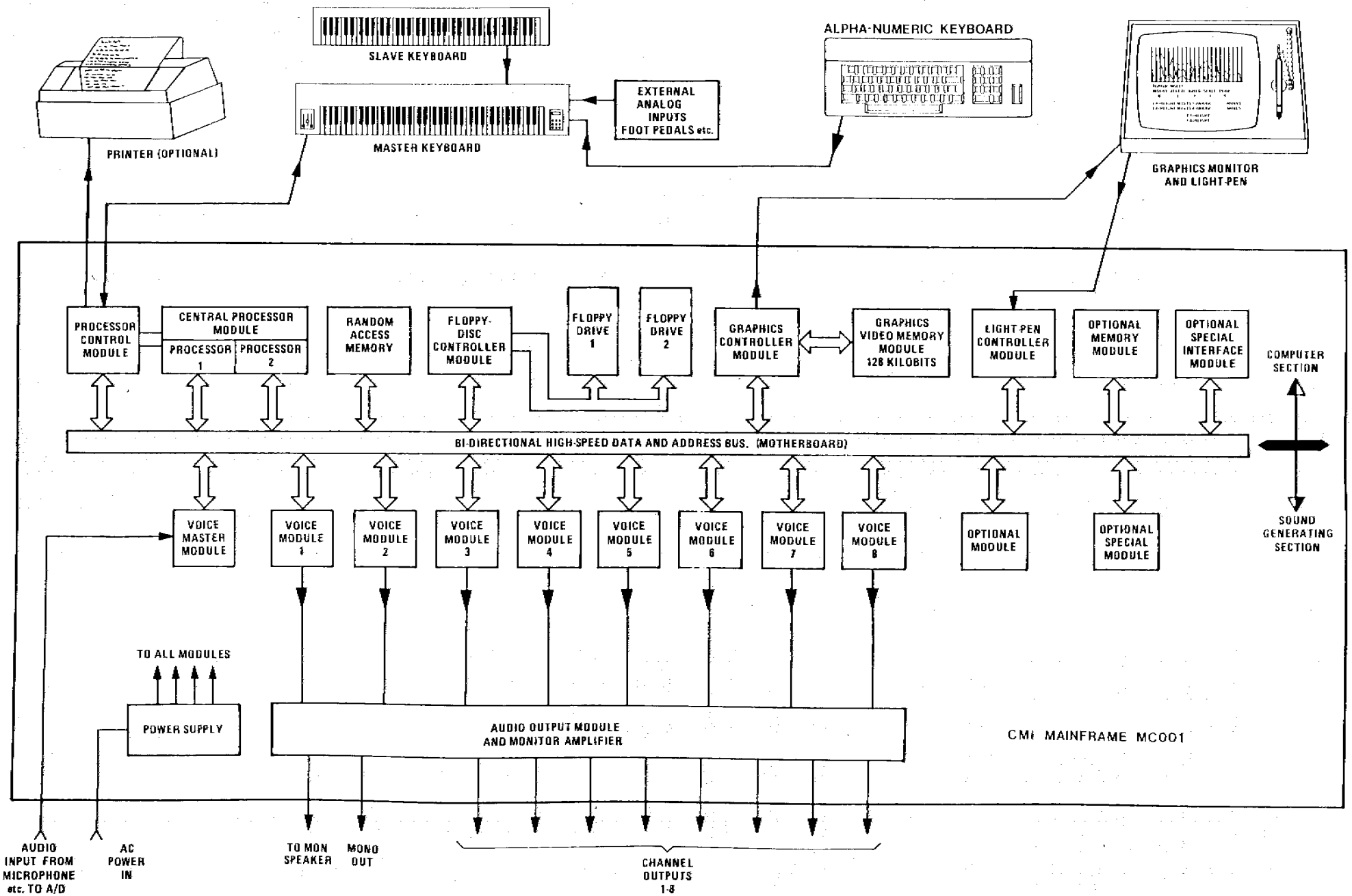
The system comprises for main units (Refer Fig. 1).

1) Mainframe: Houses the computer section, floppy disk drives, audio generation section and power supplies.

2) Graphics Terminal: The primary display terminal for the computer. It is a 15 inch C.R.T. display with lightpen.

3) Alphanumeric Keyboard: Sends serial ASCII data to the computer. Used for operator input of commands etc.

4) Music Keyboard: Piano-like keyboard sends serial data to the computer on each key depression. Used for live playing. Also includes several analog controls and switches which are digitised, and a numeric keypad with 12 character alpha-numeric display which serves as a secondary Input-Output device.



gure 1. C.M.I. SYSTEM BLOCK DIA

2. FUNCTIONAL DESCRIPTION

2.1 COMPUTER SECTION (MAINFRAME)

The computer section of the C.M.I. houses all the digital control and sound generating hardware. It can be considered a stand-alone operational unit. With nothing connected to it it is possible to start up the system and bootstrap load the disks (BOOT the system). On power-up, EPROMS located on the C.P.U. Control Card Q-133 will control the Boot process.

As soon as a disk is placed in the left-hand drive (Drive 0) a special sector known as the Boot Block is read into RAM and executed. The code in the Boot Block then completes the Boot by reading in the C.M.I. Operating System. The system is then ready to accept commands from the alpha-keyboard, music keyboard or light pen.

For deatailed information refer to the C.M.I. MAINFRAME SERVICE MANUAL.

2.2 GRAPHICS TERMINAL

Display data for the Graphics Terminal is generated by the Graphics Display card Q-219 in the form of a composite video signal. The display format is a bit-mapped image of 16 kilobytes of VRAM, displayed as a 512 (Horizontal) by 256 (Vertical) matrix.

The Light-Pen operates by sending a pulse back to the computer when the phosphor dot is "seen" to flash past. The Light Pen Interface Q-219, located in the Mainframe generates X-Y co-ordinates from the timing of this pulse. As well as this "Hit" signal from the lightpen, there is a "Touch" signal, which indicates that the operator has activated the pen by touching the tip.

For detailed information, refer to the GRAPHICS TERMINAL SERVICE MANUAL.

2.3 MUSIC KEYBOARD

The music keyboard interfaces to the Mainframe via a bi-directional RS-232C port located on the processor control card Q-133. The Baud rate is selected by D.I.L. switches inside the keyboard. These must be set to 9600 Baud.

The keyboard is controlled by an on-card M6802 microprocessor executing a program in EPROM. As well as data communications with the Mainframe, data coming in from the alpha-numeric keyboard is pre-processed before being forwarded to the mainframe.

Data is sent to the computer whenever:

1) A music key is depressed or released
2) A key on the alpha keyboard is pressed
3) One of the three faders is moved
4) A switch or pedal plugged into the keyboard is operated.

Keystroke data is sent in the form of three-byte packets. This includes keyboard number, key number, depression/release flag and key velocity data. Key velocity is calculated by the on-card processor which times the flight of the key contact as it travels between two busbars.

The 12 digit alpha-numeric display on the right-hand end of the keyboard is used to display messages to the operator in circumstances where the Graphics Terminal is not being used. The display is controlled by the processor on the keyboard. On power-up, the message - POWER ON - is displayed. This is generated locally by the keyboard itself. Once Booting has commenced, the message LOADING is displayed. This message is sent by the mainframe, via the serial link.

The control devices (faders, switches and pedals) are digitised by an eight-bit Analog to Digital converter in the music keyboard and when the data changes, a packet of data is transmitted down the serial link to the mainframe.

For detailed information, refer to the MUSIC KEYBOARD SERVICE MANUAL.

2.4 ALPHA-NUMERIC KEYBOARD

This keyboard uses another M6802 microprocessor which controls scanning of the 62 Hall-effect switches and serialises the data which is transmitted in ASCII format, RS-232C protocol. Data rate used is 9600 Baud, selected by D.I.L. switches on the circuit board. The processor executes firmware stored in EPROM.

Normally the alpha-numeric keyboard is plugged into the music keyboard. It receives its power from there, and sends its data to the processor in the music keyboard. The data is flagged as alpha-numeric, queued until there is no music keyboard data, and then forwarded to the mainframe. If desired, the alpha keyboard can be plugged directly into the Keyboard connector on the mainframe, bypassing the music keyboard. This can be a useful diagnostic aid.

2.5 INTERCONNECTING CABLES

The four major sub-systems are connected by pluggable cable sets which should be treated with the same suspicion warranted by mechanical parts. The signals carried by each cable, together with pin numbers, are described fully in section 4, below.

3. TROUBLESHOOTING

This section covers troubleshooting the C.M.I. system only to the level of identifying which of the four sub-systems (mainframe, music keyboard, alpha-keyboard or graphics terminal) is at fault. Having done this, service personnel should refer to the service manual for the offending item.

NOTE: Remember that the C.M.I. is a complex piece of hardware running sophisticated software, and it is sometimes hard to differentiate between a hardware fault, software bug, and operator error. If there is any doubt, the same sequence of operations should be tried on a known good system before attempting hardware repairs. In executing the following diagnostic procedures, the serviceperson should be aware that a faulty System Disk can cause what appears to be hardware faults. Furthermore, hardware faults can cause disks to be destroyed, either physically or by corrupting data, so it is wise to keep a good supply of C.M.I. system disks and diagnostic disks on hand.

3.1 SUB-SYSTEM SUBSTITUTION

The easiest way to identify the faulty sub-system is to exchange whole units for known good ones if such are available. If a complete working system is on hand, exchange each sub-system in turn, starting with the most likely to be responsible for a given fault. Some common fault symptoms and suggested substitution procedures follow.

3.1.1 System will not boot. Sucessful Boot is indicated by Page 1 appearing on the screen, or Page 1 Ready message at the music keyboard.

Unplug keyboard from mainframe. If it still does not boot, the fault is in the mainframe. If it does boot, try substituting the music keyboard. If it still does not boot, substitute the alpha-keyboard. The Graphics Terminal should not be able to affect booting. If the problem does not go away at any stage, substitute the interconnecting cables one by one.

3.1.2 System boots (Page 1 on screen or message at keyboard) but does not respond to alpha keyboard commands.

Substitute music keyboard, then alpha keyboard, then graphics terminal, then cables. If problem persists, the fault is in the mainframe.

3.1.3 No sound when voice loaded and music keyboard played.

Substitute music keyboard first, then cables, then alpha keyboard, then graphics terminal. If problem persists, the fault is in the mainframe.

3.1.4 System works properly except Graphics display or lightpen malfunctions.

Substitute graphics terminal and cable first. If no better, fault is almost certainly in mainframe.

3.1.5 Other strange behaviour.

Start by substituting mainframe.

3.2 SUB-SYSTEM CHECKOUT WITHOUT SUBSTITUTION

In many cases the faulty sub-system will have to be identified using only commonly available test equipment. Minimum requirements are a multimeter for measuring volts D.C. and resistance, an oscilloscope, and the usual set of tools such as screw drivers, pliers, soldering iron, etc.

The faulty sub-system can usually be isolated by the following tests:

3.2.1 System will not boot.

Unplug keyboard input and try again. If system does not boot, fault is in mainframe. If it now boots, fault is in music keyboard, alpha keyboard or cables. To isolate which, try again with alpha keyboard plugged straight into mainframe to eliminate music keyboard.

3.1.2 System boots but does not respond to alpha keyboard commands.

Most likely fault is in alpha-keyboard or cable. If the keyboard does not click when a key is pressed, either the keyboard is faulty or the power supply to the keyboard has failed. Check the supplies and data output at the keyboard plug using the Signal List. See Section 4.

3.1.3 No sound when voice loaded and music keyboard played.

Check for normal operation with the alpha-keyboard plugged directly into the mainframe. Check for correct signals at the power and signal connectors at the music keyboard. See Section 4.

3.1.4 System works properly except Graphics Terminal malfunctions.

Check video ouput signal at the Graphics connector. If this is normal, fault is in Graphics Terminal or cable. Note that a negative image can be caused by a fault in the graphics terminal or the mainframe, and cannot be easily seen by looking at the signal on an oscilloscope. To achieve a substantially black image for examination with the oscilloscope, remove the system disk and restart both processors. This will result in the words LOAD SYSTEM DISK IN DRIVE 1 on a black screen, in which case the scope display should show any fault clearly.

3.1.5 Lightpen does not work but everything else normal.

Point the lightpen at a light area of the screen. If there is a cursor which disappears when the Touch is activated, then the fault is in the mainframe. Otherwise the fault may be in the Graphics Terminal, lightpen or cables. Check for proper Hit and Touch signals at the Graphics connector at the mainframe by unplugging the cable and using an oscilloscope. If these are not correct the fault is in the Graphics Terminal. Otherwise the mainframe is faulty.

3.1.6 Other strange behaviour.

Most other faults such as improper operation of one or more of the sound channels or unreliable response from the computer can be attributed to a fault in the mainframe. To eliminate all other possibilities a useful diagnostic trick is to start the system playing a long Page R, Page C - M.C.L. or Page 9 Sequencer loop and un-plug all cables except the mains input and audio ouput. If the fault is still evident, then the mainframe is definitely to blame.

4. SIGNAL LISTS

This section describes the signals present in each conductor of each interconnecting cable in the C.M.I. System when functioning normally. Refer to Figure 2 for cable identification.

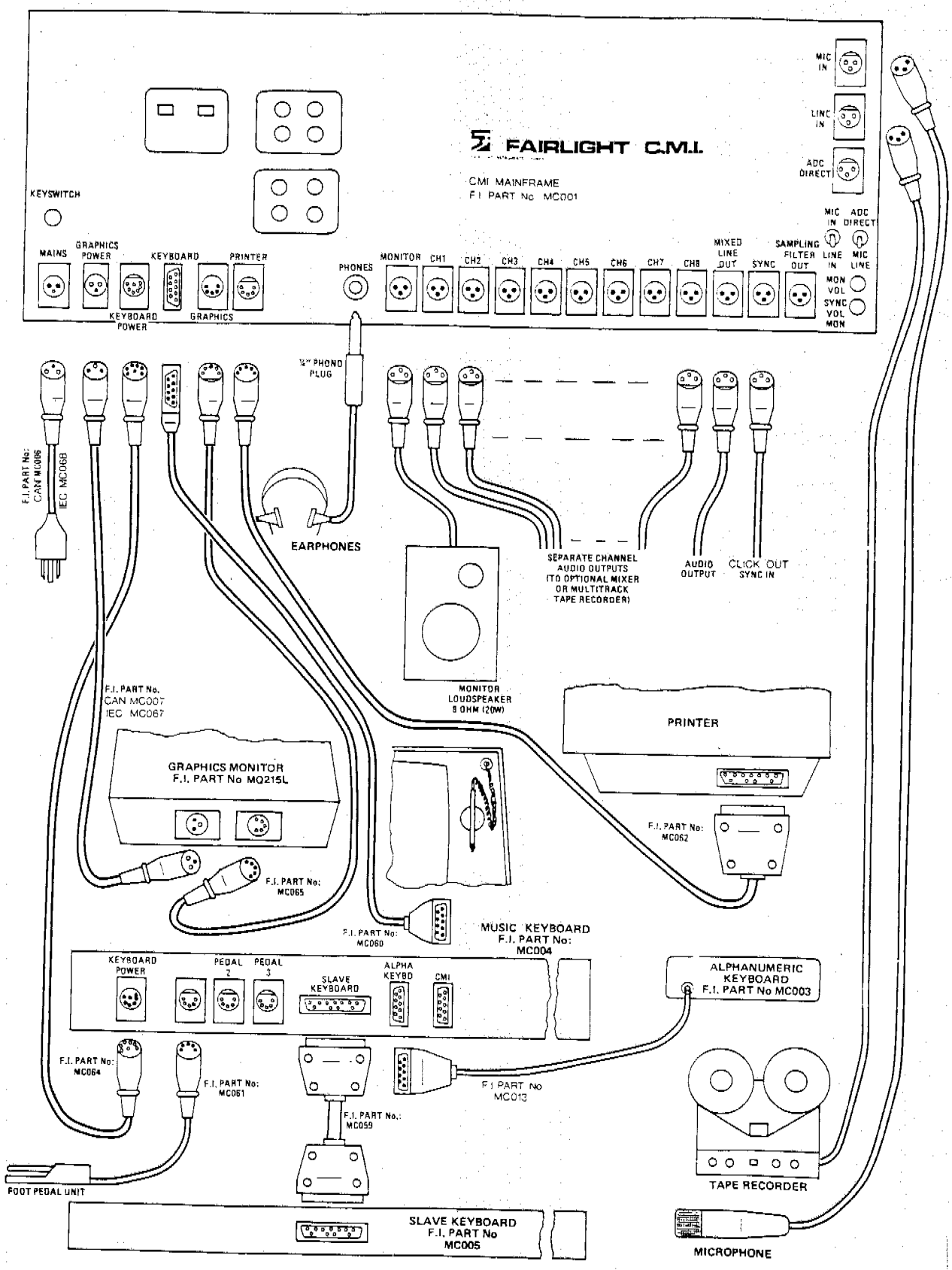


Figure 2 C.M.I. SYSTEM INTERCONNECTION CABLES

4. SIGNAL LISTS (continued)

4.1 Mains Cable: Part no. MC068 (I.E.C.)

A.C. Mains Neutral, Active and Ground.

4.2 Graphics Terminal Power: Part no. MC067 (I.E.C.)

A.C. Mains supply to Graphics Terminal. Switched by key switch on mainframe. This supply is always the same as the local mains potential.

4.3 Graphics Terminal Signal: MC065

Video signal to Graphics Terminal and Light Pen signals to mainframe.

Connector Type: Cannon 5-pin.

Pin 1 Lightpen Hit. T.T.L. level, asserted low. On oscilloscope, appears as a series of low-going pulses about 1uS wide, repeated every 20mS, when the pen is pointed at a bright area of the screen. (See fig 3a)

Pin 2 Lightpen Signal Return. Ground for lightpen signaal cables.

Pin 3 Lightpen Touch. T.T.L. level, asserted low. Normally at approximately +4 volts, goes low (less than 0.4 V) when the end of the lightpen touched.

Pin 4 Video Return. Ground for Video signal cable.

Pin 5 Composite Video. 1V P-P video signal to Gr aphics display. Format is 625 lines, 50 Hz frame rate. See fig 3b.

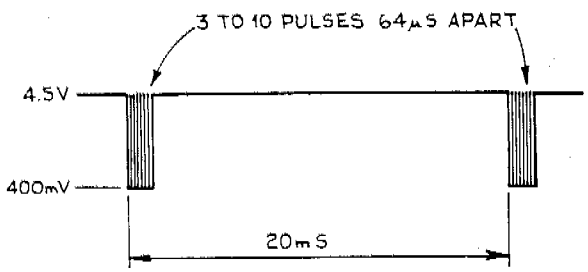


Figure 3a LIGHTPEN HIT SIGNAL

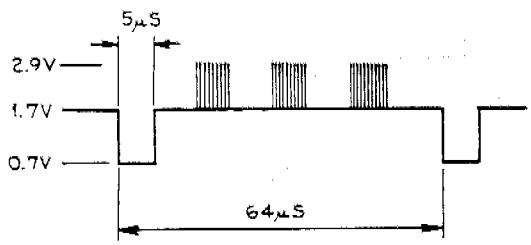


Figure 3b COMPOSITE VIDEO

4.4 Music Keyboard Power: MC064

Unregulated power supply to music keyboard. Also indirectly supplies alphanumeric keyboard.

Connector Type: Cannon 7-pin.

Pins 1,2 +10V Return. Return (ground) for +10V supply.

Pins 3,4 +10V Supply. Unregulated supply, +9 to +11 volts.

Pin 5 -20V Supply. Unregulated supply, -18 to -22 volts.

Pin 6 +20,-20 Return. Return (ground) for + and - 20 supplies.

Pin 7 +20V Supply. Unregulated supply, +18 to +22 volts.

4.5 Music Keyboard Signal: MC060

Bi-directional serial data between mainframe and music keyboard, including "busy" flags in both directions. Power supply is also carried by this cable, to power the alpha-numeric keyboard if it is connected instead of the music keyboard.

Connector Type: 9 Pin "D-Mini"

Pin 1 +18 to 22 volts unregulated supply. This is not used by the music keyboard.

Pin 2 DON1. Signal to enable transmission of data from the keyboard. RS-232C levels. Enabled: >7 volts. Disabled <-7 volts. With nothing being transmitted from the keyboard, this signal should be at approx. +10 volts. When keys are pressed or released a burst of -10 volt pulses should be seen for between 2 and 10 milliseconds.

Pin 3 -18 to -22 volts unregulated supply. This is not used by the music keyboard.

Pin 4 FLAG1. Signal to diasble transmission of data from the mainframe to the keyboard. Signal is normally +10 volts.

Pin 5 SIGNAL RETURN. Ground for data paths.

Pin 6 DATA IN. Serial data from keyboard to mainframe. Format is RS-232C. Normally at -10 volts. When a key is pressed or released a burst of +10 volt pulses lasting approx. 3 mS sholud be seen.

Pin 7 POWER RETURN. Return (Ground) for + and - supplies.

Pin 8 Not Connected.

Pin 9 DATA1. Serial data from mainframe to keyboard. Format is RS-232C. Normally at -10 volts. For each character sent from the mainframe to the alpha-numeric display a burst of +10 volt pulses lasting approx. 1 mS should be seen.

4. SIGNAL LISTS (continued)

4.6 Alpha-numeric Keyboard Power/Signal : MC013

Unregulated power supplies to alphanumeric keyboard, serial data from alphanumeric keyboard.

Connector Type: 9 Pin "D-Mini"

Pin 1	+18 to +22 volts unregulated supply.
Pin 2	Not Connected.
Pin 3	-18 to -22 volts unregulated supply.
Pin 4	Not Connected.
Pin 5	SIGNAL RETURN. Ground for data paths.
Pin 6	DATA OUT. Serial data from keyboard. Format is RS-232C. Normally at -10 volts. Each time a key is pressed a burst of +10 volt pulses lasting approx. 1 mS should be seen.
Pin 7	POWER RETURN. Return (Ground) for + and - supplies.
Pin 8	Not Connected.
Pin 9	Not Connected.

4.7 Slave Keyboard Power/Signal : MC059

The Music Keyboard sends power and key multiplexer addressing data to the slave keyboard. Key data is returned from the slave keyboard.

Connector Type: "D Mini" 25-pin.

Pins 1,2	POWER SUPPLY RETURN. Ground.
Pin 3	KEY ADDRESS 0 Least significant key multiplexer address bit.
Pins 4,7	KEY ADDRESS BITS 1-4
Pin 8	SIGNAL RETURN Ground.
Pin 9	KEY DATA 1. Data returned from key multiplexer scanning the lowest 24 keys. Normally at approx. -5 volts. Goes to 0 volts while key is in flight, and +5 volts when key is at rest in fully depressed position.

Pin 10 KEY DATA 2. Data from middle 24 keys.

Pin 11 KEY DATA 3. Data from top 25 keys.

Pins 11-21 Not Connected

Pins 22,23 -20 SUPPLY. Unregulated power supply to slave keyboard, +18 to +22 volts.

Pins 24,25 +20 SUPPLY. Unregulated power supply to slave keyboard, -18 to -22 volts.

4.8 Printer : MC062

Serial data from mainframe to optional printer, "busy" flag from printer to mainframe, plus "device on" signal used to switch on printer in readiness to receive data.

Connector type: Cannon 5 pin.

Pin 1 Signal Ground.

Pin 2 Not Connected.

Pin 3 FLAG0. "Busy" flag from printer. RS-232C levels. <-7 volts when printer ready, >+7 volts when printer busy.

Pin 4 DON0. "Device On" control from mainframe to printer. RS-232C level, >+7 volts to enable printer, <-7 volts to diable printer. This signal is optional as some printers do not require it.

Pin 5 DATA0. Serial data to printer. RS-232C levels, ASCII format. Normally at -10 volts. For each character sent from the mainframe to the printer a burst of +10 volt pulses lasting approx. 1 mS should be seen.

4.9 Phones

Output for driving headphones. Monitors the MIXED LINE output. Internally, this output is taken from the MONITOR (speaker) output via a 100 ohm resistor.

Connector type: 1/4" (6.25 MM) stereo phono jack.

The following signal lists refer to connectors on the rear of the C.M.I. Mainframe.

4. SIGNAL LISTS (continued)

4.10 Monitor

Output for driving a monitor speaker. The internal monitor amplifier will deliver a maximum of 20 watts R.M.S. into an 8 ohm speaker. Note that the Mainframe is fitted with a 1 amp speaker fuse which will blow if the monitor amplifier is driven to full output under load for more than a second.

Connector Type: Cannon 3 pin.

Pins 1,2 Ground

Pin 3 Active. With all channels producing a full-amplitude sinewave and the MONITOR control turned up to the point of clipping, this output should be approx. 38 volts P-P (with no load).

4.11 Channels 1-8

Individual channel outputs (balanced, 600 ohms impedance).

Connector type: Cannon 3 pin.

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3.7 volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

4.12 Mixed Line Output

Mixed output of all eight channels (balanced, 600 ohms impedance).

Connector Type: Cannon 3-Pin

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3.7 volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

4.13 Sync

Synchronising input and output, for use with Real-Time Composer (Page R), Music Composition Language (Page C) or Keyboard Sequencer (Page 9). This connector serves as both an input and ouput.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 Sync Input. Pulses or tone of 1 to 20 volts P-P. Waveform unimportant. Frequency range 2 Hz to 5 kHz. Impedance 10 K ohms.

Pin 3 Click Output. Periodic pulse, rate controlled by Page R - R.T.C., Page 9 Keyboard Sequencer or Page C - M.C.L. Waveform is a spike of approx. 5 volts peak, approx. 5 mS wide, alternately positive and negative going.

4.14 Filter Output

Output of the bandpass filter used by the Analog to Digital converter. It is designed to enable the operator to monitor the effect of various bandpass filter settings.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 OUTPUT. Amplitude for full-scale conversion is 10 volts P-P. Source impedance 600 ohms.

4.15 Mic In

Balanced, 600 ohms input suitable for high output dynamic or condenser microphones. When the MIC/LINE switch is in the MIC position, this input is fed to the Analog to Digital converter.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A

Pin 3 INPUT B

4. SIGNAL LISTS (continued)

4.16 Line In

Balanced, 600 ohm line level input. This input is connected to the Analog to Digital converter when the MIC/LINE switch is in the LINE position.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A. Amplitude of 1.4 volts P-P required for full scale conversion.

Pin 3 INPUT B. Amplitude of 1.4 volts P-P required for full scale conversion.

4.17 ADC DIRECT

Direct input to the Analog to Digital converter when the ADC DIRECT/MIC LINE switch is in the ADC DIRECT position. Because this input is Direct Coupled, any D.C. offset on this input will result in a D.C. shift of a sound sample.

Connector Type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 INPUT. Amplitude for full scale conversion is 10 volts P-P.

5. REPAIR PROCEDURE

Having isolated the faulty sub-assembly, service personnel should refer to the relevant service manual for further details about that item.

6. PREVENTATIVE MAINTENANCE

Under normal conditions, the only preventative maintenance required for the C.M.I. is periodical cleaning of the mesh above the blowers in the Mainframe. Refer to the C.M.I. Mainframe Service Manual for full details.

C.M.I. MAINFRAME - #MC001

SERVICE MANUAL

FAIRLIGHT INSTRUMENTS - FEBRUARY 1985

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1. INTRODUCTION

The C.M.I. Mainframe houses all the data processing and audio generation hardware of the C.M.I. System, including D.C. power supplies and floppy-disk drives.

This manual is designed to help service personnel locate and rectify a fault in the C.M.I. mainframe.

Note that this manual only refers to the Mainframe itself. The remainder of the C.M.I. System is covered by the following related documents:

C.M.I. SYSTEM SERVICE MANUAL
MUSIC KEYBOARD SERVICE MANUAL
ALPHANUMERIC KEYBOARD SERVICE MANUAL
GRAPHICS TERMINAL MAINTENANCE MANUAL
DISK DRIVE MAINTENANCE MANUAL

1.1 Card Cage

A 21-slot card cage houses a printed-circuit motherboard carrying edge connectors into which the C.M.I. circuit boards are inserted. The cards can be accessed by hinging down the front panel, and they can removed from the front of the unit without requiring the use of any tools.

1.2 Audio Board

Cables from the front of each channel card connect to the audio board located inside the rear panel of the mainframe. This card supports a variety of audio functions, including balanced line drivers for the eight channels and mixed output.

This card is accessed by removing the four mounting screws securing the rear panel and swinging the panel down. The card itself is held in place by screws. All connections are made by plug-in cables.

1.3 Power Supply

D.C. power is provided by a conventional transformer/rectifier system mounted inside the left-hand end of the card cage. This supplies power for the card cage, audio board, floppy-disk drives, music keyboard and alpha-numeric keyboard.

1.4 Floppy-Disk Drives

Two eight-inch, double sided, double density disk drives are mounted to the right of the card cage. They connect to the power supply via a wiring harness and to the floppy-disk controller card in the card cage via a 50-way ribbon cable.

1.5 External Connections

All external connections are made by means of plug-in cables. The mainframe is normally connected to A.C. mains, Graphics Terminal, Music Keyboard and audio equipment such as monitor speaker or mixing console.

The precise function of each external connection is described under Signal Lists.

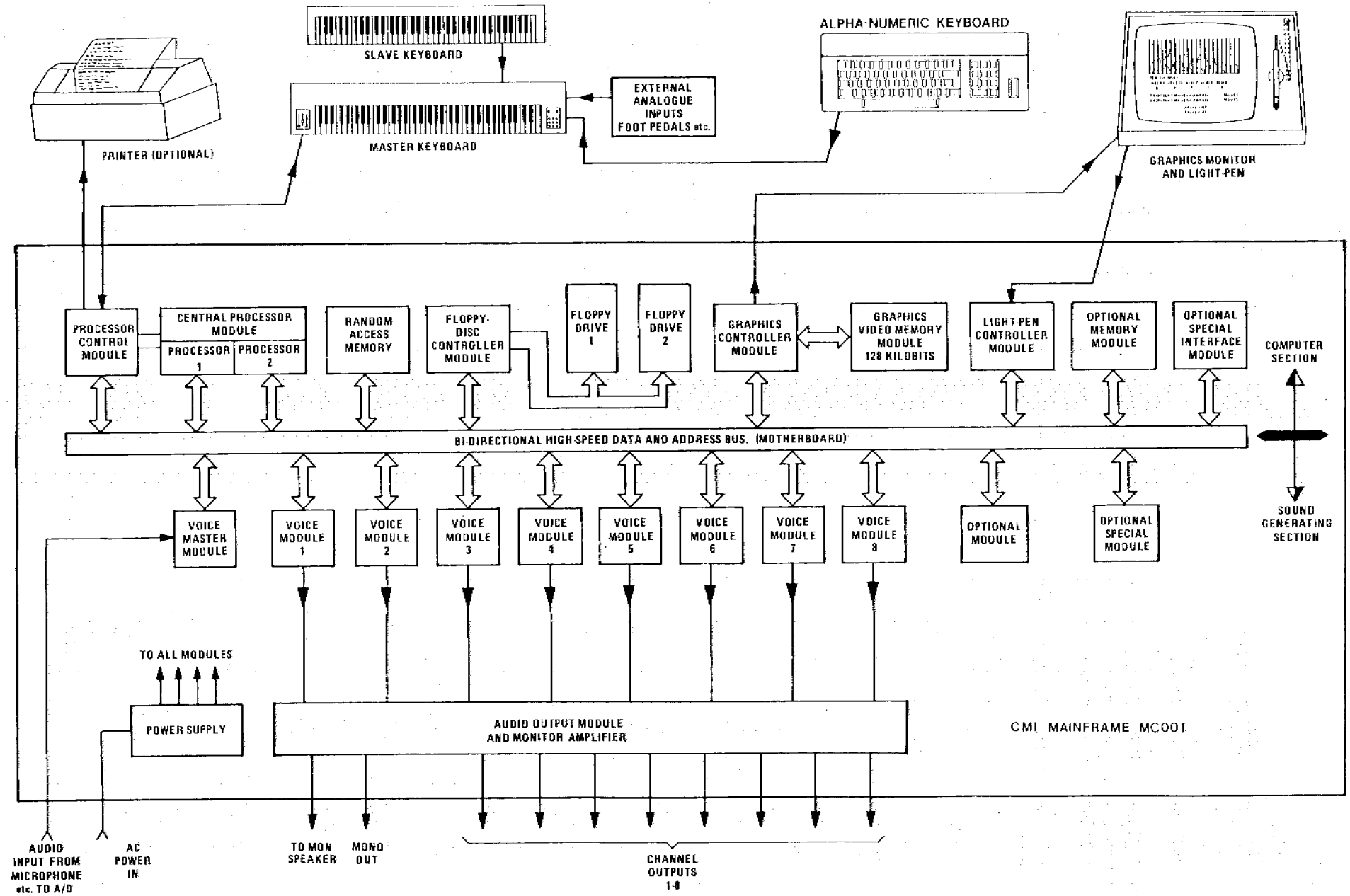


Figure 1 C.M.I. MAINFRAME BLOCK DIAGRAM

2. SYSTEM OVERVIEW

2.1 General Principles
(Refer to Figure 1)

The C.M.I. is a complex special-purpose computer system which embraces many different hardware and software technologies. All processing and sound generation functions are performed by the Mainframe, while the Graphics Terminal and Keyboards serve as peripherals for operator interfacing.

The mainframe is capable of operating quite autonomously, that is, it is not reliant on any external connections for proper functioning. Under certain conditions it is possible for a fault condition to inhibit proper Mainframe operation, so the serviceperson should be wary of being mislead. Of course, without the peripherals connected it is often hard to know if the system is functioning properly, but this point should be borne in mind when trouble-shooting.

Operator input to the Mainframe comes from three sources: music keyboard, alphanumeric keyboard and lightpen.
Output devices include the Graphics Display terminal and the audio outputs. A printer may also be optionally used.

The heart of the system is the Central Processing Module, which uses two Motorola 6809 microprocessors in a dual-processor configuration. Both processors share a common buss which allows them both to communicate with the other cards in the Mainframe.

The Processor Control Module provides EPROM for system startup and bootstrap, RS-232C serial input from the keyboard, serial output to the keyboard and printer, and various other C.P.U. support functions such as interrupt prioritisation.

Main program memory is the 256K RAM card. This holds all the operational software, much of which is overlayed from disk as the code exceeds 256K.

The Floppy-disk controller uses Direct Memory Access techniques to transfer data between memory and the two floppy-disk drives.

The Graphics Display is a bit-mapped image of 16K bytes of VRAM. This is displayed as an array of 256 by 512 points. Special hardware provides support functions for automatic vector drawing, which considerably enhances the speed of displaying graphical information. Hit and touch signals from the Lightpen are interfaced to the system buss.

Eight identical Voice Modules also share the buss. They each have 16K bytes of waveform RAM, as well as all the control and audio circuits required to support it.

A Voice Master module controls the voice modules, as well as providing the Analog-to-Digital converter function of the system.

Audio from the Voice Modules is buffered by the Audio Output Module, which provides independent balanced outputs for each channel as well as a mixed (LINE) output.

2.2 Hardware/Software Relationships

This section gives a summary of the operational concepts involved in each of the C.M.I.'s major functions. This information should help relate a particular software function to the appropriate piece of hardware.

The software system is divided into two main sections, the resident software and overlays. The resident part is responsible for all the real-time functions such as sound generation, keyboard input processing and lightpen operation. The overlays are used for the various control and sound manipulation functions provided by the display pages. Changing pages on the C.M.I. loads a new overlay for that page from disk. Some pages use further overlays themselves, so that when certain functions are invoked from a particular page for the first time, a disk access will be made as the overlay is loaded.

Both processors access 65K bytes of program RAM, switched from the 256K memory board, so that some of the code may be executed by each processor individually, and both processors can share common data structures. As a rule, processor 1 is responsible for controlling the voice modules (channel cards) and handling data from the keyboard. Processor 2 carries out the non real-time functions such as disk I/O and graphics display.

A broad description of a range of specified functions follows.

2.2.1 System Startup/Boot

When power is first applied to the system, a power-on reset signal is generated for about a half second by a timer located on the Processor Control card, Q133. At the end of this time, both processors fetch restart vectors from EPROMS, also on the Q133 card and start executing the startup procedure in EPROM. Processor 1 initialises all the registers of the peripheral controller devices such as P.I.A.s and A.C.I.A.s. Processor 2 initialises the Graphics Display, clears the screen, and displays the **LOAD SYSTEM IN DISK DRIVE** greeting. The message - **POWER ON** - is sent to the music keyboard display via the serial link on the Q133 card. Processor 1 then loops, waiting to be triggered by Processor 2, which in turn loops waiting for a disk to be inserted in drive 0, as indicated by the appropriate status bit from the Floppy-disk Controller Card QFC9.

When the system disk has been correctly inserted, processor 2 executes the first stage of the bootstrap loader firmware (located on the Q133 card). This involves reading in the boot block, which is a special sector on the system disk. The code stored in the boot block is then executed, which completes the boot load by loading the operating system and the Page 1 overlay. When Page 1 starts up, the message **PAGE 1 READY** is sent to the music keyboard display.

2.2.2 Disk Operations

The C.M.I. uses two eight-inch double-sided disk drives. Format is soft sectored, 128 bytes per sector (single density), or 256 bytes per sector (double density). FM recording is used for extra reliability.

The drives themselves are controlled by a Western Digital WD1791 L.S.I. controller located on the Floppy Disk Controller Card QFC9.

The disk driver EPROM located on the Q133 card is used as the lowest level disk driver. Routines in this EPROM provides utilities including read sector, write sector, and verify C.R.C. which are called by the RAM-resident disk-operating system.

In the event of a disk error being detected during a read or write operation, the software will perform a number of re-tries, including head relocation, to try to recover from the error. If the error persists, a **DISK READ/WRITE ERROR** message is displayed.

2.2.3 Lightpen/Graphics Display

The graphics display is generated by writing a bit-mapped image to the dedicated 16K byte VRAM. This block of RAM is mapped in and out of the processor memory space under software control.

The lightpen is interfaced via the Q219 Lightpen/Graphics Card, and an interrupt to Processor 2 is generated each time the lightpen the lightpen Touch and Hit signals are asserted simultaneously. The processor 2 resident code is then executed to poll the lightpen co-ordinate registers and the appropriate action ensues.

The lightpen cursor is a hardware function. See Q219 functional description.

2.2.4 Command entry

Data arriving from the Music Keyboard is fed to the A.C.I.A. on the Q133Processor control card. The A.C.I.A. generates an interrupt on processor 1 as each byte is assembled. Data from the music keyboard and characters from the alphanumeric keyboard both arrive at the same A.C.I.A. They are distinguished by the fact that music keyboard data has the high bit set. Data from the Music Keyboard arrives in the form of three-byte packets. These are assembled and queued by processor 1 for playing. Alphanumeric characters are passed on to processor 2. This is done via common memory and an inter-processor interrupt. Interprocessor interrupts are generated by special hardware located on the Master Card CMI02. See functional description.

2.2.5 Loading/Saving Sounds

Sounds are stored as contiguous VOICE files on disk. Each voice file occupies about 20K bytes of disk space. An entry in the directory on track zero gives the physical sector number of the start of the file. When a file is loaded, the directory is searched and the address of the file found. The sound is then loaded. Since processor 1 controls the channel cards, data is passed between the processors via a buffer in common memory.

If more than one channel is being loaded with the same sound, multiple channels are enabled by the Master Card so that they can be written to simultaneously. See Master Card functional description.

Saving sounds to disk operates by the reverse process.

2.2.6 Sound Sampling

Audio input for sampling is fed to either the LINE input or MIC input connector on the rear panel. It is amplified on the Audio Card CMI04 and then fed to the Master Card CMI02 via a 10-way ribbon cable. The signal is then attenuated by a digitally controlled attenuator and filtered by separate low pass and high pass filters on the Audio Card. These filters are also software controllable. The attenuator is controlled by the LEVEL control on PAGE 8 of the C.M.I. system software, and filter cutoff points are controlled by the Filter High and Filter Low controls.

From the filters the audio is fed to the Analog-to-Digital converter. The sample rate is governed by the frequency of a pulse stream coming from the Channel Card in channel one position. The sample rate is therefore established by software which sets up channel one to operate at the frequency specified as SAMPLE RATE on PAGE 8. Note that this **STOPS** channel one from sounding whenever PAGE 8 is selected.

Processor 1 is used to read data from the A to D converter and store it in the desired channel cards' waveform RAM. To synchronise the processor with the converter, processor 1 is forced to a HALT state while conversion is in progress. This causes processor 1's LED (on the Q209 Dual Processor Card) to glow whenever PAGE 8 is selected.

The TRIGGER LEVEL function on PAGE 8 is purely a software function. When the SAMPLE command is issued, the processor starts conversions and loops until the data read is of a greater absolute value than the number specified as TRIGGER LEVEL. It then begins transferring data to the waveform RAM.

2.2.7 Music Playing

Data arriving from the music keyboard is separated from alphanumeric keyboard strokes and assembled into three byte packets by processor 1. The A.C.I.A. routine is interrupt driven. Once a three-byte music keystroke packet has been assembled, the required note is played or stopped. The packet gives the keyboard number, whether the stroke was a depression or a release, and a key velocity number.

Once the correct channel or group of channels has been identified by software relating to the keyboard/register map on PAGE 3, they are started by the appropriate sequence of software commands. The channel cards generate a number of interrupts as the sound progresses and various parameters need to be updated.

Parameters fed to the channel card specify pitch, instantaneous amplitude, amplitude change (automatic ramping up or down), and position within the waveform.

The audio output from each channel card is fed to the audio card by a 10-way ribbon cable plugged into the front of the card.

2.2.8 Music Keyboard Functions

As well as sending music key depression/release data to the mainframe, the music keyboard has a number of ancillary functions.

A multiplexed analog-to-digital converter samples the level of the three faders on the left-hand end of the keyboard as well as the three pedal inputs on the rear. Whenever one of these changes its level by more than a certain amount, a packet of data is transmitted to the mainframe, giving the device number and the new level.

The two switches on the left of the keyboard and the three switches which plug into the rear of the keyboard are also scanned, and when any of these are opened or closed, suitable data is sent to the Mainframe.

Pressing a key on the numeric keypad on the right-hand end of the keyboard sends a character to the Mainframe in exactly the same way as an alphanumeric key depression.

The alphanumeric LED display on the music keyboard is driven by the serial link coming from the Mainframe. The processor in the keyboard controls the displaying of individual characters as well as **<rubout>** and **<clear>**. When messages longer than the 12 digits of the display are required, a horizontal scrolling routing in the C.M.I. system software is used.

2.2.9 Keyboard Sequencer - PAGE 9

When recording on the Keyboard Sequencer (PAGE 9), a hardware timer located on the Master Card CMI02 is used to measure the elapsed time between events such as key depressions or releases. As each event takes place, processor 1 assembles the keystroke or control change data into a five-byte packet along with the time to the next event and queues it. When the queue is half-full, Processor 2 writes the data to the sequence file on disk, emptying the queue.

In playback mode, Processor 2 reads the playback file into a queue. Processor 1 takes keystroke and timing packets from the queue and sets the timer on the Master Card for the time to the next event. When this time has elapsed, the timer generates an interrupt and the next event is pulled from the queue and played.

The MERGE function uses both RECORD and REPLAY.

When running on SYNC=INT(ernal), the timer operates by counting the system clock. When external synchronization is selected, SYNC=EXT(ernal), the timer is configured to use the external clock, which is derived from the SYNC input on the rear of the Mainframe, via suitable signal processing circuitry. The external sync is fed through another programmable timer so that it can be divided if desired.

2.2.10 Music Composition Language - PAGE C

M.C.L. data is stored on disk in the form of M.C.L. notation. The LOAD command simply causes processor 2 to read the file specified into RAM. No processing of the data is done at this stage.
When the PLAY command is issued, processor 2 starts compiling the source code and generates keystroke packets which it queues along with the time to the next event, which it calculates from the combination of up to eight parts which it may be played simultaneously. These packets are then processed by processor 1 in much the same way as for the PAGE 9 sequencer.

Internal/external synchronization works the same way as for PAGE 9.

3. SPECIFICATIONS

3.1 ELECTRICAL

Power Requirements
- Mains Voltage: 100-120 or 200-250 switch selectable
- Mains Current: 2 amps @ 240V, 4 amps @ 120v
- Mains Frequency: 50/60 Hz

3.2 AUDIO

Channel Outputs
- Connector type: Cannon XLR 3 pin (balanced)
- Number of channels: 8 (maximum)
- Output level: 3.7 volts p-p
- Output impedance: 600 ohms
- Output load: Greater than 600 ohms

Mixed Line Output
- Same as channel outputs

Monitor Speaker Output
- Connector type: Cannon XLR 3 pin
- Load impedance: 4 ohms (minimum)
- Power output at clipping: 20 watts maximum
  (This output is not intended to be driven to full output continuously)

Headphone Output
- Connector type: 1/4" Stereo Phones
- Signal: Derived from monitor speaker output via 100 ohm resistor

Sync Input
- Connector type: Cannon XLR 3 pin
- Level: 1 volt (min) to 20 volt (max) p-p
- Frequency range: 2 Hz to 5KHz
- Impedance: 10KHz

Click Output
- Connector type: Cannon XLR 3 pin
- Output signal : 5 volt spike, approx 5 msec wide, alternatively negative and positive going.

Mic Input
- Connector type: Cannon XLR 3 pin
- Impedance: 600 ohms
- Microphone type: Balanced, high output dynamic or condenser type

Line Input
- Connector type: Cannon XLR 3 pin
- Input signal: Balanced
- Sensitivity: 1.4 volts p-p required for full scale conversion

ADC Direct Input
  Connector type: Cannon XLR 3 pin
  Input signal: D.C. coupled
  Sensitivity: 10 volts p-p for full scale conversion
  Impedance: 100K ohms

3.3 DIGITAL

Processor: Dual 6809

Memory: 256K bytes Program RAM
        128K bytes Waveform RAM
        16K bytes Video RAM

Floppy Disk: 2 x Mitsubishi M2896-63
             8 inch double sided, single/double density
             Soft sectored, 128/256 bytes per sector

Graphics Display: Bit mapped VRAM
                  Composite video output
                  1 volt p-p nominal
                  75 ohms impedance

Input/Output: Serial RS232C, 9600 Baud

3.4 MECHANICAL

Dimensions: Width 750 mm
            Depth 450 mm
            Height 320 mm

Weight: 40 kilograms

4.0 FUNCTIONAL DESCRIPTION

This section describes the operation of each of the circuit boards used in the C.M.I. mainframe. The information is presented primarily to give service personnel a thorough understanding of the operation of the system as an aid to fault diagnosis to the board level. Once the faulty board has been identified, it is recommended that the Mainframe be repaired by board exchange. The faulty item should be returned to Fairlight Instruments for repair.

4.1 Q209 DUAL 6809 CENTRAL PROCESSOR FUNCTIONAL DESCRIPTION

4.1.1 INTRODUCTION

The Q209 contains the dual 6809 processors, on board processor communication hardware entailing, indivisible instructions, processor readable identification/map state, interprocessor interrupts, automatic map switching FUSE register and hardware trace logic to enable single stepping for software debugging.

The Dual Processor card multiplexes each processor onto a common address and data buss in an interleaved manner, each processor therefore may simultaneously access the same memory location without any contention, if the memory is mapped onto both proccessors. (See Q256 functional description)

The memory addresses are issued to the buss 225 nanoseconds prior to the access cycle, allowing addresses to be mapped by the memory card, to allow for accessing greater than 65k of RAM.
Many global timing signals are issued from the processor for general buss control.

4.1.2 TIMING AND MEMORY CONTROL LOGIC
(refer to drawing Q209-02)

4.1.2.1 Master Timing Signals

All system timing signals are derived from crystal-controlled 40Mhz oscillator Q1. Flip-flop 10F derives two opposite phase 20 Mhz square waves. Quad D-type latch D2, together with the NAND gate in 7F, forms a 10 state Johnson, or twisted-tail ring counter. Each state is of 50ns duration. The system signals are decoded by NAND gates in 8E from the output of this counter.

4.1.2.2 Dynamic Memory Timing Signals

Four non-inverting buffers of 10A are driven by latch E1 to provide CAS (Column Address Strobe), RAS (Row Address Strobe), CA (Column Address, active low) and RA (Row Address, active low). RAS is delayed relative to CAS by about 20ns by the propagation delay of 11E. RA and CA are complementary.

4.1.2.3 Data and Address Buss Multiplexing
(refer to drawing Q209-03)

Flip-flop 6F, along with associated gating generates the 6809's E signals. The system address buss is multiplexed by the ADDRESS signals ADD1 and ADD2, (active low). One-of-four decoders 3E and 4E are used to enable the appropriate address and data buffers, to perform the multiplexing. The data buffer enable signals WRITE1, WRITE2, READ1, READ2 are generated by logical combinations of R/W, VMA, processor phase 2 and DMA lines. The address buss is actually multiplexed 4 ways, as the vectored interrupt system may also acquire the buss' least significant bits of the address buss for either processor's vector fetch cycle. The address buffer enables are a function of the Address signal and the Interrupt acknowledge.
Phase 2 reference and Address references for each Processor are fed to the buss via buss drivers.

4.1.2.4 Interrupt Strobe Generation
(refer to drawing Q209-02)

Dual D-type flip-flop 9D and 3-input AND gate 8D feed Interrupt Strobe pulses to the buss. These are used by the Priority Interrupt Control Units (PICUs) used to provide Vectored interrupts, and also to strobe the vector address latches 8A and 9A. The PICUs are located on the Q133 card. These signals strobe the priority latches continuously, until an interrupt is acknowledged. In this way the Interrupt Priority is maintained at its latest level regardless of delay between an interrupt request being received by the PICU and the associated vector-fetch cycle being executed.

4.1.2.5 Direct Memory Access
(refer to drawing Q209-00)

DMA requests for each processor are clocked into flip-flop 11D on the falling edge of the phase 2 signal of the respective processor. DMA acknowledge is sent to the buss via buffers and drive signals to the processors are suspended in the phase 1 state for the duration of the DMA cycle. The maximum permissible DMA duration is 5 microseconds. Worst-case DMA latency is 1 microsecond. Latency is the time required to service the request.

4.1.3 CPU MEMORY SWITCHING and VECTORS

4.1.3.1 Vector-Fetch Decoders
(refer to drawing Q209-01)

The vector state of the processors are decoded by the one-of-four decoders, 2D and NOR gates in 1D. These correspond to addresses in the range FFF0 to FFFF. They correspond to the processor fetching vectors FIRQ, NMI, SWI1, SWI2, SWI3, IRQ and RESTART. The Restart vectors come from ROM so when this is sensed the ROM is enabled and the ram disabled. This is achieved by the ROMEN signal on buss pin 44. On detection of an Interrupt Request vector address from the processor, decoder 2D causes the normal address buss drivers for bits 1 to 4 to be disabled and the Interrupt Address buffers to be enabled in lieu.

4.1.3.2 Processor System Control

These general functions are controlled through ports at the following locations ...

$FC5E	Indivisible instructions	read
$FC5E	Various CPU functions	write
$FC5F	Map status and CPU ID	read
$FC5F	Automatic map switching FUSE	write

The ID can be read to determine the status of the memory map switching harware. The CPU ID bit can be read by the CPU to find out which CPU is running the program.

The bits are defined as

D0	CPU ID 0=P1 1=P2
D1	P1 map status 0=map B, 1=map A
D2	P2 map status
D3	zero
D4	n/c (indeterminate)
D5	n/c
D6	n/c
D7	n/c

The "Various CPU functions" is an 8 bit register in which each bit may be independently written to. This register is at location 6D, and it is decoded by devices at 9B and 7A. When written to, the bit address is selected by the 3 least significant bits of the data byte. The state of data bit 3 determines whether the bit is set or cleared.

The four functions provided per processor from this register are

0+P	interprocessor interrupt
2+P	hardware trace
4+P	map switch select
6+P	fast interrupt request

where P is "0" for processor 1 and "1" for processor 2.

Fast interrupts may be generated either by an external signal or from the bus. The on-card FIRQ must be reset by the processor concerned, by writing a reset bit to the register.

4.1.3.3 Automatic Map Switching
(refer to drawing Q209-02)

The memory cards support hardware selectable memory maps. The processors can control the A/'B select lines, allowing automatic switching between "user(B)" and "system(A)" maps.

Whenever an interrupt or processor restart occurs, the A map will be automatically selected. During an interrupt, the switching will occur after the registers are stacked and before the interrupt vector is fetched.
A FUSE location is provided which causes the map to be switched after a specified number of CPU clock cycles have elapsed. These counters are at 8C for CPU1 and 9C for CPU2. The data written to these counters is buffered by the buffer at 7C. The map changed to is determined by the value of the map switch select bit.
The map switch will occur after the Nth CPU cycle after the FUSE register write. The delay is required so that a known number of instructions can be excecuted for house keeping before the CPU's memory is swapped.
Hardware also selects the A map whenever DMA occurs.

4.1.3.4 Hardware Trace

An NMI may be generated after each instruction execution for software debugging. This is done by flip-flops 5D and half of AND gate 4F. This function is enabled under software, by access to $FC5E.
Enabling this function inverts the NMI signal from the front panel, so that if the trace hardware is left in the triggered state, front panel NMI requests will still be recognized, but on the opposite edge (since NMI is an edge triggered input).

4.1.3.5 Indivisable Instructions
(refer to drawing Q209-00)

For the test-and-set and double byte load/store instructions to be effective, the processor not executing the instruction must not be able to alter the flag memory location in question. To this end, the execution of these read/modify/write instructions effectively hangs the other processor for its duration, thus preventing race conditions. This is achieved by flip-flops 10D, 10E associated gating and the BUSY outputs from the processors. The BUSY outputs are active when the test and set instruction is executed, and the other processors clock is stopped for its cycle, in the same manner as for DMA transfers. The flip-flops asociated with this are reset at power-on to enable the clocks to the 6809's to allow them to be internally reset, at power-on reset. To enable this function the instruction to be made indivisible must be immediately preceded by a read from hardware location $FC5E. No interrupt must be allowed to occur between the read and the instruction. This function is automatically disabled at the end of the instruction following the read.

4.1.3.6 Link Options

The links have the following functions ...

Option	CPU	LINK	Function
W1	P1	1-2 *	enable map select output
		2-3	disable
W2	P1	1-2 *	enable DMA to select A map
		2-3	disable
W3	P2	1-2 *	enable map select output
		2-3	disable
W4	P2	1-2 *	enable DMA to select A map
		2-3	disable
W5	P1	1-2	disable P1 DMA during indivisible P2 cycles
		2-3 *	enable
W6	P2	1-2 *	disable P2 DMA during indivisible P1 cycles
		2-3	enable

These links are set by PCB traces in the positions marked by * and should not need to be changed.

4.2 Q133 C.P.U. CONTROL CARD FUNCTIONAL DESCRIPTION

4.2.1 INTRODUCTION

The CPU Control Card provides several support functions required by the CPU card. These include startup and bootstrap ROM, 4 serial communication ports, interupt prioritisation, dynamic ram refresh, day/date/time of day clock, P1 DMA daisy chain, and a parallel port.

4.2.1 Address Map

The Debug Card occupies the last 4K bytes of the 65K byte memory addressing space and is set up as follows:-

ADDRESS (HEX)	FUNCTION	
F000-F7FF	Rom0	common rom
F800-FBFF	Rom1	processor unique
FC00-FCEF	Available for peripherals	
FC80-FC8F	ACIA registers	
FC90-FC97	Timer (6840)	
FCF0-FCFF	PIA registers, user and clock	
FCFC	CPU#1 interrupt prioritiser	
FCFD	CPU#2 interrupt prioritiser	
FD00-FEFF	Shared 512 byte RAM	
FF00-FFFF	Unique 256 byte RAM for each processor	

4.2.1.2 Restart and Interrupt Vectors

RAM space allocated uniquely to each processor provide independent restart and interrupt vectoring. The vector locations are as follows:

ADDRESS (HEX)		VECTOR
FFFE/F		Restart
FFFC/D		NMI
FFFA/B		SWI1
FFF8/9		Unused
FFF6/7		FIRQ
FFF4/5		SWI2
FFF2/3		SWI3
FFF0/1		Unused
FFEE/F	(lowest)	IRQ level 7
FFEC/D		IRQ level 6
FFEA/B		IRQ level 5
FFE8/9		IRQ level 4
FFE6/7		IRQ level 3
FFE4/5		IRQ level 2
FFE2/3		IRQ level 1
FFE0/1	(highest)	IRQ level 0 (highest)

4.2.1.3 Debug Monitor ROM

The Q133 contains two 2K ROMs that contain all the basic driver and initialization routines, such as loading the disk drivers and Q256's maprams. The monitor ROM occupies 1K bytes from F000 to F3FF and may be accessed by either processor. Processor-unique workspace RAM is used by the monitor so both processors can be executing the monitor independently.

Commands

AAAA/	Open 1-byte unit at address AAAA
/	Reopen last open address as a 1-byte unit
AAAA\	Open 2-byte unit at address AAAA
\	Reopen last open address as a 2-byte unit
$A	Open CPU accumulator A
$B	Open CPU accumulator B
$X	Open CPU index register X
$P	Open CPU program counter
$H	Open user SWI handler address
$C	Open CPU Condition Code register
$D	Open CPU D register (A,B concatenated)
$Y	Open CPU index register Y
$U	Open CPU User Stack pointer U
$S	Open CPU Stack pointer S
$R	Open program segment Relocation Register
$G	Open CPU direct page register
$F	Open monitor flag byte

<return>	Close the open location
<linefeed(CTRL J)>	Close current, open next location
<^(SHIFT N^)>	Close current, open previous location
>	Close current, take branch offset and open
@	Open location pointed by current location

AAAA;B	Insert a breakpoint at address AAAA
;L	List all active breakpoints
AAAA;D	Delete breakpoint at address AAAA
;C	Clear all breakpoints

AAAA;T	Insert tracepoint at location AAAA (non-stopping breakpoint)
AAAA;K	Kill tracepoint or breakpoint at AAAA

AAAA;G	Start a user program at address AAAA
;P	Proceed from breakpoint, abort, or call

AAAA;O	Calculate branch offset from open location to address AAAA

HH;F	Fill memory from beginning address to end address
BEG ADDR	User prompt for beginning address
END ADDR	User prompt for end address
<CTRL X>	Abort current command line, take no action
<	Close current location, return to sequence start and open
AAAA,R	Relocate address AAAA by register R. R may be any of the CPU registers, the user relocation register, the monitor flag byte or the currently open location
AAAA.	Relocate address AAAA by Relocation Register $R
:	Same as linefeed (CTRL J) except that no new line is taken, and neither the address nor contents of the next location is displayed
AAAA#LL	Memory dump of LL lines (16 bytes/line) starting from address AAAA
'<ASCII chr>	Input ASCII character value instead of hex value for any of the above commands

The 6809 monitor will also accept input of signed hex numbers.

4.2.1.4 System Boot/Disk ROM

This ROM is used by CPU#2 for disk booting operations and occupies locations F800 to FBFF in the unique ROM space for CPU#2.

The following functions calls are provided:-

* Boot load QDOS operating system from disk
* Initialise disk controller
* Read full last sector
* Read partial last sector
* Read verify (CRC check only)
* Write and verify CRC
* Restore head (seek track 0)
* Seek to specified track
* Write test
* Write D.D. mark to sector
* Write sectors and verify CRC
* Write sectors and don't verify CRC
* Check and abort if non-recoverable error

This ROM contains the code to load the actual disk drivers into system RAM. The driver routines themselves are stored in RAM after being loaded from the ROM on the QFC9 floppy controller card, and the Q077/Q087 Hard Disk card if present.

4.2.2 ADDRESS DECODING and RAM REFRESH CONTROL

4.2.2.1 Address Decoding
(refer drawing Q133-00)

The System Address Buss is buffered by non-inverting buffers A1 and A4. NAND gate B1 generates an output (asserted LOW) when an address in the range FXXX is detected. This is fed out to the buss on edge connector pin 60B. Further decoding by combinational logic at B4, D4, B3, C2 and C1 generate select signals for the two EPROMS, $\overline{\text{ROM0}}$, $\overline{\text{ROM1}}$.

Selection of the on-card static RAM and peripheral devices in the FCFX range are also decoded.

These six select signals are latched by hex flip-flop B6. Hex flip-flops C7 and D7 latch the 11 low-order address bits, as well as the READ/WRITE signal. When any of the on-board devices are read from, inverting data buss transceiver A5 drives the buss. (See drawing Q133-03). At other times, A5 buffers the data into the card.

4.2.2.2 RAM Refresh Control

Rate multiplier C10 is configured to produce a 1 microsecond pulse every 16 microseconds. This output generates a DMA request for Processor 1 ($\overline{\text{RDMA}}$), via DMA hardware at C8, B10 ,B5 and C4. The refresh has the highest priority in the P1 DMA daisy chain.
The $\overline{\text{ENL}}$ signal, (Enable Next Level), indicates to the next device along the daisy chain when it may make DMA requests. It normally goes low every second P1 cycle, but if a refresh request is pending, the low pulse is inhibited.
When this request is acknowledged, by the ACK1 buss signal from the Q209 CPU (asserted HIGH), flip-flop B10 generates a $\overline{\text{REF}}$ (Refresh, asserted LOW) signal on the buss, which signals a refresh cycle to the dynamic RAMs in the system. At the same time, the output of the refresh address counter A2 is driven onto the buss by tri-state buffers A3. At the completion of the refresh (DMA) cycle, the refresh address counter is incremented ready for the next cycle.

4.2.3 EPROM, RAM, ACIA, PIA
(refer to drawing Q133-01)

4.2.3.1 Static RAM

A small amount of static RAM is provided for use as scratchpad during disk calls and monitor firmware execution. It is organised as follows:

CPU #1	FF00-FFFD
CPU #2	FF00-FFFD
Both	FD00-FEFF

The addressing function for this purpose is generated by multiplexer C9 which is driven by an OR funtion of address bits 8 and 9. The RAM itself is in the form of two 1k X 4 devices at D8 and D9.

4.2.3.2 EPROM

Four kilobytes of U.V. erasable ROM are used. These are 2716/2516, single 5 volt supply type.

Their functions are:

Location	Address Range	CPU #	Function
D2	F800-FBFF	1	Startup
D4	F800-FBFF	2	Disk boot
D5	F400-F7FF	Both	I/O functions
D6	F000-F3FF	Both	Debug monitor

4.2.3.3 ACIA (Asynchronous Communications Interface Adapter)
(refer to drawing Q133-02)

6551 ACIAs at E4, E5, E1, E2, E3 are used to receive and transmit serial data. The BAUD rate is determined internally via internal dividers, from the baud-rate generator master 1.8432Mhz oscilator at D1.

Interrupts generated by the ACIAs go to the system buss via pin 68B of the edge connector.

Data input and output level conversion for the RS232C standard is provided by circuitry on Sheet 3.
The 6551 used for keyboard data is at location E2, 3. The ACIAs at E4 and E5 have optional RS422 transceivers at F7 and F8 as well as RS232C, at F6 and F5. The 555 timer at D10 is used in the RS422 buss timeout control.

4.2.3.4 PIA (Peripheral Interface Adapters)
(refer to drawing Q133-01)

PIA (F10,11,12) is used to provide two general purpose parallel ports. Peripheral connections are made through a 26-way ribbon cable connector on the front of the card.

Interrupts from the PIA are presented to the buss via pins 66B and 67B.

PIA (E9,10,11) is used to interface the clock/calander chip at E12. This clock has a 3.7 volt Lithium cell to maintain the time when the computer is turned off. The battery is not rechargeable and must be replaced when flat. Battery life is approximately 3 years. Diodes CR5 and CR4 isolate the battery from the 5 volt supply, so that the battery is only connected to the clock when the 5 volt supply drops. Transistors Q2, Q1 on drawing Q133-03, and associated components interface the PIA's signal levels to the clock and control the power-down function of the clock so that no false writes occur at power-on and off. An optically isolated power down signal is available at connector pins 61B and 62B, from the opto-isolator at A11.

4.2.4 MANUAL CONTROLS, POWER-ON RESET
(refer to drawing Q133-03)

4.2.4.1 Manual Controls

Restart, halt and interrupt contols are provided on the front-panel card Q137. The sole use is for system debugging. In normal use all signals from the Q137 are inactive.

Activating either HALT switch on the front panel sends $\overline{\text{HLT1}}$ or $\overline{\text{HLT2}}$ to the corresponding processor on the Q209 CPU. When halted , the Buss Available signals from the CPU card W1 and W2 drive open-collector buffers B12 to turn on the WAIT LEDs on the card.

The system can run without a front panel being connected.

4.2.4.2 Power-on Reset

555 Timer A12 is used to generate a system-reset signal on power-up or manual restart from the front panel console, if restart is enabled on both processors. This is a low-going pulse of about 500 milliseconds on buss pin 42.

4.2.5 INTERRUPT PRIORITY LOGIC AND DATA BUFFERS
(refer to drawing Q133-03)

4.2.5.1 Interrupt Priority Logic

8214 Priority Interrupt Control Units (PICU) are used to latch interrupt requests and generate a priority level which is used by the CPU card to create an interrupt vector address. Each processor has its own PICU.

The priority level for each PICU is established by writing the complement of the desired priority level into the status register. The address for CPU 1 is FCFD, for CPU 2 it is FCFC. Decoding for this purpose is performed by one-of-eight selector B8.

Interrupt requests generated by the PICU are latched by flip-flops B9, which are reset when the PICUs are written to to establish the new priority level mask.

The PICUs are clocked by Interrupt Latch Strobe signals from the bus (ILS1 and ILS2).

Each PICU supports up to eight levels of interrupt.

4.3 Q256 256K RAM CARD FUNCTIONAL DESCRIPTION

Note - In this document active low signals are indicated by a slash (/) in front of the signal name. This document is updated for the Rev. 2 Q256.

4.3.1 INTRODUCTION

The Q256 is a 256K x 9 bit dynamic RAM, organised as four blocks of 64K and mapped in 2 or 4K chunks. 32 different mappings from "processor space" to physical memory space may be set up. The mapping selected for any given cycle is automatically switched according to the current machine state. The machine state comprises which processor is on the buss, the user state/system state output of the processor, and which DMA channel is active, if any.

The ninth bit in the memory is a parity bit. Parity generation takes place automatically upon writing to the RAM and parity error detection is automatic when reading. If a parity error is detected, an interrupt is generated. A status register records that a parity error occurred, the physical memory block in which it occurred, and the upper five bits of the processor address which was active at the time of the error. The error status bit is automatically cleared after the register has been read.

The map selection logic also generates three control signals:

1) PENB is a universal buss signal which enables or inhibits access to all peripherals on the buss. This signal is fed via the motherboard back into the Q256 since the map selection logic and the mapram are themselves peripherals. The output signal is forced active after power up to ensure configuration of the mapping system is possible, and released by the first read of the parity status register.
2) VENB is a video ram enable bit which allows accesses in the range $8000 to $BFFF to read or write to the graphics ram or user ram which may be mapped into this area instead.
3) PERGEN is a bit used to artificially generate parity errors to for testing purposes.

4.3.1.1 Options

Option blocks W1 and W2 allow selection of mapping on 2K or 4K byte boundaries as marked on the component overlay. If 4K mapping is selected, every second double-byte mapram location is not used. W1 and W2 must be configured identically. Default links on the PCB are for 2K mapping.

Option block W3 is for debugging purposes and need only be installed if a faulty card is crashing the data buss of the test machine. The default PCB link to +5V must be cut. There are two non-default options. Option 3 (GND) permanently inhibits the data buss driver buffer. The memory can still be written to but read data will only get as far as the buss output buffer. This facility allows the operating system to boot and test programs to run on a healthy board while the faulty board runs in parallel without driving the data buss e.g. for signature analysis. Option 2 prevents the data buss driver from outputting data only until the first read from the status register. This was handy in debugging the prototype but is unlikely to be much use for routine testing. The standard restart ROM checks all parity status registers automatically so a non-standard ROM would have to be used.

A four-way DIP switch is provided to allow multiple Q256 boards to be installed. Only switches 1-3 are used, so up to 8 boards can be installed. Close a switch for each zero in the board number, i.e. card 0 has all switches closed. SW1 is the LSB.

4.3.2 ADDRESS DECODING and MAPPING LOGIC

4.3.2.1 Map Selection Logic
(Refer to drawing Q256-00)

The function of the map selection logic is to encode the current system state and generate a five-bit map selection number. It also generates the peripheral enable output signal (PENBOUT), the video ram enable signal (VENB) and a parity error generate signal (PERGEN) which forces an artificial parity error for testing purposes.

There are six possible states for each processor:
A or System state, no DMA
B or User state, no DMA
DMA on any one of four DMA channels. (Processor automatically switches to A state for DMA cycles).

The A/B/DMA state is encoded as three bits and the processor phase signal is added as a fourth bit and presented as an address via the multiplexor IC 4B to the map selection RAM (mapsel) ICs 5D and 6D. Thus each state corresponds to a location in the mapsel and its output data is the map selection number.

DMA claim signals (DMACpn, where p=processor and n=DMA channel) occur when a DMA peripheral has received a DMA acknowledge from the processor and arrive during the data phase preceding the actual DMA cycle. IC 13A is an 8 to 3 line encoder but since there are four channels for P1 and four for P2 the most significant output line only duplicates the processor phase signal and is not used. The GS output indicates that some DMA channel is active. Each processor has its own A/B line (AB1 and AB2). The nand multiplexor 9A selects whichever is relevant for the next cycle. This signal, plus the combinatorial logic of 10B, 11A and 11B and the buffered phase signal (/Bø22) provide the four-bit state number to the multiplexor 4B.

The mapsel RAM occupies locations FC40-FC4F. Since there are six possible states per processor only twelve locations are actually used, as follows:

FC40	P2 B state
FC43	P2 A state, no DMA
FC44	P2 A state, DMA channel 1
FC45	P2 A state, DMA channel 2
FC46	P2 A state, DMA channel 3
FC47	P2 A state, DMA channel 4
FC48	P1 B state
FC4B	P1 A state, no DMA
FC4C	P1 A state, DMA channel 1
FC4D	P1 A state, DMA channel 2
FC4E	P1 A state, DMA channel 3
FC4F	P1 A state, DMA channel 4

Access to these locations for initialization of the mapsel is decoded by IC 1B, along with the peripheral enable input PENBIN. The output of IC 1B is latched on rising BRA by IC 4A (drawing Q256-03) to produce /LFC4X.

Writing to the mapsel RAM is the most time-critical of all operations on the Q256. Normally the entire current data phase is available to generate the map selection number for the next cycle but when writing, the current data phase must be used to write to the mapsel ram as well. This is achieved by making mapsel write cycles very short. To choose locations within $FC4X the mapsel address multiplexor IC 4B is switched over to the lower four latched address bits on the falling edge of ADD2ø2 (data and address busses are in phase). The data is written into the mapsel ram on the rising of /BRA (IC 10B). The write pulse is removed and the multiplexor switched back to the current state number only 50nS later by the falling of /BCAS (IC 10A).

The lower five bits of the mapsel RAM are the map select number (MAPSEL0-4). This plus the controls PENBOUT, VENB and PERGEN are latched on the rising of ADD2ø2 which begins the next address cycle.

The peripheral enable signal (PENBOUT) and the graphics enable (VENB) come from bits 7 and 5 of the mapsel ram respectively. After power up or system reset they are both forced active (high) by the flip-flop IC 14B so that access to the mapsel ram is ensured for initialization. This flip-flop also inhibits the data buss driver IC 9B (drwg Q256-03) if W3 has been linked to option 2 for debugging. The flip-flop is triggered as soon as either processor reads the parity status register and will remain set until the next /SYRES.

Format of data written to the mapsel RAM is as follows:

Bit 0-4 Map select number MAPSEL0-4. (Inverted)
5 VENB (Write 0 to enable graphics ram)
6 PERGEN (Normally 0, 1 to force a parity error)
7 PENBOUT (Write 0 to enable peripherals)

4.3.2.2 Address Translation
(Refer to Drawing Q256-01)

This section performs the mapping from the 64K processor address space onto the 256K physical address space. The outputs LMAP0-4 and MAP5,6 plus standard address lines MA0-10 constitute the 18 bit address required to uniquely access any location in 256K.

All mapping data is stored in the two 2148 static RAMs (mapram), each containing 1024 x 4 bits. If 2K mapping is selected, the lower five address lines of the mapram come from the upper five processor address bits via multiplexor ICs 2B, 3B and 3D. This divides the 64K processor space into 32 blocks of 2K each. In 4K mode only the top 4 processor lines are used and the LSB of the mapram address is tied low. The upper five mapram address lines come from the latched map select number, thus any one of 32 different complete mappings may be selected. The data outputs from the mapram include a card select bit (CSEL), a two-bit 64K rank select (MAP5,6), and a five bit page select which is latched on rising BRA (LMAP0-4). The page select bits become the upper physical address bits.

Although the mapram is 1K bytes in size it in fact occupies 2K of address space, from $F000-F7FF. Even locations in this range are dummy locations which serve only to set up the CSEL flip-flop, IC 1E. Writes to odd locations then store this single bit along with 7 bits of mapping data in the mapram. So a single 16-bit write to the mapram maps one 2K or 4K page of processor space to any 2K or 4K physical page in the 256K available. The processor space being mapped is determined by the address within $F000-F7FF written to and the physical page selected is given by the data written.

Valid addresses in the mapram range are decoded with the buffered peripheral enable signal (BPENBIN) by IC 2A and the write map (WMAP) signal is latched by IC 4A (drwg Q256-03). The mapram address lines are switched over to LA1-LA10 on the rising of /ADD2ø2 by IC 2D. The 2148s have common data-in and data-out lines multiplexed by the write (/W) input. If an odd address is being written, the buffered data buss is driven into the 2148s from IC 4C and the /W input strobed by the upper LS20, IC 1D on the rising of /BRA. The write pulse is terminated by falling /ADD2ø2, and data hold time to the 2148s is provided by the disable delay of IC 4C.

Writing to an even address triggers the CSEL flip flop IC 1E on rising /BRA. The data to this flip flop is the result of the three-bit comparison of BD0-2 with the card select no. set up on the DIP switch, qualified by BD7 which may be used as an overall page enable bit. Thus mapram data format is as follows:

Even locations
- Bit 7 Page enable
- Bits 5-3 Unused
- Bits 2-0 Card select

Odd locations
- Bit 7 Unused
- Bits 6,5 Physical 64K block select
- Bits 4-0 Physical 2K block select
  (Bit 0 not used in 4K mapping configuration)

Note that when mapping multiple pages of memory in or out the CSEL flip-flop need only be set up once, after which only writes to odd locations in mapram are required.

4.3.2.3 Memory Block Decoding
(Refer to Drawing Q256-02)

This section generates RAS and CAS controls for each of the four memory ranks according to mapping outputs MAP5,6 and the card select signal CSEL.

MAP5,6 are decoded to a 1-of-4 block select signal by IC 1E provided a valid address is on the buss (VMA), the Debug's Ram inhibit (/RAMINH) is inactive, and neither $FC4X nor the mapram are being accessed. IC 5E latches this select along with the refresh signal REF, read/write (mapsel, mapram, or status), read/write memory, and access memory signals on rising BRA. IC 2E generates the READ signal to drive the data buss while /BRA is high (see drwg Q256-03).

Refresh cycles cause the system RAS signal to be distributed to all four memory ranks simultaneously through ICs 6F and 6E. No rank select and thus no CAS is generated during refresh cycles. During a valid memory access one rank is selected and CAS is routed to that block through ICs 5F and 6E. The R/W signal drives all ranks through ICs 5F and 3E.

4.3.3 BUSS INTERFACE
(Refer to Drawing Q256-03)

The buss address lines are buffered by ICs 6B and 5A and latched on rising BRA by ICs 4A and 5B for mapram and mapsel ram writing and status register reading, along with address decode signals WMAP and /FC4X.

Unmapped address lines MA0-10 (and MA11 in the 4K mapping configuration) plus mapping outputs LMAP0-LMAP4 (excluding LMAP0 for 4K mapping) are multiplexed onto the RAM address lines by ICs 5C and 6C.

IC 9B latches the RAM outputs on the falling edge of CAS and drives the buss when READ is high unless the debug option W3 prevents this. Data is buffered off the buss to mapsel, mapram, main RAM and parity generator by IC 7B.

4.3.4 Parity System
(Refer to Drawing Q256-04)

The parity bit is automatically generated by IC 7D from the data on the buss when writing to RAM. This bit is written into the appropriate 6665 when the corresponding CAS signal is generated (see drawing Q256-02).

A RAM read cycle causes the parity bit from the selected block to be read out of the parity RAM while IC 7D simultaneously regenerates the same parity bit from the data actually leaving the main RAM and coming back in again through data buffer IC 7B. Thus parity errors may be caused by buss errors as well as RAM faults. The parity memory bit and the regenerated parity bit are compared by exclusive or gate IC 4F. The result of this comparison is only valid for about 150nS and is clocked by rising /BRAS into flip flop 14B to generate the parity error interrupt (PERRINT) and the parity error status bit (PERR). Further clocking to the flip flop is disabled by the /Q output going low.

On each RAM cycle, the rank select lines MAP5, 6 and 5 upper processor address lines are latched by IC 7A. As soon as a parity error occurs this latching is disabled by the /Q output of the parity flip-flop so that the physical block and the processor 2k address space in which the error occurred is recorded.

The parity system status register occupies the same space as the mapsel ram: FC40 to FC4F. (The mapsel is write only, the status register is read only). The lower 3 bits of the latched address are compared with the module select lines MS0-2 from the DIP switch by IC 2F so that in a multi-card system parity registers on cards 0-7 are at FC40-7 respectively. A read from the status register enables the latch 7A and buffer 6A onto the data buss on the rising of /BRA and the parity error is cleared by a very short pulse (approx 20nS) on the rising of BRA at the termination of the read cycle. The flip flop is also cleared automatically by /SYRES.

The parity error generate signal PERGEN is used to artificially create a parity error for testing purposes. The I input of IC 7D is simply a ninth data input so that if it is 0 when a RAM location is written it must also be 0 when that location is read, otherwise an "error" will be generated. When testing the parity system, a location is written with the I input 0 and the read back just as the I input is switched to 1. PERGEN is the control for this and comes from the mapsel logic. Since the mapsel outputs are of a lookahead nature, the PERGEN signal is delayed by half a cycle by first latching on rising ADD2ø2 at IC 4D then clocking on rising /ADD2ø at flip flop IC 1E.

In the diagnostic tests the A state is initialised with PERGEN reset and the B state is initialised with PERGEN set. After writing a location in the A state, the processor switches to the B state at the instant of reading back the location.

4.3.5 MEMORY ARRAY

(Refer to Drawing Q256-05)

The dynamic memory array consists of four ranks of nine RAM ICs. Each IC is a 64k x 1 bit device, so each rank forms one byte plus parity bit. Which rank is accessed depends on which /RAS and /CAS lines are driven low by the decoding circuitry.

The RAM chips each have 8 address lines. Since 64k space requires 16 address bits the full address is multiplexed onto the 8 lines. The lower 8 bits ("Row" address) is latched into the RAM chips when /RAS goes low. After a period of address hold time the address multiplexor switches over and drives the upper 8 bits ("Column" address) into the RAMs. This is latched into the RAMs when /CAS goes low.

During a write cycle, data is latched into the RAMs on the falling edge of /CAS. In the case of a read cycle, data out becomes valid within 75nS of the falling edge of /CAS. The data lines are driven by the selected rank of RAMs while /CAS is low, and go tri-state at other times.

The state of the /W signal while /CAS is low determines whether the cycle is read or write.

Due to the capacitive input impedance of the MOS RAM ICs, the address and data input lines are driven through series resistors to limit the voltage undershoot.

4.4 QFC9 FLOPPY DISK CONTROLLER FUNCTIONAL DESCRIPTION

4.4.1 INTRODUCTION

The floppy interface card interfaces the bit parallel/serial buss of floppy disk drives to the C.M.I.'s interleaved parallel buss. The interface is a combination of device driver software, controlling disk data format and initialization of data transfer parameters, and the hardware which carries out the transfers without processor intervention.
Data is stored on the floppy disk itself on its magnetic coating, in concentric rings. In a standard, 8 inch floppy there are 77 such rings on each side called tracks. Tracks are divided into data blocks called sectors. Sectors in Fairlight disk formats are either 128 or 256 bytes per sector, depending on operating system being used. The smallest amount of data that can be read to or from a disk is one sector. Sectors on a disk may be randomly accessed.

Track 0 is outermost. The controller automatically restores to this track on power on, and on reaching track 0, signals the controller by a mechanical switch generated signal. All head movement is relative to this reset state.

Floppy drives transfer data serially. They also have parallel control lines to control drive number selection, head stepping direction, head load, disk write and disk write enable. The head of the drive must be lowered to the disk surface before a transfer may take place, this is operation referred to as "head load". Index pulses are generated by the drive so that the controller knows the location of the rotating disk. This pulse occurs once per revolution, so the start of tracks can be determined by the controller. Also, the controller generates pulses that are used to step the head in and out to position it over the required track.

The Floppy Disk Controller/Formatter uses the WD1791 controller LSI. It is software selectable to double density, double sided in addition to single density, single sided. It is designed to work with CPU #2's, transferring data to and from memory by DMA on Processor 2. The processor is not involved with transferring data to and from the disk. Once a data transfer is set up the processor may continue processing other tasks until the interrupt for "command complete" is issued by the controller.

4.4.1.1 Address Map
(refer to drawing QFC9-01)

The controller is accessed through two locations, in a memory map which enables access to peripherals. An address register is set up to point to the required controller register. All data is read or written through a single data register.

ADDRESS (HEX)	READ	WRITE
FCE0	data	data
FCE1	status register	address register

The 7 controller registers are ...

00 control register
02 DMA address (low byte)
04 DMA address (high byte)
06 byte count to read/write (low byte, inverted)
08 byte count to read/write (high byte, inverted)
0A command location to load device driver ROM into RAM
WD1791 L.S.I
0C cmd (write) status(read)
0D track r/w
0E sector r/w
0F data r/w

The definitions of the control register bits are ...

0 DS0 drive select address bit 0
1 DS1 drive select address bit 1
2 enable interrupt (active high)
3 enable DMA address incrementing (active low)
4 DMA transfer direction(1= to disk)
5 side select
6 retrig head load timer
7 DENS density selection

The definitions of the control status bits are ...

0 0 always zero
1 n/c
2 n/c
3 ready
4 two sided
5 disk change
6 interrupt
7 device driver loading (active low)

4.4.1.2 Commands

The extensive instruction set of the 1791 LSI can be obtained from the manufacturers data sheets for the 1791. This device handles all data conversions between the disk drive and the C.M.I. buss.

4.4.2 DATA BUFFERS, DMA ADDRESS COUNTER
(refer to drawing QFC9-02)

4.4.2.1 DMA address Counters

Sixteen bit counter chain C1 to C4 is used to provide the address for DMA transfers. The starting address for each disk transfer is established by writing the appropriate byte address to the address register then writing the address byte to the data register and then repeating for the other address byte. This causes the address to be preset into the DMA address counters by means of parallel-load strobe pulses STAL (low byte) and STAH (high byte). The incrementing of the DMA counters may be inhibited under software control, so that disk data may be dumped directly into the data portholes on channel cards.

4.4.2.2 DMA byte transfer counters
(refer to drawing QFC9-04)

Sixteen bit counter chain C5 to C8 is used to transfer the required number of bytes to or from disk. It must be initialized with the inverse of the number of bytes to be transfered. Any number may be specified up to a maximum of 65,535 bytes. Only those bytes specified will be transfered to memory on a disk read. This allows less than a sector to be read from disk, and saves the software overhead required to handle partial sector reads. The read takes place but the buss VMA signal goes inactive after the required number of bytes have been transfered, so disabling memory writes. The VMA disable signal is generated from the ripple carry out on this counter chain, by buffering /FINPS, (Finished Partial Sector).

When a transfer occurs, the DMAC (Direct Memory Access Claim) line is generated so that the memory card swaps maps, allowing data to be dumped into memory currently not mapped into the processor's address space. This signal is generated by the components around flip-flop A11.

4.4.2.3 Data Buffers
(refer to drawing QFC9-02)

Data is propagated from the system data bus via latch B6 which holds the data across the processor 1 phase. This latched data also becomes the DATA FROM BUS via buffer B5, to the floppy-controller LSI.

Data written to the system control register at 00 is latched by B7. This controls such functions as drive select and DMA direction.

4.4.3 ADDRESS DECODING, CONTROLLER LSI

4.4.3.1 Address Decoding

Address range $FCE0-$FCE1 is decoded by gates B1, E1, B2, E1 and latched by D2.

Address $FCE0 is used to enable the internal data buss to read and write to controller functions.
Address $FCE1 data is latched by B8 and with the access to FCE0 generates the internal chip selects and read/write strobes through C9.

Inverting buffer E5 and open collector drivers E6, E7 are used to interface the 1791 LSI controller to the disk drive cable. Incoming disk status signals are pulled up by 150 ohm terminating resistors.

4.4.3.2 Controller L.S.I.

The Interrupt Request from the LSI is gated with the Interrupt Enable to provide an open-collector interrupt signal for the system IRQ on buss pin 63A.

4.4.4 DMA LOGIC
(refer to drawing QFC9-03)

Data requests from the 1791 or Device Driver ROM loading are synchronised with Processor 2 Phase 2 using flip-flops C1 and A10. This sets up a DMA request to the processor (RDMA). DMA cycles are granted by ACK acknowledge signal.

Flip-flop A11 only allows a DMA cycle to occur every second Processor cycle (the floppy drive can not transfer at that rate but this is a system constraint on other DMA devices in the DMA daisy chain).

The DMA daisy chain is controled by /ENL and /EDL. Respectively these stand for, Enable Next Level and Enable DMA Level. When /EDL is active, a DMA request may be requested by the highest priority device. The /ENL signal informs the next device in the daisy chain that it may make a request if higher priority devices have not.
Depending on which function has been requested (Reset, Read, write) the required DTB (Data to Bus), and ATB (Address to Bus) signals are issued.

4.4.5 CONTROL REGISTER

The control register contains the drive number select bits, density selection, interrupt enable, increment DMA address enable, data transfer direction, side select and retrigger head load delay. This register is the latch at B7. The "retrig head" signal is used to reactivate the head load delay when the drive number has been changed, to allow for head bounce.

4.4.6 MASTER OSCILLATOR
(refer to drawing QFC9-05)

The LSIs used on the card require a master 16MHz clock. This is generated with the components around the 74S04 at F5. The FDC9229 generates the 2 Mhz clock for the 1791, by dividing this internally.

4.4.7 WRITE PRECOMPENSATION

In double density operation there may be a time shift applied to the data when it is being written to the inner disk tracks (>45). The amount of shift is determined by the LSI and the floppy disk suport device 9229. They produce a programmable delay of 1 to 3 clock cycles.

The amount, if any, is specified by the drive manufacturer. Links W4, W5, W6, W7 select the amount. The amount on inner and outer tracks can be independently set.

W5	W6	W7	Precompensation Value (in nS)
0	0	0	0
0	0	1	62.5
0	1	0	125
0	1	1	187.5
1	0	0	250
1	0	1	250
1	1	0	312.5
1	1	1	312.5

The precompensation value is normally set to 0 on inner and outer tracks. It is more important on inner tracks as the bit density on the disk is greater.

W4 selects minifloppy drives and also requires the board to be made with a 34 pin connector (or a special cable) and an 8MHz crystal.

4.4.8 DATA SEPARATOR

The serial data stream that comes from the drive is in a synchronous form. It has embedded the required data as well as clock pulses and syncronization "marker bytes".

The data separator is used to generate the data window from the FM (single density) or MFM (double density) encoded READ DATA supplied by the disk drive. The separator tracks, so that incoming data is always in the center of the data window. This data window informs the controller chip which bits in the data stream it is receiving are data and which are clock bits just used in the data encoding scheme.

The separator is a digital phase locked loop in the FDC9229 chip at E10. This chip does all the work of data separation.

4.4.9 DEVICE DRIVER ROM

The disk controller software may be placed in a 2K or 4K EPROM on the controller card. This EPROM is not in the processors directly addressable memory. It is executed by reading the software into RAM. This is done by DMA. The EPROM is copied into RAM as if reading a disk, except much faster.
The least significant DMA counter lines are used as addresses on the EPROM, so the EPROM can only be loaded into memory on 2k or 4k boundaries. The flip-flop C11 and gates in D11 and B11 produce a DMA write to memory request that is terminated after the byte counter times out.

4.5 Q219 LIGHTPEN/GRAPHICS SYSTEM

4.5.1 Introduction

The Q219 provides a graphics display and light pen input system. The 16 kilobytes VRAM is displayed as an array of 512 pixels (horizontal) by 256 lines (vertical). The lightpen can detect points within this array.

To increase graphics drawing speed, extensive use is made of special hardware functions which provide automatic address incrementing or decrementing along either or both axes and individual pixel writing at the current address.

Video RAM is arranged such that consecutive bits in each byte correspond to consecutive pixels in the horizontal line. With 512 pixels per line, 64 bytes of VRAM is required per line. Thus there are 64 bytes between a given pixel and the pixel vertically below it. The first byte in VRAM ($8000) appears at the top left corner of the screen.

Locations FCD0 to FCDC perform store and auto-increment/decrement functions as follows:

FCD0 just store at current position
FCD1 store and Inc Y
FCD2 store and DEC Y
FCD3 store as byte at current Pos
FCD4 store and Inc X
FCD5 store and Inx X,Inc Y
FCD6 store and Inx X,Dec Y
FCD7 store as byte,and Inc X
FCD8 store and Dec X
FCD9 store and Dec X,Inc Y
FCDA store and Dec X,Dec Y
FCDB store as byte and Dec X

FCC4 scroll latch (port A of PIA)

The pattern contained in the register stored at the particular location above may be varied to produce solids or various forms of dotted or dashed lines on the screen.

The current position is established by directly accessing the VRAM with a dummy read. Subsequent use of the special locations then work from that position on the screen in various directions.
The byte mode operations are provided for the writing of alpha-numeric data to the screen. The VRAM arrangement explained above means that the fastest way to place characters on the screen is to write a series of horizontal slice bit pattern to consecutive vertical locations. Note that byte mode operations only work in the vertical (x) direction. This direction requires the actual VRAM address to be advanced by 64 bytes. Byte mode in the (y) horizontal direction is achieved by storing directly into successive locations in VRAM.

All non-byte operations store one point on the screen. What is written to this point (0 or 1) depends on what is in the corresponding bit position of the accumulator used to store the data.

4.5.2 VIDEO TIMING LOGIC
(refer to drawing Q219-03)

All timing is derived from a crystal oscillator and a counter chain.

4.5.2.1 Dot clock Generation

The dot clock is constucted around inverter F2 and the 10.38Mhz crystal. The string of counters at F9 to F11 and E11 to E13 count the dotclock DOTCLK and with the aid of SROM produce all video related signals.

The screen area is organized as 84 bytes on the line and 304 lines in the frame. The actual displayed area is 64 bytes on the line and 256 lines. One byte time is 8 DOTCLK pulses or 770ns.
The SROM prom at E10 generates the horizontal sync pulse and an advanced blanking signal. The horizontal blank signal (HBLNK) is the 7th bit of the horizontal byte count. The horizontal sync pulse lasts for 6 byte times and starts at the 68'th byte position on the line. The vertical sync is generated by gates in E9, F6, D13 and E11. This pulse starts at line 272 and lasts 4 lines.

Gate in E11 generates the last line count (LASTL) at line count 304 and resets the entire counter chain to zero ,the first byte and first line of the displayed area.

4.5.2.2 Video FIFO and Shift Register
(refer to drawing Q219-02)

To compensate for the fact that bytes from memory need to be fetched at greater than 1 Mhz, (1.185Mhz i.e., 64 bytes need to be displayed in one active line time of 54us) for displaying, a FIFO register (first-in, first-out) is used. Data from the VRAM (MO1-MO8) is latched by octal latch B9. When FIFO input is not full, the IR signal causes a data request to be clocked through flip-flop E6, which in turn generates a shift in (SI) pulse to the FIFO. This occurs every microsecond until the FIFO input queue is full, as indicated by IR returning to a logic zero.

Data is shifted out of the FIFO to the parallel-in serial-out shift register F7 by SO (Shift Out) pulses coming from the bit counter chain and SROM. They start one byte time before the line is unblanked and stop one byte time before the line is blanked. One byte is transfered from the FIFO to the shift register every eight picture bits. The picture information is shifted out by clock pulses from the bit rate oscillator (DOTCLK).

4.5.2.3 Video Output

Video data from the shift register is EXCLUSIVE-ORed with the INVERT signal from the PIA at D, E4. With a logic 1 at this pin the picture appears normally with set bits in the VRAM displayed as bright pixels. If a logic zero is applied, the picture is inverted (negative) so that ones in VRAM appear as black pixels on a BRIGHT background.

The output from this exclusive-or gate passes through another, and is gated with the lightpen cursor signal INV.

The output from this gate is serrated at the bit rate by ANDING with DTCLK* at F6. This is done to avoid horizontally adjacent dots merging to appear brighter than vertically adjacent ones.

The serrated video is then blanked by gating with the combined horizontal and vertical blanking signals by F5 and F6. This removes unwanted (inactive) display time from the display. Sync is added to the video by combining the horizontal and vertical sync pulses in F5 and resistor network R10 and R9. This is buffered for low impedence driving by transistor Q1. The composite video signal is available at both 10-way connectors at the front of the card.

4.5.3 SELECT LOGIC AND DATA CONTROL
(refer to drawing Q219-01)

4.5.3.1 Address Decoding

The Lightpen/Graphics Card occupies two areas of memory space. The VRAM uses 16K bytes from $8000 to $BFFF. The various auto-incrementing portholes use 15 bytes $FCD0 to $FCDB ,and the PIA and TIMER use FCC4 to FCDF. Addresses in the FCCX to FCDX range are decoded by half of NAND gate A2. VRAM addresses in the $8000 range are decoded by the other half of A2. These are enabled by AND gate D3, and gating together VMA, ENBL and ADD1/ADD1* which makes VRAM processor unique.

Either processor can always access the PIA and Timer on the card, if peripherals are mapped in. See Q256 ram card for explanation of mapping and peripheral control.

The select signals from this gating are latched, along with the five least significant address bits and the read/write line, by octal latch B3.

The 16 auto-increment functions are decoded from the four least significant address bits by dual one-of-four selector C3.

4.5.3.2 Data Buffers

Octal buss Buffers B8 and transceiver B7 interface the card to the system data buss. Buffer enables and control signals are generated via the buss control prom BROM. The buss control prom is used to simplify the complicated enabling of the buffers as they must be enabled at several different addresses and modes of operation of VRAM access.

4.5.4 VRAM ADDRESSING LOGIC

4.5.4.1 Addressing counters

The address being accessed within VRAM is determined by the state counter chain B4, B5, B6, A4 and A5. These are up-down counters which provide the auto-increment (and auto-decrement) functions. The starting address for any operation is established by any access to the VRAM. This is achieved by the counters being parallel-loaded by ADLD (address load) that occurs when a read is made between $8000 and $BFFF, in a map that contains the graphics ram.

Horizontal incrementing or decrementing is achieved by pulses YUP and YDN clocking the low-order 9 bits of the counter chain. The 3 lowest bits are used to select the bit within the byte. Vertical incrementing or decrementing is acheived by clocking the highest 8 bits of the counter.

4.5.4.2 Bit Selection

The 16K byte of VRAM is bit addressable, that is each row of chips can be individually written to.

For Byte mode operations, the BYEN signal is TRUE, and when a memory write is performed, the WROM A6 (write control prom) activates all the write lines causing the whole byte to be written irrespective of the current bit position within the byte.

For Bit mode operations, only the bit determined by the contents of A5 will have its W* signal activated .

4.5.4.3 Vertical Scrolling
(refer to Q219-05)

Counter chain D5, D6 and D8 generate the 14 bit address for the VRAM display operation. Each time a byte is fetched into the FIFO an INCA (Increment Address) pulse clocks the counters on to the next byte. The starting line is preset into counters D5 and D6 during line 304 by signal SYNR* produced by F13 and SROM. (This also resets the FIFO and allows it to be filled with the data for the first displayed line before the line is unblanked. This prefilling is necessary as the FIFO is emptied faster than it can be filled, during the active part of a line.)
The starting line number comes from port A of the PIA. Using this side of the PIA allows the starting line to be read from the latch directly via software.

4.5.5 VRAM Address Multiplexing
(refer to drawing Q219-06)

Quad data multiplexers C6 to C8 multiplex the addresses of the VRAM between processor accesses (addresses from counter chain B4, B5, A4, B6 and A5) and video display addresses (counter chain D5,D6 and D8).

Switching is done by BADD2X signal which is derived from phase two of the processor to which access has been enabled.

4.5.6 LIGHT PEN
(refer to Q219-04)

4.5.6.1 Introduction

The Light Pen is used to generate co-ordinate data from Hit and Touch signals coming from the light pen. These come onto the card via the lower 10-way connector.

It is achieved by latching the bit, byte and line counters in the video chain when a touch and hit occur from the lightpen. The co-ordinates are then available to be read from the card by the processor.

The light pen is activated by touching the insulated end of the pen, which generates a Touch signal. The interface can be configured to generate an interrupt when the touch signal is activated.
The card can also be configured so that the Hit signal causes the picture information to be inverted, which generates a "cursor" on the display at the position the pen is currently "seeing".

The Hit signal from the pen is de-glitched by the interface so that random noise due to external interference will not cause false triggering.

4.5.7 Co-ordinate counters, Deglitcher, PIA, Timer

4.5.7.1 Hit Deglitcher

Deglitching operates by ensuring that light pen hits are repeated a minimum number of times on successive display lines.

Counter E2 is normally in its terminal count state, counting being inhibited by RCO being high, which forces P low. A Lightpen Hit pulse arriving at gate D1 will RESET the counter via its clear input, CLR. This will clock the bit and byte latches via LPBITS through gate D3 and flip-flop E6 after being synchronized with the valid bit clock.
The counter then procedes to count line blanking pulses, HBLNK. Once two lines has been counted, the next Hit pulse will cause a logic 1 to be clocked by flip-flop D2. On the next byte parallel load , PLOAD*, this is propagated to the second flip-flop D2, generating a LPSTB pulse to clock the line latch. If no Hit occurs during the third line after the first hit, the count continues to its terminal state (16) without a LPSTB being generated.

4.5.7.2 Hit and Touch Receivers

The Hit and Touch lines from the lightpen are TTL compatible signals, active low. They are terminated at the receiving end by resistor networks R1, R2, R6 and R7. Depending on the state of the mode bit TFH the Touch signal may be ANDed with the Hit signal to generate a valid Hit pulse.

Note that gating is arranged to disable the cursor when the Touch is asserted. This is to ensure that the pen has something to "see" when activated.

The lightpen has its own supply regulator to reduce noise sensitivity. This is provided by a 78L05 device.

4.5.7.3 Co-ordinate Latches
(refer to drawing Q219-03)

The current bit within the byte is counted by F9. The byte on the line is counted by F10 and F11. Their contents are latched by D9 and D10 when a valid hit occurs by LPBITS, (deglitched Hit).
The least significant bit within the byte is available at bit 7 of port B of the PIA. The rest are read by the processor when LPL1* is active.

The line in the frame is counted by E13 and E12 and latched at D12 by LPSTB. This octal latch is read when LPL2* is active.

4.5.7.4 Control PIA
(refer to Q219-01)

Peripheral Interface Adapter D, E4 provides read/write ports for a variety of different functions. The side A is configured as outputs and are used to control the screen scrolling. The B side is input and output and controls screen invertion, processor access to VRAM, TFH (touch for hit) mode, lightpen cursor enable , lightpen touch status and the least significant bit within the byte counter.

The PIA is also used to generate interrupts. Two separate interrupt outputs are possible, one for Touch and one for Hit. These are generated by the PIA CA1 and CB1 outputs respectively.

4.5.7.5 Timer

An M6840 Timer is provided for general system use. This device contains three independent 16-bit counters which can be configured under software control to count external events or internal clock pulses. Counter 1 is clocked by HBLNK to count lines, counter 2 is clocked by VSYNC to count frames, and timer 3 is clocked by a 1MHz system timing signal to count microseconds.

For full operational specifications of the 6840 refer to manufactures data sheets.

4.5.8 VIDEO MEMORY VRAM
(refer to drawing Q219-06)

The 16 kilobytes of VRAM is provided by eight 4116 16,384 bit dynamic MOS devices. The timing required for these devices is preset in the system timing signals. These signals are buffered and fed directly to the rams as BRAS* , BCAS* and BCA*. Memory refresh is done in the continuous access for screen refresh.
Whenever the VRAM is directly accessed, the decoding at A2, 7D, 7E generates RENB, (active low). This disables the memory card in the 16K block used by VRAM and saves duplicating maps in the Q256 ram card.

4.6 CMI02 MASTER CARD - FUNCTIONAL DESCRIPTION

4.6.0 Introduction

The CMI02 Master Card performs a variety of functions including control of the eight channel cards, analog to digital conversion for sound sampling, and timer functions for sequencer and Music Composition Language. It occupies the first slot from the left in the card cage of the C.M.I. Mainframe.

This card occupies 64 bytes of processor address space. It can be accessed by either processor. The address map is as follows:

ADDRESS (Hex)	FUNCTION
E000-E01F	CHANNEL CARD REGISTERS
E020	CHANNEL MASK DATA REGISTER (P.I.A)
E021	CHANNEL MASK CONTROL REGISTER (P.I.A.)
E022	MASTER TUNING DATA REGISTER (P.I.A.)
E023	MASTER TUNING CONTROL REGISTER (P.I.A.)
E024	A.D.C. DATA HIGH BYTE
E025	A.D.C. DATA LOW BYTE
E026	HALT PROCESSOR 2
E027	UN-HALT PROCESSOR 2
E028	LEVEL CONTROL DATA REGISTER (P.I.A.)
E029	LEVEL CONTROL CONTROL REGISTER (P.I.A.)
E02A	FILTER CONTROL DATA REGISTER (P.I.A.)
E02B	FILTER CONTROL CONTROL REGISTER (P.I.A.)
E030	P.I.C.U. ENABLE CURRENT STATUS
E031	INTERRUPT PROCESSOR 1
E032	CLEAR PROCESSOR 1 INTERRUPT
E033	INTERRUPT PROCESSOR 2
E034	CLEAR PROCESSOR 2 INTERRUPT
E038-E03F	TIMER REGISTERS (6840)

4.6.1 ADDRESS DECODING, CHANNEL SELECTION, MASTER TUNING REGISTER (Refer to Drawing CMI02-01)

4.6.1.1 Address Decoding

Addresses in the range E000-E03F are decoded by NAND gate A1. Once addressed, the SEL (Select) signal is latched by D-type flip-flop C1. Channel card addresses in the range E000-E01F are decoded by NOR gate C2 to produce $\overline{\text{CHSEL}}$ (Channel Select).

4.6.1.2 Channel Selection

All eight channels occupy the same address space and channel selection is achieved by establishing a mask of desired channels in the B side of P.I.A. BC9 (Channel Mask). NAND gates A10 and B10 enable one or more channels when a WRITE to a channel card address is performed. It is not possible to read from more than one channel at a time without buss contention, so circuitry is provided to protect against crashes which may result from a software bug which causes inadvertant reading from multiple channels. ROM A9 is programmed to generate a logic zero if more than one bit is set in the channel mask. If a READ is attempted under these conditions, the $\overline{\text{CHSEL}}$ is inhibited.

4.6 CMI02 MASTER CARD - FUNCTIONAL DESCRIPTION

4.6.1.3 Master Tuning Register

The B side of P.I.A. BC9 is configured as outputs, the data written to it being used as Master Tuning control (MT0-MT7) by the Master Pitch generator (Sheet 2).

4.6.2 INTERRUPT CONTROL, MASTER OSCILLATOR, MEMORY CONTROL
(Refer to Drawing CMI02-02)

4.6.2.1 Interrupt Control

The eight channel cards generate Processor 1 interrupts which occupy the eight interrupt levels supported by the C.P.U. Control Card Q133. To support the remaining interrupts, a second P.I.C.U. (Programmable Interrupt Control Unit) is provided on the Master Card. It is cascaded with the one on the Q133 card.

The P.I.C.U. C8 normally provides the three highest priority interrupts to Processor 1. These are, IRQSYN from the keyboard A.C.I.A., $\overline{\text{TIMINT}}$ from the 6840 timer, and interprocessor interrupts. The current interrupt priority level is written to the P.I.C.U. by a WRITE to E030 (hex). If an interrupt of a higher priority arrives, the $\overline{\text{INT}}$ output of the P.I.C.U. will be asserted (low), setting the flip-flop formed by gates A10, B2 and generating a Processor 1 Interrupt Request (IRQ1). The level of the interrupt is presented to the Interrupt Address Buss IA01-IA21. This address is used as bits 1 to 4 of the memory address when fetching the interrupt vector.

The interrupt latch is cleared when a new interrupt status is written to the P.I.C.U.

4.6.2.2 Master Oscillator

Transistor Q1 and crystal Y1 form a 34.29 MHz oscillator from which the channel card pitch reference is derived. Flip-flop E10 divides the output of the oscillator by 2 to provide a symmetrical square wave at 17 MHz. This is fed to rate multipliers C10 and D10, which give a small range of frequency control, as determined by the data from the Master Pitch register (sheet 1). The output of these rate multipliers is fed to all channel cards via buffer A7.

4.6.2.3 Memory Control

Counters E8 and D8 are clocked by the 17 MHz signal from the crystal oscillator and their output addresses timing ROM B8. This ROM generates the timing signals required by the Waveform RAM on the Channel Cards. They are SREF (Refresh), $\overline{\text{SRA}}$ (Row Address), $\overline{\text{SRAS}}$ (Row Address Strobe), $\overline{\text{SCAS}}$ (Column Address Strobe). The outputs of the ROM are latched by quad flip-flop B7 and buffered onto the buss by A7.

4.6.3 Analog to Digital Converter
(Refer to Drawing CMI02-03)

The Analog to Digital converter is an AD571 (D7), of 10-bit accuracy. The sample rate is determined by the frequency set up by the Channel Card in the Channel 1 position of the Mainframe. This clock arrives at the Master Card edge connector pin 44. ADM (A-D Mode) is normally low, enabling the ADCLK (A-D Clock) through to one-shot D2. This one-shot generates the 2 uS pulse required by the AD571 to start a conversion cycle.

When waiting for a conversion cycle, Processor 1 halts itself by accessing E026 (hex). This generates a $\overline{JAM}$ strobe, CLEARing flip-flop D3 which causes $\overline{HLT}$ (Halt) to go low.

When the conversion is complete (approximately 30 microseconds later) the $\overline{DR}$ (Data Ready) output of the AD571 goes low, forcing the output of NOR gate D9 High, clocking the data latches C5 and C7, which capture the data ready for reading by the processor. At the same time as the conversion is completed, flip-flop D3 is clocked, setting it. The $\overline{Q}$ output is forced LOW again, removing the HALT condition from Processor 1 and allowing it to run again and read the A-D data. If Processor 1 is held halted for more than 100 mS, one-shot D2 times out, allowing it to run again. This is to protect against system hang-up in the event of an A-D failure.

The audio signal arrives at the Master Card at pin 9 of the 10-way ribbon cable plugged into the front of the card. Sample-and-hold E9 is gated by the $\overline{DR}$ (Data Ready) signal from the DAC to ensure that the signal input to the DAC remains constant while a conversion is in progress.

4.6.4 A-D FILTER SYSTEM
(Refer to Drawing CMI02-04)

Low-pass and high-pass filters are provided for limiting the bandwidth of the signal being fed to the Analog to Digital converter. The cutoff points of each are individually controllable.

Signal arriving at the Master Card at pin 1 of the 10-way ribbon connector is attenuated by MDAC E4. The attenuation is controlled by the data written to the A side of P.I.A. DE5. Op-amp F3 in combination with CMOS switches E1, F1, F5 form the low-pass filter. The cutoff frequency is determined by the resistors selected by the switches, which are addressed by the low four bits of the B side of P.I.A. DE5. Output of the low-pass filter is available for monitoring at test point TP9.

Op-amp E7 together with switches F7, F8 and F10 form the high-pass filter. The cutoff point of this filter is controlled by the high four bits of the B side of P.I.A. DE5.

The plus and minus supplies for the CMOS switches are provided by zener diodes ZD1 and ZD2. 5.6 volt zeners are used so that the supplies to the switches will exceed 5 volts to prevent distortion of the signal which can be up to 10 volts peak-to-peak.

4.7 CMI01-A CHANNEL CARD - FUNCTIONAL DESCRIPTION

4.7.1 INTRODUCTION

The Channel Cards are the audio generation and manipulation system of the C.M.I.

Up to eight channel cards may be installed. All eight cards are identical and interchangeable. Their assignment (1 to 8) is a function of which slot they are plugged into in the C.M.I. Card Cage.

Each Channel Card contains 16K bytes of waveform RAM in which sounds are stored. Circuitry is provided to clock out this memory to a digital to analog converter, also located on the channel card.

The speed at which the memory is clocked out, and hence the pitch of note produced, is controlled by a 12 bit number written to the pitch register on the card.

A tracking filter follows the DAC. This automatically follows the frequncy of the channel, filtering out unwanted noise at a certain number of octaves above the fundamental frequency. The ratio of the filter cutoff to the pitch being played is controllable by writing to the filter control latch (used by the FILTER control on Page 7 of the C.M.I. system software.)

Each channel card occupies 32 bytes of memory space from E000 to E01F. The 16 kilobytes of waveform RAM are accessed by a single "porthole" at E000. Auto-incrementing hardware causes data to be read or written to each byte sequentially as repeated accesses are made to this location. The starting byte number is established by writing to a special register.

As all eight channels live at the same address, a mechanism for selecting which channel(s) are accessed is provided. This is controlled by the Channel Mask Register, located on the Master Card CMI02.

Audio output is taken from the 10-way ribbon connector on the front of each channel card. This is in the form of a balanced signal. The signal is also available at the test points at the front of each card. Refer to the Diagnostic Software section of this manual for full details.

Power for the analog cicuitry (+ and - 15 volts) is fed to the Channel Cards via the same ribbon cable.

Details of Channel Card operation are proprietary information which is not available outside the Fairlight factory in Sydney.

4.8 CMI04 AUDIO MODULE - FUNCTIONAL DESCRIPTION

4.8.1 INTRODUCTION

The Audio Module interfaces the audio input/output connectors on the rear panel of the C.M.I. mainframe with the appropriate internal circuitry.

Functions include buffering of audio outputs from the channel cards, generation of a mixed line output, provision of a monitor amplifier for driving a monitor speaker or headphones, processing of sync input and output signals, and supply of power to the channel cards.

4.8.2 MIXER, LINE DRIVERS
(Refer to Drawing CMI04-01)

4.8.2.1 Mixer

Audio from the channel cards arrives at the Audio Module by means of a fifty-way ribbon cable. This cable is split down to eight separate groups which plug into the channel cards.

The signal is balanced, to minimise noise pollution. Each channel is received by a differential amplifier which removes common-mode noise. The channels are then mixed down by eight resistors feeding a virtual-earth summing amplifier IC5 to form the Monitor output.

4.8.2.2 Line Drivers

All eight channels, plus the monitor output, are buffered before being fed to the appropriate output via a 330 ohm isolation resistor. An op-amp inverter provides an anti-phase signal for each balanced output.

4.8.3 MONITOR AMP, INPUT AMPS, SYNC IN/OUT
(Refer to drawing CMI04-02)

4.8.3.1 Monitor Amplifier

Signal from the output of the mixer (sheet 1) is fed via the Monitor potentiometer (on the rear panel of the Mainframe) to the monitor amplifier. It arrives at the speed of light at pin 30 of the edge connector, from where it is amplified by audio amplifier IC12. Power boost for this amplifier is provided by transistors Q1 and Q2.

Pulses from the Click Monitor potentiometer are mixed into the Monitor amplifier by resistor R3 and capacitor C14.

4.8.3.2 Input Amplifiers

The Microphone Input is amplified by op-amp IC7. The noise of this stage is reduced by using transistors Q3 and Q4 as the gain elements of the op-amp. Transistors Q5 and Q6 form a current source for the differential input stage.

Line input is buffered and un-balanced by differential amplifier IC8.

Output from the Mic pre-amp or Line input amplifier is routed to the Master Card as determined by the setting of the MIC/LINE switch on the rear panel of the C.M.I. Mainframe.

After filtering on the Master Card, the audio signal is returned to the Audio Module via pin 8 of the ribbon cable connector SO2. It is buffered by op-amp IC9 and fed to the FILTER OUT connector on the rear panel, as well as the INT/EXT ADC selector switch.

4.8.3.3 Sync In/Out

The Click signal from the Master Card is a symmetrical square wave. It arrives at pin 7 of SO2. It is filtered by IC10 and associated components, resulting in a pulse waveform which is fed to the Click Output on the rear panel, and also the Click potentiometer on the rear panel.

Sync input to the Mainframe arrives at pin 72 of the edge connector SO3. IC15 is configured as a Schmitt Trigger which squares up the incoming waveform and rejects noise by virtue of its hysteresis. Zener diodes ZD2 and ZD3 clip the output of the op-amp to limit the excursion to about + and - 4.5 volts. Resistor R104 and zener diode ZD1 further limit the excursions of this signal to approximately +4 and -.7 volts, suitable for feeding to the Master Card via ribbon cable connector SO2 pin 6.

4.8.4 POWER SUPPLY

Raw D.C. supplies of approximately + and - 20 volts arrive at the card via connector PL4. When power is first applied, relay RLA is open and no power is fed to the regulator ICs. As capacitor C50 charges, the current through transistor Q8 increases until the voltage accross resistor R108 excedes .7 volts. Transistor Q7 then switches on, pulling the base of Q8 up to the supply, which causes relay RLA to close.

Power is then applied via RLA1 and RLA2 to the regulator ICs IC13 and IC14.

The purpose of this delay is to mute the audio outputs until the processor system has started up and initialised the channel card hardware.

4.9 QPSA D.C. POWER SUPPLY ASSEMBLY - FUNCTIONAL DESCRIPTION

4.9.1 INTRODUCTION

The D.C. Power supply provides regulated power for all the circuit boards within the C.M.I. card cage, the floppy-disk drives, the music keyboard and alphanumeric keyboard.

Power for the analog (audio) circuitry is provided by regulators located on the Audio Card CMI04, mounted inside the rear panel of the mainframe. This provides plus and minus 15 volts for the Channel cards, Master Card and Audio card. The remainder of the digital electronics is supplied by regulators mounted on the rear of the card cage. This provides +5, +12 and -12 for the cards within the card cage, and +24 and +5 for the floppy disk drives.

4.9.2 UNREGULATED SUPPLIES
(Refer to drawing MC001-01)

The Unregulated Supply assembly is constructed as an integral part of the C.M.I. Card Cage assembly. It comprises a transformer, rectifiers and filter capacitors. A schematic diagram of the assembly is shown on drawing MC001-01.

Transformer T1 is supplied with A.C. mains via a fuse, mains switch, line filter and voltage selector. A 10 V.A.C. winding supplies bridge rectifier DB1 to give 10 volts raw D.C. across C1 at its full load of 20 Amps maximum. Its fuse is located on the regulator assembly P.C.Board.

A 28 V.A.C. winding feeding bridge rectifier DB2 provides +40 volts, smoothed by C2 and fused by F2. A centre-tapped 32 V.A.C. winding in conjunction with DB3 supplies plus and minus 20 volts to smoothing capacitors C3 and C4 and fuses F3 and F4 respectively.

A 33 V.A.C. winding feeding bridge rectifier DB4 and capacitors C5 and C6 provide the plus and minus 20 volts D.C. to the regulator on the Audio Card CMI04.

4.9.3 REGULATOR 5 VOLT 18 AMP
(Refer to drawing QPSA-01)

This regulator is part of the regulator assembly located at the rear of the C.M.I. Card Cage.

IC1 is the regulating element of the circuit. Transistor Q2 senses the current drawn by IC1, driving parellel transistors Q3 to Q6. Equal current sharing is ensured by emitter resistors R7-R10.

Current limiting is provided by germanium transistor Q1, which uses the drop across sensing resistor R1 as a current sense. Short circuit current is limited to approximately 20 Amps, regulation falling off above about 18 Amps.

Over-voltage crowbar protection is provided by SCR1. If the output of the 5 volt regulator rises above 6 volts zener diode ZD1 conducts, switching on the S.C.R. This protects components using the 5 Volts supply in the event of regulator malfunction or an inter-supply short-circuit. If the crowbar circuit does switch on, 15 Amp fuse FS1 will blow.

4.9.4 ± 12 VOLT, 24 VOLT SUPPLIES
(Refer to drawing QPSA-02)

The plus and minus 12 volt supplies are simply regulated by integrated circuits IC3 and IC4 respectively. The +12 volt supply is current-limited to about two amps by the regulator I.C. IC3. The -12 volt supply is current limited to about 1 amp by regulator I.C. IC4.

The 24 volt supply is regulated by integrated circuit IC2. Transistor Q7 boosts the available current to about 3 Amps. Zener Diode ZD1 provides a voltage drop to protect the regulator I.C. from excessive input voltage.

4.10 Q137 FRONT PANEL CONTROL - FUNCTIONAL DESCRIPTION

4.10.1 INTRODUCTION

This board contains the controls used for system debugging and reset. It contains 2 push button switches, one for RESET and one for NMI. The remaining toggle switches activate halting of each CPU and enabling of the appropriate labelled function.

4.10.1.1 Operation

The 555 timer is wired as a low frequency oscillator and is used to flash the LED associated with each "armed" switch.
The CMOS NAND gate is used for debouncing of the pushbutton switches.
Each switch has two poles. One activates the function while the other is used to connect the oscillator to the LED.

For a function to operate the associated LED must flash.

4.10.2 COMMUNICATIONS PORT

The front pannel also carries a 10-way flat cable connector, P2, that contains serial communications lines from the Q133 card.

4.11 Q077 HARD DISK CONTROLLER DMA INTERFACE - FUNCTIONAL DESCRIPTION

4.11.1 INTRODUCTION

The hard Disk Subsystem is in three parts. The D.M.A. interface that plugs into the C.M.I. buss, the Western Digital Controller that connects to this and the Winchester drive itself.
The Q077 card interfaces the Western Digital WD1002-05 Winchester/Floppy Controller, to the C.M.I. buss. This parallel interface allows transfers via D.M.A. for maximum speed. The cable connecting the Q077 to the controller contains an 8 bit bi-directional data buss, 3 address lines, read and write strobes and D.M.A. handshaking lines.

4.11.2 ADDRESS MAP
(refer to drawing Q077-01)

The controller is accessed through two locations, in a memory map which enables access to peripherals. An address register is set up to point to the required controller register. All data is read or written through a single data register.

The following 3 registers are directly accessable in the C.M.I's address space by processor 2.

DATA REGISTER AT	FC5A	(HDDR)
ADDRESS REGISTER AT	FC5B (write only)	(HDAD)
STATUS REGISTER AT	FC5B (read only)	(HDST)

The following registers are accessed by writing the required registers address to the address register, HDAD, and then accessing the data register. The first 8 locations are in the Western Digital controller and the rest are in the Q077.

$0	Data register	WD1002-05 register
$1	Error register	"
$2	Sector Count	"
$3	Sector Number	"
$4	Cylinder low	"
$5	Cylinder high	"
$6	Size/Drive/Head	"
$7	Status Register	"
$10	DMA address low	
$11	DMA address high	
$12	control register	
$13	lower partial sector byte count (inverted)	
$33	upper partial sector byte count (inverted)	
$53	partial sector fill character	
$73	starts DMA of rom into ram (access to start)	

STATUS REGISTER bit definitions (HDST)

0	0	zero (used to identify board present)
1	n/c	
2	n/c	
3	n/c	
4	CDCPT	command complete
5	n/c	
6	INTERUPT	the OR of IRQs generated
7	DTRQST/	controller data request

CONTROL REGISTER bit definitions (register 12)

0	REST/	disables DMA logic (active low)
1		transparent command complete interrupt enable
2		command complete interrupt enable
3		increment DMA address enable (0=enable)
4	n/c	
5	n/c	
6	DMA direction (1=DMA write)	
7	GREST/	master gypsy reset (active low)

4.11.3 COMMANDS

The extensive instruction set of the controller can be obtained from the manufacturers data sheets for the WD1002-05 Intelligent Controller. This device handles all data conversions between the winchester drive and the C.M.I. buss.

4.11.4 DMA ADDRESS COUNTERS
(refer to drawing Q077-04)

Sixteen bit counter chain D1 to D4 is used to provide the address for DMA transfers. The starting address for each disk transfer is established by writing the appropriate byte address to the address register then writing the address byte to the data register and then repeating for the other address byte. This causes the address to be preset into the DMA address counters by means of parallel-load strobe pulses STAL (low byte) and STAH (high byte). The incrementing of the DMA counters may be inhibited under software control, so that disk data may be dumped directly into the data portholes on channel cards (CMI-01-A).

4.11.5 DMA BYTE TRANSFER COUNTERS
(refer to drawing Q077-04)

Sixteen bit counter chain E5 to E8 is used to transfer the required number of bytes to or from disk. It must be initialized with the inverse of the number of bytes to be transfered, (programmed as well as DMA transfers). Any number may be specified up to a maximum of 65,535 bytes. Only those bytes specified will be tranfered to memory on a disk read. This allows less than a sector to be read from disk, and saves the software overhead required to handle partial sector reads. The read takes place but the buss VMA signal goes inactive after the required number of bytes have been transfered, so disabling memory writes. The VMA disable signal is generated from the ripple carry out on this counter chain, by buffering FINPS, (Finished Partial Sector). When a transfer occurs, the DMAC (Direct Memory Access Claim) line is generated so that the memory card swaps maps, allowing data to be dumped into memory currently not mapped into the processor's address space. This signal is generated by the components around flip-flop C10.

4.11.6 DATA BUFFERS
(refer to drawing Q077-02)

Data is propagated from the system data bus via latch B4 which hold the data across the processor 1 phase. This latched data also becomes the DATA FROM BUS via buffer B5, to the controller card.

Data written to the system control register is latched by C4. This controls such functions as controller reset.

4.11.7 ADDRESS DECODING, CONTROLLER

Address range $FC5A-$FC5B is decoded by gates B1, C1, F4, F1 and latched by F3.

Address $FC5A is used to enable the internal data buss to read and write to controller functions. The least significant 3 address bits written to latch B7 are propogated down the cable to the controller card
Address $FC5B data is latched by B7 and with the access to FCE0 generates the internal chip selects and read/write strobes through E5. The least significant 3 address bits written to latch B7 are propogated down the cable to the controller card.

Buffers C9, C8, are used to interface the Q077 to the controller 50-way cable. All cable signals are terminated in 220ohm/330ohm terminating networks.

The Interrupt Request from the controller is gated with the Interrupt Enable to provide an open-collector interrupt signal for the system IRQ on buss pin 63A.

4.11.8 DMA LOGIC
(refer to drawing Q077-03)

Data requests from the controller or Device Driver rom loading are synchronised with Processor 2 Phase 2 using flip-flops B9 and A10. This sets up a DMA request to the processor (RDMA).
DMA cycles are granted by ACK acknowledge signal.
Flip-flop B9 only allows a DMA cycle to occur every second Processor cycle (the floppy drive can not transfer at that rate but this is a system constraint on other DMA devices in the DMA daisy chain).
The DMA daisy chain is controlled by $\overline{ENL}$ and $\overline{EDL}$. Respectively these stand for, Enable Next Level and Enable Dma Level. When $\overline{EDL}$ is active, a DMA request may be requested by the highest priority device. The $\overline{ENL}$ signal informs the next device in the daisy chain that it may make a request if higher priority devices have not.
Depending on which function has been requested (Reset, Read, write) the required DTB (Data to Bus), and ATB (Address to Bus) signals are issued.

During a D.M.A. cycle, the address to the controller board is set to $0 by the AND gates at B10. This selects the FIFO in the controller card which is the origin (for a read) or destination (for a write) for the data in the transfer.

4.11.9 CONTROL REGISTER

The control register contains the controller reset, interrupt enable and increment DMA address enable. This register is the latch at C4.

4.11.10 DEVICE DRIVER ROM
(refer to drawing Q077-05)

The disk controller software may be placed in a 2K or 4K EPROM on the controller card. This EPROM is not in the processors directly addressable memory. It is executed by reading the software into RAM. This is done by DMA. The EPROM is copied into RAM as if reading a disk, except much faster.
The least significant DMA counter lines are used as addresses on the EPROM, so the EPROM can only be loaded into memory on 2k or 4k boundaries. The flip-flop C10 and gates in D9 and B8 produce a DMA write to memory request that is terminated after the byte counter times out.

4.12 CMI28 GENERAL INTERFACE - FUNCTIONAL DESCRIPTION

4.12.1 Introduction

The General Interface Card (CMI28) is an optional card for the Fairlight CMI Series IIX. Please note that for use in the Series IIX machines a **CMI-25 rev-3** motherboard is required (or equivalently modified old motherboard). The General Interface Card is designed to handle reading and generating of SMPTE code and to control four MIDI ports as well as controlling the CLICK feature. Because its main purpose is for SMPTE and MIDI it is often referred to as the **SMIDI Card.** In the Series IIX machines the card is plugged into the second slot on the left between the Master Card and a Channel Card.

The SMIDI card is connected to the General Interface Support Card, the CMI-29 via a 26-way cable. This card is housed in a box bolted to the back of the CMI. This support unit has the opto-couplers, and open collector buffers for receiving and transmitting MIDI as well as the analog circuitry for reading and generating SMPTE code to tape.

The SMIDI card in general is a microcomputer system with a Motorola 68000 microprocessor, either 8k or 16k words of ROM and either 8k or 32k words of static RAM. It is possible to extend this to 64k words. It has a DMA interface to the CMI with the capability of DMAing to either P1 or P2. In Series IIX machines the DMA is only on P1. The card has 4 ACIA's (68B50) for the 4 MIDI ports, two 68B40 Programmable Timer Modules as well as associated circuitry for reading and generating SMPTE code and click/sync in and multiple syncs out.

4.12.2 Memory Configuration

There are four 28-pin sockets for ROM and static RAM. The minimum configuration is 8k words of ROM (2 x 2764) and 8k words of static RAM (2 x 6264). The ROM can be configured for 16k words by breaking the link (LK1) between pin 27 of the ROM and +5v and join the link LK1 to A15 from the processor and plugging in the appropriate two 27128's. Similarly the RAM can be arranged to accommodate 32k static RAM chips (e.g., MK4856 pseudo-statics) by breaking the links LK2 and LK3 to +5v and connecting A14 and A15 to pins 26 and 1 of the RAM chips (via LK3 and LK2), respectively. Further, there is an option for 64k words of RAM; by soldering two 32k RAM chips on top of each other except for pin-20, the chip select, which should be connected to the pads provided from the select circuitry, the AND gates (D12). All these memory expansions will depend on the availability of these chips.

NOTE; when plugging in the ROM's, they should be labelled 'odd' and 'even'. The even one should be plugged into E5,6 (near the 68000) and the odd one into E8 (between the RAM chips).
Memory addressing: ROM starts at $000000 and RAM starts at $080000.

4.12 CMI28 GENERAL INTERFACE - FUNCTIONAL DESCRIPTION (continued)

4.12.3 68000/6809 DMA Bus Interface

(Refer to Drawing CMI-28 rev 2 page 4.)

Communication between the 68000 processor and the 6809 CPU is achieved by DMA (Direct Memory Access) on the system bus. The 68000 waits until no higher priority device is occupying the bus and then either 6809 (P1 or P2) is temporarily hung while the 68000 executes a normal bus cycle writing to or reading from memory or a peripheral on the bus. In this manner the entire 64K address space of each 6809 processor appears as a small slice of the 16 megabyte address space of the 68000. Software then defines various protocols for the different processors to pass messages and data to one another by simply placing them in system memory.

The DMA interface provided on the 68000 SMPTE/MIDI Card is a very flexible one. It automatically handles either 8 or 16-bit data transfers (doing double cycles across the 8-bit CMI bus in the latter case) and can do so on either P1 or P2 cycles, selecting any desired memory mapping which has been set up on the Q256 memory card.

DMA is initiated by the 68000 when it accesses any address in the range $040000 to $05FFFF. These addresses are decoded by the LS259 (E12) on drawing CMI-28-1/7 and result in the $\overline{\text{CMI}}$ signal being asserted (low). Since the rest of the interface circuitry is not activated yet, PACK (to be explained later) will be low and a low will be presented at the data input of flip flop C12(a) whose function is to synchronise the transfer with the CMI bus.
Address line A16 is used to select which 6809 processor's bus cycle(s) are to be used for the transfer. The timing signals for both processors are input to LS241 buffer A7 which is wired as a muliplexer:-

If A16 is low, P2ø2 is enabled through to become Pø2, ADD2 becomes PADD and so on.
If A16 is high, P1's timing signals are enabled instead.

By this means, the address range specified above is split in two: from $040000 to $04FFFF the transfer automatically occurs on P2 bus cycles, while from $050000 to $05FFFF it occurs on P1 cycles. Refer to the 6809 CPU documentation for more information on the interleaved P1/P2 CMI bus cycles.
Thus at the beginning of the data cycle of whichever processor is selected, the Pø2 signal clocks the LS74, recording the fact that a DMA cycle is required.

All DMA devices are interconnected on the motherboard in a "daisy chain". Each device is assigned a given priority in the chain and must wait until no higher priority device is already using the bus. The 6809 CPU is the always the last device in the chain. There are two separate daisy chains in the CMI system, one for each 6809 CPU. Since the 68000 SMIDI card can perform DMA on either CPU's cycles, it is a member of both chains. $\overline{\text{ETL1}}$, $\overline{\text{ENL1}}$ and $\overline{\text{RDMA1}}$ are the chain signals for P1, $\overline{\text{ETL2}}$, $\overline{\text{ENL2}}$, $\overline{\text{RDMA2}}$ are for P2. Which set are used is again selected by the state of A16 at the time of transfer.

The selected $\overline{ETL}$ (Enable This Level) signal is low when no higher priority device is occupying the bus. After the CMI signal has been latched, nothing happens until this signal is low, whereupon the $\overline{RDMA}$ (Request DMA) is driven low through the selected LS12 gate. Any DMA device pulls this open collector line low to to request bus access to the CPU. At the same time, the selected $\overline{ENL}$ (Enable Next Level) signal is inhibited. Normally, the low on $\overline{ETL}$ comes in and goes out again on $\overline{ENL}$ to indicate to lower priority devices that the bus is available but when the 68000 requires a transfer $\overline{ENL}$ is held high to hold up the lower devices.
The CPU acknowledges that it will hang and release the bus for the next cycle by asserting ACK1 or ACK2; the selected ACK signal becomes PACK. When a request has been generated (C12(a) $\overline{Q}$ hi) and this level is enabled ($\overline{ENL}$ lo), the rising edge of PACK clocks a low into flip flop B11(a) to generate $\overline{DCYCLE}$. This signal indicates that the next bus cycle is definitely going to be a 68000 DMA transfer and remains asserted until the end of the address phase of the actual DMA cycle.

The other half (b) of B11 is also clocked by PACK to generate the P1 or P2 $\overline{DMAC}$ (DMA Claim) signal as selected by A16. This signal goes to the Q256 RAM card to select the memory mapping which has been set up specifically for the 68000. In this way the 68000 may have access to part or all of the same physical memory space as the 6809 CPU or it may have access to an entirely different part of physical memory as required by software. The $\overline{DMAC}$ signal is asserted during the data cycle preceding the actual transfer.
The address phase of the DMA cycle is indicated when $\overline{ATB}$ (Address To Bus) is asserted by the LS10 B10. At this time the lower 15 bits of the 68000 address bus are enabled on to the CMI bus through the two LS244's A2 and A3 to select the required location within the 6809 address space. VMA is driven high through LS125 B1 to indicate a Valid Memory Address and the 68000 R/W line is driven through the same buffer to indicate a read or write cycle. When the 68000 performs 8-bit memory accesses, the $\overline{UDS}$ and $\overline{LDS}$ signals (upper and lower address strobes) indicate whether an even or odd address is being accessed. The sense of these signals are clocked into JK flip flop H12 at the beginning of $\overline{DCYCLE}$ to generate HIBYTE and LOBYTE. The latter signal becomes the least significant address line driven onto MA0 through A3.

In the case of 16-bit accesses, the hardware automatically requests two successive DMA accesses across the 8-bit CMI bus. Both $\overline{UDS}$ and $\overline{LDS}$ are asserted so that the JK outputs HIBYTE and LOBYTE simply toggle on each access. It does not matter which byte transfers first and in fact this depends on the initial state of N6. LOBYTE directs the data to or from the odd or even address and both signals control whether the higher or lower 8 data lines are directed to the data bus.

The data bus interface consists of Schmitt bidirectional bus transceiver LS640 A6 and bidirectional driver/latches C5 and C6 (LS646s). The data phase of the DMA transfer is indicated by the assertion of DTB (Data To Bus) at the rising edge of BRA when a DMA cycle is in progress. This is performed by flip flop MN4. DTB enables the bus transceiver A6 and the direction is determined by the 68000 R/W signal.

If the 68000 is writing to the CMI bus, C5 or C6 simply act as buffers to transfer the high or low 68000 data signals (PD0-15) through to A6. HIBYTE or LOBYTE plus CMI being asserted will drive the G input of the appropriate LS646 for the duration of the DMA cycle (LS02 and LS32 gates M2 and M1).

When the 68000 reads from the CMI bus, C5 or C6 must latch the data in from the bus to hold it until the 68000 terminates its own cycle and latches the data internally, about 50nS after the end of the DMA cycle. 100nS before the end of the data phase, the CMI timing signal CAS goes low, resulting in a rising edge on BCAS. Data from memory is guaranteed to be valid at this time. B10 generates the LDATA (Latch Data) signal which is ANDed with either HIBYTE or LOBYTE to latch the data coming into the A side of C5 or C6. The output of the latch (B side of the selected LS646) is driven onto the PD lines until the 68000 completes its cycle and negates CMI.

Termination of the transfer after single or double DMA cycles is controlled by the two flip flops in LS74 C10:

In the **single (8-bit)** transfer case, either UDS or LDS will be low. This will cause the LS10 A10 to output a high, and DTACK2 will be generated as soon as LDATA occurs. The 68000 will then terminate its cycle immediately, after only one DMA cycle.

In the **double DMA cycle (16-bit)** case, both UDS and LDS are high so DTACK2 will not be generated until the first flip flop in C10 is set. Initially this flip flop is reset. At the first LDATA pulse a high is clocked in but DTACK2 is not generated because of the propagation delay through to the next flip flop. Since DTACK2 is not asserted, the 68000 still waits with address and address/data strobes asserted. If writing, the data remains asserted by the 68000 but both address and data are removed from the CMI bus when ATB and DTB are negated respectively. If reading, the first byte read in is latched and held by C5 or C6. Since CMI will still be asserted and PACK will have been negated, the whole process of waiting for daisy chain priority and DMA requesting begins again in order to perform a second DMA cycle. The second cycle can be held up indefinitely by higher priority devices using the bus after the first cycle. When the second LDATA edge comes along the high on the LS10 output is clocked into the second C10 flip flop and DTACK2 is asserted. On the next falling edge of PCLK, the 68000 recognises that DTACK has been asserted. On the second falling edge of PCLK the data is latched internally for a read, and the address and strobes are released. The low on BAS resets the flip flops at C10.

4.12.4 Debugging Notes for the DMA Circuitry

If the timing circuitry of the DMA interface is faulty, the most likely result is that DTACK2 will never be generated and the 68000 will simply hang which makes debugging easy. In this case, check first that the address decoding is generating CMI, then that the daisy chain signals are present. Then look for an 800nS pulse on DCYCLE, indicating that DMA cycles are actually ocurring. Continue through to the ATB, DTB and LDATA signals, checking not only that they are generated but also that they get to their respective destinations in the circuitry.

If the DMA cycles are being synchronised and timed correctly check that the address buffers and data buffer/latches are being enabled and clocked at the correct times.

If all timing circuitry is correct, the last possibilty is data or address bus shorts, open circuits or faulty drivers. Special test ROMs are available which cause the 68000 to repetitively copy bytes and words from one location to another in CMI memory. The 6809 monitor can then be used to deduce which data or addresses cause problems.

4.12.5 SMPTE/MIDI Card Peripheral Circuits

There are four different peripheral circuits on the SMIDI card. Firstly, there are the four ACIA's (G7-11) which are the MIDI ports A,B,C, and D. Then there is the Timer (bottom rev.2 G5,6) which is used in conjuction with the SMPTE read and generate circuits (which are the other two circuits) as well as the Click In and Out.

The ACIA's and Timers work from an 8-bit data bus with (asynchronous) interfacing circuitry. They are driven also by the E (enable) signal from the 68000. The frequency of this clock is one-tenth of the 68000 clock (10MHz) with a 60/40 duty cycle (6 clocks high, 4 clocks low)

Initially the flip-flops (F2) are cleared causing a high $\overline{\text{DTACK3}}$ output setting the LS646 transceiver (G4) into the transparent mode. The direction of data flow is determined by the R/W line with the IO selected. Without IO line selected it appears in write mode. The peripheral is selected by the LS138 enabled by the $\overline{\text{CS}}$' signal. The first flip-flop F2(a) is clocked on the first falling edge of E with the IO select and the data strobe high (ie either $\overline{\text{LDS}}$ or $\overline{\text{UDS}}$ low). The Q output of F2(a) is applied to the NAND gate (G3), asserting $\overline{\text{CS}}$'. Selecting the peripheral at this time ensures that the peripheral has adequate address setup time.

On the next falling edge of E, the $\overline{Q}$ output of F2(b) is clocked low asserting DTACK3 and latching data in the transceiver (G4). The asserted DTACK3 signal deselects the peripheral by causing CS' to go high. Flip-flop F2(a) is cleared by IO going low when the access terminates. Clearing flip-flop F2(a) also initializes the interface circuitry for the next access.

The ACIA's are selected by E10 and appear at addresses; $60020, $60030, $60040 and $60050. They share a common interrupt level - level 3. Their transmit and receive data lines are wired to the 26-way connector to be connected to the MIDI drivers and opto-coupler receivers.

The programmable timer (G5,6) appears at the general address $60000, and has an interrupt level-2 to the 68000.

RAM is fast enough (150ns) to not need a delay on the $\overline{DTACK}$ line, so that when RAM is selected $\overline{DTACK}$ is also enabled. Not so with ROM, a delay is needed and is provided by the LS161 counter (F1) which delays the enabling of the $\overline{DTACK}$ line by 12 processor clock cycles.

4.12.6 Interrupts

The 68000 has seven levels of interrupts. The priority for the interrupts is made by hardware through the 74LS148 ic (C2). The lowest level interrupt ($\overline{INT1}$) and the NMI ($\overline{INT7}$) are enabled and cleared by the CMI through the control port (B4). $\overline{INT2}$ is for the 68B40 Timer, $\overline{INT3}$ is for the ACIA's. $\overline{INT4}$ is for reading a SMPTE 'one' and $\overline{INT5}$ for a SMPTE 'zero' and are cleared by addressing location SMPTEWR on i.c. E10 (LS138). $\overline{INT6}$ is for SMPTE generation and is cleared by writing to the shift registers (C7,C8), i.e. by signal $\overline{SMPTERD}$.

4.12.7 SMPTE Generating Circuitry

An oscillator (3.84MHz) is divided by 10 (G2,G1) to provide a standard for generating the 3 different rates of SMPTE code (24, 25 and 30 frames per second). All three are denominators of 384,000. Further division, depending on the frame rate selected, is done by the Timer (G5,6) giving the signal CLK2, which is the bit rate for a SMPTE 'one' (ie 160 bits per frame). This is in turn divided by 2 (C11) giving CLK1 which is the bit rate for a SMPTE 'zero' (ie 80 bits per frame). When a SMPTE word is ready it is written to the Parallel-In-Serial-Out registers (C7,C8)at address $60070 (through B9,B8 and B7). When this writing takes place the interrupt $\overline{INT6}$ if it has been asserted is now cleared. The data in the shift registers (C7,C8) is clocked out by CLK1, a 4-bit counter (D11) is also clocked which causes the interrupt on level-6 (INT6) when it reaches its terminal count of 16. Now, if a 'zero' is shifted out from C8 the flip-flop C11 is toggled at the rate determined by CLK2, but if a 'one' is shifted out from C8 the flip-flop C11 is toggled at the CLK1 rate. Thus, the word stored on the shift registers is outputted in SMPTE form.

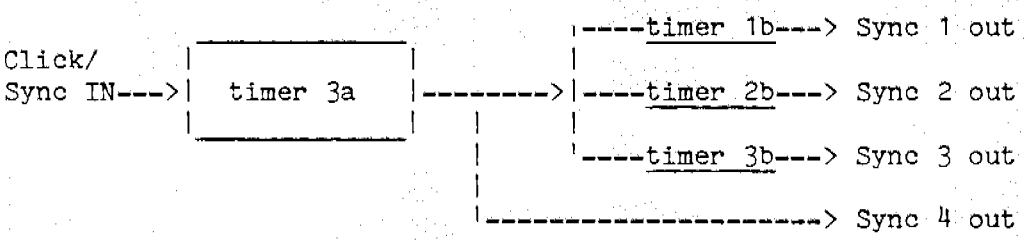
4.12.8 SMPTE Reading Circuitry (Refer to Timing Diagram)

SMPTE code coming from tape, being converted to TTL signal levels by the CMI-29 board, is received by the CMI-28 through pin 17 of the 26-way connector. The circuitry consisting of the EXOR gates (C1) and the resistor-capacitor combination creating a pulse (at pin 6 of C1) for every up or down transition of the incoming signal.

The required output from this SMPTE data separator is to have one interrupt occur for every SMPTE 'one' read and another interrupt for every SMPTE 'zero' read. This process can be followed through with the timing diagrams. The 68B40 timer is set, according to the frame rate of the SMPTE being read, to 3/4 of the time for one bit cell. The circuit then detects whether there has been a transition in that time or not. If there has been a transistion then a 'one' is read, if no transition occurred then a 'zero' is read.

4.12.9 Sync In and Out

The SMIDI card also takes care of some of the sync-ing functions of the system. On revisions 1 (modified) and 2 of the CMI-28 SIDI board there are two 68B40 programmable timers (each with 3 timers inside), one wired on top of another. The input clock of 3rd timer in the bottom 68B40 (timer a) is wired to the Click/Sync input socket on the support box mounted to the rear panel of the mainframe. The output of this timer is fed into the inputs of the three timers in the top i.c. (timer b) providing a cascaded timer system. These four outputs are fed to the CMI-29 in the support box, to a 5-pin DIN socket via open-collector buffers.



4.12 CMI28 GENERAL INTERFACE - FUNCTIONAL DESCRIPTION (continued)

4.12.10 General Interface Support Card CMI-29

This circuit board contains the analog circuitry required for the I/O for SMPTE and MIDI. There are 3 MIDI inputs (A, B & C) and 4 MIDI outputs (A, B, C & D). Provision has been made for a fourth MIDI input (D). The SMPTE input has a balanced line receiver. The signal is then filtered and converted to TTL compatible signals through the LM311 comparator. The SMPTE out signal is converted from a TTL to a balanced line signal. The SMPTE in and out signals are received and transmitted via two 3-pin XLR sockets and are connected to the board via the 20-way socket. The MIDI I/O circuitry is the standard current loop drivers (open-collector buffers (U10) and receivers (fast opto-couplers (U5-U8)).

There are two other output (5-pin DIN) sockets. One is the CLOCK output, containing the CLOCK, RESET/START and RUN/STOP TTL compatible signals. This CLOCK output is designed to control Roland-type drum machines, etc. The other is the multiple SYNC output. A click or sync signal received through the CLICK input is fed to the 68B40 Timers (see above). The outputs are connected to the DIN socket driven by open-collector buffers. You will notice that the SYNC out 4 signal is the same as that of the CLOCK and of CLICK out.

4.12.11 Pin Connections for the 26-way Connector between the CMI-28 and CMI-29.

Pin 1	MIDI out A.	
Pin 2	+5 volts.	
Pin 3	MIDI in A.	
Pin 4	SYNC out 1.	
Pin 5	MIDI out B.	
Pin 6	SYNC out 2.	
Pin 7	MIDI in B.	
Pin 8	SYNC out 3.	
Pin 9	MIDI out C.	
Pin 10	Digital Ground.	
Pin 11	MIDI in C.	
Pin 12	Digital Ground.	
Pin 13	MIDI out D.	
Pin 14	RESET/START.	
Pin 15	MIDI in D.	
Pin 16	RUN/STOP.	
Pin 17	SMPTE code in.	
Pin 18	Digital Ground.	
Pin 19	SMPTE code out.	
Pin 20	CLICK out; SYNC out 4.	
Pin 21	CLICK in.	
Pin 22	(CMI29) Analog Ground.#	(CMI28) n/c.*
Pin 23	(CMI29) +15 volts.#	(CMI28) CPU Halt switch.*
Pin 24	(CMI29) -15 volts.#	(CMI28) Digital Ground.*
Pin 25	(CMI29) n/c.#	(CMI28) CPU Reset switch.*
Pin 26	(CMI29) n/c.#	(CMI28) Digital Ground.*

NOTES:

these connections are from the CMI29 board to the Audio Board only.
* these connections (from the CMI28 board only) are for debugging purposes only. If two push-button switches are connected between pins 23 & 24 and pins 25 & 26, they can be used to manually halt and reset the 68000 processor, respectively.

4.12 CMI28 GENERAL INTERFACE - FUNCTIONAL DESCRIPTION (continued)

4.12.12 Pin connections for the 20-way connector (CMI-29 board)

Pin 1	n/c
Pin 2	Analog ground
Pin 3	-15 volts
Pin 4	+15 volts
Pin 5	Analog ground
Pin 6	n/c
Pin 7	n/c
Pin 8	n/c
Pin 9	n/c
Pin 10	Analog ground
Pin 11	SMPTE in+
Pin 12	SMPTE in-
Pin 13	SMPTE out+
Pin 14	SMPTE out-
Pin 15	Click/Sync in
Pin 16	Analog ground
Pin 17	Sync-4 out
Pin 18	Analog ground
Pin 19	Key + (MIDI D in)
Pin 20	Key - (MIDI D in)

4.13 CMI07 - ANALOG INTERFACE FUNCTIONAL DESCRIPTION

The Analog Interface Card provides 16 voltage inputs and 16 voltage outputs. These are fully protected and cover the full control voltage range of analog synthesizers, calibrated at the standard rate of 1 Volt per octave with one millivolt resolution.

The 16 outputs are driven from individual sample and hold op amps, locations F1 - F8, signals multiplexed via IC's AD 7501, location E4 and E5, scaled through op amps location E2 and E3 and latched D/A converters AD 7524 location D3, D4, D5. The main signal comes from a 14 bit D/A converter AD 565, location E6,7. Main D/A data is latched into the AD 565 from IC LS 273 location D6 and D7.

The 16 analog input channels are concentrated after input protection diodes D1 - D32 through input multiplexers AD 7501 location E8 - E9 and scaled at op amp location F12.

A/D conversion is performed using a 14 bit ADC AD 574 location E10, E12, input data latched into IC LS 374 location D11.

Analog scale calibration for inputs and outputs is simple with precision multiturn trimpots VR2 and VR1 located near the top handle of the board. Detailed information about calibration is given in Section 6.10 - Diagnostic Software of this manual.

Analog power is supplied to the board via a 10 pin ribbon cable connector located at the centre front between the input connector and the output connector.

All on board functions are controlled from a 6809 processor location C5,8 and programmable system timer 6840 location C10,12. Vector software and parameters are down loaded and reside in 16k bytes of dynamic RAM location X1 to X8. Buss data is buffered via IC LS 640 location C4, onboard data through IC LS 373 location C3, address buffers are IC's LS 257 location A3, A4, B3, B4.

IC's A6 to A12, B5 to B12, and C9 are used for miscellaneous buss timing decoding and buffering, link blocks LK1 and LK2 determine the board's base address.

5. TROUBLESHOOTING

5.1 Introduction

The C.M.I. system relies on a complex interaction of hardware and software for proper operation. It is often difficult to differentiate between hardware faults, software bugs and operator errors. Before attempting repair of the Mainframe, establish that the fault is definitely a hardware fault in that unit. If in doubt, try the same series of operations on another system of the same revision level to ensure it is not a software bug and check with the Users Manual to ensure it is not operator error.

Refer to the C.M.I. System Service Manual for information on how to ascertain that the fault lies within the Mainframe itself and not one of the other system units.

Due to the complexity of the system, this manual does not attempt to present an exhaustive list of faults and repair procedures. Instead, the detailed descriptions (above) should provide service personnel with a thorough understanding of the hardware so that the problem area can be identified.

Extensive diagnostic software is provided to thoroughly test most of the hardware. Of course, in order to run the diagnostics the computer section must be running at least to the stage of loading and executing the software. Use of the diagnostic software is described in detail in section 6 (below).

A guide to troubleshooting the major components of the Mainframe follows:

5.2 Power Supply

A fault in the power supply will usually result in complete failure of the system (the computer does not run, so no message is displayed on the screen). An exception to this is a failure of the analog supply (+/- 15 volts to the channel cards, master card and audio card). In this case, the C.M.I. should appear to function normally although no sound will be produced.

Three L.E.D.s are provided on the front panel of the C.M.I. to indicate the state of each of the digital supplies, +12, -12 and 5 volts. These are the supplies to the cards in the card cage, supplied by the Motherboard. The L.E.D.s will not light if the relevant supply drops below two-thirds of the nominal voltage. Note that these L.E.D.s pick up their supplies via the ribbon cable connected to the Q133 card, so it is possible that a fault in the Q133 could cause the L.E.D.s to malfunction.

Fuses for the +24 volt supply (disk drives) and +/- 12 volt digital supplies are located on the transformer cover plate at the left-hand end of the card cage. They are accessed by hinging down the front panel. The +/- 12 volt fuses actually protect the raw D.C. supply to the 12 volt regulators. See Section 4.9, QPSA. As this raw supply also powers the music and alphanumeric keyboards, a fault in either of these units could blow the fuse. The +/- 12 volt supplies are current limited so that a fault on a circuit card will not normally blow a fuse.

The raw supply to the +5 volt regulator is protected by a 15 amp cartrige fuse mounted on the regulator P.C. card. This fuse should never blow except in case of catastrophic power supply failure. See Section 4.9 QPSA.

All other fuses are located on the rear panel of the mainframe.

In the event of a power supply failure, be suspicious that the failure may have been caused by a malfunction elsewhere, or incorrect setting of the mains voltage selector (on the Mainframe rear panel).

5.3 Computer Section

A failure in the computer section may result in permanent or intermittent malfunction of the system.

If the system will run to some degree (i.e. load a disk and respond to commands) the diagnostic software described below should be run to localise the fault and the offending card can then be replaced.

If the system will not run at all (will not load the diagnostic disk) start by checking the following:

1) ENABLE/SAFE switches on the front panel must be in the Down (RUN) position.
2) Mains voltage selector on the rear panel must be set correctly.
3) Power must be applied, as indicated by the three L.E.D.s on the front panel.
4) The System Disk must be in good order (as indicated by testing in another system) and inserted correctly.

If these items are all in order, but the system disk will not load, confirm that the fault lies in the Mainframe by disconnecting everything except the A.C. supply from it and trying to load the disk again.

If the disk will still not load, the system should be "stripped down" until operation is restored. Remove cards in the following order, attempting to load the disk after each stage:

1) Remove all eight channel cards (CMI01-A)
2) Remove the graphics/lightpen card (Q219)
3) Remove the master card (CMI-02)

If the disk will still not load, substitute the remaining cards with known good spares one at a time. If the fault persists, the problem must be in the power supply, disk system, motherboard or cabling. Refer to Section 7 (Motherboard Signals) and Section 8 (External Connections) below, for details of motherboard and external signals.

5.4 Disk System

The Disk system consists of three sections - the floppy-disk controller card QFC9, interconnecting cables, and the two floppy-disk drives themselves.

A fault in the controller card or cabling will generally result in hard disk errors or total failure to access disks. Soft or intermittent disk errors will usually be caused by a faulty or misaligned drive.

A toggle switch mounted on the front edge of the controller card reverses the drive select signals to the drives so that the logical drive numbers can be swapped for diagnostic purposes. For example, if a disk error is reported during boot-load, the drives can be swapped (switch down) and the system disk inserted in the right-hand drive. If it then loads sucessfully, the left-hand drive is faulty. If the fault persists, the fault is in the controller, cabling or power supply, unless the system diskette itself is faulty.

Refer to the Fairlight Disk System Service Manual for full details of disk drive maintenance.

5.5 Channel Cards

Incorrect operation of individual channels is caused by a faulty channel card or audio card.

Comprehensive diagnostic software is available for testing the channel cards. The digital circuitry is tested automatically, and the analog circuitry requires waveform measurement using an oscilloscope.

Channel selection is performed by the Master Card (CMI-02). A fault in this area will show up as a digital failure of one or more channel cards when the diagnostic software is run.

In case of an audio fault in one particular channel, it is not always clear whether the fault lies in the channel card or the audio card. This can be resolved by swapping the suspect channel card with a good spare, or with another good channel card in the same Mainframe. If the fault remains in the same channel output, the fault is in the audio card, or possibly the ribbon cable connecting the channel card to the audio card.

5.6 Master Card

Special Master Card diagnostic software is provided to test all functions (see section 6 below). The Master card is responsible for the following major functions:

5.6.1 Channel Card Selection

Faulty channel card selection will show up as channel card failures when running the digital tests of the Channel Card diagnostics. If a channel card fault is detected by the diagnostics, and the fault persists when the card is changed, then the master card may be at fault and should be exchanged for a good spare.

5.6.2 Channel Card Master Clock

The crystal oscillator located on the master card provides the master pitch reference and memory timing signals for all channel cards. These signals for all eight channel cards are bussed together. A fault in this area will cause identical faults in all channels, manifested primarily as Memory or Pitch test failures.

5.6.3 Analog to Digital Conversion

Improper operation of the Sound Sampling (Page 8 of the C.M.I. System Software) will be caused by a fault in the Master Card, Audio Card, or interconnecting cabling.

As a first step, the Master Card should be exchanged with a good spare. If the fault persists, the Audio Card should be replaced next. Finally, the intercornecting cables should be checked using the Mainframe Wiring Diagram (Drawing number MC001-01), Audio Card Functional Description and Master Card Functional Description as a guide.

5.6.4 External Synchronisation and Timer

Improper operation of the Sync Input or Click Output function (Page R, M.C.L. or Page 9) can result from a fault in the Audio card or Master Card, or the 10-way ribbon cable connecting the two together.

Diagnostic software is provided for testing the operation of both the input and output. Refer to Section 6 - Diagnostic Software for full details.

The fault should be isolated by replacing the Master Card with a good spare, followed by the Audio Card, and finally the interconnecting cable.

5.7 Audio Card

The Audio Card (located inside the rear panel of the mainframe) provides buffering for the analog signals entering and leaving the Mainframe, as well as regulating the +/- 15 volts power supply to the analog circuitry.

The following types of fault will usually indicate a faulty Audio Card:

1) Audio faults appearing in a particular channel which are not cured by exchanging channel cards.

2) The Mixed Line Output does not function properly, although each individual channel output is correct.

3) The Monitor speaker output or Headphone output is faulty.

4) Sound sampling using Mic input does not work, but the Line input does (or vice versa).

The following faults may be caused by an Audio Card malfunction or some other fault:

1) Sync input or output does not function properly.

2) Analog power supply (+/- 15 volts) incorrect.

3) Improper operation of an individual audio channel.

No.3 - "Zero Crossing Flag"
ose: Test "middle of segment" flag.

d at the middle of every segment by waveform address counter . The flag
n when the within-segment byte count reaches 64. The test asserts LOAD
s the counter then does 63 writes to waveform memory, checking each time
flag is clear. One more write should then set the flag.

No.4 - "Zero Cross Interrupt Flag"
ose: Test "middle of last segment" flag.

ssing interrupt occurs on first zero crossing after the segment timer
The timer is programmed to be clocked by the internal clock. Until it
, the zero-crossing interrupt is checked for no premature flag. After
he status is read again to check that the zero-crossing flag has
. The address counters are clocked at maximum pitch during the test.

6. DIAGNOSTIC SOFTWARE (continued)

The following is a list of the chain files currently in use.

CHAIN	FUNCTION	NOTES
CMITEST	tests **Q256 256K Memory Card,** CMI-02 Master Card, CMI-01-A Channel Cards (digital section) and CMI Interrupts	
DISKETTE	checks the Diagnostic Disk	Not actually CMI hardware
AUDIO	tests each Channel Card for an audible output	
VIDEO	tests Q219 Graphics/Lightpen card	Type **CHAIN VIDEO**<return> **then type C** for a green screen. The lightpen can now be tested on the screen. Type **<ESC> to start** Video Ram test. Random patterns on screen.
AIC	Test the inputs and outputs of CMI07 Analog Interface card	Inputs and respective outputs must be connected together a shorting plug.
ANALOG	Test the analog hardware	

6.1.3 Running the individual Test Programs

Most of the diagnostic programs make use of a common command interpreter for operator control, so there is a uniform command syntax employed throughout, and several test options available as standard. Tests may be run by typing

<test name>[,<option1>,<option2>...,<optionN>]<return>

where the <test name> is as described in each section. Options are of the form

<O>=n where <O> is a single character and n is an integer.

Standard options are

P=n Repeat test command n times. Using "C" instead of an integer initiates continuous testing.

N=n Select test number n. There are usually several test commands with the same name. By default, all tests are executed sequentially but single tests or subsets of the available tests can be specified.

For example	N=1	Test no. 1 only
	N=1,3,5	Tests 1, 3 and 5
	N=4-7	Tests 4 to 7 inclusive

Some tests, which require a waveform to be observed, wait for the spacebar to be pressed before terminating or proceeding to the next test.

To obtain a reminder of what tests are available from the current test program being run, type

LIST<return>

To repeat the last test, just type

R<return>

If an error condition occurs, a moderately helpful message is printed on the console and the program returns to the command interpreter or continues testing depending on the setting of the errors option.

ERRORS is a standard command used as follows ...

ERRORS - the error counter is displayed on the screen.

ERRORS,E=0 - error counter is reset

ERRORS,C=1 - count errors and continue testing regardless

ERRORS,C=0 - abort test (and CHAIN if one is running) on error

The C option defaults to 0.

Successful tests terminate without comment and return to the interpreter or proceed to the next test as soon as completed. Certain tests require the user to check waveforms with an oscilloscope and will not terminate or proceed to the next test until the spacebar is pressed.

6.1.4 Measurement Tolerances

A tolerance of +/- 15% is acceptable for most voltage or frequency measurements. Filter attenuation levels are harder to control and may be subject to +/- 20% variation. Changes to analog circuitry in design revisions may also effect level measurements. Values quoted here are valid for the revisions referred to in the text.

6.2 Channel Card Tests

A program for testing CMI channel cards is CMITST.CM which can be run by typing

```
CMITST
```

with the CMI diagnostics disk in drive 0.

It can test channel cards individually or up to eight at a time. There are eight different tests within CMITST, each exercising a different part of the channel card.

The standard command interpreter is used so the LIST ERRORS and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<return>

A "C=n" option is avilable for all tests, which specifies the channel number(s) to be tested, in the range 1 to 8. Default is 1. Multiple channel numbers can be specified separated by commas or a hyphen.

```
e.g. FILT;C=3
     FILT;C=1-4
     FILT;C=3,5
```

One side of the balanced analog output of the channel card is available at test point 6 (TP6) at the front of the card. The row of test pins is numbered from 1 at the bottom. Pins 1 and 2 are connected to digital ground, 3 and 4 to analog ground.The other side is available at test point 5. Measurements quoted in this text refer to TP6. However if a complete CMI is being tested, it may be more convenient to use the Fairlight Analog Tester box (see section 6.10.3 for how to connect it to the CMI and an oscilloscope). Waveforms observed from the tester will be of the same form as TP6 but different levels. Refer to the Waveform Summary (section 6.11) for Analog Tester levels.

Note that Fairlight DO NOT release schematics of the Channel Card as all repairs are done on a return-to-factory basis.

Board component references are for the Series II Channel Card CMI-01-A, revisions 1-4 only. This section describes CMITST Revision 3.30.

CAUTION: WHENEVER CHANGING OR REMOVING THE CMI MASTER CARD OR CHANNEL CARDS, OR PLUGGING RIBBON CABLE CONNECTORS ONTO THESE CARDS, ALWAYS SWITCH OFF POWER FIRST. FAILURE TO DO SO WILL ALMOST CERTAINLY CAUSE HARDWARE DAMAGE!

6.2.1 Trimming Tests

Test name: TRIMA
No. tests: 9
Purpose: Alignment of the seven trimpots used in the Series II channel card.

The calibration process is intended to be self explanatory by means of running each of the TRIMA tests in turn and following the instructions printed on the CMI display. All 9 tests begin by filling 4 segments of waveform memory with a fundamental sine wave and playing it back with pitch, envelope, volume and filter controls set appropriately for adjusting one control at a time. Revisions 1 and 2 channel cards contain a CEM 3320 filter, while the Revision 3 and 4 cards have this replaced by a SSM 2045 chip. The calibration procedure is slightly different for the two devices, and the SNR and distortion performance is better for the latter. The three tests affected by this change have an "R" option.

Typing TRIM A or
TRIMA,R=3 will call the trimming procedure for Rev 3 and 4 cards.

Type TRIMA,R=1 or
TRIMA,R=2 to get the earlier version procedure.

All comments below referring to the Rev 3 card also apply to the Rev 4 card.

In some cases insertion of an external test signal and connection of a distortion meter is required and this is facilitated by a 10 way unprotected header at the front of the board. Looking at the front edge of the board, pin 1 is the bottom outer pin of the header, pin 2 is the bottom inner pin (closest to the PCB) and so on. The pins connect as follows:

Pins 1-4: Analog ground
Pin 5 : VCA out
Pins 6,7: Filter out
Pin 8 : Waveform DAC out
Pin 9 : VCA in
Pin 10 : Filter in

6. DIAGNOSTIC SOFTWARE (continued)

In normal operation, pin 9 is shorted to pin 7 and pin 10 is shorted to pin 8.

Several of the TRIMA tests require the use of the AWA Noise and Distortion meter which is also an RMS level meter. For all such tests the 20kHz filter in the meter should be switched in to remove digital noise and RFI picked up by the connecting cables. Positioning of the meter can be critical: check that proximity to VDUs, power supplies and other sources of interference are not disturbing the readings. The 400Hz filter in the meter may be used to remove hum and is required for the SNR measurement (test 9). However if its effect on other readings is large an interconnection fault is probably causing undesirable levels of hum.

The various connection changes required by the calibration process have been facilitated in the test department by a relay box to which the cards under test, oscillator, distortion meter and CRO are connected. Code has been added to all the TRIMA tests to drive the relays through the user PIA on the Q133 debug card. Refer to internal Test Department documentation for operation of the relay box.

Test N=1, Envelope Offset Coarse Adjustment (VR1)

A 1Khz sine wave is played while the ENV signal is ramped up and down as in the RAMP,N=2 test (see sect A.3). Observe the waveform DAC output at TP9 and adjust VR1 to achieve 100% modulation. This is indicated by no sine pattern appearing where the ENV signal reaches its minimum. This adjustment is required before the VCF and VCA can be trimmed but it is more accurately acheived later by test N=8 (which cannot be performed until the VCA is trimmed). The maximum amplitude of the signal should be 9Vp-p on revs 1 and 2, 8Vp-p on rev 3.
Volume is set to full, and the filter set to $80 (four octaves above fundamental) but these settings are not relevant to the adjustment of VR1

Test N=2, Filter Control Bias (VR6)
Option: R - channel card Revision
Range 1-3, default 3.

This test requires TT10 and TT8 to be shorted.
The filter is calibrated so that the lowest user setting (1 on CMI system PAGE 7) results in -3dB attenuation at the fundamental frequency being played by the channel card.

Revs 1 and 2: Envelope is set to $FF (max) and a 100Hz sine wave played. This should be 9Vp-p at TP9. An resistor in the range 62k - 75K should be inserted in R20. This is chosen to optimise the distortion/SNR tradeoff later but is arbitrary at this stage. First the passband output level (0dB) is measured (this differs between 3320s) at TP7. To ensure the 100Hz signal is not being attenuated by the untrimmed filter, twiddle VR6 until digital steps are visible in the waveform. If the distortion trim is grossly out of setting, the level may also be affected. Twiddle VR2 to ensure that the waveform at TP7 does not have a straight-edged "triangular" character. The next step sets the minimum -3dB frequency: digital zero on the filter control and zero in the pitch register resulting in a 16.32Hz sine wave. Adjust VR6 to obtain the passband level divided by root 2 (-3dB).
A control voltage of approx 140mV at TP10 achieves this cutoff.
Envelope and volume are set to max ($FF)

Rev 3: Envelope is set to $FF (max) and a 100Hz sine wave played. This should be 8Vp-p at TP9. Twiddle VR6 until digital steps are visible in the waveform at TP7 to ensure the filter is set well above 100Hz then set the passband level to 2.5Vp-p at TP7 by adjusting VR2. The next step sets the minimum -3dB frequency: digital zero on the filter control and zero in the pitch register resulting in a 16.32Hz sine wave. Adjust VR6 to obtain 1.8 Vp-p at TP7 (-3dB).

Test N=3, Filter Control Gain (VR7)
Option: R - channel card Revision
Range 1-3, default 3.

This test requires TT10 and TT8 to be shorted.
This adjustment matches the volts/octave control voltage swing at TP10 to that of the filter which is nominally -18mV/octave. The same sine wave as TRIMA,N=2 is played six octaves higher (00-03 set to 6). Adjust VR7 for the same -3dB attenuation at TP7. (1.8 Vp-p for Rev 3). This corresponds to a control voltage of approx 140 - 6*18mV = 32mV. Envelope and volume are set to max. If the filter cannot be set properly, establish whether the fault lies in the control circuit or the filter itself by checking for a 140mV to 32mV change at TP10 between tests N=1 and N=2. This is produced by a change at the DAC output as follows:

Rev	Ref voltage	DAC Output swing, tests N=2,3
1	-15V	0 to 5.6
1 (modified)	-5V	0 to 1.88
2,3	-6.9	0 to 2.6

6. DIAGNOSTIC SOFTWARE (continued)

Test N=4, Filter Distortion (VR2)
Option: R - channel card Revision
Range 1-3, default 3.

Remove the short between TT10 and TT8 for this test.
Second harmonic distortion in the CEM 3320 VCF (Revs 1 and 2 only) is minimised by adjusting the resonance control bias. The adjustment is made using a sine wave signal in the pass band of the filter, i.e. well below cutoff.
A dummy sound is played by the channel card at zero pitch, envelope and volume in order to deactivate the FET mute at the VCF output (Rev 1, unmodified only). The filter latch is set to $FF (maximum cutoff).
Revs 1 and 2: A 9V p-p low distortion 1kHz sine signal should be inserted at TT10 . The filter output is available at TT6 for connection to a distortion meter. Select the minimum R20 in the range 62k - 75k which allows VR2 to trim the distortion to better than -40dB. This maximises the output level from the filter and hence the signal to noise ratio.
Rev 3: There is no distortion trim for the SSM 2045 on Rev 3 boards. With an 8V p-p low distortion 1kHz sine wave inserted at TT10, measure the distortion from the filter at TT8 (level here and TP7 should be 2.5 Vp-p as set by TRIMA,N=2. Distortion should be less than -60dB

Test N=5, VCA Control Bias (VR4)
Short TT9 to TT7 and TT10 to TT8 and select REL on the RMS meter.

This test sets the zero volume output level of the channel card.Monitor the level from the balanced outputs with an accurate RMS meter. A 1Khz sine wave is first played at full envelope and volume with the filter set to $80 (4 octaves up). The bias control should be adjusted to obtain 4Vp-p at TP6. Check that 4Vp-p also appears at TP5 and set the 0dB reference level on the meter connected to the balanced outputs. When the space bar is next pressed, volume is set to zero. Adjust VR4 down to -80dB on the meter. This is at a control voltage (TP11) of approx 486mV.

Test N=6, VCA Control Gain (VR5)

Leave the same test terminals shorted as the last test and do not change the meter's 0dB reference.
VR5 matches the control voltage range at TP11 to the sensitivity of the dbX VCA. The same 1Khz sine wave is played, this time at full ($FF) volume. Adjust VR5 for 0dB again on the RMS meter and 4Vp-p at TP6 and TP5.
If there are problems check that full volume produces 2.56V at the DAC output and zero volume produces zero volts, and that this swing translates to a 6mV to 486mV change at TP11.

Test N=7, VCA Distortion (VR3)

Remove the short between TT9 and TT7 for this test.
Insert a low distortion sine wave at TT9 and adjust the level for 4Vp-p at TP6. Connect the distortion meter to TT5 and calibrate it (select CAL and set 0dB level). Then read the distortion level (select READ) and adjust VR3 for better than -60dB.

Test N=8, Envelope Offset Fine Adjust (VR1)

Select REL and connect the meter to the balanced channel outputs with TT10 shorted to TT8 and TT9 shorted to TT7.
The accuracy of this setting ensures smooth envelope decays with no click at the end of a note.
A 1kHz sine is played at full volume and envelope to set the 0dB reference. When the space ba is hit the envelope is reduced to zero. VR1 should be adjusted for minimum level which should be less than 20mV at TP9 or -55dB on the meter. At the next hit of the space bar the envelope is set to 1. This corresponds to a level of 1/256 = -48dB. The envelope is then restored to max to check the 0dB level again. If the error here is too great (>1dB) it means the setting of test N=1 was not accurate so the VCA, and possibly the VCF, should be retrimmed.

Test N=9, Signal to Noise Ratio

This test does not set a trimpot but should be performed immediately after trimming as above. Leave the meter connected and set as in test 8. A full scale sine wave is played to check the 0dB reference. Then waveform memory is zeroed and played at full volume. A SNR of < -78dB should just be obtained for modified Rev 1 boards and Rev 2 boards. Rev 3 boards should have a typical SNR better than -85dB but -83dB should be considered as the brick wall specification.

6.2.2 Filter Tests

Test name: FILTA
No. tests: 14
Purpose: Checks filter control operation, calibration and roll-off slope of filter.

These tests perform the the same function for the Series II channel card as the FILT tests do for the previous revisions. Do not use FILTA for old cards or FILT for series II cards as the results will be meaningless.
The first and last tests (N=1, N=14) test the filter at zero and maximum cutoff respectively. The other tests check that each of the 12 bits input to the filter control system are effective in setting the filter cutoff to a predetermined frequency. The basic method is to compare two tones of differing frequencies: one just within the pass band for the given cutoff and the other at the -6dB attenuation frequency for the same cutoff. It is easy then to verify that one frequency is filtered to half the amplitude of the other.

6. DIAGNOSTIC SOFTWARE (continued)

For practical reasons there is some variation between the tests in the way in which this procedure is implemented, as described below. All tests fill the first four segments of waveform memory with a sine wave having a predetermined number of cycles per segment and a higher harmonic in the next four segments. The 0dB/6dB frequencies never turn out to be exact harmonics of each other so different pitches are set each time frequency is switched (the absence of this control in the FILT test results in considerable inaccuracy on some settings). Octave settings are never changed when switching frequencies because this would move the filter cutoff.

Tests N=1 and N=2

These test the zero setting and bit 00. Since the cutoff frequencies are very low the frequency is switched only every 1.5 sec or so to allow a stable CRO trace to be obtained. The channel loops over segments 0 to 3 with max envelope and volume, LOAD asserted, until a software timer expires. Then the channel is stopped (RUN off), the segment counters preset to segment 4, pitch register set to the 2nd pitch, and the channel started again (RUN on). At the next timeout the channel is switched back to the first four segments at pitch 1 in the same manner and this is repeated until the space bar is hit.

Tests N=3 to N=5

At octave settings 2, 4, and 8 corresponding to the three bits set in these tests the cutoffs are high enough to switch between the two harmonics automatically by looping over segments 0-7 continuously. Thus both frequencies can be displayed on the CRO simultaneously. The pitch adjustment is maintained "on the fly" by the processor polling the PIA (D6789) for the segment Zero Crossing (ZX) flag. At the zero crossing between segments 3 and 4 pitch 2 is set and between segments 7 and 0, pitch 1 is set.

Tests N=6 to N=13

These tests check each bit of the filter latch in succession. To enable the fast frequency switching, a frequency offset of four octaves (bit 02 is set always) is added. The effect of the lower order filter latch bits on the filter cutoff is very small (1/32nd of an octave in the lsb case, which ain't much even in the 4th octave) so to make sure the bit under test is working, it may be toggled by pressing the RETURN key. The resultant trace alternates between the normal 0dB/-6dB display and one in which both harmonics are more severely attenuated when the bit is reset. The filter bit may also be toggled automatically by software if the TOGGLE opion is set to one, e.g. FILTA,N=6,T=1.

Test N=14

This test checks the wide-open bandwidth of the filter by setting all bits high.

The following table preserves for posterity the filter control voltage, 0dB and -6dB frequencies for each test. The control voltages are only included as a guide, and may be subject to variation generated by component tolerances but the important thing is the cutoff frequency achieved. The table is only for the CEM filter used in Rev 1 and 2 card. There are two graphs attached, one for the CEM filter and one for the SSM filter (Rev 3).

Test	Bit set	TP10 (mV)	Pitch 1 (0dB)		Pitch 2 (-6dB)	
1	none	136.5	9.2	(Hz)	48.5	(Hz)
2	00	119.3	16		86.2	
3	01	102	37		157	
4	02	67	114		537	
5	03	-1.7	1400		6053	
6	F0	68	110		547	
7	F1	67.5	112		558	
8	F2	65.5	120		577	
9	F3	63.3	140		627	
10	F4	59	150		730	
11	F5	50	200		990	
12	F6	33	370		1830	
13	F7	-1.6	1470		6030	
14	all	-128	4540		19300	

Note Fn indicates filter latch bit n

6.2.3 Waveform Memory Tests

Test Name: MEM
No. tests: 8

Test No.1 - "Read-write 0"
Purpose: Tests memory read-write ability.

First the waveform address counters are reset (A4,B3,B4) then the entire memory is written with zeros. The address count is automatically incremented after each write by having LOAD asserted and RUN not asserted. Memory is read back in the same way to verify data.

Test No.2 - "Read-write FF"
Purpose: Tests memory read-write ability.

Writes $FF sequentially to entire memory and reads back to verify as in test 1.

Test No.3 - "Read-write and Refresh AA"
Purpose: Tests memory read-write ability.

Writes $AA to the entire memory, executes a delay loop for 5 seconds then verifies the contents of memory as in test 1.

6. DIAGNOSTIC SOFTWARE (continued)

Test No.4 - "Channel-Segment-Byte Uniqueness Forward"
Purpose: Checks that each byte in 16K memory of each channel card being tested can be addressed uniquely.

Memory is filled with 4-byte uniqueness patterns. Each pattern consists of the channel mask selecting that channel, the segment number being written to, and the double-byte offset of the first byte in the pattern. Each channel memory is then read back in the same order to verify the patterns.

Test No.5 - "Channel-Segment-Byte Uniqueness Reverse"
Purpose: Addressing uniqueness.

This test is identical to No. 4 except that channel memories are filled beginning with channel 8 instead of channel 1. This in case a fault on channel 1 is causing a fault to appear on another channel.

Test No.6 - "Segment Random Access using Load"
Purpose: Tests ability to preset waveform segment counters.

Waveform segment counters (B1,B4) are preset from the WS outputs of PIA C6789. This test can only be performed after test No.5 since it reads the uniqueness patterns to check that the correct segment has been selected.

A bit-swapping routine is used to generate a set of 127 non-sequential segment numbers. Each segment preset is loaded when the LOAD signal (also from PIA) is toggled, and the second byte of the uniqueness pattern at that preset is read to check the segment number.

Test No.7 - "Segment Random Access using Run"
Purpose: Waveform segment presettability.

Tests waveform segment preset as in test 6 but preset is loaded when RUN signal toggles.

Test No.8 - "Sequential Access"
Purpose: Checks that segment 1 of each channel can be written with an incrementing pattern. Writes to all channels simultaneously from zero address through to the end of memory then reads back, starting with channel 1.

6.2.4 Memory Dump

Test name: DUMP
No. tests: 1

Test No.1 - "Dump Channel Card Segment"
Purpose: Assists in examining Channel Card memory. DUMP prints the contents of 1 or more segments. The number of segments and which channel's memory is examined, are controlled by the options.

Options:	C=n	Channel select Range 1-8, default=1
	S=n	First segment Dumped Range 0-127, default 0
	L=n	Length of dump in number of segments Range 0-127, default 1

6.2.5 Envelope Control Tests

Test name: RAMP
No. tests: 4
Options : F=n Filter cutoff frequency
Range 1-127, default=8
S=n Ramp speed (tests 1 and 2 only)
Range 1-127, default=60

The nominal ramp levels at TP8 and TP9 changed slightly between Rev 2 and Rev 3 of the channel card. Levels quoted below are for the Rev 3 card. For Rev 2 cards, read 4.3V at TP8 instead of 4Vp-p, and 9Vp-p at TP9 instead of 8Vp-p.

Test No.1 - "Ramp Preset, DC wvfm"
Purpose: Tests ability to preset the counters and drive the envelope-shaping DAC.

The envelope counters (ICs E5 and E6) are preset from the RP outputs of PIA C6789. Waveform memory is filled with $FF which corresponds to a steady DC level. However, the envelope DAC is cycled linearly between 0 and $FF and back to 0 at a rate determined by the speed option and a software delay loop. The envelope up/down counters are preset directly from the PIA by toggling the LOAD signal. The outputs of the counters drive the envelope DAC (IC F5) up and down. A low frequency triangle waveform should result at TP8 with 4V p-p amplitude and since this is the reference to the waveform DAC, its inverse, also 4V p-p (4.3Vp-p for Rev 2) appears at TP9. Due to the low frequency of this signal and the AC coupling between the waveform DAC, filter, and VCA stages nothing very meaningful comes out at TP5 or 6 so this test is not appropriate to be performed on a complete CMI with the Analogue Tester box. Terminate test and advance to the next by hitting the space bar.

6. DIAGNOSTIC SOFTWARE (continued)

Tests No.2 - "Ramp Preset, Sine Wvfm"
Purpose: Tests ability to preset the counters and drive the envelope-shaping DAC with output from TP5,6.

RAMP,N=1 is best for debugging the envelope shaping circuit and waveform DAC since a DC waveform is simplest. This tests the same hardware but generates an output at TP5,6 for final testing use.
Waveform memory is loaded with a sine wave and it is played at high (approx 2kHz) frequency. The envelope counters are cycled linearly from 0 to $FF and back at a rate determined by the speed option and a software delay loop. The counters are preset directly from the PIA at segment boundary crossings. The same 4Vp-p triangle appears at TP8 as was observed for RAMP,N=1 but the waveform at TP9 is a 100% triangle-modulated sine, 8Vp-p. At TP5 and 6 the same waveform appears with a magnitude of 4Vp-p.

Test No.3 - "Ramp Auto Run"
Purpose: The envelope of each segment may be ramped automatically by the up/down counters (E5, E6).

The ramping rate is controlled by timers 2 and 3 for even and odd segments respectively. The timers are clocked internally. LOAD is not asserted so that the clock to the counters (ECLK) bypasses the rate multiplier resulting in linear ramping. A clock pulse occurs as each timer times out and the counters increment or decrement according to the DIR output from the PIA (C6789). Timer 1 is set to a time long enough to ensure the envelope reaches the maximum or minimum. At the segment crossing after the timeout of timer 1, the ZCINT flag is generated. The software polls this flag and when it occurs, the DIR bit is switched to reverse the dirction of ramping.
All this happens while a sine wave is played so the result is a clipped triangle 4Vp-p at TP8 and a clipped triangle-modulated sine wave, 8Vp-p at TP9 and 4Vp-p at TP5,6.
When testing multiple cards it should be noted that the ZCINT flag of only one card is polled to control when DIR is switched. By default, the lowest number card installed is used but the user may overide this with the TEST option, e.g. RAMP,N=3,C=2-5,T=3 tests cards 2 to 5 using the flag of card 3 to control ramping direction changes.
Terminate test by hitting the space bar.

Test No.4 - "Force Ramp Up and Down"
Purpose: Checks ramp up/down override and exponential ramping in mode 4.

Ramp counters are allowed to ramp up and down as in test 3 but the DIR control is overridden by the Force Ramp Up (FRU) and Force Ramp Down (FRD) controls, which are asserted by accessing addresses $E003 and $E004 respectively. Also, LOAD is asserted so that the clock to the envelope counters comes from the rate multiplier whose inputs are the 4 m.s. envelope bits (IC E12). A sine wave is played so the result is an exponential ramping waveform, 4Vp-p at TP8 and an exponential-modulated sine 8Vp-p at TP9 and 4Vp-p at TP5,6.

Test No.5 - "Ramp Zero Offset"
Purpose: Checks noise or control feedthrough of waveform DAC.

Waveform memory is filled with audio zero (digital $80) then the envelope ramped up and down as in test 1. There should be negligible output (less than 20mV p-p) from the channel card at TP9.

6.2.6 Volume Control Tests

Test name: VOL
No. tests: 4
Purpose: Checks volume control DAC.
Options: F=n Filter cutoff harmonic
Range 1-127, default 8
S=n Volume change speed
Range 1-127, default 1

Test No. 1 - "Volume Triangle"

The volume control VCA (F9) and its control circuitry is the last stage in the audio processing system. The data latched into the volume DAC (IC 8F) is cycled repetitively between zero and $FF. The result is a triangle wave approximately 480mVp-p at TP11. Waveform memory is loaded with a sine wave and this is played at approximately 1kHz with envelope set to max ($FF). The result at TP5,6 is sine modulated by the exponential response of the VCA to a linear ramp (see diagram). The volume control filtering circuitry prevents the triangle from reaching its full level (the channel card is running and the FET override is off) so the maximum amplitude of the output at TP5,6 only reaches approximately 2.6Vp-p.
Terminate the test by hitting the space bar.

Test No.2 - "Zero Offset Test"
Purpose: This test checks the control feedthrough of the VCA.

Control feedthrough is a change on the output of th VCA caused by a change on the control voltage when the signal input is zero. Waveform memory is zeroed and a sawtooth waveform is generated by the volume control DAC (F8). Check that less than 20mV p-p output appears at TP6.
Terminate the test by pressing the space bar.

Test No.3 - "Smoothed Volume"
Purpose: Checks the volume control RC filter is working.

A low frequency square wave is generated by alternately latching 0 and $FF into the volume DAC F8. With RUN on, (FET off), this should be heavily filtered by R37 and C13 following the DAC's buffer. A 480mVp-p RC-type waveform should be observed at TP11. Again a sine wave is played which gets exponentially modulated at the VCA by this already exponential waveform. The result at TP5,6 is modulation which rises slowly and drops rapidly, approximately 3.6Vp-p (see diagram).

Test No.4 - "Unsmoothed Volume"
Purpose: Checks the FET bypass is operating.

The purpose of the FET bypass around the volume control voltage filter formed by R37 and C13 is to ensure fast attacks at the beginning of a sound if required. This is displayed by playing tone bursts.
With RUN off and R37 bypassed, the volume is stepped to $FF. A short delay (approximately 0.5mS) is allowed for C13 to charge through current limiting resistor R35 then the envelope is set to $FF and RUN asserted to play a full level sine wave. The tone burst is approximately 20mS then envelope is reset to zero, RUN turned off and volume stepped back to zero for another 20mS period before starting again. So to get a fast attack, the FET bypass must be active while the tone is not playing; in particular, for the 0.5mS between volume being set to $FF and RUN being asserted.
The control voltage at TP11 should be a 480mV p-p square wave with slightly rounded corners, and the tone burst at TP6 should be a neat rectangle.
It has been found that if a poor quality capacitor is used as C13, dialectric absorption of the step transient in the control voltage results in a fast attack followed by a dip in the envelope at TP6. The exponential response of the VCA means that a very tiny dip in the control voltage results in a quite marked dip in the envelope.

6.2.7 Timer Tests

Test name: TIM
No. tests: 3

Test No.1 - "Timer Read/Write Latches"
Purpose: Checks ability to communicate with timer.

The 6840 timer contains 3 16-bit timer counters and 3 associated preset latches. First all timers are held in preset state and outputs enabled by writing $81 to the internal control registers. Then timer 1 preset latch is written with all numbers from 0 to $FFFF and its associated timer read back for verification after each write. (In the preset state each counter reflects the contents of its preset latch). The other two timers are then tested in the same way.

Each write/read is a double-byte transfer through the 8-bit buss.

Test No.2 - "Timer Internal Clock Timeout"
Purpose: Checks timeout action using internal clock.

Timers are programmed to be decremented from the internal clock and are all initialised to $FFFF. Timeout occurs when a timer decrements to zero. All three timers should timeout together. A software timer is used as a reference to detect early or missed timeouts. The 6840 status register is repetitively polled to check when timeout occurs.

Test No.3 - "Timer External Clock Timeout"
Purpose: Checks timeout action using external clock.

Clock timeout is verified using the external clock inputs. Using the same reference as test No.2, all three timers should timeout simultaneously.

6.2.8 Pitch and Octave Control

Test name: PIT
No. tests: 2

Test No.1 - "Octave Register"
Purpose: Checks accuracy of the octave control PIA.

With the pitch register held at maximum, octave register is cycled from 0 to 8. At each setting, a timer is used to time a waveform by presetting a segment count appropriate to that octave and selecting the RUN mode. If timeout occurs before the End of Sound is reached or if the timer value is greater than a certain tolerance when the end is reached, an error is generated. The timer is clocked by the internal clock.

Test No.2 - "Pitch Register Test"
Purpose: Checks accuracy of pitch control from PIA.

With the octave register held constant, the 10-bit pitch register is cycled from zero to maximum and and the same method is used to verify the waveform accessing frequency as in test No.1.

6.2.9 Interrupt Flags

Test name: FLG
No. tests: 4

Test No.1 "End of Sound Flag"
Purpose: Test the "last segment" flag.

An end-of-sound interrupt is generated when the waveform address counters reach maximum. To test this, the segment count is preset to the last segment ($7F), and 127 writes to waveform memory are executed. On each write, premature end-of-sound is checked for. The 128th write should then produce the interrupt.

Test No.2 "Terminal Ramp Flag"
Purpose: Test "clipping" flag.

Generated by zero or max count being reached by ramp counters. With direction bit set to "down", $80 is written to the ramp preset register. The status is then read to check for no terminal ramp flag. Then zero is written to the ramp preset and read again to check that the terminal ramp flag is present.

The direction bit is then cleared (ramp up) and $7F and $FF written to the ramp preset to alternately clear and set the terminal ramp flag.

Test No.3 - "Zero Crossing Flag"
Purpose: Test "middle of segment" flag.

Generated at the middle of every segment by waveform address counter . The flag goes high when the within-segment byte count reaches 64. The test asserts LOAD to clears the counter then does 63 writes to waveform memory, checking each time that the flag is clear. One more write should then set the flag.

Test No.4 - "Zero Cross Interrupt Flag"
Purpose: Test "middle of last segment" flag.

Zero crossing interrupt occurs on first zero crossing after the segment timer timeout. The timer is programmed to be clocked by the internal clock. Until it times out, the zero-crossing interrupt is checked for no premature flag. After timeout the status is read again to check that the zero-crossing flag has occurred. The address counters are clocked at maximum pitch during the test.

6.3 Master Card Tests

The master card can be diagnosed using the program MAST.CM, run by typing

MAST<return>

with the CMI diagnostics disk in drive 0.
The standard command interpreter is used so the LIST ERRORS and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<return>

Some MAST tests require at least one channel card to be installed in the CMI. These are indicated by the presence of a C option in the descriptions below.

This section describes MAST Version 3.12

6.3.1.1 Timer Tests

Test name: TIM
No. tests: 3

Test No.1 "Master Timer Read/Write Latches"
Purpose: Check ability to communicate with timer.

The 3 timers in the 6840 timer are put into the preset state and all numbers from zero to $FFFF written to the timer 1 latch. Each write is followed by a timer read for verification. Timers 2 and 3 are then tested in the same way.

Each write/read is a double byte transfer through the 8-bit buss.

Test No.2 "Master Timer Internal Clock Timeout"
Purpose: Check timeout operation under internal clock.

The timers are clocked by the internal clock. All three timers are initialised to $FFFF then started. A software timing loop is used as reference, and the timer status is continually polled for premature timeout. Timeout must occur within a certain tolerance before or after reference timeout. Clock outputs are enabled during the tests.

Test No.3 "Master Timer External Clock Timeout"
Purpose: Check timeout operation under external clock.

Timers are programmed as follows:-
Timer 2 Internal clock
Continuous operation
Initialised to 1
Output enabled

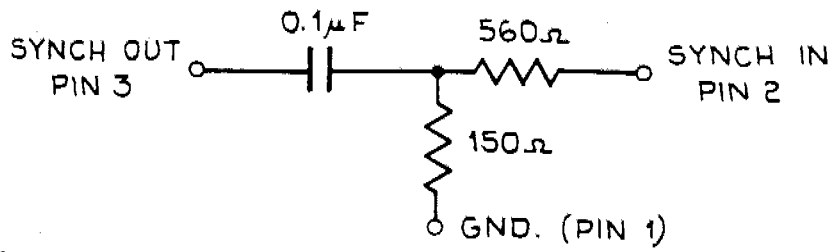
Timers 1 & 3 External clock (Timer 2 output)
Single shot
Initialised to $FFFF/2
Outputs enabled

The same reference is used to check that timers 1 and 3, being clocked by timer 2, times within tolerance.

6.3.1.2 Click Out/Sync In Tests

Test Name: "Sync"
No. tests: 2

Both require Sync In to be connected to Click Out via an attenuator/filter circuit in order to load the output. The circuit is illustrated below.



Sync Test Plug Circuit (3-pin Cannon)

Test No.1 "Click Out/Sync In 250Hz (Time)
Purpose: Checks click output and sync input circuits

The first test clocks the Synch In timer (timer 2) with a known frequency and checks its timeout against the software reference. During initialisation, timer 1 is checked to be working (i.e. that it can be made to time out). It is then programmed for internal clock, and preset to run continuously at 250Hz with its output enabled. Timer 2 receives the sync input pulses and times out in single shot mode after 100 clocks (about 400mS). This timeout is verified against the software timer. Timer 3 is not used.

Test No.2 "Click Out/Sync In 1KHz (Count)
Purpose: Checks click output and sync input circuits

The second test sends a fixed number of pulses from timer 1 to timer 2 and checks that timer 2 receives the correct number. Timer 1 is set to internal clock and runs at 1000Hz. Timer 2 is initialised to $FFFF. The status register is polled for timer 1 timeouts and it is stoppped after 3000. Then timer 2's counter is read to check that it decremented to the correct number.

6.3.2 Master Pitch Register Test

Test name: PIT
No. tests: 1

Test No.1 "Master Pitch Register Test"
Purpose: Check for presence and accuracy of the master pitch reference signal MOSC.

This test requires a working channel card to be installed in the channel 1 slot. Each of the master pitch rate multipliers are tested separately by timing a number of segments and comparing it to a fixed value. The channel card is set at a fixed pitch, then the master pitch is preset through the master pitch register, starting with the lowest pitch. Timer 3 on the channel card is used to time the segments. The end-of-sound flag is cleared on the channel card then RUN mode selected and the timer started. The channel status is polled for the arrival of the end-of-sound and if it arrives outside a set tolerance from the timer 3 timeout, an error is generated.

This cycle is repeated for all master pitch settings.

6.3.3 A-D Converter System Tests

6.3.3.1 AD Tests using External Analog Source

These tests are designed for complete CMI's being tested with the Analog Tester Box.

Test name: AD
No. tests: 2
Purpose: Software check of A-D convertor system using a known analog input.
Options: C=n Channel no.
Range 1-8, default 1
Channel 1 is always used, others may be specified.

Test No.1 "Analog to Digital Convertor 20.1kHz"

The Fairlight Analog Tester box provides a triangle wave of 10V p-p at 30Hz as a known input to the master card for sampling via the ADC switch on the back panel. The switch should be set to EXT ADC. Note that this switch setting bypasses the master bandpass filter so that the filter is eliminated as a source of AD conversion problems. Some cable rearrangements are required to use the tester:

(1) Keyboard Power cable, normally connected from the CMI to the Music Keyboard, should go to the analog tester.
(2) Alphanumeric keyboard, normally connected to the Music keyboard, should be connected directly to the CMI rear panel.

The analog tester brings out both sides of the balanced outputs from the channel cards. With the oscilloscope set on 1V/div, add CH1 and CH2 and trigger on CH1. Set the tester switches to SYNC and NORMAL.

The analog input is a triangle of a set frequency such that at the given sample rate (20.1kHz) the difference in consecutive samples is 0 or 1. The sample rate is initialised by loading a pitch into the pitch register of channel 1. This generates the buss signal ADCLK which is gated through to the AD571.

A maximum allowable number of zero differences and a small number of "jumps of two" allowed are specified in the software. Non-zero differences should all be in the same direction for a rising or falling waveform.

Channel 1 and any other specified channels are set up to receive the converted data. Sampling starts, but no samples are recorded in waveform memory until a zero byte is read, which must occur within a set timeout period (software timeout, doesn't use 6840 timer). Once a sufficient number of samples have been made and stored in channel 1 (& others if specified), sampling is stopped and the data in channel 1 read to check for a continuous rising ramp followed by a continuous falling one. Each sample in the falling ramp is complemented first and then checked as if it were a rising ramp.

Test No.2 "Analog to Digital Converter 30.2kHz"

This test is identical to test No. 1 except that a 30.2kHz sampling rate is used.

Error reports

If an error is occurs, a message is printed containing the error identification number, a description of the error, and an offset indicating the address in the channel card memory where the error was detected. Some different error IDs give the same descriptive message and require further explanation:

Error #3 - "Difference too small"
Too many successive samples were identical. Test N=1 allows only one repeated value, while N=2 allows two.

Error #6 - "Difference too large"
The difference between two sucessive samples was 2 or more. The comparison of samples is unsigned so this message may also be generated when the difference is -1 (or any negative quantity), that is, when the ramp reverses its current direction for one or more samples.

Error #7 - "Difference too large"
Too many jumps of two were detected over the whole ramp. Test N=1 allows up to 10 jumps of two but N=2 does not allow any.

```
Test name: ADCHK
No. tests: 2
Purpose:   AD conversion test for debugging.
Options:   C=n     Channel number
                   Range=1-8, default 1 (always used)
           R=n     Audtype
                   Range 0-2, default 0

Test No.1  "AD Run Continuous 16kHz"
Test No.2  "AD Run Continuous 30.2kHz"
```

These tests are the same as the AD tests except that sampling continues indefinitely to assist in debugging problems discovered by AD.

```
Test Name: DI
No. tests: 1
Purpose:   AD conversion display.
Options:   C=n     Channel no.
                   Range 1-8, default 1
```

Test No.1 "Display Routine"

This simply sets up the specified channel to play back the sampled waveform last recorded by AD or ADCHK. Monitor it at TP6 or the mixed output. It should be a low frequency triangle. It is not necessary to do this except for debugging purposes as the software checks for the correct sampled data itself.

```
Test Name: DUMP
No. tests: 1
Purpose:   For close examination of sampled data
Options:   C=n     Channel no.
                   Range 1-8, default 1
           S=n     Segment no.
                   Range 0-127, default 0
```

The contents of the specified channel and segment are printed on the screen in hexadecimal. Divide the offset printed by the error report by 128 to calculate which segment to display.

This is the same DUMP routine as used in the channel card tests CMITST to examine channel memory faults. See Section 6.2.2.

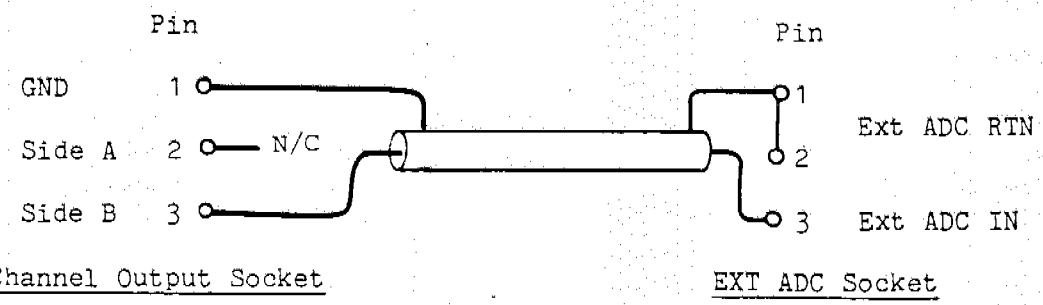
6.3.3.2 AD Tests Using Internal Analog Source

These tests are designed to check the analog to digital converter where a complete CMI is being tested without using the Analog Tester box.

```
Test Name: ADI
No. tests: 4
Purpose:   Tests A-D conversion system using a known analog input, generated
           from one of the channel cards.
Options:   C=n     Channel no.
                   Range 1-8, default 1
                   (Channel 1 always used, plus others
                   as specified).
           R=n     Audio board type
                   Range 0-2, default 0
```

```
Test No.1 "Analog to Digital Convertor 16kHz"
Test No.2 "Analog to Digital Convertor 30.2kHz"
Test No.3 "Analog to Digital Convertor 16kHz"
Test No.4 "Analog to Digital Convertor 30.2kHz"
```

Channel 1 must be available to provide the AD conversion clock to the master card. The other channels specified (or channel 1 by default) are loaded with a two-segment triangle wave to simulate the test waveform provided by the Analog Tester in the AD test. If testing a complete CMI, connect the output of the channel to be used as the analog source to the EXT ADC input as below and set the ADC selector to EXT ADC (this bypasses the master bandpass filter).



1) This is a self-test of the A/D converter on the master-card, using a ramp output from any channel in the range 2-8 (CH1 is used to provide the ADCLK signal, the pitch set in the pitch register of CH1 controlling the frequency of ADCLK and hence the A/D sample frequency).

2) The specified signal source channel (CH<opt>) is loaded with a monotonic ramp waveform occupying two segments of waveform memory (256 bytes) and then turned on.

3) The signal from the channel output is fed via the cable to the AD input, and the AD conversion routine writes the digital data to a 256 byte buffer in program memory.

4) The 256K sample saved in this program buffer is then checked to see if it is vaguely ramplike and down-going (N.B. don't use TP6, as this will give an up-going ramp). If this check fails, then a message is displayed: **DATA NOT RAMP,CHECK CABLE CONNECTION.**

5) **ADI,N=1** and **ADI,N=2** test the ADC at 16KHz and 30.2KHz respectively. Although in an ideal case the sample captured by the ADC should have no zero jumps or jumps of two,(as the input signal has been adjusted to have the same slew rate (dV/dT) as the ADC at that particular frequency), a few of these anomalies must be allowed because of system 'jitter'.
The T (2-jump) and Z (0-jump) options are provided and must be set at such a level that good ADCs are passed and bad ones failed. This is left to the experience of the test engineer to select, as T and Z limits will be different according to the characteristics of the channel-card producing the signal. (The main difference being between old type and new type channel-cards).

6) **ADI,N=3** and **ADI,N=4** again are the same test at 16KHz and 30.2KHz respectively. These tests perform 128 passes of the ADC test, with T and Z set to such high values that no vaguely working ADC will be rejected. (Bad faults, such as missed codes, two 0-jumps in a row, or jumps of 3 will still be reported as errors!) Data from the 128 iterations of the test is then displayed. The average no. of 0-jumps and 2-jumps per iteration are given, as is the no. of 0-jumps and 2-jumps for the worst case encountered.

These tests can be used to calibrate the T and Z options used in the previous two tests, provided a known good master card is used as a standard.

Test Name: DBI
No. Tests: 1
Purpose: Close examination of sampled data.

Test No.1 "Display Contents of Buffer"

Half of the contents of the 256-byte buffer in RAM, representing one side of the sampled waveform are printed on the screen.

Test Name: DII
No. Tests: 1
Purpose: Replay sampled waveform
OPtions: C=n Channel no.
Range 1-8, default 1

Test No.1 "Display Routine"

The contents of the RAM buffer are moved to the specified channel card memory and the channel set running until <CNTRL-ESC> is typed. Monitor the waveform at TP6. It should be a low frequency triangle.

This test allows a quicker check of sampled data than DBI. Both display routines are only necessary for debugging as the ADI test itself checks if sampled data is correct.

Test Name: JAM
No. tests: 2

Test No.1 "P2 Jam and Unjam"
Purpose: Checks correct functioning of the processor 2 HALT circuit used by AD conversions.

The ADM signal from PIA DE5 is asserted so that the AD571 (IC D7) is clocked by DLE every time the low order converted byte is read. The two processors execute synchronised code using some common data:

P1STD = flag to indicate processor 1 has started its part of the test code
CNT = counter which allows processor 1 to monitor processor 2's activity

The test proceeds as follows ...

Processor 1	Processor 2
	Initialises and clears halt flag by accessing UNJAM Starts P1 Goes into loop which checks P1STD. If P1 doesn't start within timeout, generates error and exits
Sets P1STD Short delay	Clears CNT Goes into loop incrementing CNT stays there until P1STD is cleared again
Halts P2 (JAM) Reads CNT Short delay Reads CNT again - if it has changed, P2 hasn't stopped Starts P2 (UNJAM) Short delay Reads CNT again - if it is the same P2 hasn't started again Clear P1STD	Tests error flags and terminates test

Test No.2 "P2 Jam Timeout"
Purpose: Tests the automatic processor 2 restart.

In the event of UNJAM never being accessed or a conversion never being completed, a hardware timeout is provided by one-shot D2 to restart P2. It must be possible to stop processor 2 for at least 200uS but no more than 1mS. The same common data is used as test No.1.

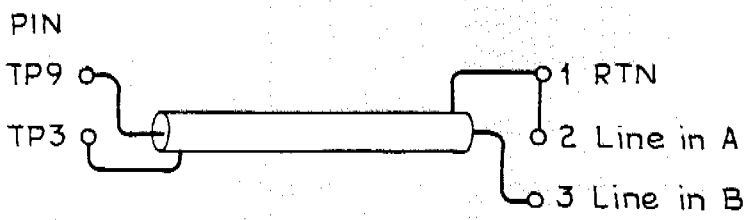
The test proceeds as follows:

Processor 1	Processor 2
	Initialises and clears halt flag by accessing UNJAM Starts P1 Goes into loop which checks P1STD. If P1 doesn't start within timeout, generates error and exits
Sets P1STD Short delay	Clears CNT Goes into loop incrementing CNT stays there until P1STD is cleared again
Halts P2 (JAM) Reads CNT Short delay Reads CNT again - if it is different, P2 hasn't stopped. Starts counting loop for up to 1mS, checking CNT to see if P2 has restarted automatically. If timeout, UNJAM to try to restart P2 else, check loop counter to ensure P2 was stopped at least 200uS.	
Clear P1STD	Tests error flags and terminates test

6.3.4 Master Bandpass Filter Tests

Test Name: FILT
No. tests: 17
Purpose: Check characteristics of A-D converter input filter.
Options: C=n Channel number
Range 1-8, default 8

The specified channel is set up to provide an analog test waveform. A special cable with a plug matching the row of channel card test pins is used to take signal from channel card TP9, the unfiltered analog output, to the LINE IN input of the audio board and thence to the master card Filter Input. Having made the connections as below, select LINE IN and INT ADC. Monitor the waveform at pin 3 of the SAMPLING FILTER OUT socket (pins 1 and 2 are GND) or TP10 of the master card.



CHANNEL CARD TEST POINTS LINE IN SOCKET

This test can also be performed using the Analog Tester box but the tester cannot gain access to the unfiltered channel output and uses the filtered output instead. This can indicate whether there is a major fault in the master filter but there is no point making accurate level measurements since the frequency responses of the channel card, master card, MIC or LINE input amplifiers and the tester itself are all superimposed. Set the tester to FILT OUT ONLY.

The filter settings have the following effect:

$X8-XF	LPF at minimum cutoff frequency
$X0	LPF at maximum cutoff frequency
$0X	HPF at maximum cutoff frequency
$8X-FX	HPF at minimum cutoff frequency

Tests 1 to 9 fix the HPF at minimum cutoff while ranging the LPF from maximum to minimum respectively (0-8). Tests 10-17 fix the LPF at maximum cutoff while ranging the HPF from minimum to maximum (7-0). Step through the tests using the space bar.

All tests fill 4 segments of the specified channel with a fundamental sine wave, followed by another 4 segments of the 3rd harmonic. Channel pitch is set for each filter setting to obtain a predetermined attenuation ratio between the two frequencies. Timer 1 of the channel is set to loop around the 8 segments continuously and they are played through the analog bandpass filter at maximum vol and ramp settings.

Refer to Section 6.9 for expected waveforms.

High-pass Filter 6dB Point

The 6dB point of the Master Filter at the lowest setting of the high-pass filter should occur at less than 20Hz. This can be tested by typing

FILT,N=9<return>

This sets the filter at $F8, which is the lowest setting of both high pass and low pass filters. Instead of using the channel card as analog input as above, connect a signal generator to the LINE IN socket (if single-ended, use side B, pin 3). Set input selector to LINE IN.

Monitor the master filter output at TP10 of the master card.
With a line input of about 2.6V p-p at 500Hz, the filter output should peak at 10V p-p. Adjust frequency downwards until the filter output is 6dB down, i.e. 5V p-p. This frequency should be less than 20Hz.

6.4 Q256 MEMORY CARD DIAGNOSTICS SOFTWARE

When testing system memory it is desirable to have as little memory space as possible taken up by the operating system and the memory test itself. In order to restrict the memory diagnostics within a 16K block, they are split into three separate programs: **MEM256**, **MAP256** and **DMA256**. The first performs bulk memory testing in 16K chunks and exercises the parity generation/checking system. MAP256 tests the full capability of the memory management system, except for the automatic DMA map selection, which is tested in DMA256.

A fourth program, MEMDBG is a small and simple program which exercises specific sections of the Q256 circuitry in very tight loops and thus generates the stable CRO traces needed to find circuit malfunctions. It is only appropriate to use MEMDBG once MEM256 or the other diagnostics have been used to obtain an approximate area of the fault. See Section 6.4.5.

The first three tests, MEM256, MAP256 and DMA256, are run in the same way. To run MEM256, for example, type

MEM256<return>

with the CMI diagnostics diskin the left hand drive.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in Sec. 6.1.2. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<return>

To understand the information below, three definitions are required:

Logical or Processor Space: is the numerical range of addresses actually put out on the processor address buss. The logical address may also come from a DMA device such as the Floppy or Hard Disk controllers, MIDI card or Waveform Processor.

Physical Space: is the area of RAM which is actually accessed in response to the logical address.

Mapping: is the translation of any given logical address to any physical address. The Q256 does this on 2K "pages". Data which is contiguous within a single page of logical space will be contiguous within a page of physical memory. However all the pages that are contiguous within logical space can be arbitrarily shuffled in physical memory without the processor being aware of this when running programs etc. Also, an area of physical memory can appear in zero, one, two or more different places in the logical space.

6.4.1 Common Initialization, Options and Test Procedures

The three test programs share common initialization and option selection routines, and use common move and mapping routines to test the area of memory occupied by the operating system and test program.

Initialization: When the test program is first entered, the PIA setup of the graphics card is read and saved, for later restoration after tests which change this setup.
When the user types a command, one or all of a group of tests with the same name are executed sequentially. Before each group is run, the error counter is zeroed. Before each individual test is executed, a standard test mapping is set up in map 28, then all system states are switched to map 28. The standard test mapping is as follows:

Processor Space	Physical Memory
0 - $7FFF	Blocks 0,1 (Block 0 includes QDOS and test prog)
$8000 - $FFFF	Deselected

At the end of each test or during an abort caused by errors, the graphics card PIA setup is restored to the state which was saved on program entry. Then a check for any parity errors which occured during testing is performed, and a message printed if an error is found. The operating system and test program are moved back to the bottom of physical memory if necessary, and QDOS mapping reinitialized. Lastly the disk driver routines are reloaded to the top of processor RAM space from the floppy disk controller ROM and hard disk controller ROM if installed. The reloading of disk drivers is necessary because they are not part of the protected operating system and may have been overwritten by the memory tests.

Options: A number of options which apply to all tests can be set using the SEL command, rather than having to specify them each time a command is typed. To obtain a display of current option settings just type

SEL<return>

To change an option, type

SEL,<option>=n where n is a number.

The options available are -

	Range	Default
C - Card select.	0-15	0
B - Block(s) select.	0-15	0-15.
E - Error limit.	0-127	0
D - Display	0-1	0
V - Video ouput	0-1	1
L - Line printer output	0-1	0

The Card select option allows multiple boards to be tested. This is useful in testing a board which is not working sufficiently to be able to load the operating system and test diagnostics. The default of zero tests the system card. Note that although the test can handle up to 16 cards, the standard CMI motherboard has only two Q256 slots.
Each card contains 256K bytes of memory consisting of four columns of 64K chips. The memory management hardware divides the 256K physical space into 128 pages of 2K each, but the bulk memory tests deal with sixteen blocks of 16K each (each 16K block therefore consists of 8 2K pages). The B option allows selection of which blocks are to be tested. The default option tests all blocks, from block F (15) downwards, which means the operating system block (Block 0) gets tested last.
The error limit determines how many errors can be logged before the test aborts. The display option enables the printing of each card and block number as it is tested. Since several of the tests take a fairly long time to execute, particularly in a multi-card test rig, this option reassures the operator that the test is still running and has not crashed due to errors in the system memory.
The video option allows the above display to be printed on the system video console, while the L option prints it on a line printer if this is connected to the back panel of the CMI.

Error Messages

For most tests, if an error occurs a common error message routine is called which indicates where in memory the error occurred, the data which was expected, and the data which was actually read. It then reads the error location again. If on the second read the data is correct, the error is indicated as "SOFT". If it is still wrong and the same as it was the first time, it is indicated as "HARD". If the second read is wrong but different from the first read, the error is "RANDOM".

Testing Physical Block 0

The operating system (OS) normally resides in the bottom 16K of both logical and physical space, within processor addresses 0 to $3FFF. All testing takes place in the processor address range $4000 to $7FFF. When Block 0 is to be tested, the OS must be moved to a different block. The new block is first mapped into the address range $4000 to $7FFF then Block 0, residing in 0 to $3FFF is copied up to the new block. This moves QDOS, the test program, and Processor 2's stack into the new block. Processor 1's stack is in separate RAM on the Q133 and so is not affected by the Q256 diagnostics. At this point two copies of the OS exist, with P2 actually executing the one in Block 0. The new block is mapped into the address range 0-$3FFF so that now P2 is executing the new copy. Block 0 is then free to be mapped by the normal mapping routine into the $4000-$7FFF address range for testing. When the test on Block 0 is complete, the OS is again copied into $4000-$7FFF, then Block 0 is mapped back into 0-$3FFFF.

6.4.2 MEM256

This section describes MEM256 V1.5.
MEM256 performs the bulk memory data and addressing tests, refresh and parity system tests.

Test name: 29
No. tests: 8
Purpose: Checks both processors' abilities to write rapidly varying data throughout memory.

In each test, the SELected blocks are mapped one at a time into $4000 to $7FFF and a semi-random data sequence written by either or both processors in an order as specified below. Each processor then checks its own data.

Test no.1: "P1 ODD UP, P2 EVEN UP"
P1 writes to all odd locations starting from $4001 and proceeds upwards, while P2 writes to even locations starting from $4000 and proceeds upwards.

Test no.2: "P1 ODD DOWN, P2 EVEN UP"
P1 writes to all odd locations starting from $7FFF and proceeds downwards, while P2 writes to even locations starting from $4000 and proceeds upwards.

Test no.3: "P1 ODD DOWN, P2 EVEN DOWN"
P1 writes to all odd locations starting from $7FFF and proceeds upwards, while P2 writes to even locations starting from $7FFE and proceeds downwards.

Test no.4: "P1 ODD UP, P2 EVEN DOWN"
P1 writes to all odd locations starting from $4001 and proceeds upwards, while P2 writes to even locations starting from $7FFE and proceeds downwards.

Test no.5: "P1 ODD, P2 EVEN"
P1 writes to all odd locations starting at $4001 then $7FFF and proceeds by writing alternately to bottom and top of memory working in towards the middle. P2 writes to even locations starting from $4000 and $7FFE and proceeds in a similar fashion towards the middle. The verify phase starts from the middle and works outwards.

Test no.6: "P1 EVEN, P2 ODD"
P1 writes to all even locations starting at $4000 then $7FFE and proceeds by writing alternately to bottom and top of memory, working in towards the middle. P2 writes to odd locations starting from $4001 and $7FFF and proceeds in a similar fashion towards the middle. The verify phase starts from the middle and works outwards.

Test no.7: "P1 ALL"
P1 writes to all locations starting at $4000 then $7FFF and proceeds by writing alternately to bottom and top of memory working in towards the middle. The verify phase starts from the middle and works outwards. P2 executes a dummy routine.

Test no.8: "P2 ALL"
P2 writes to all locations starting at $4000 then $7FFF and proceeds by writing alternately to bottom and top of memory working in towards the middle. The verify phase starts from the middle and works outwards. P1 executes a dummy routine.

Test name: WA
No. tests: 2
Purpose: Checks for addressing errors.

Test No.1: "WALKING ADDRESS P1"
Test No.2: "WALKING ADDRESS P2"
The test block is first filled with random data. Then each even/odd pair of bytes is written with the address of the even byte (e.g. $4000 is written to $4000,$4001). Each byte of data is verified immediately after it is written, and when the block has been filled, all data is verified again in read-only pass.
In test No. 1, P1 performs the test, while P2 executes a dummy, and vice-versa for test No. 2.

Test name: REF
No. tests: 4
Purpose: Checks that dynamic memory refresh is working.
Options: T=n Time option
Range 1-100, default 5
O=n Operating system block
Range 0-3, default 0

Test No.1 "REFRESH"
P2 fills all the test blocks except the OS block with $50 plus the block number, then executes a delay loop for T seconds. It then checks the data in each block. If refresh is not working, the default delay of 5 seconds is ample for the memory contents to largely decay away. P1 executes the same delay loop but does no testing.

Test No.2 "REFRESH WITH TAS, P2 ONLY"
P2 fills all the test blocks except the OS block with $50 plus the block number, then executes a delay loop for T seconds, exercising the CPU card indivisible instruction hardware while it waits. It then checks the data in each block. P1 executes the dummy wait loop and does no testing.

Test No.3 "REFRESH WITH TAS, P1 ONLY"
This is the same as test no.2, with the processors swapped.

Test No.4 "REFRESH WITH TAS, BOTH CPUS"
P2 fills all the test blocks except the OS block with $50 plus the block number. P1 and P2 then both execute a delay loop for T seconds, exercising the CPU card indivisible instruction hardware while they wait. P2 then checks the data in each block.

Test Name: PARITY
No. tests: 2
Purpose: Verifies operation of the parity checking system.
Options: D=n Data used in test
Range 0-255, defaults 170, 168
respectively.

Test No.1: "PARITY SYSTEM - EVEN"
Test No.2: "PARITY SYSTEM - ODD"
These tests use the special parity error generation hardware on the Q256 card to predictably generate a parity error. Test no. 1 uses data with even parity (170=$AA), and test no. 2 uses data with odd parity (168=$A8).
Only P2 runs the test. Initially it is in the A, or system state and map 28 is selected. Map 29 is configured with the same standard test mapping (see 6.4.1) then P2 B state is allocated to map 29 with the Parity Error Generate (PERGEN) bit set. Then on each test block, a quick fill (every 128th byte) of the test data as indicated by the D option is performed, followed by a special quick verify with parity error generation. For each verify, the parity register of the current test card is first read to check for any prior errors which should not be there yet. Then the CPU fuse register is set up to switch to the B state, just as the test data byte is read. Since the byte was written in the A state with PERGEN not set (as is normal), and is read back in the B state with PERGEN set, a parity "error" should be generated at the moment of reading. We then switch back to the A state and interrogate the current test card's parity status register to check the presence of the parity error flag, the correct physical 64K rank number, and correct upper 5 bits of the processor address at which the "error" occured. The register is then read again to check that the first status read automatically cleared the error.

6.4.3 MAP256

This section describes MAP256 V1.6

Test name: MAP
No. tests: 15
Purpose: Tests the mapping functions of the Q256.

Test no. 1 "PAGE UNIQUENESS - P2"
Test no. 2 "PAGE UNIQUENESS - P1"
Options: O=n1,n2...n4 OSBLK: Operating system block
Range 0-3, default 0-3
(4 options)

These tests check that each 2K physical page (there are 128 on each Q256) can be accessed uniquely. The general approach is to write each page with its own page number, and then verify them all to ensure no page overwrote another. Getting around the operating system complicates things slightly.
The test is actually run four times. According to the default OSBLK option it is first run with the OS in Block 0 (no moving required). Block 0 occupies pages 0 to 7 so pages 8 to 127 are mapped into $4000 to $7FFF in groups of 8 and "quick-filled" (every 128th byte) with the page number. Pages 8 to 127 are then quick checked to still contain their page numbers. Then the OS is moved to the second OSBLK option, Block 1, which occupies pages 8 to 15, so pages 0-7 and 16-127 may be tested with filling and verifying page numbers. Similarly the OS is moved to Block 2 while testing pages 0-15 and 24-127 and finally the OS is moved to Block 3 while testing pages 0-23 and 32-127. Which blocks are used for the OS and in what order may be changed using the O option.
Processor 2 executes test no.1, and P1 runs test no. 2; the procedure is the same for both.

Test no. 3 "P2 MAPPING, P1 TAS"
Test no. 4 "P1 MAPPING, P2 TAS"

This test ensures that the indivisible instruction hardware on the CPU card can be rapidly accessed simultaneously with mapping operations on the Q256. The MAPPING processor (P2 in test 3, P1 in test 4) follows the same procedure as in the page uniqueness tests 1 and 2. Again the test is run four times with the OS in one block while all other physical pages are filled and verified with page numbers. Meanwhile, the other processor loops around quickly doing two Test-And-Set instructions followed by two Clear instructions on a flag byte in memory. The flag byte is not used for any other purpose. The TAS processor continues testing and doing IO services until another flag is set by the MAPPING processor to indicate it has finished.

6. DIAGNOSTIC SOFTWARE (continued)

Test No. 5 "PROCESSOR UNIQUENESS"

The capability of the two processors to be mapped independently is tested by selecting different blocks in 2 different maps and running tests with different data on both processors simultaneously. The test is run once for each card under test. P1 is left as initialized in map 28, and Block 1 of the test card is mapped into $4000-$7FFF. P2 is switched to map 29 and Block 2 of the test card is mapped into P2's $4000-$7FFF. P1 then fills its test area with $AA while P2 fills its area with $55. The two processors then verify their own areas to contain the correct data.

Test No. 6 "FAST MAPPING - P2"
Test No. 7 "FAST MAPPING - P1"

These tests ensure that rapid writing to the mapram does not interfere with normal memory accesses. One processor loops over all test blocks (as selected by the SEL command) writing to all locations starting at $4000 then $7FFF and proceeding by writing alternately semi-random data to bottom and top of memory working in towards the middle. The verify phase starts from the middle and works outwards. (This is the same as the ALL tests in MEM256,N=7,8).
Meanwhile the other processor switches to map 29 and rapidly maps blocks in and out of $4000-$7FFF. All blocks except the current OS block and the block being tested by the first processor are mapped into $4000-$7FFF and quick-filled (every 128th byte) with zeros. After the last block, a flag is set to tell the first processor to stop testing.
In test no. 6, P2 does the fast mapping while P1 tests memory, and vice-versa for test no. 7.

Test No. 8 "SELECT ALL MAPS - P1"
Test No. 9 "SELECT ALL MAPS - P2"

32 different mappings may be set up in the Q256 mapram. Each map from 0 to 31 is initialised with Block 0 containing the OS mapped into 0-$3FFF and a different physical page mapped into logical page 8. (Physical page 8 is used in map 0, page 9 in map 1,... page 39 in map 31). After each initialization the processor switches to that map, and fills logical page 8 with the map number. We then start again at map 0 and verify that its logical page 0 contains zero, and repeat through to map 31.
P1 runs the test in no. 8, P2 runs no. 9.

Test No.10 "A/B SELECT - P2"
Test No.11 "A/B SELECT - P1"

The Q256 allows for different mappings to be selected depending on whether the processor is in the A (System) or B (User) state. Map 29 is initialised with the standard test mapping and the B state is allocated map 29. Then the following procedure is repeated on each test card: starting in A state, Block 1 of the test card is mapped for all states into $4000-$7FFF (call this area K1) and filled with $AA. Block 2 is then mapped for all states into K1 and filled with $BB. Next Block 1 is mapped to K1 for A states only, and Block 2 is mapped to K1 for B states only. Still in the A state, K1 is verified to contain all $AAs. Then the processor switches to the B state and verifies K1 to contain all $BBs. Thus far it is proven possible to read from different areas of physical memory in the two processor states.
The second stage of the test switches back to the A state and fills K1 with $11. Then the processor switches to the B state again and fills K1 with $22. Still in the B state, Block 1 is mapped into K1 for all states and checked to still contain $11 then Block 2 is mapped into K1 for all states and checked to contain $22. This proves that data written while in the A or B state can be directed to different areas of memory. The processor switches back to the A state for the next card to be tested or to exit the test.
P2 runs test no. 10; P1 runs test no. 11.

Test No.12 "PERIPHERAL DISABLE - P1"
Test No.13 "PERIPHERAL DISABLE - P2"

These tests check the peripheral enable output from card 0 which allows the peripherals (i.e. everything on the bus except the RAM card itself) which usually reside above $E000 in the processors' logical address space, to be disabled and replaced by extra RAM. The Q256 mapping system is itself a peripheral - the mapram lives from $F000-$F7FF (one logical page) so this test works by trying to change the mapping when peripherals are disabled.
Map 29 is initialised with the standard mapping and the B state is allocated map 29 with peripherals disabled. Then for each test card the following procedure is followed:
Still in the A state (and map 28) physical pages 8 and 9 are mapped to logical pages 8 and 9 respectively. Page 8 is filled with $AA and Page 9 is filled with $55. Then for map 29, physical page 9 is mapped to both logical page 9 and logical page 30 i.e. to the same logical area as the mapram. From the B state, reading the mapram area would now get all $55s.
We switch to the B state and attempt to map logical page 9 to physical page 8 in map 29 (the B map). With peripherals disabled, this should not work, and logical page 9 is verified to still contain $55.

If all is well so far, the Peripheral Enable probably works, so we attempt to completely clobber the mapram by filling it with $AA from the B state. Since peripherals are disabled in the B state, this should merely write to physical page 9 without changing any mapping. Logical page 30 is verified to contain $AA, then we switch back to the A state and verify logical pages 8 and 9 as both containing $AA. (Since peripherals are disabled, the last state switch can not be achieved by writing to the processor card control latch - a dummy software interrupt is called instead. The A state is automatically selected on interrupts.)
P1 runs test no. 12; P2 runs test no. 13.

N.B. - Only Card 0 is effectively tested by this test because it is the only card whose Peripheral Enable output pin is connected on the motherboard to its own and all other RAM card's PENB inputs.

Note also that if an error occurs while testing in the B state, the A state must be reselected in order to print the error message. The standard error message routine re-reads the incorrect location to ascertain what kind of error has ocurred, and since the mapping has changed it will no longer be reading the correct physical location. Thus errors which are in fact "Hard" will be indicated as "Soft", or possibly "Random".

```
Test No. 14 "GRAPHICS RAM DISABLE - P1"
Test No. 15 "GRAPHICS RAM DISABLE - P2"
Option:  R=n
                    Range 0-1, default 0
```

Checks VRAMEN output from the memory management system which allows the 16K of dedicated RAM on the Q219 graphics card to be mapped in or out of either processor's address space.
The video graphics RAM (VRAM), if enabled, occupies the address range $8000 to $BFFF. The contents of VRAM are copied down to $4000 to $7FFF to be saved while testing takes place. Then VRAM is checked to be working by filling with $AA and verifying (the $AA pattern appears on the console screen). Map 29 is initialised with the standard mapping and the processor switches to map 29 with graphics access disabled. It attempts to clear VRAM then reselects map 28 with graphics enabled to verify $AA is still there. Finally the saved contents of the screen are copied back.
P1 runs test no. 14; P2 runs test no. 15. Normally only one processor has access to the VRAM and this is selected through the PIA control on the Q219 at system start-up and by some application programs. Both tests 14 and 15 can run because the PIA set-up is saved on entry to MAP256 and restored at the end of each test. The tests also run on the old graphics cards Q218 and Q045 but in the latter case, which processor has graphics card access is hardware selected, so one of the tests will exit without testing.
N.B. - Only Card 0 is effectively tested by this test because it is the only card whose VRAM Enable output pin is connected on the motherboard to the graphics card.

6.4.4 DMA256

This section describes DMA256 V1.6

Test Name: DMA
No. tests: 2

Test no.1 "P2 DMA MAP SWITCHING"
Test no.2 "P2 DMA/P1 UNIQUENESS"

DMA256 tests the automatic selection of special DMA mappings via the DMA claim lines which are input to the Q256 memory cards from all devices on the bus which use DMA (Floppy Disk Controller, Hard Disk Controller, General Interface card).

P2 initializes map 29 with Block 2 of the test card mapped into K1 (logical area $4000 to $7FFF) as a 16K DMA buffer, and switches into map 29 to fill the buffer with its own page numbers. Then P2 switches back to the standard map 28 which has Block 1 mapped into K1 and fills it with a semi-random sequence. A disk operation is then initiated which writes the DMA buffer out to disk and into a file called DMAFILE.TF. Map 29 is selected again and the DMA buffer cleared. P2 switches back to map 28 and starts a second DMA operation, this time reading the buffer in from disk. K1 in map 28 is checked first to be still containing the random sequence, then map 29 is selected to verify the page numbers read in from disk. The procedure is repeated for all test cards.

In test no. 1, only P2 runs the test. In test no. 2, P2 runs the same test while P1 continually random fills and checks its own separate block (Block 4 of the test card) in the same logical test area using map 27.

The test file DMAFILE.TF is not deleted at the end of the test so that in the event of errors, the file may be examined using the QDOS command DUMP (this is not the same as the Channel Card diagnostic DUMP command!). It is not required to exist before the DMA test runs, so the user may delete the file at any time.

6.4.5 MEMDBG

The diagnostic programs MEM256, MAP256 and DMA256 provide the comprehensive tests which thoroughly check the Q256 256K Ram card operation. However the size and complexity of these diagnostics mean that they are not very easy to use for chip-level debugging of known faulty boards. MEMDBG is small and simple program which exercises specific sections of the Q256 circuitry in very tight loops and thus generates the stable CRO traces needed to find circuit malfunctions. The absence of error checking means that the processor does not end up spending most of its time printing error messages. It is only appropriate to use MEMDBG once MEM256 or the other diagnostics have been used to obtain an approximate area of the fault.

6.4.5.1 Use of MEMDBG

To start MEMDBG, type

MEMDBG<return>

with a diagnostics disk containing MEMDBG.CM in the left hand drive. When the program is first entered, it calculates its own checksum in case memory faults have prevented a successful load. If the checksum is wrong, the program exits back to QDOS. This check can be overidden by typing

MEMDBG;-C<return>

to start the program.

The user is presented with a menu of tests indicating which parts of circuitry are exercised by each test. Simply type the number of the required test then answer the prompts for data such as which processor is to run the test, what data is to be used, what 16K memory block is to be written/read etc.

Once all data required for the test is obtained the test loop is entered immediately. The only thing left to do then watch the signals of interest behave as the test loop requires. In general it is best to connect the CRO before starting the program so that accidental shorts don't crash the system before you get to see anything. To keep the loops as tight as possible, there is no provision for terminating the test - just hit reset or console interrupt (NMI). The latter only works if P2 is running the test, and the front panel P2 NMI switch is enabled only. After a console interrupt the program may be re-entered from the monitor without reloading by typing

2000;G

A board which is unable to load the system and/or MEMDBG can only be debugged by optioning it as Card 1 and installing it along with a healthy board as Card 0. If the faulty board still crashes the system, disable the data driver using option W3 (see Q256 hardware documentation).

6.4.5.2 Adding Your Own Test Loops

The eight tests contained in the program should be sufficient to solve most problems on the Q256. However MEMDBG has been written such that debug technicians can easily add their own test loops tailor made to investigate particular curly problems if the need arises. To do this a disk containing the following files should be placed in the right hand drive:

MEMDBG.SA	Source file
MEMDBG.CF	Chain file for editting and assembling
QEQU.SA	QASAR system equates
MAC256.SA	Q256 mapping macros

6. DIAGNOSTIC SOFTWARE (continued)

A system disk containing the following files should be booted in the left hand drive:

RASM09.CM 6809 assembler
EDIT.CM Cyword editor
IO.CM or QIOPACK.CM QASAR IOpack required for editor.

A 6809 assembler manual will also be required.

The procedure for adding a new loop is contained in the chain file. Just type

CHAIN MEMDBG:1<return>

to start the process. The chain calls the editor followed by the assembler to generate a new MEMDBG.CM on drive 1. Options in the chain include:

C - generate an assembly listing in the console screen
P - print assembly listing on the line printer
L - save assembly listing as the file MEMDBG.AL:1

For example, type

CHAIN MEMDBG:1;C<return> to list to the console.

The program consists of three sections: A test executive, the menu, and the collection of test loops. Only the menu needs to be modified to include the new loop, which should be typed into the source file after the other loops. Refer to the fully commented source file for further information on its structure. After adding another test loop the version number and "last modified" message should be updated to distinguish the new program from old versions.
Once the program is modified, the checksum will no longer be correct. Use the -C option to run the program and get the checksum error message. The formula for calculating the new checksum i

new CHKSM = complement(old CHKSM - error CHKSM reported) + 1

Run the chain again and modify the CKSM byte to the new value.

6.5. Central Processor Control Module

Few diagnostics are available for testing this card (Q-133) since it is not possible to load the DOS and run a test without most of the card functioning correctly.

6.5.1 User Peripheral Interface Adapter

The user PIA is tested by the program DBTST.CM, which may be run by typing

DBTST<return>

with the CMI diagnostics disk in drive 0.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<return>

The PIA tests require a special test plug to be inserted in the user PIA socket (the one nearest the top of the board) which has the effect of connecting the A side of the PIA to the B side. Connections are as follows:

1 - 24, 2 - 25, 3 - 26,5 - 22, 6 - 21, 7 - 20,
8 - 19, 9 - 18, 10 - 17,11 - 16, 12 - 15.

Test Name: PIA
No. tests: 6

Test No.1 "PIA B/Send A/Receive"
Test No.2 "PIA A/Send B/Receive"
Purpose: With the test plug connecting the two sides of the PIA, A should be able to write to B and vice-versa.

Both tests check each side of the PIA individually first by defining the side as all bits inputs, changing them to outputs, then writing 0, $FF, $FE etc. down to 0 again to the data register and reading back to verify each write.

Test no. 1 then sets side A as all inputs and side B as all outputs and writes all values from 0 decrementing back to 0 to side B, AND reading from side A. Test no.2 does the same in the opposite direction.

Test No.3 "CB2/Send CA2/Receive -ve"
Test No.4 "CB2/Send CA2/Receive +ve"
Test No.5 "CA2/Send CB2/Receive -ve"
Test No.6 "CA2/Send CB2/Receive +ve"
Purpose: Interrupt inputs/control outputs check.

The signal specified by "Send CX2" is configured as a control output whose state is determined by CRB-3 in the PIA control register. The other signal is configured as an interrupt input which will set the interrupt flag in the control register on an edge whose direction is indicated by the "Receive +ve or -ve".

The transmit end is first set to the state which will allow the wrong transition to cause an interrupt, (i.e. if the interrupt receiver is +ve edge triggered, the transmit end is set high) and the flag is checked as clear. Then the transmit state is toggled and checked again as still clear. A second toggle should trigger the interrupt flag. The actual IRQ output is disabled during the test.

6.5.2 System Timer

Test Name: TIM
No. tests: 2

Test No.1 "System Timer Read/Write Latch"
Purpose: Check ability to communicate with timer.

The 3 timers in the 6840 timer are put into the preset state and all numbers from zero to $FFFF are written to the timer 1 latch Each write is followed by a timer read for verification. Timers 2 and 3 are tested in the same way. Each write/read is a double byte transfer through the 8-bit buss.

Test No.2 "System Timer Internal Clock Timeout"
Purpose: Check timeout operation under internal clock.

The timers are clocked by the internal clock. All three timers are initialised to $FFFF then started. A software timing loop is used as reference, and the timer status is continually polled for premature timeout. Timeout must occur within a certain tolerance before or after reference timeout. Clock outputs are enabled during the tests.

6.5.3 Interrupts

Test Name: INT
No. tests: 1

Test No.1 "Interactive Interrupt Test"
Purpose: Test interrupts.

Enable interrupts, then display any which occur. Exit when <ESC> typed. Interrupts may be induced by user poking interrupt lines with an earthed probe.

6.5.4 Asynchronous Communications Interface Adapter

Test Name: ACIA
No. tests: 1

Test No.1 "Comms ACIA Send/Receive 19200 Baud"
Purpose: Tests asynchronous transmit/receive.

Checks that DCD and DSR status bits follow RTS, character is sent and received, interrupt flag set after character is sent, parity error and framing error. This test requires a 10-way loop back plug to be inserted.

Test Name: LATCH
No. tests: 1

Test No.1 "Comms Latchup Protect"
Purpose: Test if ACIA latched up (usually on power up).

Transmits a character and goes into a software timeout loop. Error message displayed if character not received.

6.6.1 LGTST

Use Light Pen/Graphics test, LGTST.CM by typing

LGTST<return>

with the CMI diagnostics disk in drive 0.

The standard command interpreter is used so the LIST and R commands, and P and N options are available as described in the general introduction. Tests are run by typing

<test name>[,<option1>,<option2>...,<optionN>]<return>

6.6.2 Light Pen Timers

Test name: TIM
No. tests: 4

Test No.1 "Light Pen Timer Read/Write Latches"
Purpose: 6840 timer preset latches can be written to and the counters read.

Timers are put into preset state in which the counters always reflect the contents of the preset latches. Then each timer is write/read tested with all numbers from 0 to $FFFF. Each write/read is a 16-bit transfer through the 8-bit buss.

Test No. 2 "Light Pen Timer Internal Clock Timeout"
Purpose: Correct timeout from timers under internal clock.

The internal clock is provided by the BCA signal. Timer outputs are enabled and latches preset to $FFFF. Then all three counters are released and their timeouts compared to a software status-polling (to sense timeout) timing reference loop.

Test No.3 "Light Pen Timer 2 External Clock"
Test No.4 "Light Pen Timer 3 External Clock"
Purpose: Timers under external clock.

Timer 2 counts frames, thus gets a 20mS clock cycle. The test is not synchronised to the frame pulses so a +/-10mS jitter is permissible. The timer is preset to count 200 clocks (4 secs), then released and compared to the software reference with the required tolerance.

Timer 3 is clocked by processor 2 phase 2 (1MHz). It is preset to $FFFF then released and its timeout compared to the software reference.

Both timers run in single shot mode with outputs enabled.

6.6.3 Light Pen PIA

Test name: PIA
No. tests: 1

Test No.1 "PIA Test"
Purpose: You've got 3 guesses.

Each side of the PIA is configured as all outputs then all numbers from zero backwards down to zero are written to the data latches and verified.

6.6.4 Processor Access Selection

"Test" name: SEL
Purpose: Allows user to specify which processor can access the video RAM.
Options C=n CPU selection
Range 1-2, default 2

Used for special purpose testing only. Not applicable to C.M.I which always uses processor 2 for VRAM operations.

6.6.5 Light Pen Drawing

Test name: LPEN
No. tests: 1

Test No.1 "Light Pen Drawing on Screen"
Purpose: Overall light pen operation, similar to CMILP.
Options: L=l Range 0-1, default 1
1 causes hit addresses to be written on the screen

S=s Range 0-1, default 1
0 inhibits resetting of the scroll reg.

With hit address writing enabled, the location of each hit is written on the bottom line of the screen, both as X,Y coordinates and as an address in video ram. The line number is given first (zero at the top) followed by two bytes representing the location of the hit on that line. The first byte should always be 0 or 1 and represents the least significant bit of the 9-bit location (512 dots per line). The second byte is the upper 8 bits of the location. The VRAM ADRS is the absolute address of the hit in video RAM and is followed by a byte indicating which bit of that address was hit.

6.6.6 Video RAM Testing

Test name: VRAM
No. tests: 8

Test No.1 "VRAM Processor"
Purpose: This determines which processor has access to the video RAM. To actually change processors, use the SEL command.

Test No.2 "Random VRAM Test"
Purpose: Random numbers are written to video RAM, then compared with original. Error if not the same.

Test No.3 "AA VRAM Test"
Purpose: Video RAM filled with hex number AA.

Test No.4 "55 VRAM Test"
Purpose: Video RAM filled with hex number 55.

Test No.5 "XY Byte/Inc"
Purpose: Test XY vector drawing hardware by writing random numbers and auto-incrementing. Numbers are then compared with actual video RAM contents.

Test No.6 "XY Byte/Dec"
Purpose: Same as XY/Inc except vector drawing hardware auto-decrements.

Test No.7 "XY Draw"
Purpose: Test the XY vector hardware.

This test draws a 2 byte wide by 16 byte high pattern into video RAM using the XY vector hardware, then checks that it was correctly drawn in the correct absolute locations in memory.

Test No.8 "Random XY, Byte Read"
Purpose: Video RAM is directly filled with random numbers. Random numbers are then regenerated and compared with video RAM via XY hardware.

6.7.1 Interrupt Tests - CMIINT

CMIINT.CM is a program for testing all the interrupt mechanisms in a complete CMI. It is run by typing

CMIINT<return>

with the CMI diagnostics disk in drive 0. It does not use the standard command interpreter but has its own commands to set up and run interrupt tests.

Each interrupt has a predetermined priority such that if two or more interrupts arrived since the last interrupt service, the one with the highest priority gets serviced first.

The "level" of an interrupt is a number indicating its priority such that the highest priority interrupts have a level of zero, and the others are arranged in ascending order of level for decreasing priority. The interrupts which may be tested by CMIINT, the part of the system from which they originate, their levels and the processor which services each one, are as follows:

Name	Origin	Level	Processor
CHANNEL 1	Channel 1 timer	12	1
CHANNEL 2	Channel 2 timer	8	1
CHANNEL 3	Channel 3 timer	13	1
CHANNEL 4	Channel 4 timer	9	1
CHANNEL 5	Channel 5 timer	14	1
CHANNEL 6	Channel 6 timer	10	1
CHANNEL 7	Chennel 7 timer	15	1
CHANNEL 8	Channel 8 timer	11	1
TIMER 1	Master Card timer	1	1
ACIA 1	CPU Control Card ACIA	0	1
TICKL 1	Interprocessor intrpt	2	1
TICKL 2	Interprocessor intrpt	2	2
TIMER 2	Light pen timer	1	2
DISK 1	Floppy disk controller	7	2
TIMER3	CPU Control Card	0	2
PERRINT	256K Memory	0	2
CPUIPI1	Processor	3	1
CPUIPI2	Processor	3	2
ADINT	Master Card A/D Conv.	6	2
AIC	Analog Interface	4	1

6.7.2 CMIINT Commands

RUN — Run tests on all active interrupts. Both sequential test (one interrupt at a time) and simultaneous test (triggered simultaneously, arrival checked for correct priority) will be run unless the SEQ or SIM commands have been used. See below. Run will be aborted if error count is exceeded or if the user hits CNTRL ESC (break).

REPEAT n — Sets the repeat count to n. The original value is printed. A repeat count of zero will continue indefinitely until aborted.

ERROR n — Sets maximum error count for RUN. Default is 1.

CMDS — Print a list of available commands.

LIST — List all interrupts and their statuses.

HELP — Print a summary of how to use the test

QU — Return to QDOS

+ <interrupt or function>
Activate an interrupt or function

- <interrupt or function>
Deactivate an interrupt or function

The interrupts which may be activated or deactivated using the + or - commands are as in the above list: just type "+" or "-" followed by the interrupt name. The "+" is always optional, and the name by itself will activate that interrupt or function. The functions which may be controlled in this way are:

P1	Testing of all processor 1 interrupts
P2	Testing of all processor 2 interrupts
ALL	(De)Activate all interrupts
LEVEL n	(De)Activate all interrupts of level n
SEQ	Sequential testing
SIM	Simultaneous testing
EMSG	Generation of error messages
DISPLAY	Listing of recorded interrupts on screen
WAIT	Wait after activation until NMI pressed for hardware check.

6.7.3 General Procedure of Tests

Initially, all interrupts are "active", i.e., will be tested upon typing the RUN command. Tests can be activated or deactivated using the commands above. Each test begins with the processor interrupt mask set so that interrupts currently pending are ignored. The status registers associated with each active interrupt is read in order to clear pending interrupts. These status registers generally contain a flag which indicates an interrupt has been generated and at this point the flag should be clear. All active interrupts are tested first sequentially (one at a time) then simultaneously. In the latter case, all active tests are "triggered" then the processor interrupt mask cleared.

A delay loop sufficiently long for all triggered interrupts to arrive is entered. The PICU's should continue to interrupt the processors with the currently highest interrupt pending until all have been serviced. A separate service routine is executed for each interrupt which records in a little block of data set aside for each one, its position in the sequence of interrupts when it actually arrived, whether that interrupt has been serviced before, and whether the interrupt flag in the associated status register is set. Then the flag is cleared.

At the completion of the delay loop the data blocks of each interrupt is checked to ensure the active ones arrived in the correct order and that no unexpected interrupts occurred.

6.7.4 Error Messages

If error reporting has not been suppressed by a "-EMSG" command, messages will be generated indicating the error type and the interrupt test which generated it. The types of errors detected are as follows:

(1) "High Priority Interrupt Occurred Too Late"
Generated when the interrupt just received has a priority level less than the maximum found so far.

(2) "Interrupt Late ? Due to Previous Error"

One or more interrupts may appear to be late when they actually occurred at the right time, but a previous high level (low priority) interrupt was too early and set an erroneously high current maximum level. The early low priority interrupt will not have been detected. This message is generated when the interrupt just received is consistent with the immediately preceeding interrupt (i.e. has a greater level) but has a lower level than the current maximum. Refer to the diagram on the following page for a clearer explanation of this problem.

(3) "Missing Interrupt"
An interrupt which was expected never arrived.

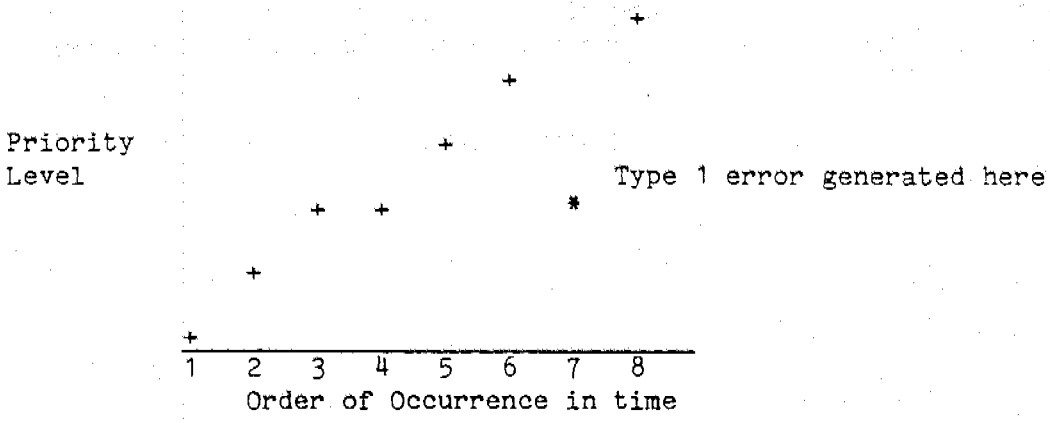
(4) "Multiple Interrupt"
An interrupt appeared to occur more than once. Usually caused by the interrupt not being cleared successfully by the service routine.

(5) "Unexpected Interrupt"
An inactive interrupt occurred.

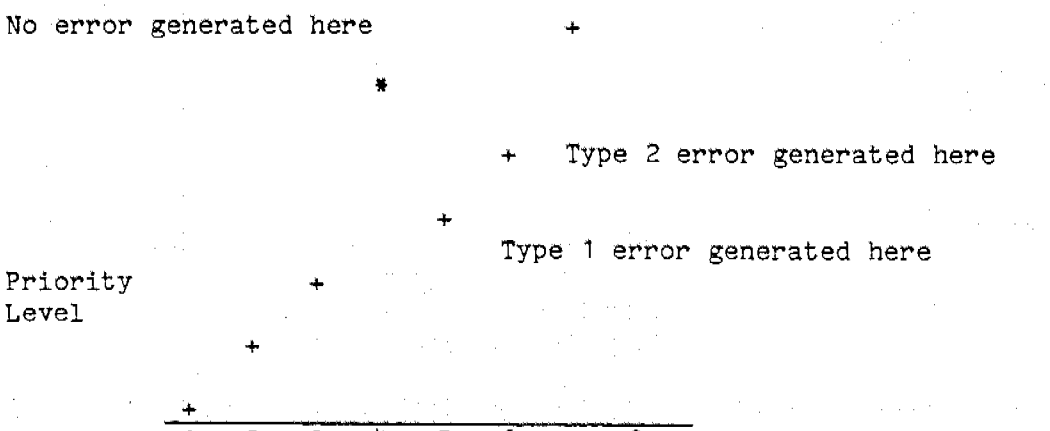
(6) "Flag Not Set"
The service routine found that its associated interrupt flag had not been raised.

6.7.5 Diagrammatic Representation of Interrupt Priority Errors

Key
\+ interrupt in correct order
* interrupt out of order



(1) Correct detection of a high priority interrupt arriving too late



(2) Incorrect error detection due to early low priority interrupt.

Early interrupt is not detected because it is the lowest priority interrupt received so far.

6.8.1 Testing a Complete CMI - Chain Tests

The CHAIN command is a facility which allows many tests such as those described above to be run with the minimum amount of human intervention. To run a series of tests, the command

CHAIN <filename><;options>

is used, where <filename> is the name of a special chain file containing a list of tests to be performed, and <options> are various option described below which control the execution of the chain.

This section is a description of the standard chain files used for testing a complete CMI.

6.8.2 Digital System Tests

Chain test name: CMITEST
Purpose : All functions of a CMI which can be tested directly under software control (i.e. no waveform observations required).

CMITEST requires a scratch or another diagnostics disk in drive 1.

Test progs run
- CMIINT
- CMITST
- MEM256
- LGTST
- MAST

Options

C=n	Channels to be tested. Default is 1-8
-T	Omit timer (TIM) test in MAST
-MAST	Omit MAST altogther
AD	Include A-D conversion tests in MAST

Test runs continuously, but can be aborted by hitting <CTRL-ESC>.
Examples are:

=CHAIN CMITEST (Run all tests as described above)

=CHAIN CMITEST;C=4,-MAST (Run all tests except Master Card and only use Channel 4)

6.8.3 Comprehensive Analog Test

Chain test name: ANALOG
To check: all analog functions of the CMI channel cards, master card, and audio card.

Test progs run	Commands executed
CMITST	RAMP, FILT, VOL
MAST	FILT, SYNC, AD.

Options:
M Omit channel card tests

This test is most conveniently used with the Analog Tester box connected to the rear panel of the CMI as labelled. Some cables need to be arranged slightly differently from normal. To make the changes, eject the disk(s), and turn power off first.
(1) Keyboard Power cable, normally connected from the CMI to the Music Keyboard, should go to the analog tester.
(2) Alphanumeric keyboard, normally connected to the Music keyboard, should be connected directly to the CMI rear panel.

The test program gives operator prompts and is thus largely self-explanatory. The following is some background on the use and functions of the analog tester.

Connection to Oscilloscope

The analog tester brings out both sides of the balanced outputs from the channel cards. With the oscilloscope set on 1V/div, add CH1 and CH2 and trigger on CH1.

The chain tests call standard tests described in previous sections which specify waveform measurements at TP6 of the channel card. This is only one side of the balanced output so measurements made using the analog tester will be about twice the amplitude found on TP6. For example in CMITST test FILT, the low frequency amplitude should be 6.8V p-p.

Switch 1 Phase Position

The phase check is to ensure that the different channels are in phase with each other.

Switch 1 Normal Position

This provides the balanced outputs to the CRO as above.

Mixed Out Test

This is the same as used in the FRV chain tests where FILT,N=1 is called repetitively starting with channel 1 only and mixing another channel in with each press of the space bar. The amplitude should increase with each new channel, reaching a maximum of 6.8V p-p. This tests the audio mixer board in the back of the CMI.

MIC/LINE switching in MASTer test

By means of software and the analog tester, the output of channel 8 is fed to the MIC and LINE inputs and one or the other is fed to the Master card via the MIC/LINE switch. Although these two levels are actually quite different, the signals from the analog tester are similar in magnitude but still distinguishable. A sinusoidal waveform followed by a heavily attenuated harmonic should be observed with a peak amplitude of 1.5V p-p for MIC and 1.3V p-p for LINE.

The SYNC test

No measurement is required: the software will inform you of a fault although there is a filtered square wave which can be observed and an audible tone whose volume can be controlled by the SYNC MONITOR pot.

AD Test

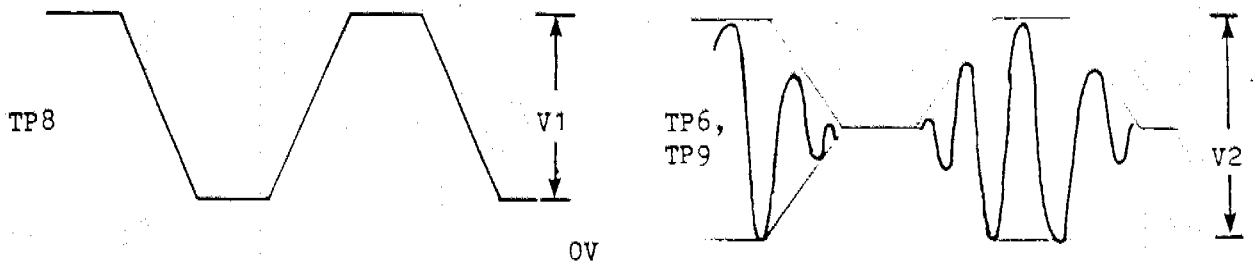
This is also a software test only (no oscilloscope monitoring).

6.9. Summary of Test Waveforms

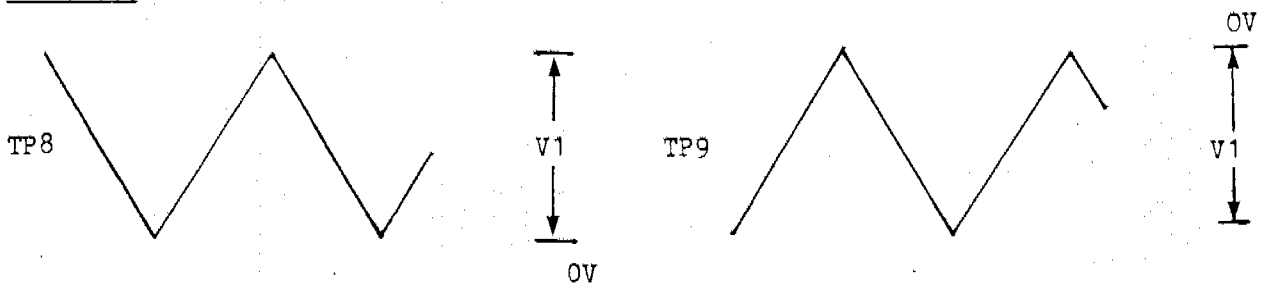
Measurement tolerances: refer to the introduction.
(TP6) means measured at Test Point 6 of the Channel Card under test.
(AT) means measured using the Analog Tester, adding CRO channels.

6.9.1 CMITST Waveforms (CMITST V3.30)

TRIMA,N=1 and RAMP,N=3

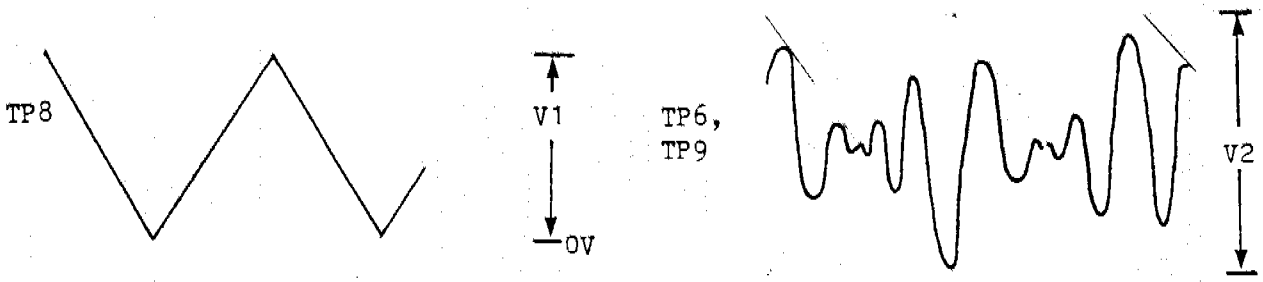


RAMP,N=1

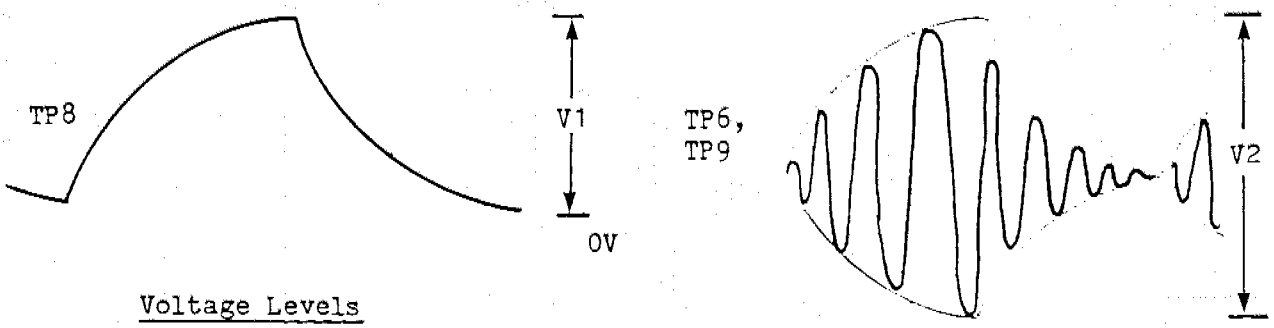


No signal at TP6 for RAMP,N=1

RAMP,N=2



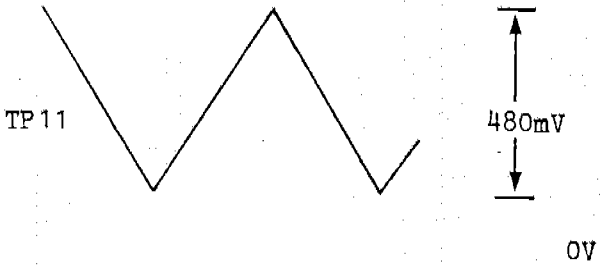
RAMP,N=4

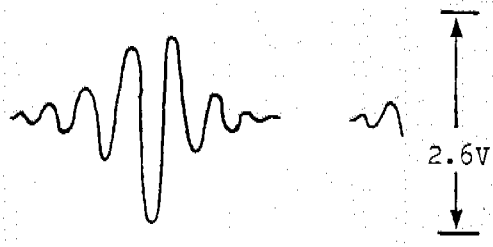


Voltage Levels

CMI-01-A	V1	V2 @ TP9	V2 @ TP6
REV 2	4.5	9	4
REV 3	4	8	4

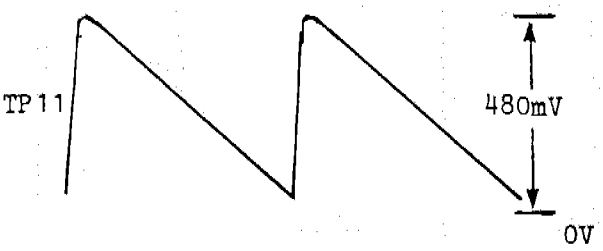
VOL,N=1





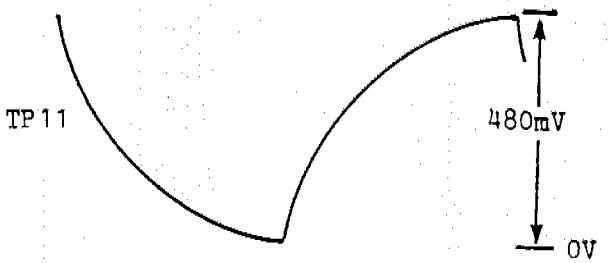
9V p-p steady sinewave at TP9

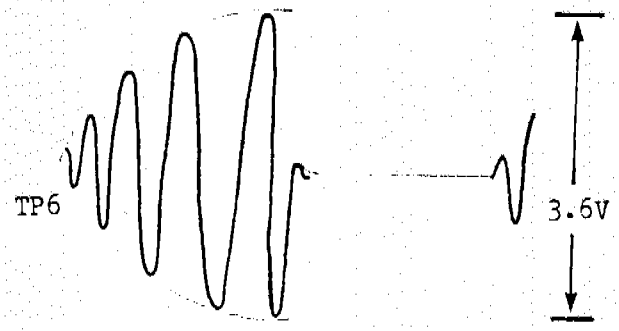
VOL,N=2



Zero signal at TP9, TP6
(check level at TP6 < 20mV)

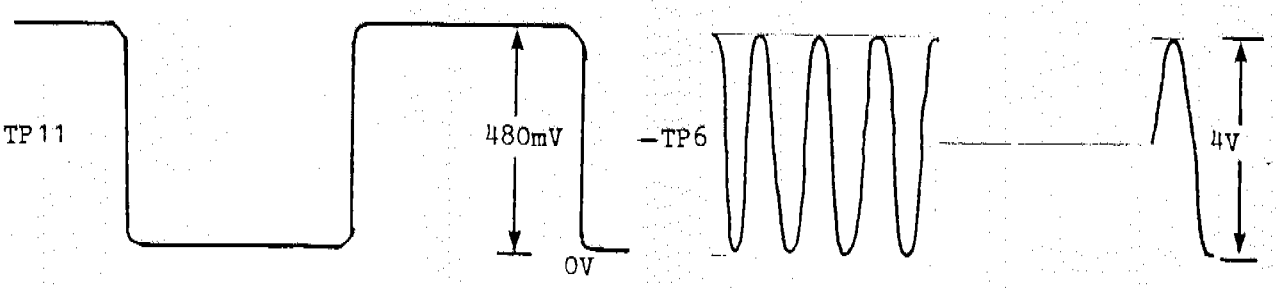
VOL,N=3





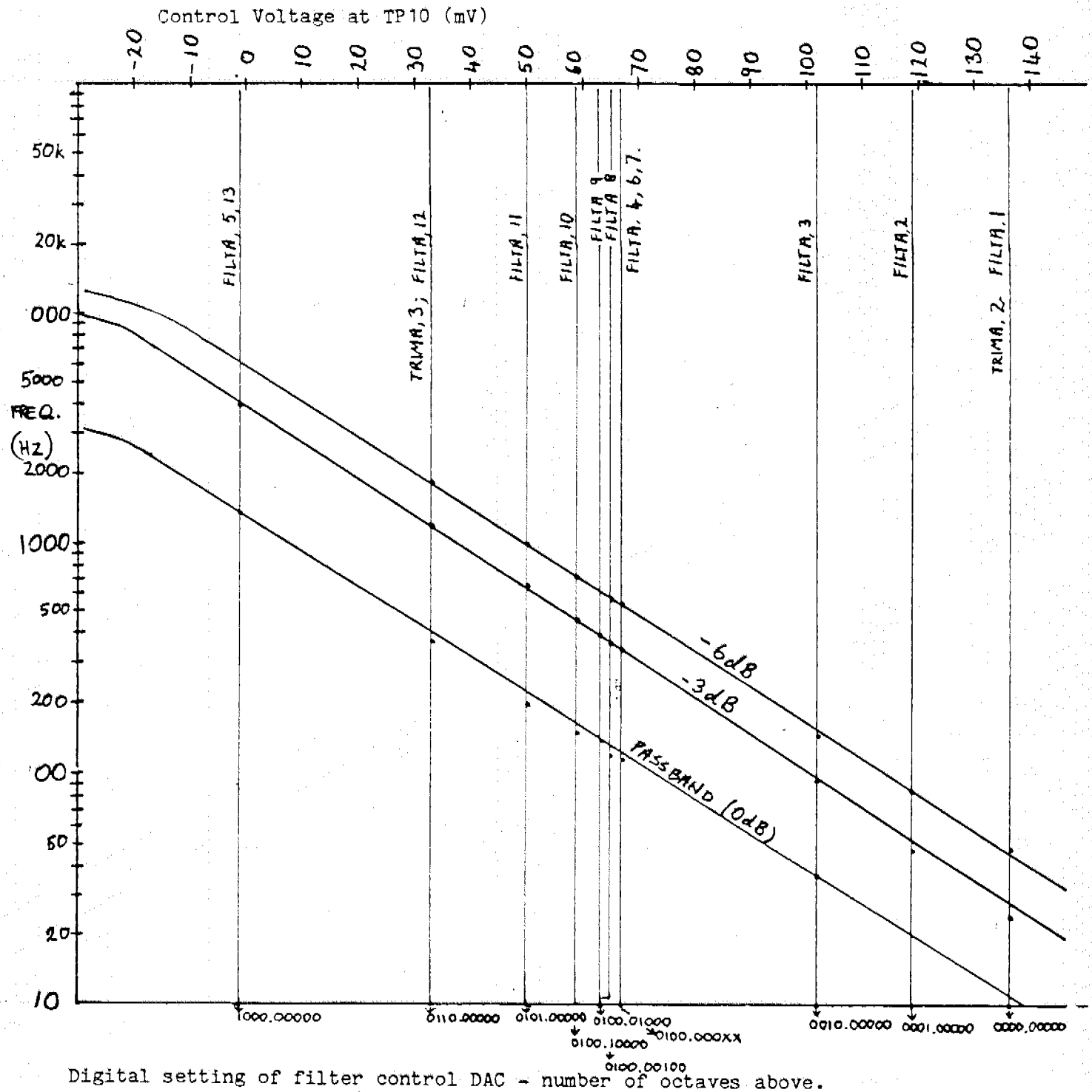
9V p-p steady sine at TP9

VOL,N=4



6.9.2 Channel Card Revs 1 and 2 (CEM Filter)

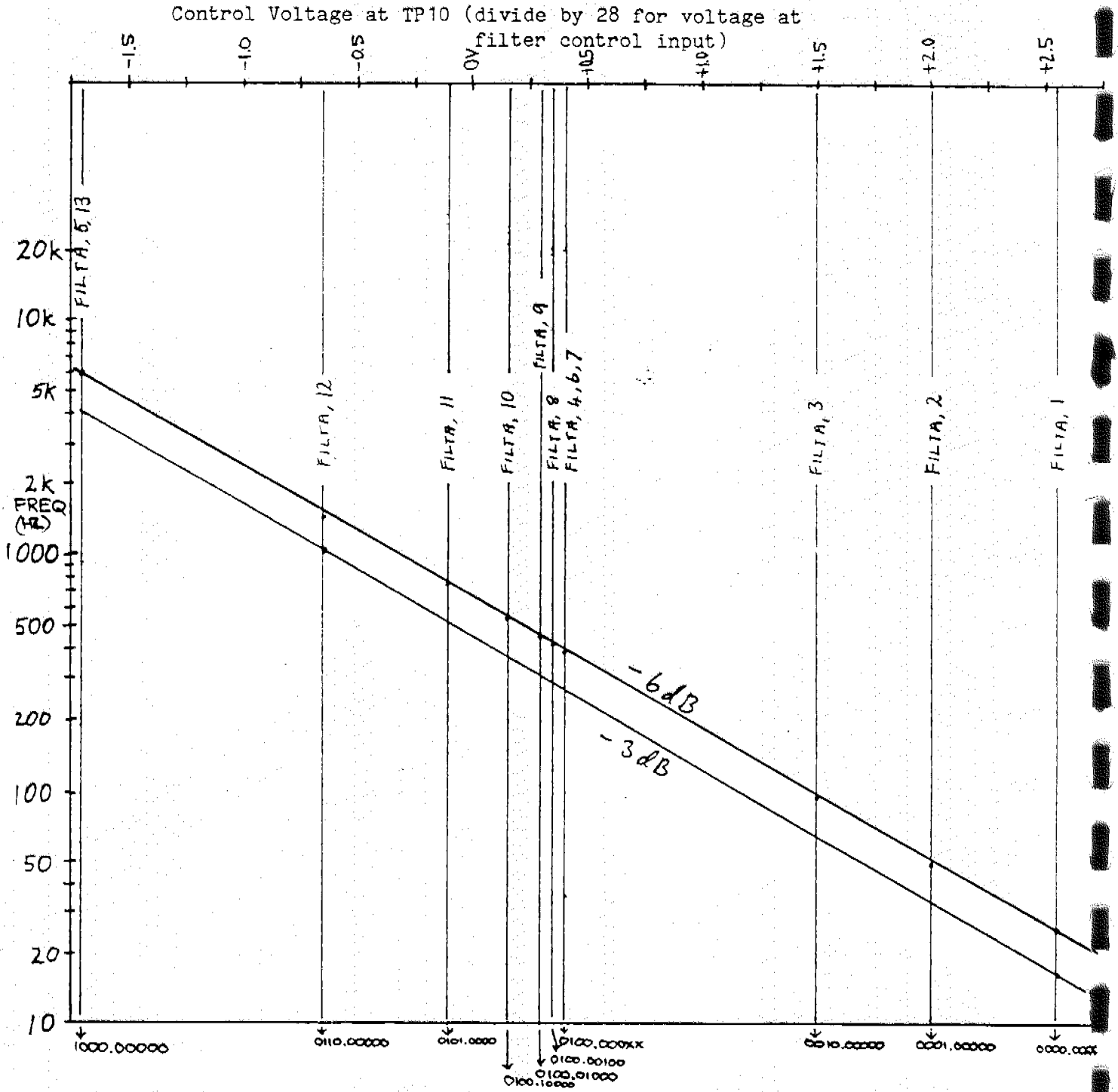
Tracking Filter Frequency Response
Related to Diagnostic Test Settings (CMI-01-A)



Digital setting of filter control DAC - number of octaves above.
Zero setting -3dB point (16Hz) expressed as binary fraction.
Decimal point is placed between D5 and D6 inputs on DAC.
(FILTA,14 setting not shown: -3dB at 13.4kHz, -6dB at 19.3kHz)

6.9.3 Series A Channel Card Rev 3 (SSM Filter)

Tracking Filter Frequency Response
Related to Diagnostic Test Settings (CMI-01-A)



Digital setting of filter control DAC - number of octaves above.
Zero setting -3dB point (16Hz) expressed as binary fraction.
Decimal point is placed between D5 and D6 inputs on DAC.
(FILTA,14 setting not shown: -3dB at , -6dB at 21.6kHz)

6.10 Analog Interface Card (AIC)

6.10.1 Starting the AIC Tests

The AIC diagnostics may be started by booting a diagnostic disk and typing:

AICTST<return>

There are three tests which may be run under AICTST;

1) RAM - an AIC RAM test
2) MUX - an AIC multiplexor test
3) DAC - an AIC DAC test.

Details on these tests are included below. Testing should proceed as follows:

1) RAM test
2) MUX test
3) tune the AIC (see section 6.10.6)
4) DAC test

6.10.2 Required Hardware configuration

An AIC must be inserted into slot CMI-07. Analog power must be supplied to the card. This is accomplished by making an analog power cable (master card power) with two ten pin flat cable connectors and plugging the extra connector into the AIC. Also, ensure that the Mother board has been modified to supply the FCXX signal to pin 54 of slot CMI-07. These modifications are detailed in Field Change Notice #39.

A special test cable is required to connect AIC inputs to AIC outputs for the MUX and DAC tests. This can be constructed by connecting a 34 pin flat cable connectors to each end of a 30 cm length of 34 wire flat cable. Pin 1 of the inputs should be connected to pin 1 of the outputs etc.

6.10.3 AIC RAM Test

The AIC RAM test can be run by typing **RAM<return>** (after typing **AICTST<return>**). 'RAM' tests the ability of the AIC 6809 processor to run programs, the AIC refresh function and the ability of the AIC and P1 to share the system bus. Several diagnostic messages can be displayed by this test. A '6809 PROCESSOR DOESN'T RESPOND' message will be displayed after P1 waits a few seconds without getting a meaningful response from the AIC. A '6809 PROCESSOR CRASHED' message is displayed if the AIC writes meaningless data into it's error queue. Memory faults are displayed in a manner similar to the CMI RAM tests.

6.10.3.1 Program Flow of the RAM test

There are two parts of the RAM test. The CMI (P1,P2) program and the AIC 6809 program. They synchronize the testing phases with the use of semaphores. The following tests are performed:

1. P2 tests all AIC memory location sequentially and using random test values. The 'FATAL AIC MEMORY ERROR' can be displayed by this phase of the RAM test.
2. P1 and the AIC's 6809 write to and read from alternate locations in the top half of AIC memory.
3. P1 and the AIC's 6809 write to and read from every 16th pair of bytes. A 100msec time delay is introduced between the read and write to test the AIC refresh
4. The AIC moves it's test program to the top half of AIC memory and P1 and the AIC's 6809 test the bottom half of memory. This test is repeated 4 times.

6.10.4 AIC Multiplexor Test

The AIC multiplexor test can be run by typing **MUX<return>** (after typing **AICTST<return>**). 'MUX' tests the input and output multiplexors and the sample and hold circuitry. The error messages are similar to those for the RAM test. The MUX test will not pass unless the test cable is connecting the AIC inputs to the AIC outputs as described in section 6.10.2.

6.10.4.1 Program flow of the MUX test

There are two parts of the MUX test: the CMI (P1,P2) program and the AIC program. The CMI program loads and starts the AIC MUX test, then waits for the AIC to set a test complete flag. If there were errors, they are displayed from the AIC error queue, otherwise a 'test passed' message is displayed.

The AIC program runs the same program for each of the 16 I/O channels of the AIC. Each I/O channel has it's own block of data which is pointed to by the 6809 Direct Page register. The Direct page register is loaded with that address for the next I/O channel each time the program is executed. Also, the Multiplexing system is configured for the next I/O channel each time the program is executed. The following description of the AIC half of the Mux test program flow is therefore for one I/O channel only. For simplicity the program flow is presented using a standard Program Design Language (PDL).

```
Increment Phase Counter
If Phase counter = 1
  generate random test value for the DAC currently being tested
Endif
If phase counter = 8
  compare test value with resulting ADC value
  if error greater than $3000
    queue appropriate values for display by P1
  endif
  let phase counter = 0 (marks end of test of current DAC)
Endif
If there are more DAC's to test
  write test values out to DAC's
  wait for timer interrupt and repeat program for next channel
Else
  set test complete flag
  halt AIC processor
Endif
```

6.10.5 AIC Analog Test

The AIC DAC test can be run by typing **DAC<return>** (after typing **AICTST<return>**). 'DAC' tests each bit of the scaling DAC's and the 12 bit input DAC. If a failure occurs the number of the bit that failed is displayed. The DAC test will not pass unless the test cable is connecting the AIC inputs to the AIC outputs as described in section 6.10.2. Also, the DAC test will not be likely to pass unless the AIC has been tuned. SEE SECTION 6.10.6.

Note that the DAC's may be separately tested using the 'N' option of the command interpreter.

6.10.5.1 Program flow of the DAC test

There are two parts of the DAC test: the CMI (P1,P2) program and the AIC program. The CMI program loads and starts the AIC DAC test, then waits for the AIC to set a test complete flag. If there were errors, they are displayed from the AIC error queue, otherwise a 'test passed' message is displayed.

The AIC program writes a special pattern of test data to the DAC currently being tested. This special pattern can be described simplistically as logarithmically decreasing data, such that each new datum should cause the ADC input (thanks to the special test cable) to decrease by one-half. The allowed deviation for the ADC input is unique for each test value, becoming smaller as the test values decrease. Any resulting ADC value outside the the allowed deviation is queued for later display by P2. This sequence is repeated with data and allowable deviations customized for each DAC.

6.10.6 AIC Tuning

The AIC must be tuned before it will pass the DAC test. Tuning is accomplished by adjusting the trimpots at the top of the front edge of the AIC. A description of the procedures for tuning AIC inputs and outputs follows.

6.10.6.1 AIC Input Tuning

The equipment required to tune an AIC input is as follows:
1) Test voltage source
2) Digital multimeter
3) Electronic Tuner (Korg chromatic tuner recommended)

The CMI software should be set up as follows:
1) Boot a CMI system disk
2) Load a first harmonic sine (with loop) into the waveform memory
3) Set up page A for a channel 1 pitch input by:
    a. setting INPUT ASSIGNMENT #1 to PITCH1
    b. setting INPUT RANGE #1 to 1 (volt/octave)

The equipment setup is as follows:
1) connect the voltage source across pin 1 and 2 (gnd) of the input (top) connector.
2) connect the digital multimeter in parallel with the voltage source.
3) place the electronic tuner next to a CMI monitor speaker.
4) place a weight on one of the keys of the music keyboard to produce a long note.

Now the fun begins. Proceed as follows:

1) determine the pitch of the note produced by the monitor speaker using the tuner.
2) note the voltage being produced by the voltage source.
3) increase the voltage by 1 volt
4) if the pitch increases by 1 octave, you are finished - otherwise proceed.
5) if the pitch is flat, turn the top trimpot counter-clockwise.
6) if the pitch is sharp, turn the top trimpot clockwise.
7) repeat 2-6 until the AIC produces a 1 octave pitch change for a 1 volt input change.

6.10.6.2 AIC Output Tuning

The only equipment required to tune an AIC output is a digital multimeter. Connect the meter across pin 1 and 2 (gnd) of the output (bottom) connector.

The CMI software should be set up as follows:
1) boot a CMI system disk
2) set up page A for a channel 1 pitch output by:
   a. setting OUTPUT ASSIGNMENT #1 to PITCH1
   b. setting OUTPUT RANGE #1 to 1

Proceed as follows:

1) play a note on the CMI music keyboard
2) note the voltage being produced at the AIC output
3) play a note one octave up from the previous note
4) if the voltage goes up by one volt, you are finished, otherwise proceed
5) if the voltage change is less than one volt, turn the bottom trimpot clockwise
6) if the voltage change is greater than one volt, turn the bottom trimpot counter-clockwise
7) repeat 1-6 until the AIC produces a 1 volt change for a one octave keyboard change

7. SIGNAL LIST

7.0 Motherboard Signal List

All CMI modules, with the exception of the Audio, Front Panel and Power Supply modules, plug directly into 78 pin edge connectors mounted on the CMI motherboard CMI-25. This is in turn mounted on the rear of the CMI card cage. The motherboard is the means by which all logic signals and power supplies are routed between the plug-in modules. This section specifies each of these signals for each module, starting from the left.

All modules are "double sided" so require two columns of pins on each connector. "Side A" refers to the wiring side of a plug-in module which corresponds to the left hand column of pins on the motherboard when viewed from the front of the card cage. Conversely, "Side B" refers to the component side of the module and connects to the right hand column of pins on the edge connector.
Pin numbers not included in the following lists are not used, and have no connection on the motherboard. Signals which are listed but have "N/C" entered as the source or destination are those which have been connected to edge connector fingers but have no connections leading to or from the corresponding pins on the motherboard.

A pin specified as an input ("I/P") will have the Source module which drives that input entered in the Source/Destinations column. Conversely an output ("O/P") will have the Destination or driven module entered in the Source/Destinations column.

Active-low signals are indicated by overlining. All other signals are active-high. Where different names have been used for one signal going between various modules, the Signal Name column contains the name for the module of the current section, and the alternative name is enclosed in brackets in the Source/Destination column.

With the exception of Section 7.6, this document refers to the CMI-25 Rev. 3 motherboard.

7.1 Common Signals Bussed to All Slots

The following connections are common to all slots and travel the full length of the motherboard in a ground shield interleave pattern which provides protection against electromagnetic noise pickup and cross-talk between adjacent signal tracks. Not all modules use all the bussed signals.

Side A

Pin	Signal Name	Function	Source
42	SYRES	System reset	Q133
41	ADD2	P2 address on buss	Processor
40	ADD1	P1 address on buss	Processor
39	P2ø2	P2 phase 2 reference	Processor
38	P1ø2	P1 phase 1 reference	Processor
37	$\overline{RA}$	Row address mux signal	Processor
36	$\overline{CA}$	Column address mux sig.	Processor
35	$\overline{RAS}$	Row address strobe	Processor
34	$\overline{CAS}$	Column address strobe	Processor
33-26	D0-D7	Data Buss	Various
25-10	MA0-MA15	Address Buss	Various
9	VMA	Valid Memory Address	Various
8	R/W	Read/write	Various
7	Key	Socket index key	
6	+12V	+12V supply rail	
3	-12V	-12V supply rail	
2,1	GND	Ground rail	

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
44-46	GND	Ground rail		
42-1	GND	Ground shielding pattern		
5,4,2,1	GND	Ground rail		

7.2 Slot 1: Master Card CMI-02

Side A Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
76	ADINT	A/D conversion IRQ	O/P	Q133 (IL62)
75	P2IR2	P2 Interprocessor intrpt	O/P	Q133 (IL22)
74	CHS7	Channel select	O/P	Channel 7
73	CHS6	Channel select	O/P	Channel 6
72	CHS5	Channel select	O/P	Channel 5
71	CHS4	Channel select	O/P	Channel 4
70	CHS3	Channel select	O/P	Channel 3
69	CHS2	Channel select	O/P	Channel 2
68	CHS1	Channel select	O/P	Channel 1
67	CHS0	Channel select	O/P	Channel 0
65	RAMEN	System RAM enable	O/P	N/C
64	IRQSYN	P1 level 0 IRQ (Keyboards)	I/P	Q133 (ACINT) & CMI-08 (MIDINT)
63	PENB	Peripheral Enable *	I/P	Q256 card 0
or	VRAMEN	Graphics RAM enable	O/P	Graphics
62	ILS1	PICU latch strobe	I/P	Processor
61	IA31	PICU cascade	O/P	Q133 (IA41)
60-58	IA21-IA01	Interrupt vector address bits 1-3	O/P	Processor
57	IRQ1	Interrupt request to Processor 1	O/P	Processor
56	XIRQ	P1 IRQ from Q133 PICU	I/P	Q133 ($\overline{IRQ1}$)
54	HLT	Processor 2 halt for A/D conversion	O/P	Processor
53	$\overline{SCAS}$	Channel memory column address strobe	O/P	All channels
52	$\overline{SRAS}$	Channel memory row address strobe	O/P	All channels
51	$\overline{SRA}$	Channel row address multiplex signal	O/P	All channels
50	SREF	Channel memory refresh cycle	O/P	All channels
48	MOSC	Master pitch oscillator	O/P	All channels
47	P1IR11	P1 level 4 IRQ	I/P	N/C
46	P1IR10	P1 level 3 IRQ	I/P	Processor (P1 IPI) & CMI-28 (SMIDINT)
44	ADCLK	A/D convert clock	I/P	Channel 1

* A 2-way link option is provided on the CMI-25 motherboard whereby a Q096 64K memory card may be installed instead of the Q256, provided an old revision (Rev 5) master card is used. The default linking on the motherboard connects pin 63A of a Rev 6 master card (PENB input) to the Peripheral Enable output of the Q256. On an old master card, pin 63A is the Video Ram Enable (VRAMEN) output which connects via the non-default link, to the Graphics Controller VRAMEN input. The Q096 RAM card is not supported by Series IIX CMI software.

7.3 Slot 2: General Interface Card CMI-08/28 (Optional)

Either the CMI-08 MIDI board or the CMI-28 SMPTE/MIDI board may be installed in slot 2.

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78,77	+5V	+5V Logic supply		
76	P2DMAC	P2 DMA claim	O/P	N/C
75	P1DMAC	P1 DMA claim	O/P	Q256 RAM
70	ETL2	P2 DMA Enable This Level	I/P	N/C
69	ENL2	P2 DMA Enable Next Level	O/P	N/C
68	ETL1	P1 DMA Enable This Level	I/P	Q133 ($\overline{\text{ENL1}}$)
67	ENL1	P1 DMA Enable Next Level	O/P	N/C
66	MIDINT	MIDI IRQ (CMI-08 only) *	O/P	Master (IRQSYN)
65	SMIDINT	SMPTE/MIDI IRQ (CMI-28)	O/P	Master (P1IR10)
64	FCXX	Port select	I/P	Q133
48	ACK2	P2 DMA Acknowledge	I/P	N/C
47	RDMA2	P2 DMA Request	O/P	N/C
46	ACK1	P1 DMA Acknowledge	I/P	Processor
45	RDMA1	P1 DMA Request	O/P	Processor

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
69	MIDINT	MIDI IRQ (CMI-08 only)	O/P	N/C
68	SMIDINT	SMPTE/MIDI IRQ (CMI-28)	O/P	N/C
67	FCXX	Port select	I/P	N/C

* The CMI-08 board only generates the MIDINT interrupt which is connected to the P1 level 0 IRQ input on the Master card, along with the ACIA IRQ from the Q133. The CMI-28 board only generates the SMIDINT interrupt which is connected to the P1 level 3 IRQ input on the Master card, along with the P1 IPI interrupt from the processor card.

The B-side signals on pins 67-69 are duplicates of the corresponding signals on side A, and are only used when a CMI-08 or CMI-28 module is installed in a Series I machine upgraded to Series IIX.

7.6 Slot 12: 64K System RAM Q-096

N.B. - These connections are only present on the Rev. 1 CMI-25 motherboard. Slot 12 is unused on later revision boards, and no connections are present other than the bussed signals on pin 42A and below. The Q096 RAM card is not supported by Series IIX CMI software.

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
67,66	RAMEN2,3	Card enable lines	I/P	N/C
65	RAMEN	Card enable	I/P	Q133 (RAMINH)
64	FCXX	MAPRAM select	I/P	Q133
63	AB2	P2 map select	I/P	Master (RAMEN)
62	AB1	P1 map select (pulled high)	I/P	N/C
60-57	MS4 -MS1	Module select lines	I/P	N/C
56	MSCOM	Ground on card		N/C
55	CSEL	Card select acknowledge	O/P	N/C
48	REF	Refresh cycle	I/P	Q133

7.7 Slots 13,14: 256K System RAM Q256

One Q256 module must be installed in slot 14. This is referred to as Card 0 and must have zero set up on the card select DIP switch on the board (see Q256 description). A second Q256 module may be installed in slot 13, and should be switched as Card 1.

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
76	BE1	P1 E signal (unused)	I/P	Processor
75	DMAC11	P1 DMA claim level 1	I/P	Gen. I/F (P1DMAC)
74	DMAC12	P1 DMA claim level 2	I/P	N/C
73	DMAC13	P1 DMA claim level 3	I/P	N/C
72	DMAC14	P1 DMA claim level 4	I/P	N/C
71	DMAC21	P2 DMA claim level 1	I/P	Floppy (DMACLM)
70	DMAC22	P2 DMA claim level 2	I/P	H. Disk (DMACLM)
69	DMAC23	P2 DMA claim level 3	I/P	N/C
68	DMAC24	P2 DMA claim level 4	I/P	N/C
65	RAMINH	System RAM Inhibit	I/P	Graphics (VRAMSEL)
64	FCXX	Port select (Mapsel RAM)	I/P	Q133
63	A/B2	P2 System/User State	I/P	Processor
62	A/B1	P1 System/User State	I/P	Processor
52	PENBIN	Peripheral Enable In	I/P	RAM, Card 0 (PENBOUT)
51	PENBOUT	Peripheral Enable Out (From Slot 14 only; Slot 13 N/C)	O/P	Various
50	VRAMEN	Video RAM Enable (From Slot 14 only; Slot 13 N/C)	O/P	Graphics
48	REF	Refresh cycle	I/P	Q133
46	PERRINT	Parity Error IRQ	O/P	Q133 (IL02)

7.8 Slot 15: Q014 4-Port ACIA Module (Optional)

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
66	ENB	Peripheral Enable	I/P	RAM (PENB)
65-58	IRQ0-7	Individual ACIA IRQs	O/P	N/C
57	IRQ8	Combined IRQ	O/P	Q133 (IL62)
56-53	AS6-AS9	Address select	I/P	N/C

7.9 Slot 16: Processor Control Module Q133

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
76	IL32	P2 level 3 IRQ	I/P	Processor (IPI2)
75	IL22	P2 level 2 IRQ	I/P	Master ($\overline{\text{P2IR2}}$)
74	IL12	P2 level 1 IRQ	I/P	Graphics ($\overline{\text{RINT}}$)
73	IL02	P2 level 0 IRQ	I/P	Q133 ($\overline{\text{RTCINT}}$) & RAM ($\overline{\text{PERRINT}}$)
72	IL31	P1 level 3 IRQ	I/P	Ch 7 ($\overline{\text{CHINTX}}$)
71	IL21	P1 level 2 IRQ	I/P	Ch 5 ($\overline{\text{CHINTX}}$)
70	IL11	P1 level 1 IRQ	I/P	Ch 3 ($\overline{\text{CHINTX}}$)
69	IL01	P1 level 0 IRQ	I/P	Ch 1 ($\overline{\text{CHINTX}}$)
68	ILS2	P2 PICU latch strobe	I/P	Processor
67-64	IA42-IA12	P2 intrpt vector addr.	O/P	Processor
63	IRQ2	P2 interrupt request	O/P	Processor
62	ILS1	P1 PICU latch strobe	I/P	Processor
61-58	IA41-IA11	P1 intrpt vector addr.	O/P	Processor
57	$\overline{\text{IRQ1}}$	P1 interrupt request	O/P	Master (XIRQ)
56	$\overline{\text{NMI2}}$	P2 NMI request	O/P	Processor
55	$\overline{\text{NMI1}}$	P1 NMI request	O/P	Processor
54	$\overline{\text{RES2}}$	P2 restart	O/P	Processor
53	$\overline{\text{HLT2}}$	P2 HALT	O/P	Processor
52	$\overline{\text{RES1}}$	P1 restart	O/P	Processor
51	$\overline{\text{HLT1}}$	P1 HALT	O/P	Processor
50	W2	P2 halt acknowledge	I/P	Processor
49	$\overline{\text{W1}}$	P1 halt acknowledge	I/P	Processor
48	REF	Refresh cycle	O/P	RAM
46	$\overline{\text{ACK1}}$	Refresh acknowledge	I/P	Processor
45	$\overline{\text{REQ1}}$	Refresh cycle request	O/P	Processor
44	ROMEN	Restart ROM enable	I/P	Processor

Side B

Pin	Signal Name	Function	Input or Output	Source/ Destination
76	IL72	P2 level 7 IRQ	I/P	Floppy, H. Disk
75	IL62	P2 level 6 IRQ	I/P	Master (ADINT) & Q014 (IRQ8)
74	IL52	P2 level 5 IRQ	I/P	Graphics (PENINT)
73	IL42	P2 level 4 IRQ	I/P	Graphics (TOUCHINT)
72	IL71	P1 level 7 IRQ	I/P	Ch 6 (CHINTX)
71	IL61	P1 level 6 IRQ	I/P	Ch 4 (CHINTX)
70	IL51	P1 level 5 IRQ	I/P	Ch 2 (CHINTX)
69	IL41	P1 level 4 IRQ	I/P	Ch 0 (CHINTX)
68	ACINT	Keyboard ACIA IRQ	O/P	Master (IRQSYN)
67	IRQPA	User PIA IRQ A	O/P	N/C
66	IRQPB	User PIA IRQ B	O/P	N/C
65	ENL1	P1 DMA Enable Next Level	O/P	Gen I/F (ETL1)
64	FCXX	Ports access	O/P	Various
62,61	____	Current loop TX	O/P	
60	FXXX	FXXX address range decode	O/P	N/C

7.10 Slot 17: Central Processor Module Q209

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
76	BE1	P1 "E" signal	O/P	RAM
75	FIRQ2	P2 Fast IRQ	I/P	N/C
74	FIRQ1	P1 Fast IRQ	I/P	N/C
73	IPI2	P2 Interprocessor Intrpt	O/P	Q133 (IL32)
72	IPI1	P1 Interprocessor Intrpt	O/P	Master (P1IR10)
71	FCXX	Port select	I/P	Q133
70	A/B2	P2 System/User state	O/P	RAM
69	A/B1	P1 System/User state	O/P	RAM
68	ILS2	P2 PICU latch strobe	O/P	Q133
67-64	IA42-IA12	P2 intrpt vector addr.	I/P	Q133
63	IRQ2	P2 interrupt request	I/P	Q133
62	ILS1	P1 PICU latch strobe	O/P	Q133
61-58	IA41-IA11	P1 intrpt vector addr.	I/P	Q133
57	IRQ1	P1 interrupt request	I/P	Q133
56	NMI2	P2 NMI request	I/P	Q133
55	NMI1	P1 NMI request	I/P	Q133
54	RES2	P2 restart	I/P	Q133
53	HLT2	P2 HALT	I/P	Q133
52	RES1	P1 restart	I/P	Q133
51	HLT1	P1 HALT	I/P	Q133
50	W2	P2 in wait state (BA)	O/P	Q133
49	W1	P1 in wait state (BA)	O/P	Q133
48	ACK2	P2 DMA acknowledge	O/P	Floppy, H.Disk
47	REQ2	P2 DMA request	I/P	Floppy, H.Disk
46	ACK1	Refresh cycle grant	O/P	Q133
45	REQ1	Refresh cycle request	I/P	Q133
44	ROMEN	Restart ROM enable	O/P	Q133
43	OSC	Master proc. clock	O/P	N/C

7.11 Slot 18: Lightpen/Graphics Interface Q219

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
68	RINT	Timer IRQ	O/P	Q133 (IL12)
67	PENINT	Light pen hit IRQ	O/P	Q133 (IL52)
66	TOUCHINT	Light pen touch IRQ	O/P	Q133 (IL42)
65	VRAMEN	Video RAM Enable	I/P	RAM
64	FCXX	Port select	I/P	Q133
63	VRAMSEL	Video Ram Select	O/P	RAM

7.12 Slot 19: Floppy Disk Controller QFC-9

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
71	EDL	Enable Daisy Links	O/P	Floppy ($\overline{ETL}$)
70	ETL	Enable This Level	I/P	Floppy ($\overline{EDL}$)
69	ENL	Enable Next Level	O/P	H.Disk ($\overline{ETL}$)
68	DMACLM	DMA claim	O/P	RAM ($\overline{DMAC21}$)
65	PENB	Peripheral Enable	I/P	RAM card 0
63	IRQD	Floppy Controller IRQ	O/P	Q133 (IL72)
48	ACK2	DMA cycle grant	I/P	Processor
47	RDMA	DMA request	O/P	Processor ($\overline{REQ2}$)

7.13 Slot 20: Hard Disk Controller Q077

Side A

Pin	Signal Name	Function	Input or Output	Source/ Destination
78-77	+5V	Logic power supply	I/P	
71	EDL	Enable Daisy Links	O/P	N/C
70	ETL	Enable This Level	I/P	Floppy ($\overline{ENL}$)
69	ENL	Enable Next Level	O/P	N/C
68	DMACLM	DMA claim	O/P	RAM ($\overline{DMAC22}$)
65	PENB	Peripheral Enable	I/P	RAM card 0
63	IRQD	Hard Disk Controller IRQ	O/P	Q133 (IL72)
48	ACK2	DMA cycle grant	I/P	Processor
47	RDMA	DMA request	O/P	Processor ($\overline{REQ2}$)

8. SIGNAL LIST - EXTERNAL CONNECTIONS

8.1 A.C. Mains

A.C. Mains Neutral, Active and Ground.

8.2 Graphics Power

A.C. Mains supply to Graphics Terminal. Switched by key switch on mainframe. This supply is always the same as the local mains potential.

8.3 Graphics

Video signal to Graphics Terminal and Light Pen signals to mainframe.

Connector Type: Cannon 5-pin.

Pin 1 Lightpen Hit. T.T.L. level, asserted low. On oscilloscope, appears as a series of low-going pulses about 1uS wide, repeated every 20mS, when the pen is pointed at a bright area of the screen. See figure 8.3a.

Pin 2 Lightpen Signal Return. Ground for lightpen signal cables.

Pin 3 Lightpen Touch. T.T.L. level, asserted low. Normally at approx +4 volts, goes low (less than 0.4 V) when the end of the lightpen touched.

Pin 4 Video Return. Ground for Video signal cable.

Pin 5 Composite Video. 1V P-P video signal to Graphics display. Format is 625 lines, 50 Hz frame rate. See figure 8.3b.

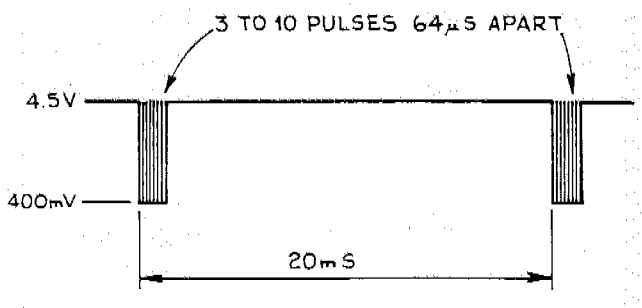


Figure 8.3a LIGHTPEN HIT SIGNAL

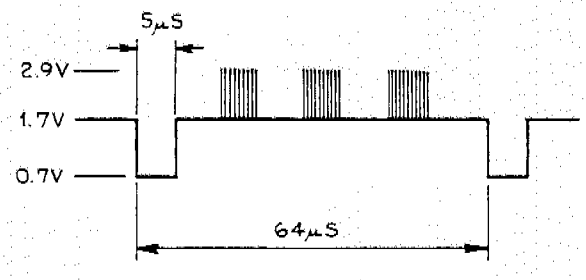


Figure 8.3b COMPOSITE VIDEO

8.4 Keyboard Power

Unregulated power supply to music keyboard (also indirectly supplies alphanumeric keyboard).

Connector Type: Cannon 7-pin.

Pins 1,2 +10V Return. Return (ground) for +10V supply.

Pins 3,4 +10V Supply. Unregulated supply, +9 to +11 volts.

Pin 5 -20V Supply. Unregulated supply, -18 to -22 volts.

Pin 6 +20,-20 Return. Return (ground) for + and - 20 supplies.

Pin 7 +20V Supply. Unregulated supply, +18 to +22 volts.

8.5 Keyboard

Bi-directional serial data between mainframe and music keyboard, including "busy" flags in both directions. Power supply is also carried by this cable, to power the alpha-numeric keyboard if it is connected instead of the music keyboard.

Connector Type: 9 Pin "D-Mini"

Pin 1 +18 to 22 volts unregulated supply. This is not used by the music keyboard.

Pin 2 DON1. Signal to enable transmission of data from the keyboard. RS-232 levels. Enabled: >7 volts. Disabled <-7 volts. With nothing being transmitted from the keyboard, this signal should be at approx. +10 volts. When keys are pressed or released a burst of -10 volt pulses should be seen for between 2 and 10 milliseconds.

Pin 3 -18 to -22 volts unregulated supply. This is not used by the music keyboard.

Pin 4 FLAG1. Signal to disable transmission of data from the mainframe to the keyboard. Signal is normally +10 volts.

Pin 5 SIGNAL RETURN. Ground for data paths.

Pin 6 DATA IN. Serial data from keyboard to mainframe. Format is RS-232. Normally at -10 volts. When a key is pressed or released a burst of +10 volt pulses lasting approx. 3 mS should be seen.

Pin 7 POWER RETURN. Return (Ground) for + and - supplies.

Pin 8 Not Connected.

Pin 9 DATA1. Serial data from mainframe to keyboard. Format is RS-232. Normally at -10 volts. For each character sent from the mainframe to the alpha-numeric display a burst of +10 volt pulses lasting approx. 1 mS should be seen.

8.6 Printer

Serial data from mainframe to printer, "busy" flag from printer to mainframe, plus "device on" signal used to switch on printer in readiness to receive data.

Connector type: Cannon 5 pin.

Pin 1 Signal Ground.

Pin 2 Not Connected.

Pin 3 FLAG0. "Busy" flag from printer. RS-232 levels. <-7 volts when printer ready, >+7 volts when printer busy.

Pin 4 DON0. "Device On" control from mainframe to printer. RS-232 level, >+7 volts to enable printer, <-7 volts to diable printer. This signal is optional as some printers do not require it.

Pin 5 DATA0. Serial data to printer. RS-232 levels, ASCII format. Normally at -10 volts. For each character sent from the mainframe to the printer a burst of +10 volt pulses lasting approx. 1 mS should be seen.

8.7 Phones

Output for driving headphones. Monitors the MIXED LINE output. Internally, this output is taken from the MONITOR (speaker) output via a 100 ohm resistor.

Connector type: 1/4" (6.25 MM) stereo phono jack.

The following signal lists refer to connectors on the rear of the C.M.I. Mainframe.

8.8 Monitor

Output for driving a monitor speaker. The internal monitor amplifier will deliver a maximum of 20 watts R.M.S. into an 8 ohm speaker. Note that the Mainframe is fitted with a 1 amp speaker fuse which will blow if the monitor amplifier is driven to full output under load for more than a second.

Connector Type: Cannon 3 pin.

Pins 1,2 Ground

Pin 3 Active. With all channels producing a full-amplitude sinewave and the MONITOR control turned up to the point of clipping, this output should be approx. 38 volts P-P (with no load).

8.9 Channels 1-8

Individual channel outputs (balanced, 600 ohms impedance).

Connector type: Cannon 3 pin.

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3.7 volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

8.10 Mixed Line Output

Mixed output of all eight channels (balanced, 600 ohms impedance).

Connector Type: Cannon 3-Pin

Pin 1 Ground

Pin 2 Output Cold. Anti-phase output, maximum level 3.7 volts P-P.

Pin 3 Output Hot. Maximum level 3.7 volts P-P.

8.11 Sync

Synchronising input and output, for use with Music Composition Language (Page C) or Keyboard Sequencer (Page 9) or Real-Time Composer (Page R). This connector serves as both an input and ouput.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 Sync Input. Pulses or tone of 1 to 20 volts P-P. Waveform unimportant. Frequency range 2 Hz to 5 kHz. Impedance 10 K ohms.

Pin 3 Click Output. Periodic pulse, rate controlled by Page 9 Sequencer or M.C.L. (Page C). Waveform is a spike of approx. 5 volts peak, approx. 5 mS wide, alternately positive and negative going.

8.12 Filter Out

Output of the bandpass filter used by the Analog to Digital converter. It is designed to enable the operator to monitor the effect of various bandpass filter settings.

Connector type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 OUTPUT. Amplitude for full-scale conversion is 10 volts P-P. Source impedance 600 ohms.

8.13 Mic In

Balanced, 600 ohms input suitable for high output dynamic or condenser microphones. When the MIC/LINE switch is in the MIC position, this input is fed to the Analog to Digital converter.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A

Pin 3 INPUT B

8.14 Line In

Balanced, 600 ohm line level input. This input is connected to the Analog to Digital converter when the MIC/LINE switch is in the LINE position.

Connector Type: Cannon 3-pin

Pin 1 GROUND

Pin 2 INPUT A. Amplitude of 1.4 volts P-P required for full scale conversion.

Pin 3 INPUT B. Amplitude of 1.4 volts P-P required for full scale conversion.

8.15 ADC DIRECT

Direct input to the Analog to Digital converter when the ADC DIRECT/ MIC LINE switch is in the ADC DIRECT position. Because this input is Direct Coupled, any D.C. offset on this input will result in a D.C. shift of a sound sample.

Connector Type: Cannon 3-pin.

Pin 1 GROUND

Pin 2 GROUND

Pin 3 INPUT. Amplitude for full scale conversion is 10 volts P-P.

9. REMOVE/REPLACE PROCEDURE

9.1 MAINFRAME FRONT PANEL REMOVE/REPLACE

1. Disconnect mains power to the CMI.
2. Slide the two moulded Front Panel hinge bolt catches towards the centre of the panel and then pull. The Front panel will hinge down to expose circuit boards.
3. Unplug the anti-static earthing strap from the card cage side plate.
4. Disconnect the 26-way ribbon cable connector from the centre connector on the Processor Control Board Q133, (slot 16). Note which connector it is connected to.
5. Unclip the hinge brackets by gently bending one of the black hinge brackets out of its hinge plate.
6. To replace Front Panel reverse the above procedure.

9.2 CIRCUIT BOARD REMOVE/REPLACE

9.2.1 Circuit board removal.

NOTE: This procedure only applies to circuit boards located within the Card Cage rack assembly.

1. DISCONNECT POWER TO CMI BEFORE PROCEDING, otherwise circuit board damage will result.
2. Remove the mainframe Front Panel as in section 9.1.
3. Locate the circuit board to be replaced. Disconnect any connector/s necessary to allow the circuit board to be removed.
4. Spread open the board's ejectors to release the card from the mother board edge connector.
5. Slowly slide out the circuit board towards the front of the Card Cage.

9.2.2 Circuit board replacement.

NOTE: Before inserting circuit board into Card Cage rack ensuse the board is the correct type for that location.Also check that the polarizing key is properly located in the edge connector for that slot.

1. Locate the circuit board onto its card cage rails. Component side of circuit board should be facing towards the right.
2. Clear the path of any connecting cables and slowing slide in the circuit board until it comes into contact with the motherboard edge connnctor.
3. Locate the board into its polarising key on the motherboard. Now firmly push the board into the edge connector. Its ejectors should be in line with the adjacent ejectors.
4. Reconnect any cables that were removed in 9.2.1.
5. Replace the card cage front panel as in section 9.1.
6. Reconnect the mains power.

9.3 MAINFRAME REAR PANEL REMOVE/REPLACE

1. Disconnect the mains power and all other cables connected to the Rear Panel.
2. Remove the four mounting screws from the rear panel, (one screw from each corner).
3. Gently pull the Rear Panel out from the mainframe and lay it down on its face.
4. Some of the connecting cables from the circuit boards in the card cage will have to be disconnected before the rear panel can be completely removed. These are the cables going to the Graphics/Lightpen board Q219 (slot 18), and the 10-way cable going to the Processor Control board Q133 (slot 16). Disconnect these connectors and let them drop down between the card cage rails onto the bottom panel.
5. Unplug the 6-way mains connector and the 15-way DC power connector going to the card cage rear panel. Each connector has a locking tab that will have to be released before the connector can be unplugged.
6. Unplug the connectors going to the disk drives.
7. Unplug the 50-way and 10-way ribbon cables going to the Audio board CMI-04.
8. Remove the Rear Panel.

9.4 AUDIO BOARD, CMI-04 REMOVE/REPLACE

9.4.1 Audio board CMI04 removal.

1. Disconnect all cables connected to the CMI rear panel.
2. Remove the four rear panel mounting screws, (one in each corner).
3. Pull out the rear panel from the mainframe and lay it facedown on the table.
4. Remove the three cables connected to the Audio board.
5. The next step is the removal of the edge connector. Using both hands, place fingers on the bottom edge of the rear panel. Place left-hand thumb 25mm from left-hand side of edge connector and right-hand thumb 25mm from right-hand side of edge connector and gently push the connector. Now move both thumbs to the centre of the edge connector and again gently push. This procedure may need to be repeated a few times until connector is completely off the board.
   NOTE: It is important NOT to apply pressure on the outer section of the edge connector as this may cause disassembly of the entire edge connector.
6. Remove the six mounting screws from the Audio board.
7. Lift out the board.

9.4.2. Audio board CMI04 replacement.

1. Place the Audio board on the rear panel with the edge connector fingers in line with the edge connector. Do not attempt to insert edge connector at this stage.
2. Replace the six Audio board mounting screws and insulating washers.
3. With all fingers equally spaced along the edge connector (remember to keep away from its very ends), push the edge connector onto the Audio board.
4. Reconnect the three cables removed previously.
5. Refit the rear panel to the CMI mainframe.

9.5 TOP COVER REMOVE/REPLACE

1. Disconnect mains power.
2. Remove the four counter-sunk Philips-head screws securing the top cover, (one on each side and two at the rear of the black tube frame at the top).
3. Lift-off the top cover.

9.6 SIDE COVER REMOVE/REPLACE

1. Disconnect mains power.
2. Remove the four counter-sunk Philips-head screws securing the side cover, (one on the top and bottom, and two at the rear of the black tube frame).
3. Lift out side cover.

9.7 BOTTOM COVER REMOVE/REPLACE

1. Remove the left-hand side cover (card cage end), as in 9.6.
2. Remove the counter-sunk Philips-head screw on the left-hand side securing the the bottom cover.
3. Place the mainframe on a soft surface and stand it on its left-hand end.
4. Remove the remaining three screws securing the base panel. There are two at the rear and one on the right-hand side on the black tube frame.
5. Lift out bottom panel. If CMI optional connectors have been fitted, then they will also have to be removed before bottom cover can be completely removed.

9.8 DISK DRIVE REMOVE/REPLACE

9.8.1 Disk Drive removal.

1. Unscrew the rear panel as in section 9.3 but do not completely remove.
2. Disconnect the disk drive's signal and power cables.
3. Replace the rear panel to the mainframe.
4. Remove both of the mainframe side covers, top cover and bottom cover, (four counter-sunk Philips-head screws secure each mainframe cover). Refer sections to 9.5, 9.6 and 9.7.
5. Turn machine over onto its left-hand side. Refer figure 9.1.
6. Remove the four screws securing the disk drive to the mainframe, (two on the top side and two on the bottom side of the disk drive mounting plates).
7. Slowly slide out the disk drive from the mainframe. Refer figure 1.

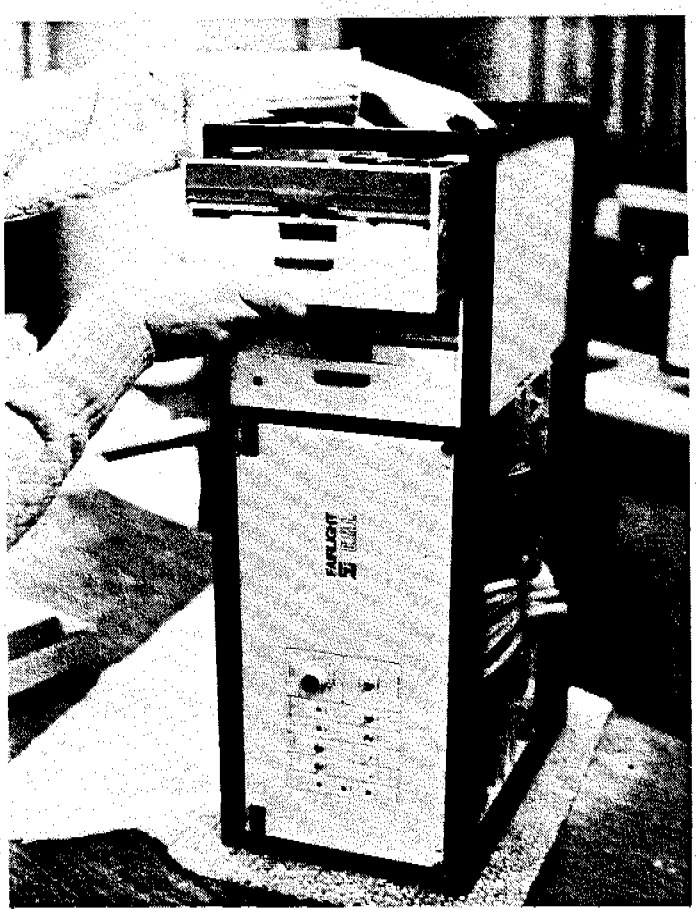


Figure 9.1 Disk Drive Removal

9.8.2 Disk drive replacement.

NOTE: Replacement disk drive should be 'optioned' and 'drive number selected' before inserting into mainframe. Refer to DISK DRIVE Manual section.

1. Once the replacement disk drive has been 'optioned' and 'drive number selected', slide the drive into the mainframe.
2. Replace the four disk drive mounting screws removed in 9.8.1.
3. Replace bottom cover and gently lower CMI back down onto its base.
4. Again remove the rear panel and reconnect the cables removed in 9.8.1. and replace rear panel.
5. Replace the two side panels and top cover.

9.9 FAN ASSEMBLY REMOVE/REPLACE

1. Disconnect mains power.
2. Remove top cover, as in section 9.5.
3. Disconnect the 6-way power cable going to the Fan asssembly. A locking tab on the connector has to be depressed before the connector can be unpluged.
4. Remove the six mounting screws and washers from the top of the Fan assembly. Note that under each washer there is a steel spacer inside the rubber grommet. Care should be taken so that these spacers are not dislodged when Fan assembly is lifted off the card cage assembly.
5. Lift off Fan assembly.

9.10 CARD CAGE REMOVE/REPLACE

9.10.1 Card Cage removal.

1. Disconnect mains power.
2. Remove top cover, as in section 9.5.
3. Remove the Fan assembly, as in section 9.9.
4. Remove left-hand side cover as in 9.6.
5. Gain access to the Card Cage rear panel by removing the CMI rear panel. Do not completely remove rear panel but disconnect the 6-way mains connector and the 15-way DC power connector that are plugged into the Card Cage rear panel. Each connector has a locking tab that has to be depressed before the the connector can be unplugged.
6. Completely remove the mainframe Front Panel, as in section 9.1.
7. The next step requires all the circuit boards in the Card Cage to be removed. Before proceding, all the circuit boards should have their relative slot number marked, in some way on the circuit board. When all the circuit boards have been marked, remove the circuit boards, as in section 9.2.

8. Now that the circuit boards have been removed all the cables coming into the Card Cage have to be pushed through the circuit board rails and dropped down onto the bottom panel, except for the 50-way cable going to the Floppy Controller board QFC9. This cable is pulled through to the CMI rear panel area behind the Card Cage rear panel.
9. Remove the two adjacent right-angled brackets securing the left-hand side of the Card Cage to the black tube frame.
10. At the slot 20 end of the Card Cage four screws secure the Card Cage to the disk drive top and bottom mounting plates. Access to the screws can be gained by 'snapping out' several circuit board rails.
11. Remove the two Allen head screws securing the left-hand side of the card cage to the black tube frame.
12. The Card Cage is now ready to be withdrawn from the mainframe. Standing in front of the CMI place your hands into the Card Cage to support its weight. Now slowly slide the Card Cage back towards the rear panel, so that the front panel hinge brackets clear the mainframe and then slide the Card Cage out to the left through the side opening.

9.10.1 Card Cage Replacement.

1. Slide the Card Cage back into the mainframe.
2. Refit the four screws at slot 20 end to secure the Card Cage to the disk drive mounting plates.
3. Refit the right-angle brackets securing the left-hand side of the Card Cage to the black tube frame.
4. Refit the two Allen head screws securing the left-hand side of the card cage.
5. The cables removed from the circuit cards will have to be brought up from the bottom panel. This can be done by removing the appropriate circuit board rails from the bottom of the Card Cage. The rails are removed and replaced by snapping them out and in to position.
6. When the cables are ready replace the circuit boards, as in section 9.2.
7. Refit the Fan assembly.
8. Refit the Card Cage front panel.
9. Reconnect the two connectors removed from the Card Cage rear panel.
10. Refit the CMI rear panel.
11. Refit the top side and bottom covers.

9.11 REGULATED POWER SUPPLY ASSEMBLY REMOVE/REPLACE

9.11.1 Regulated Power Supply assembly removal.
Refer to figure 9.2.

1. Disconnect the mains power.
2. Remove the top cover, as in section 9.5.
3. Unscrew the CMI rear panel by removing the four mounting screws, (one in each corner of the rear panel). Lay the rear panel down onto its face.
4. Unplug the 6-way mains power connector and the 15-way DC power connector going to the Card Cage rear panel. Each connector has a locking tab that will have to be depressed before the connector can be removed.
5. Running along the top and bottom of the black heatsink mounting plate is a row of four hexagon nuts with washers. Remove all eight nuts and washers and lower the Regulated Power Supply assembly down to expose the wiring loom going to its circuit board.
6. The next step is to remove the terminals off the circuit card. BEFORE REMOVING ANY TERMINAL CONNECTORS, NOTE AND MARK THEIR RESPECTIVE POSITION AND TERMINAL NUMBER ONTO THE TERMINAL CONNECTOR ITSELF. When all the terminal connectors have been marked remove them from their lugs, (a pair of long nose pliers will help).
7. Remove the Regulated Power Supply assembly from the the card cage assembly.

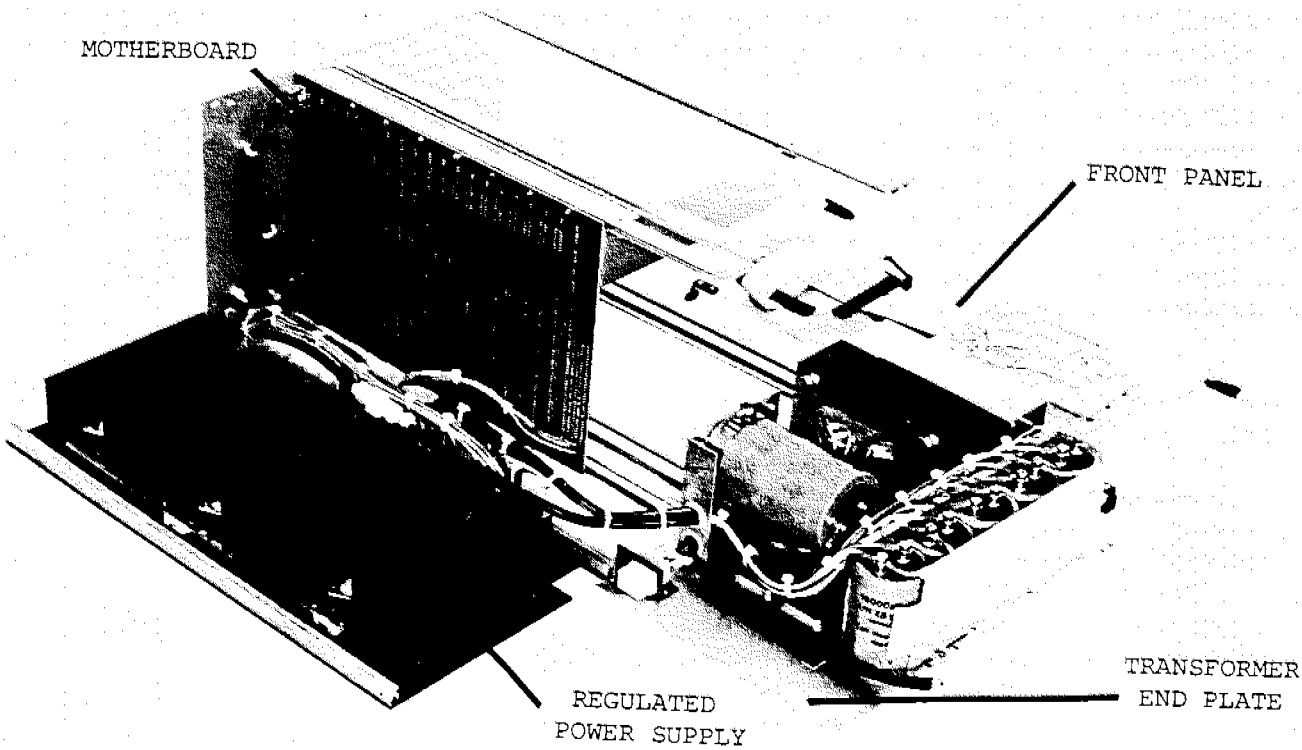


Figure 9.2. Card Cage Disassembly

9.11.2 Regulated Power Supply Asssembly Replacement.
Refer to figure 9.2.

1. Position the Regulated Power Supply assembly back into its original position so that the terminal connectors removed in the above procedure can be reconnected. Reconnect all the terminals to the circuit board terminals, OBSERVING THE TERMINAL NUMBERING MARKED WHEN THE ASSEMBLY WAS REMOVED.
2. Push the Regulated Power Supply assembly into position and align the screws in the mounting rail to the holes in the black heatsink plate.
3. Refit the eight hexagon screws and washers to the plate.
4. Reconnect the 6-way mains connector and the 15-way power connector to the card cage rear panel. ENSURE THAT THE CONNECTOR LOCKING TAB IS ENGAGED.
5. Refit the CMI rear panel.
6. Refit the top cover.

9.12 MOTHERBOARD REMOVE/REPLACE

9.12.1 Motherboard removal.
Refer to figure 9.3.

1. Disconnect mains power.
2. Remove the top cover, as in section 9.5.
3. Remove the left-hand side cover, as in section 9.6.
4. Remove the bottom cover, as in section 9.7 and leave CMI mainmainframe standing on its left-hand side.
5. Open the CMI front panel, as in section 9.1.
6. Unplug all the circuit boards from the motherboard edge connectors. There is no need to completely remove the circuit boards from the card cage assembly.
7. Replace the front panel.
8. Mark and remove the seven spade terminals going to the motherboard's +5v, 5v rtn and earth connections. The +12v, -12v and 12 rtn connections should be disconnected from the Regulated Power Supply assembly circuit board. MARK AND NOTE THEIR RESPECTIVE POSITION AND TERMINAL NUMBER BEFORE REMOVING.
9. The motherboard is screwed to the card cage mounting rails by two rows-of-eight hexagon nuts. Remove all sixteen nuts and remove the motherboard from the card cage assembly.

9.12.2 Motherboard replacement.
Refer to figure 9.3.

1. Position motherboard into card cage. Note that the polarising keys in the edge connectors have to be running along the bottom of the card cage. The motherboard mounting screws will have to be positioned with its mounting holes. The CMI should be laying down on its bottom panel for this procedure.
2. Align the motherboard over the screws and fit several nuts. Do not tighten the nuts at this stage as the edge connectors have to be aligned to the circuit boards in the card cage.
3. Stand the CMI on its left-hand side.
4. Refit the remaining nuts.

9. REMOVE/REPLACE PROCEDURE (continued)

5. Position the motherboard so that the circuit boards' edge connector fingers are aligned to the motherboard edge connectors. Temporarily secure some of the nuts. When all the circuit boards move freely in and out of the edge connectors secure the nuts. Test again that the circuit boards still move freely in and out of the edge connectors and if necessary repeat the alignment procedure.
6. Plug in all the circuit boards back into the edge connectors.
7. Reconnect the motherboard power cables.
8. Refit the bottom, side and top covers.

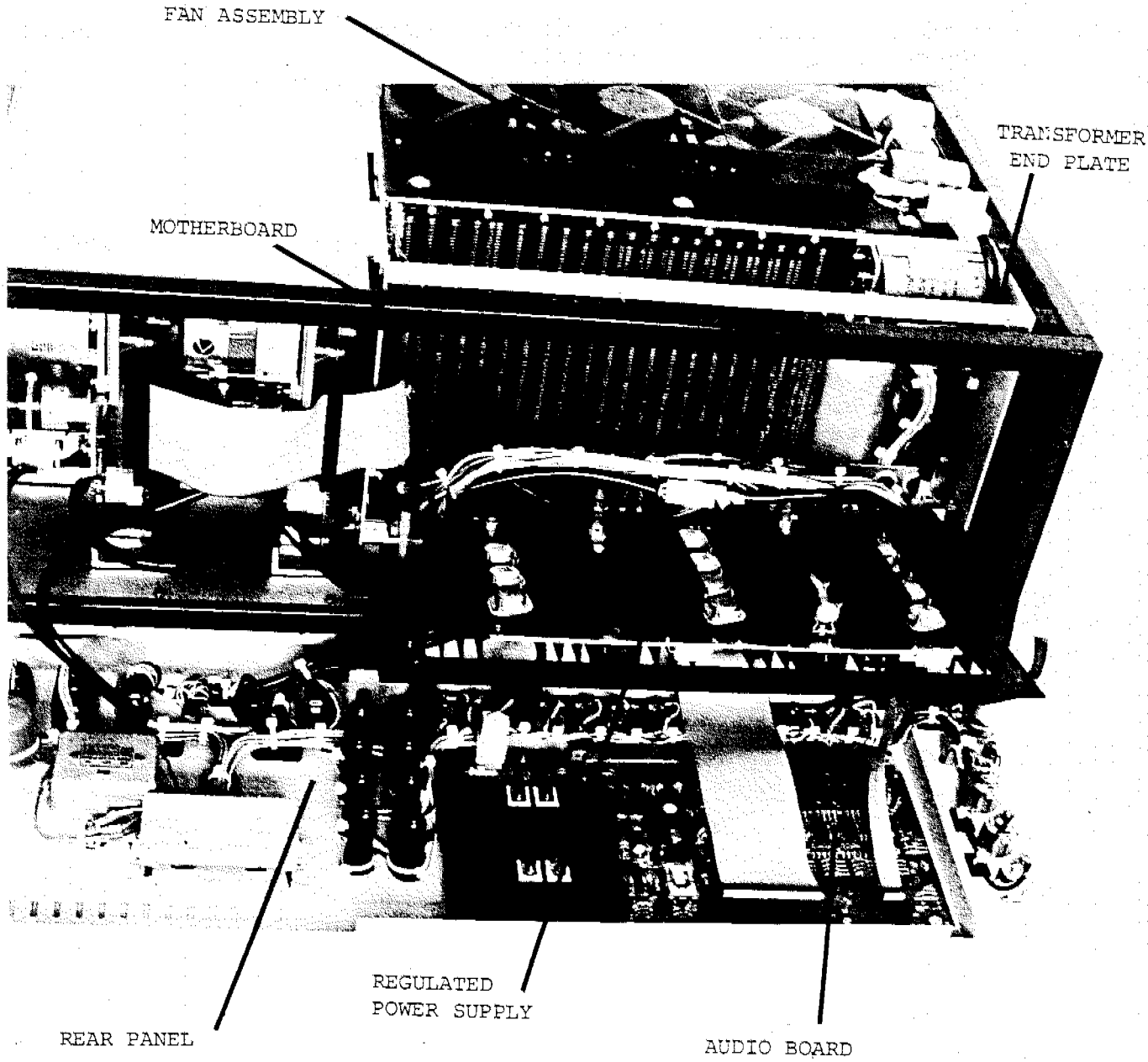


Figure 9.3 Rear View of Mainframe Showing Motherboard Access

9.13 TRANSFORMER END PLATE REMOVE/REPLACE

9.13.1 Transformer End Plate removal.
Refer to figure 9.2.

1. Remove the Card Cage assembly, as in section 9.10.
2. Remove all of the circuit board black rail guides by bending them until they snap out.
3. Disconnect the DC power wiring loom going to the Regulated Power Supply assembly circuit board from the Transformer End Plate assembly. NOTE AND MARK ALL TERMINAL CONNECTIONS BEFORE THEY ARE UNPLUGGED FROM THE CIRCUIT CARD.
4. Unscrew the six Philips-head screws and four counter-sunk screws securing the End Plate to the card cage support rails.
5. Remove the Transformer End Plate from the Card Cage assembly.

9.13.2 Transformer End Plate assembly replacement.
Refer to figure 9.2.

1. Position the assembly next to the Card Cage assembly and feed through the DC power wiring loom to the Regulated Power Supply circuit board.
2. Refit the End Plate to the Card Cage assembly using the mounting screws previously removed.
3. Reconnect the wiring loom to the ciruit board. OBSERVE THE TERMINAL MARKINGS AND NUMBERS BEFORE RECONNECTING.
4. Refit the card cage circuit board rail guides by 'snapping' them into place.
5. Refit the Card Cage to the mainframe.

10. REPAIR PROCEDURE

Having identified the faulty item, the following procedure is recommended:

1) Circuit Card Faults. Replace with spare card and return to Fairlight for repair.

2) Power Supply Faults. Repair following remove/replace instructions, functional description and related drawings.

3) Disk Drive Faults. Replace with spare drive. If fault is minor, adjust as per Fairlight Disk Drive Service Manual. In case of other fault, return to qualified Mitsubishi service centre or Fairlight for repair.

4) Electrical Faults. Repair by referring to appropriate wiring diagrams. Certain cable assemblies are available as spare parts from Fairlight (e.g. disk drive 50-way ribbon).

5) Mechanical Faults. Mechanical damage caused by wear and tear or accidental damage should be rectified by replacing the damaged item. Refer to section 16 (Exploded Views) below to identify the required part(s) for ordering.

11. PREVENTATIVE MAINTENANCE

The following procedures should be carried out every 1000 hours of operation.

1) Revove the top cover of the Mainframe and clean the mesh above the fans using a vacuum cleaner.

2) Unplug each circuit board, remove dust deposits from components and clean edge connector fingers using a soft cloth and a no-residue solvent such as freon. Check that the polarising key is properly installed in position 7 of each edge connector socket before replacing the cards.

3) Check all cables for signs of mechanical damage e.g. fraying. Ensure that all connectors are in good condition, especially mass termination ribbon connectors.

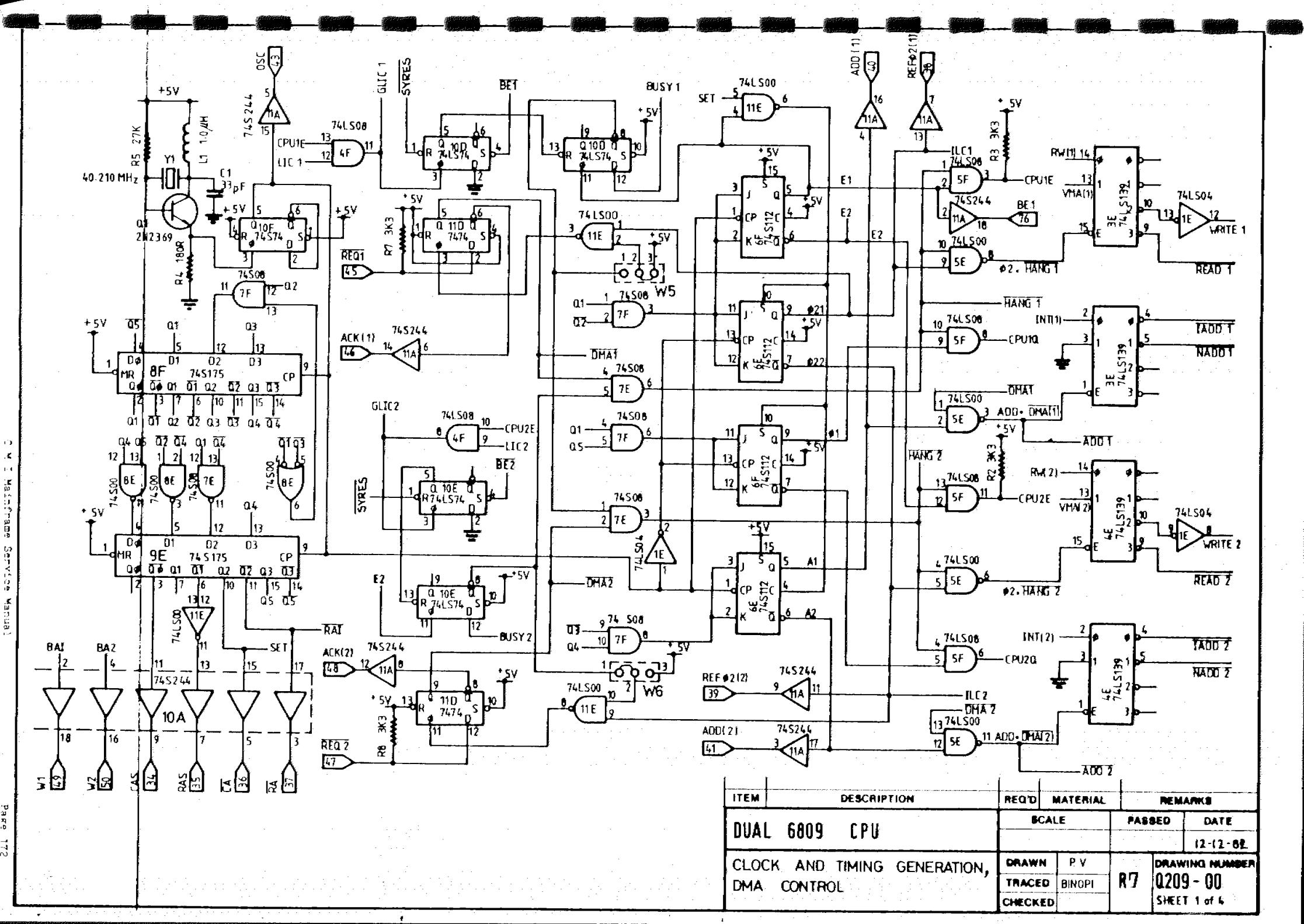
4) Check for mechanical damage such as bent panels or loose screws.

5) Check out all electronic functions using the Chain Tests (Refer to section 6 above).

6) Check disk drives as per Disk Drive Maintenance Manual.

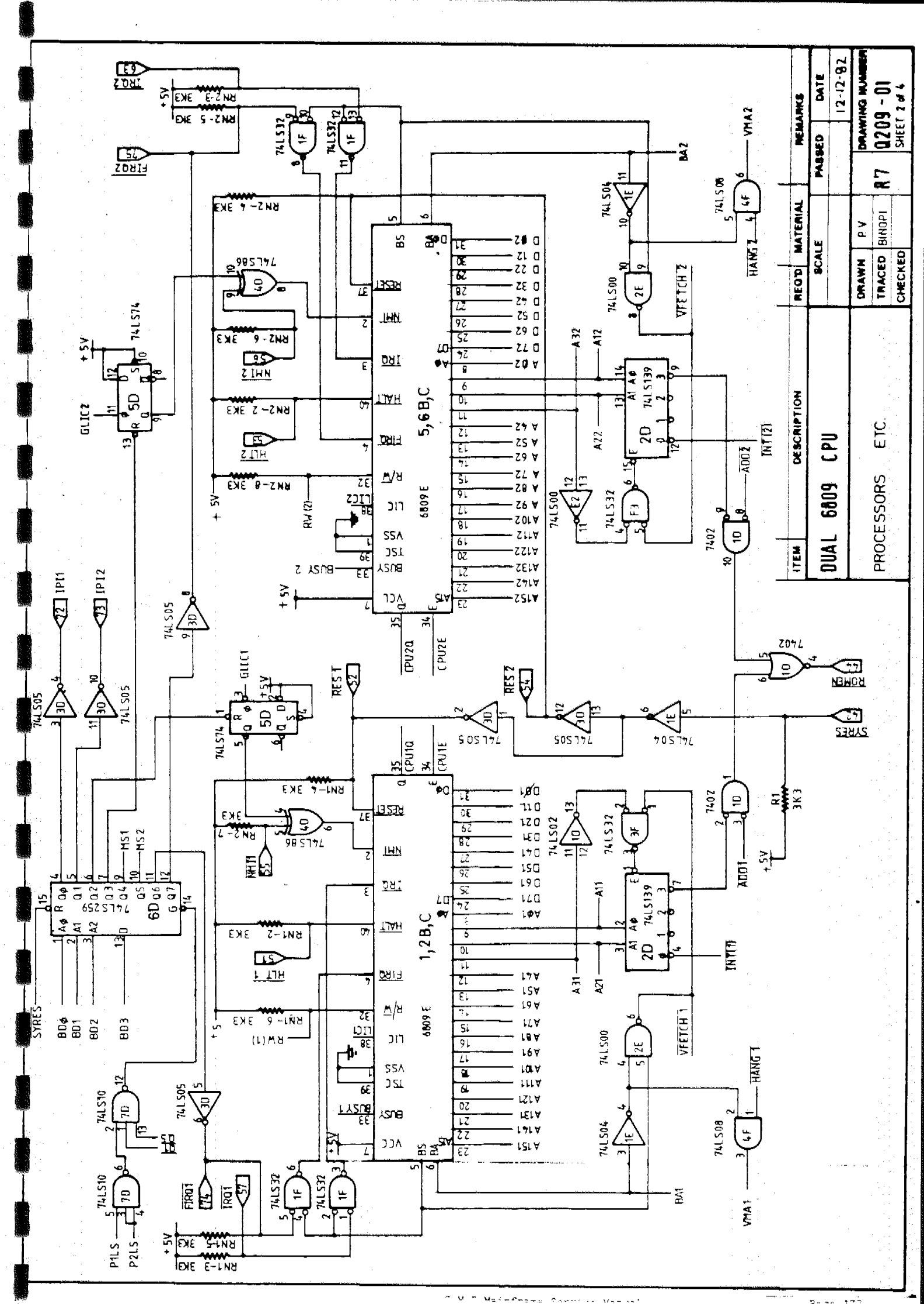
SECTION 12

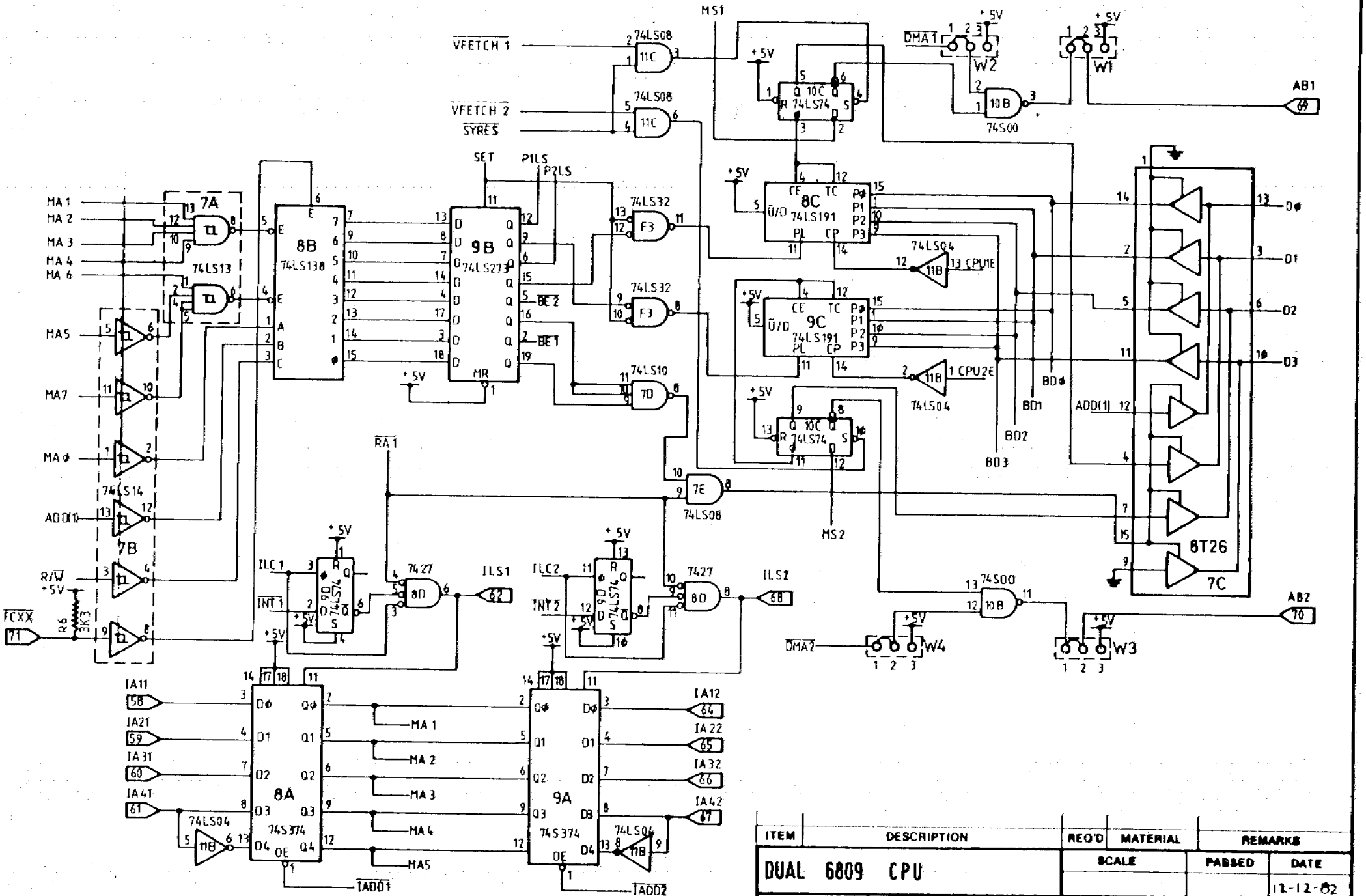
SCHEMATIC DIAGRAMS



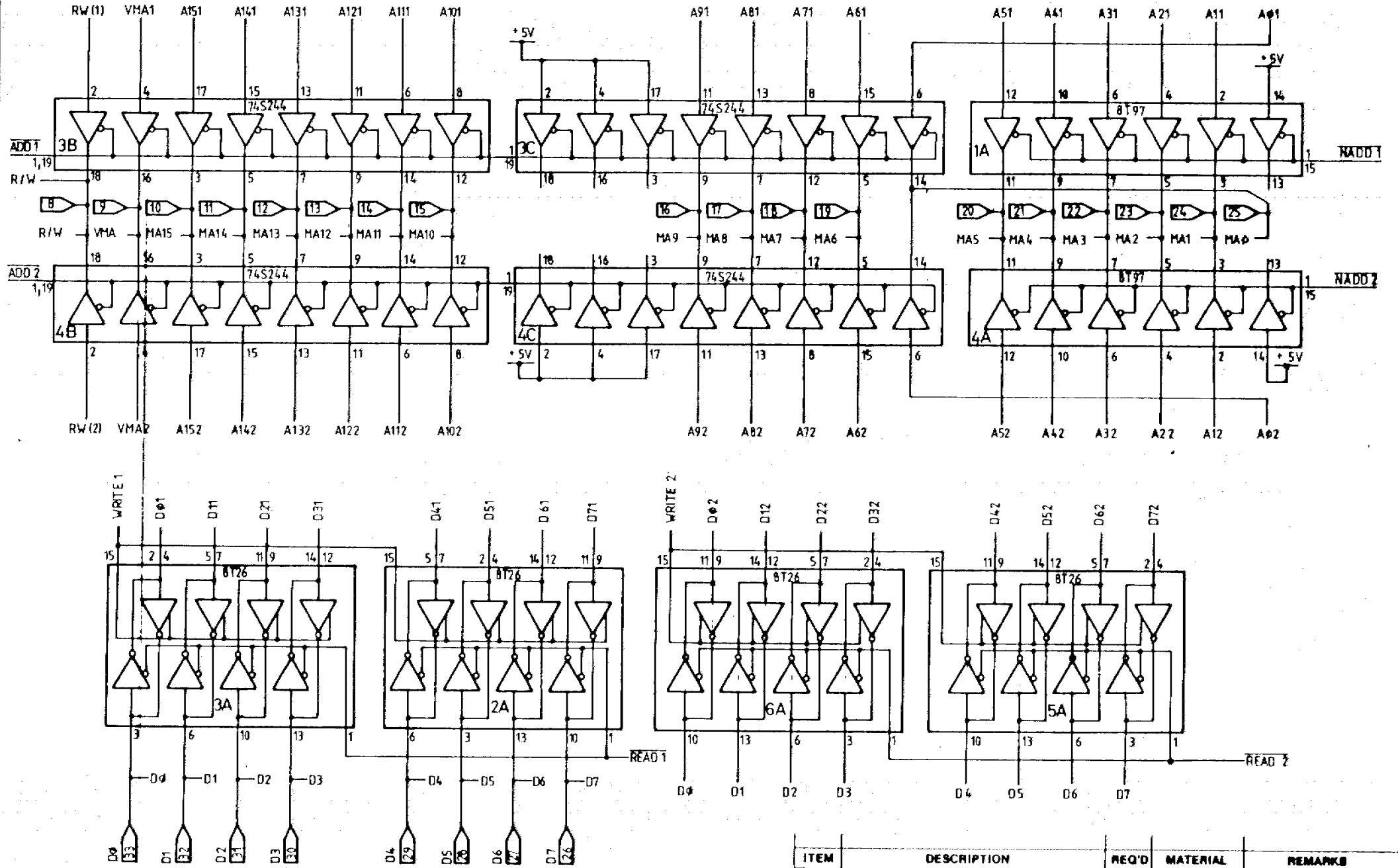
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CLOCK AND TIMING GENERATION, DMA CONTROL		DRAWN P.V TRACED BINOPI CHECKED	R7	DRAWING NUMBER Q209-00 SHEET 1 of 4

Microware Systems Corporation 1982

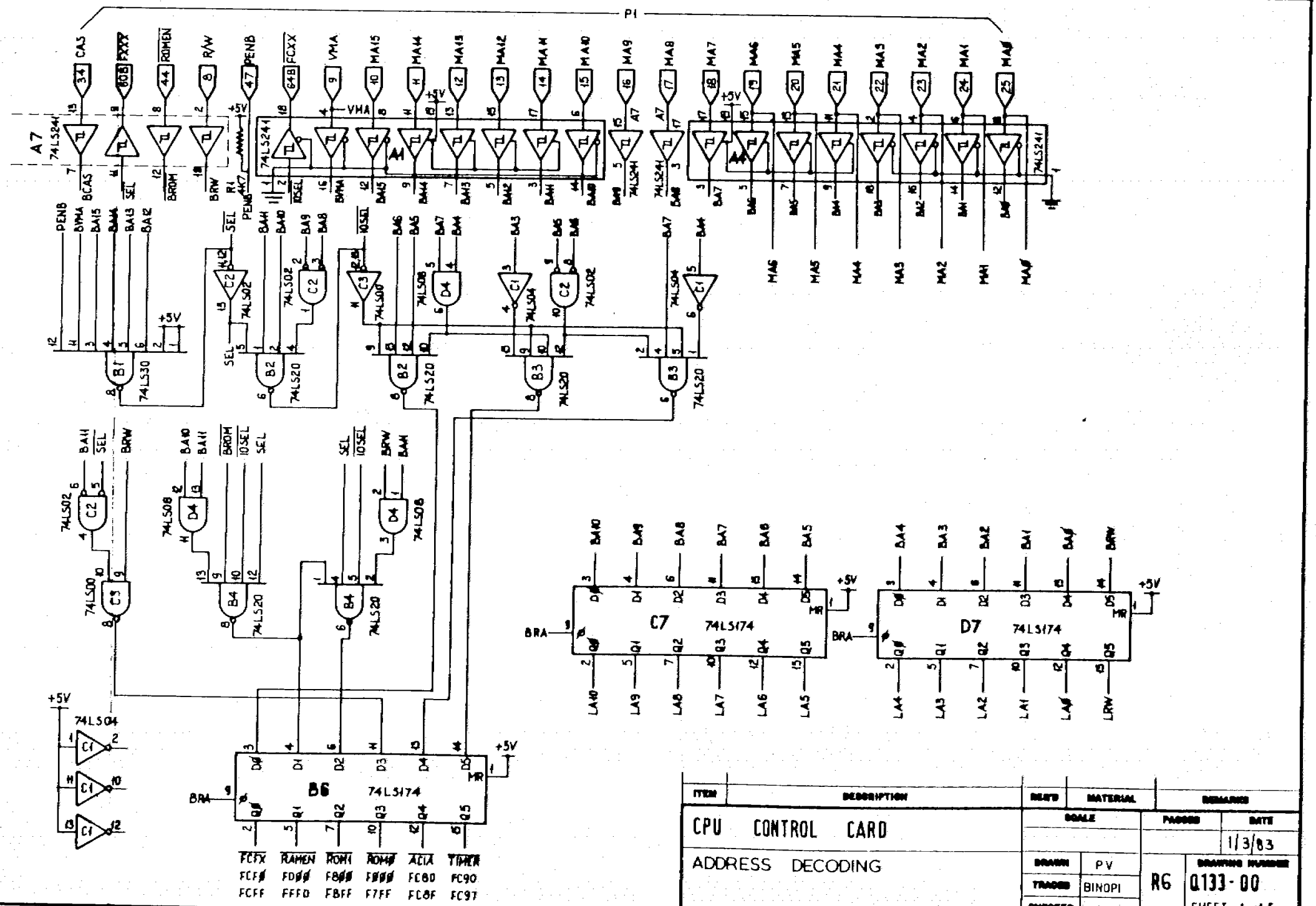

DUAL 6809 CPU
PROCESSORS ETC.
DRAWN
TRACED
CHECKED
SCALE
MATERIAL
PASSED
DATE
12-12-82
DRAWING NUMBER
Q209 - 01
SHEET 2 of 4
A7
REMARKS
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ITEM
6809 E
5,6B,C
1,2B,C
74LS139
74LS259
74LS32
74LS00
74LS04
74LS05
74LS08
74LS10
74LS14
74LS86
74LS02
7402
74LS74
RESET
HALT
NMI
IRQ
FIRQ
R/W
BUSY
TSC
LIC
VCC
VSS
BA
BS
VFETCH 2
VFETCH 1
HANG 2
HANG 1
VMA2
VMA1
INT(2)
INT(1)
ROMEN
SYRES
RW(2)
RW(1)
BUSY 2
BUSY 1
BA2
BA1
A12
A22
A32
A11
A21
A31
ADD2
ADD1
R1
3K3
RN2-2 3K3
RN2-4 3K3
RN2-5 3K3
RN2-6 3K3
RN2-8 3K3
RN1-2 3K3
RN1-3 3K3
RN1-4 3K3
RN1-5 3K3
RN1-6 3K3
RN2-7 3K3
+5V
IPI1
IPI2
P1LS
P2LS
BD0
BD1
BD2
BD3
MS1
MS2



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
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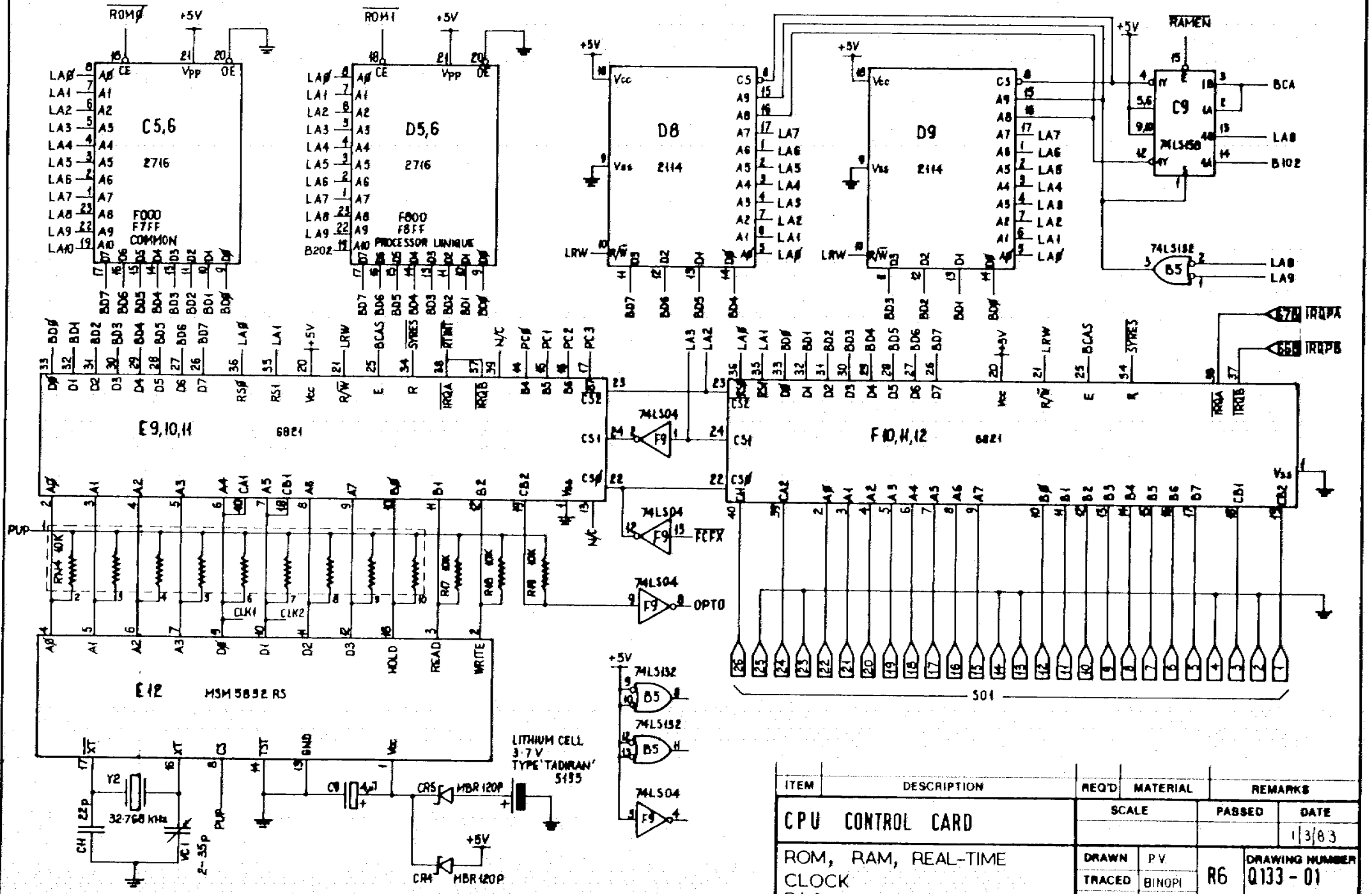


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BUS INTERFACE		DRAWN P V TRACED BINOPI CHECKED	R7	DRAWING NUMBER Q209-03 SHEET 4 of 4

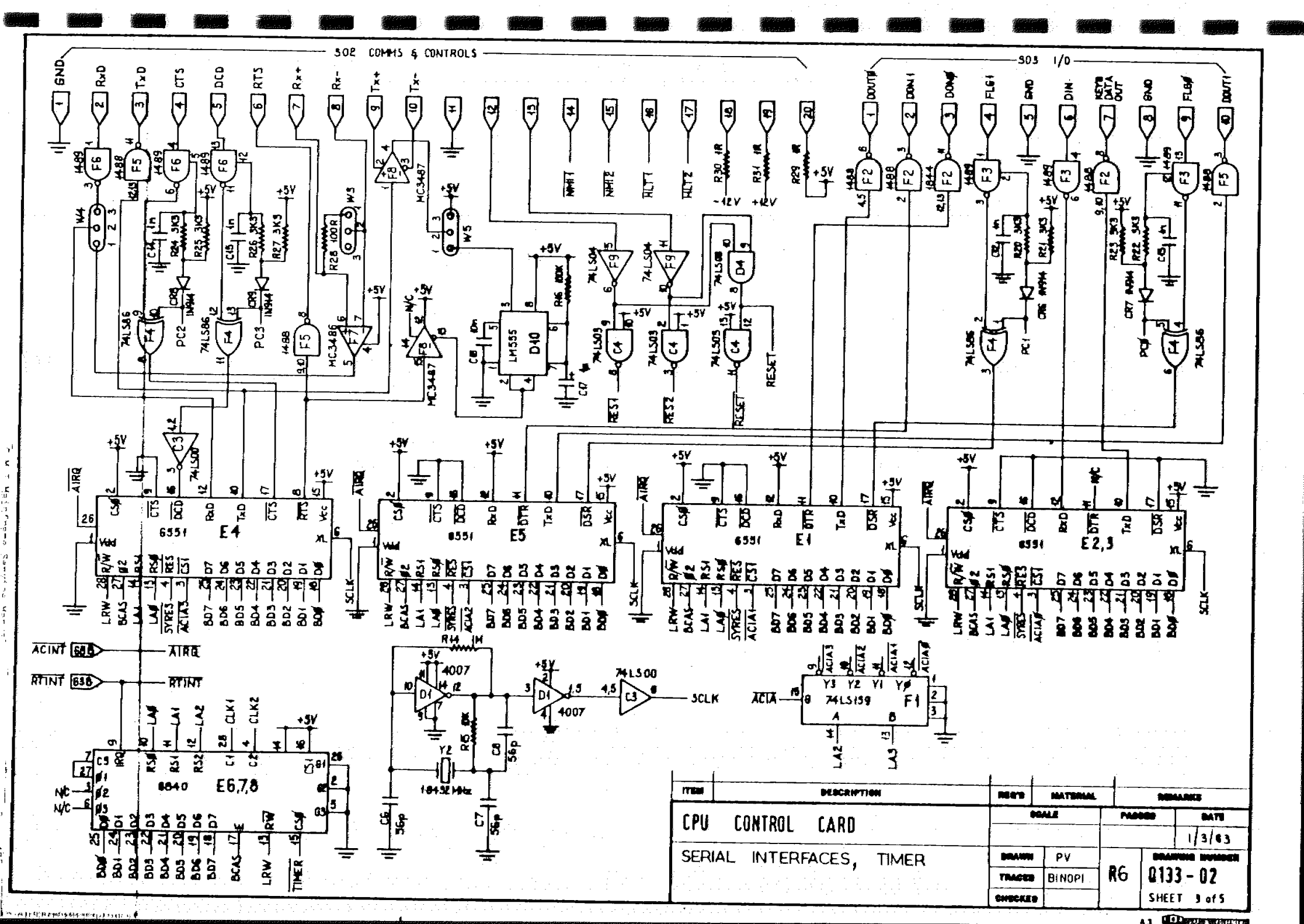


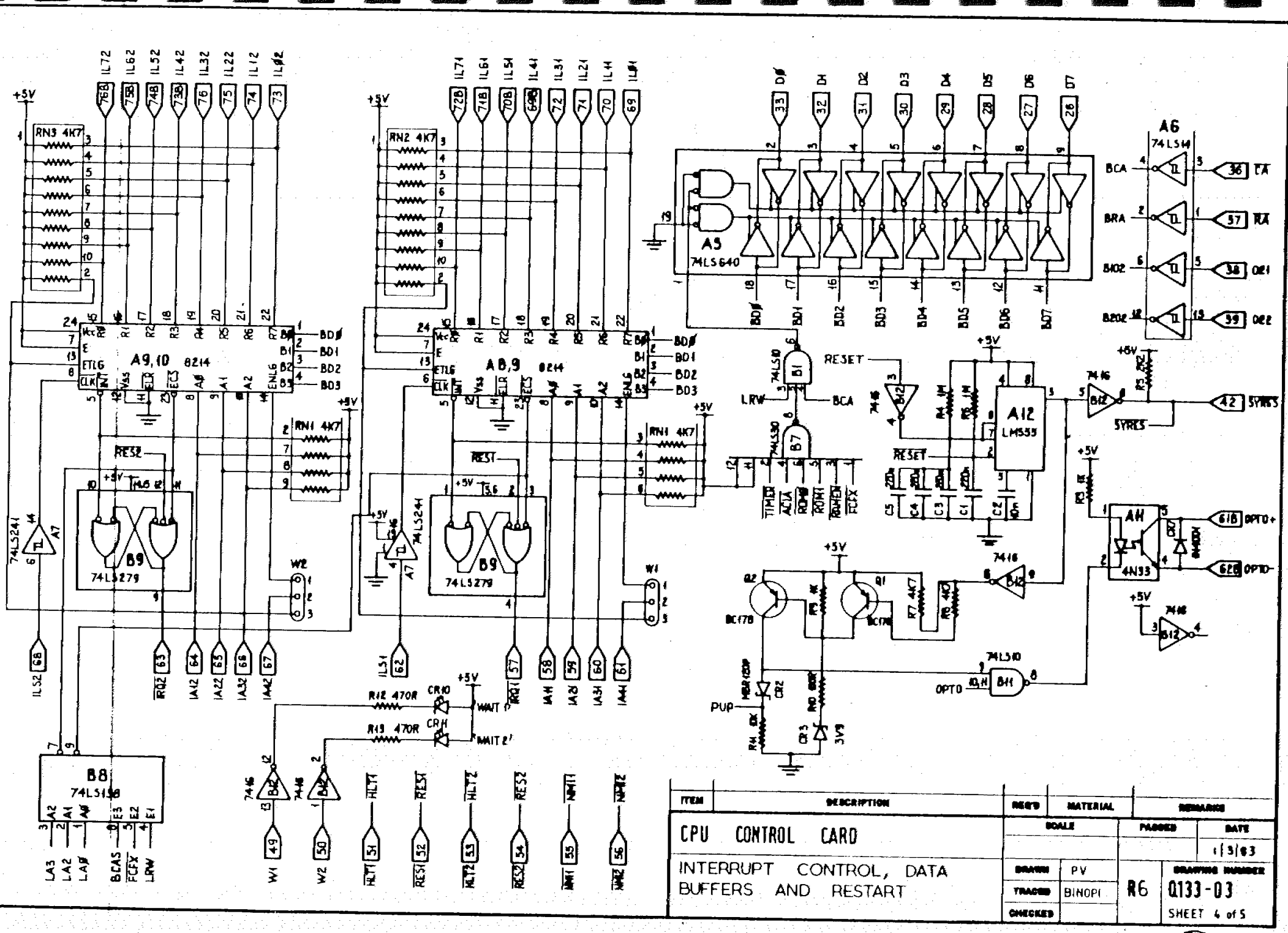
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ADDRESS DECODING				1/3/83
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		TRACED BINOPI		SHEET 1 of 5
		CHECKED		

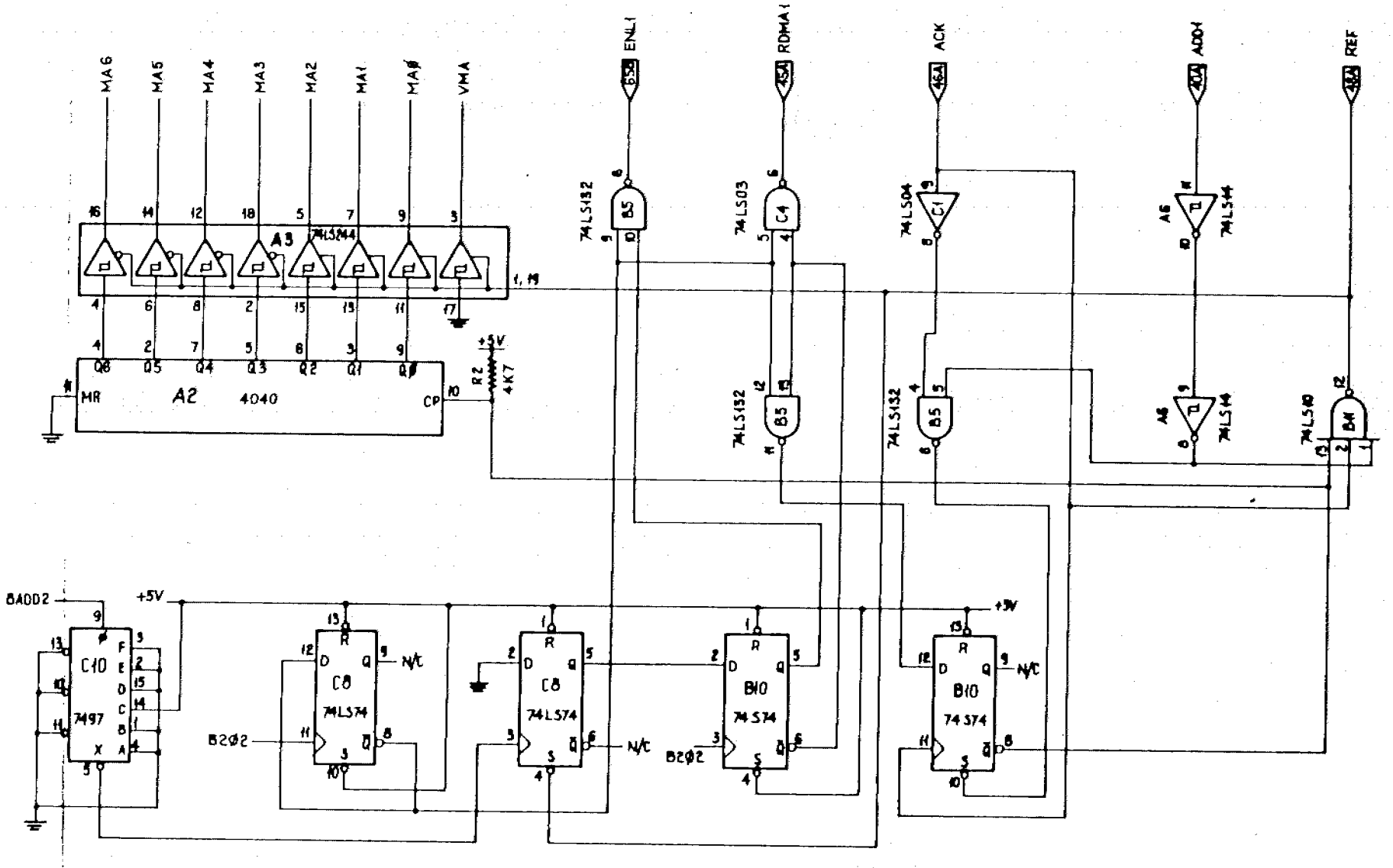
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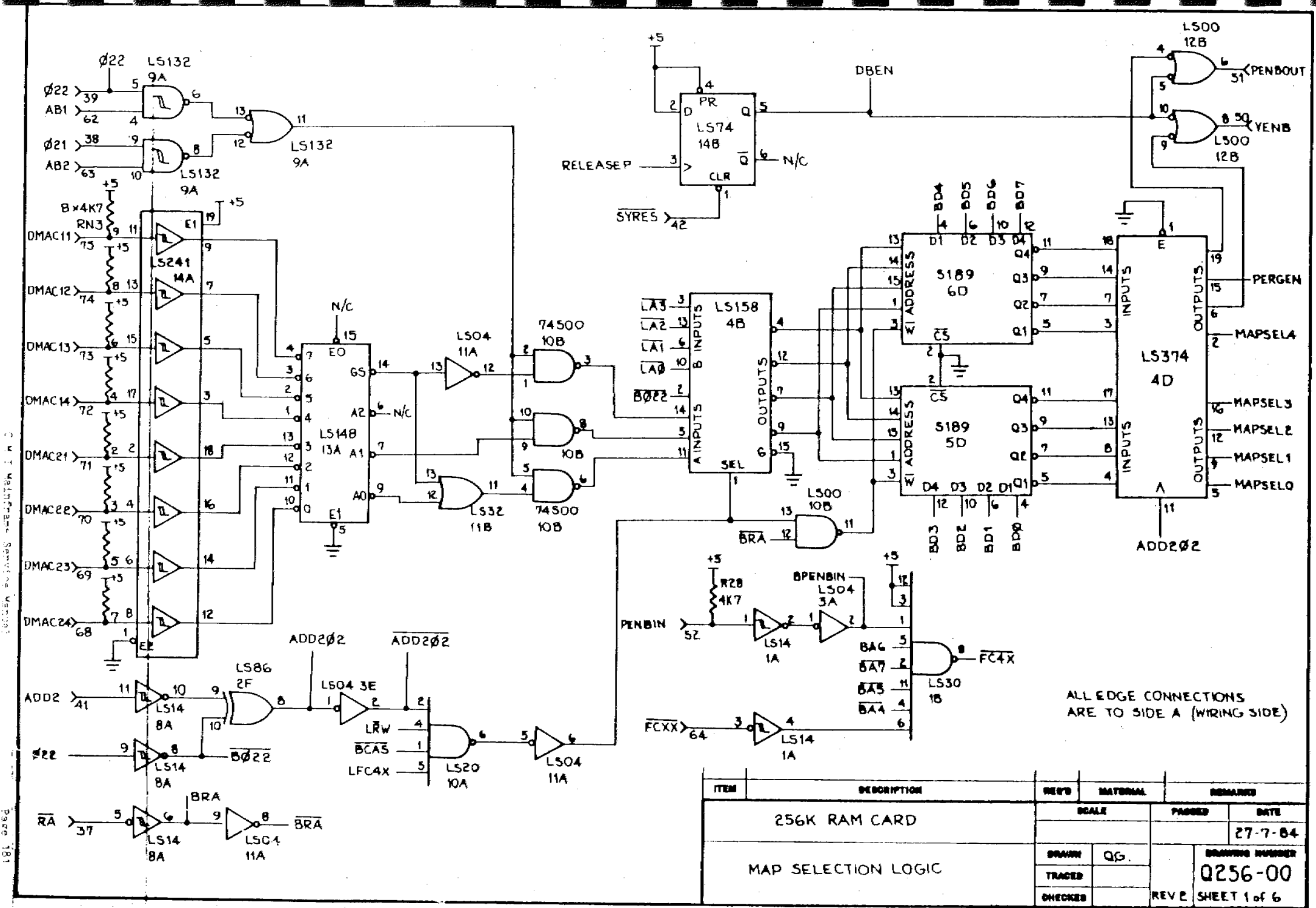

S02 COMMS & CONTROLS
S03 I/O
GND
RxD
TxD
CTS
DCD
RTS
Rx+
Rx-
Tx+
Tx-
NMI1
NMI2
RLT1
RLT2
-12V
+12V
+5V
DOUT0
DOUT1
DOUT2
FLG1
FLG0
DIN
KEYB DATA OUT
LM555
MC3487
MC3486
74LS00
74LS04
74LS08
74LS03
74LS86
74LS05
74LS06
74LS159
4007
6551
6840
E4
E5
E1
E2,3
E6,7,8
RESET
ACINT
RTINT
ATRQ
SCLK
ACIA
18432 MHz
CPU CONTROL CARD
SERIAL INTERFACES, TIMER
DRAWN PV
TRACED BINOPI
CHECKED
DATE 1/3/83
DRAWING NUMBER R6 Q133-02
SHEET 3 of 5

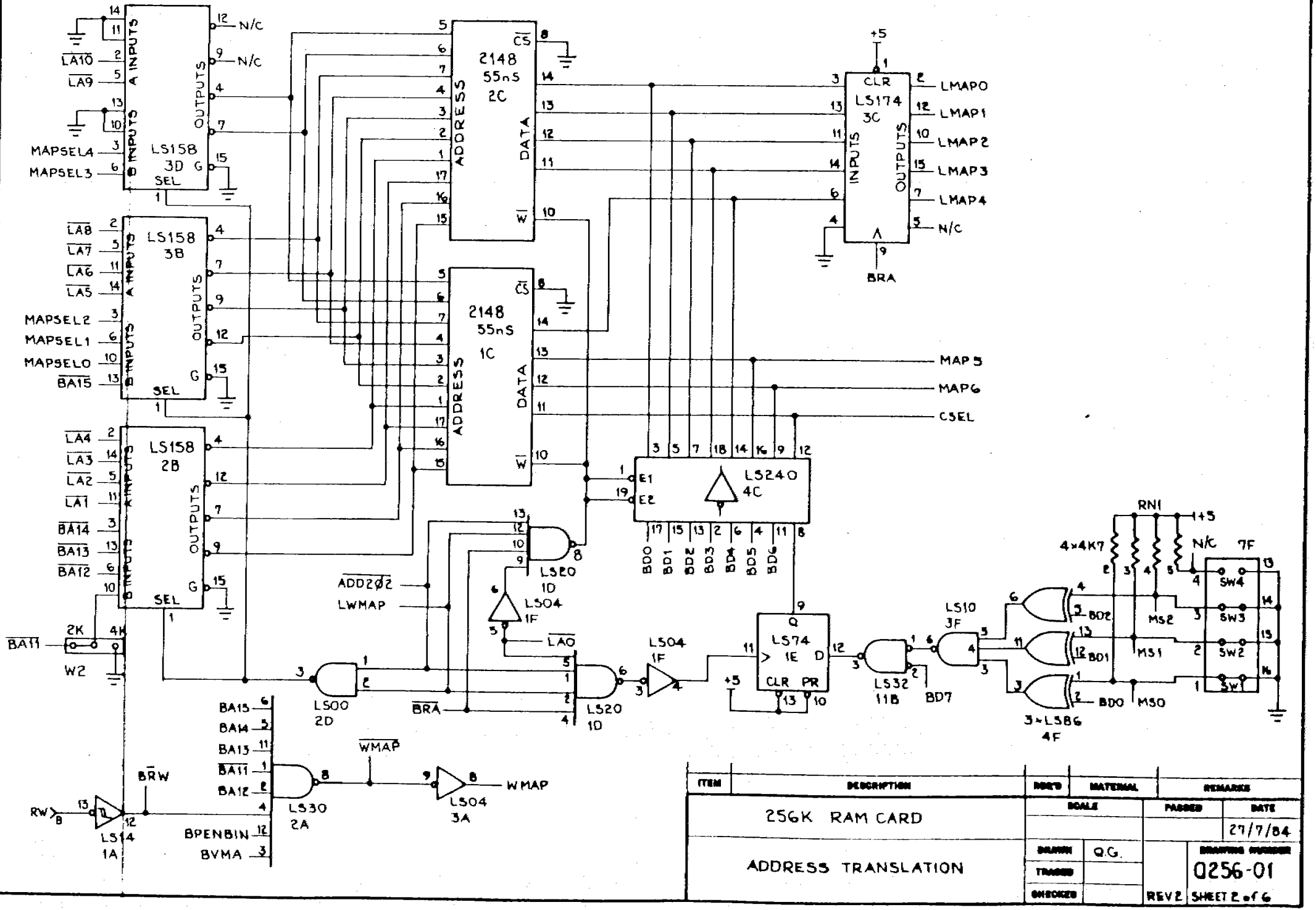

CPU CONTROL CARD
INTERRUPT CONTROL, DATA BUFFERS AND RESTART
DRAWN PV
TRACED BINOPI
CHECKED
R6
Q133-03
SHEET 4 of 5
1/3/83
A5 74LS640
A6 74LS14
A7 74LS241
A8,9 8214
A9,10 8214
A12 LM555
AH 4N33
B7 74LS30
B8 74LS138
B9 74LS279
B11 74LS10
B12 7416
RN1 4K7
RN2 4K7
RN3 4K7
RESET
WAIT
OPTO
PUP
BC178
3V9



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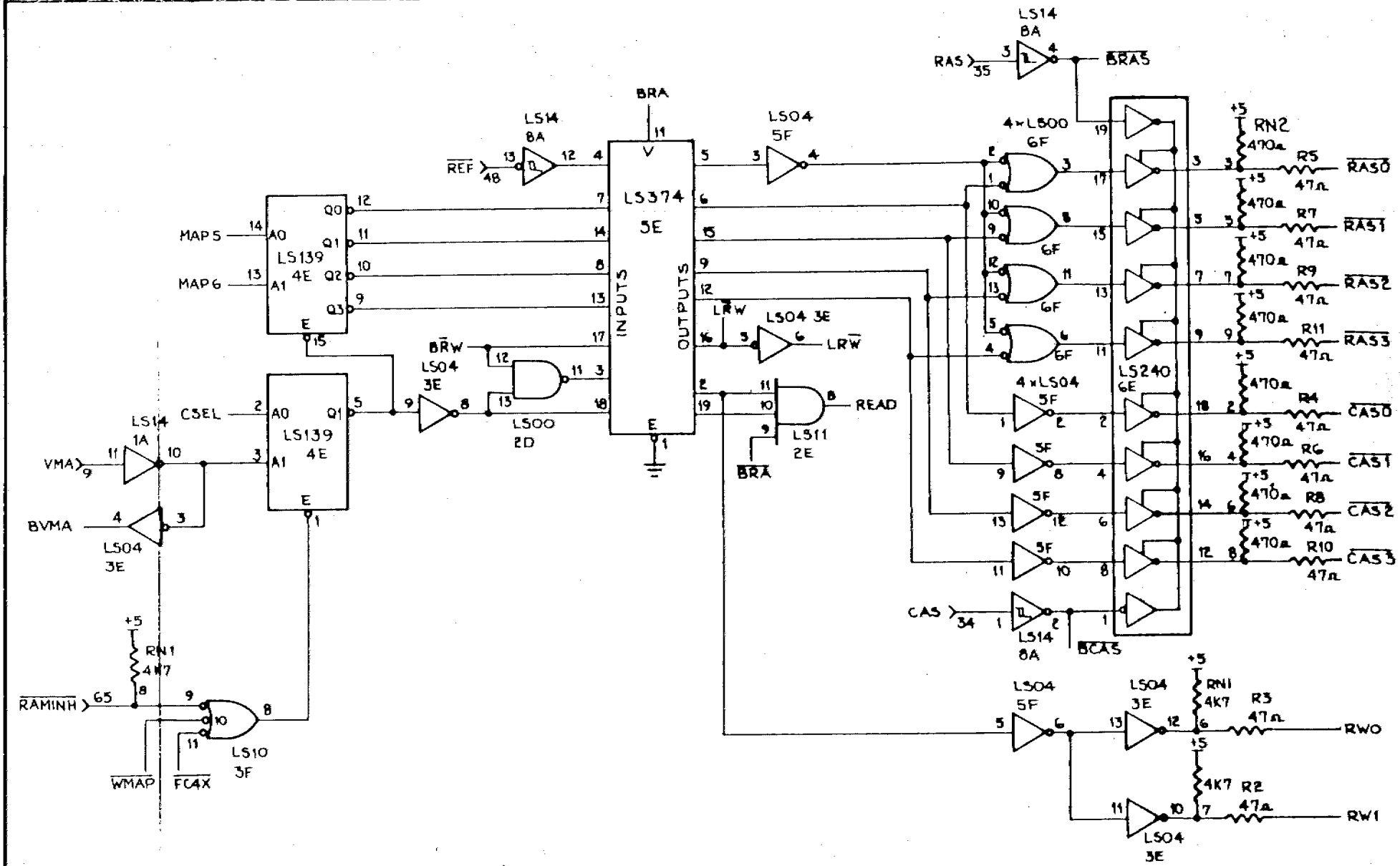
A3


Ø22
LS132
9A
AB1
AB2
Ø21
+5
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DMAC21
DMAC22
DMAC23
DMAC24
LS241
14A
EO
GS
A2
A1
A0
LS148
13A
N/C
LS04
11A
74S00
10B
LS32
11B
LA3
LA2
LA1
LA0
BØ22
LS158
4B
A INPUTS
B INPUTS
OUTPUTS
SEL
DBEN
PR
CLR
LS74
14B
RELEASEP
SYRES
S189
6D
5D
WE ADDRESS
CS
BD4
BD5
BD6
BD7
BD3
BD2
BD1
BD0
LS374
4D
INPUTS
OUTPUTS
ADD2Ø2
LS00
12B
PENBOUT
YENB
PERGEN
MAPSEL4
MAPSEL3
MAPSEL2
MAPSEL1
MAPSEL0
BRA
LS00
10B
PENBIN
R28
4K7
LS14
1A
BPENBIN
LS04
3A
BA6
BA7
BA5
BA4
LS30
1B
FC4X
FCXX
ADD2
LS86
2F
LS04 3E
LRW
BCAS
LFC4X
LS20
10A
RA
LS14
8A
LS04
11A
ALL EDGE CONNECTIONS
ARE TO SIDE A (WIRING SIDE)
ITEM
DESCRIPTION
REV'D
MATERIAL
REMARKS
256K RAM CARD
SCALE
PASSED
DATE
27-7-84
MAP SELECTION LOGIC
DRAWN
QG.
TRACED
CHECKED
REV E
DRAWING NUMBER
Q256-00
SHEET 1 of 6



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
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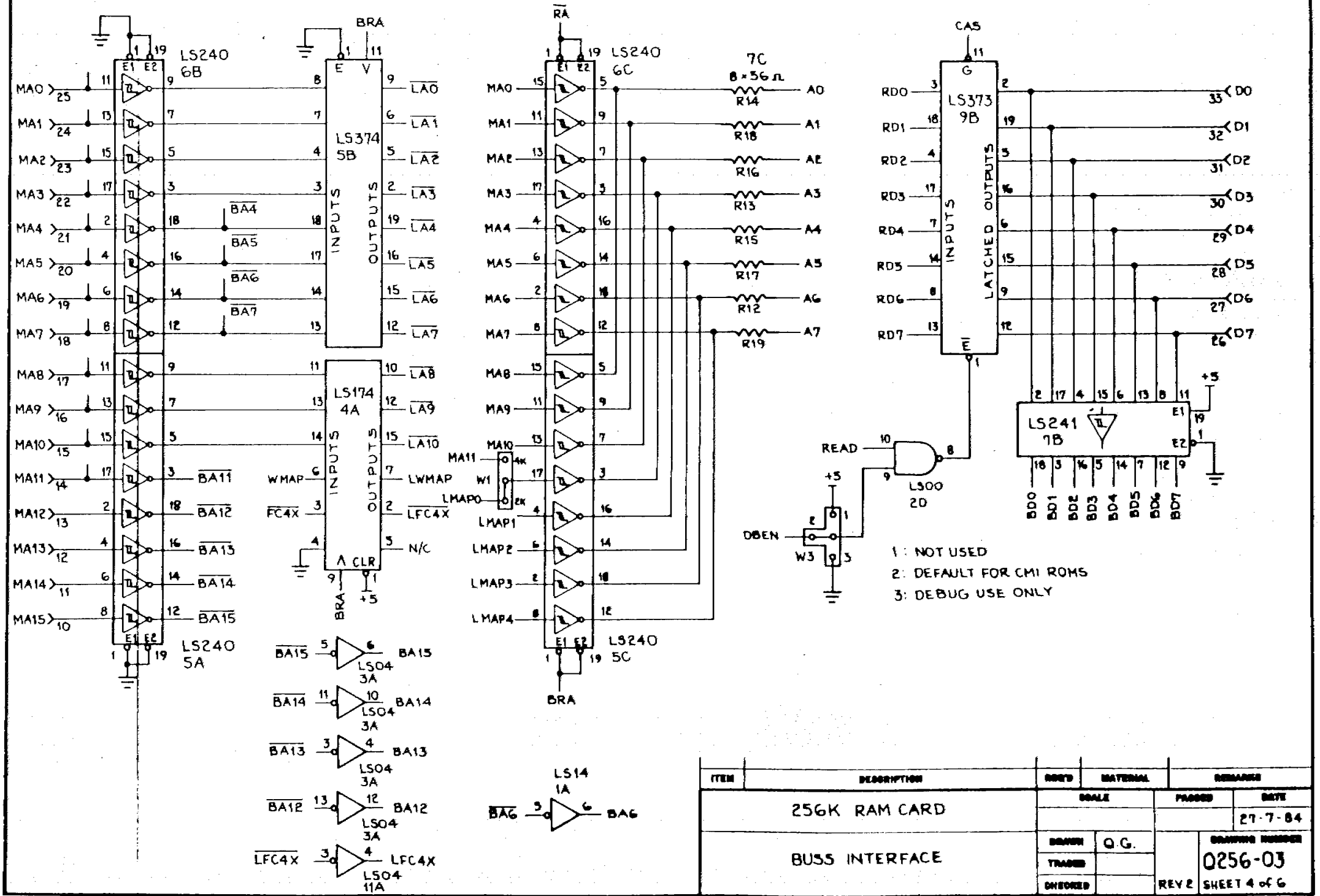
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NOTE 70nS ACCESS TIME 2148's MAY BE USED AT 1C AND 2C PROVIDED AN S139 IS USED AT 4E

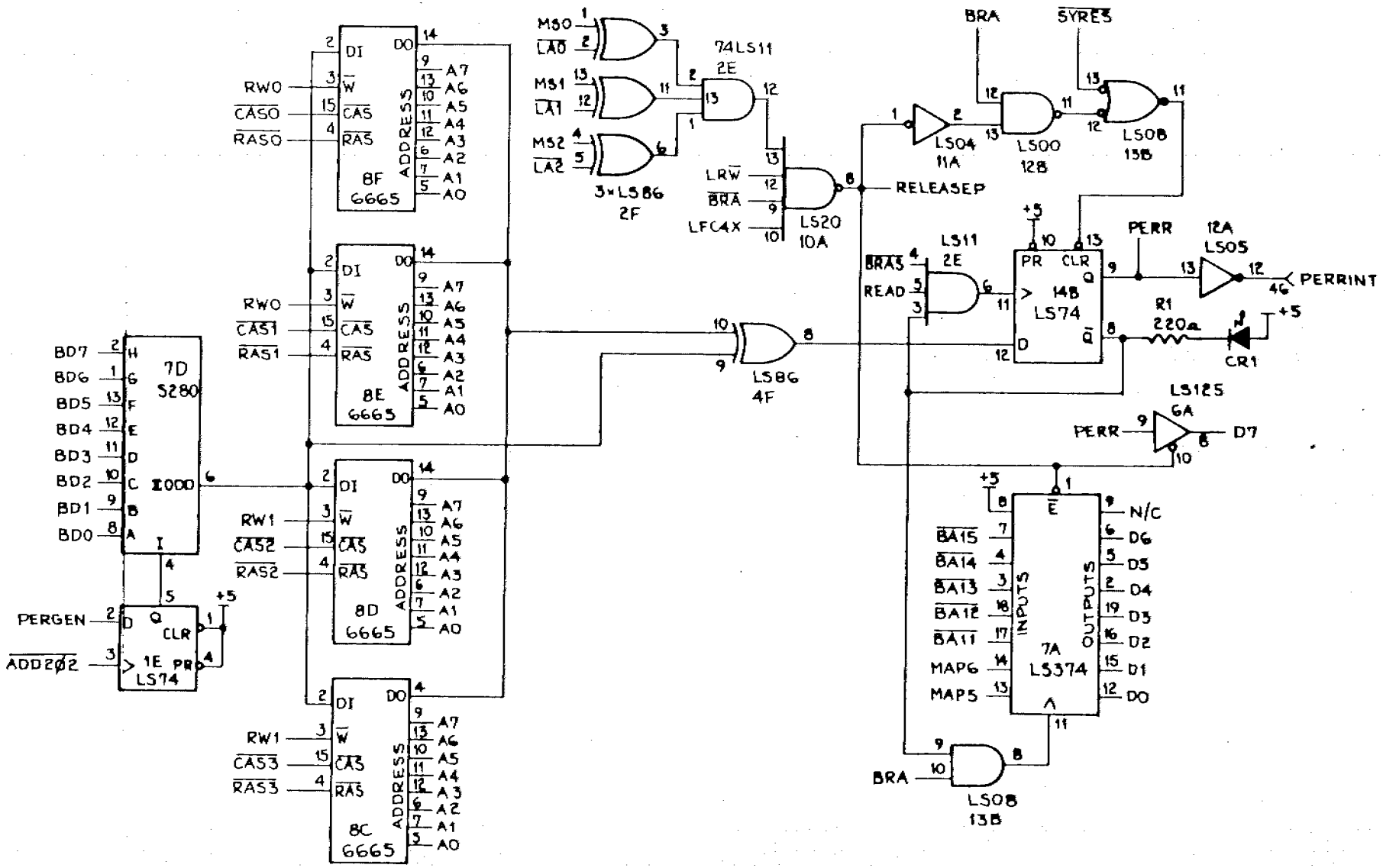
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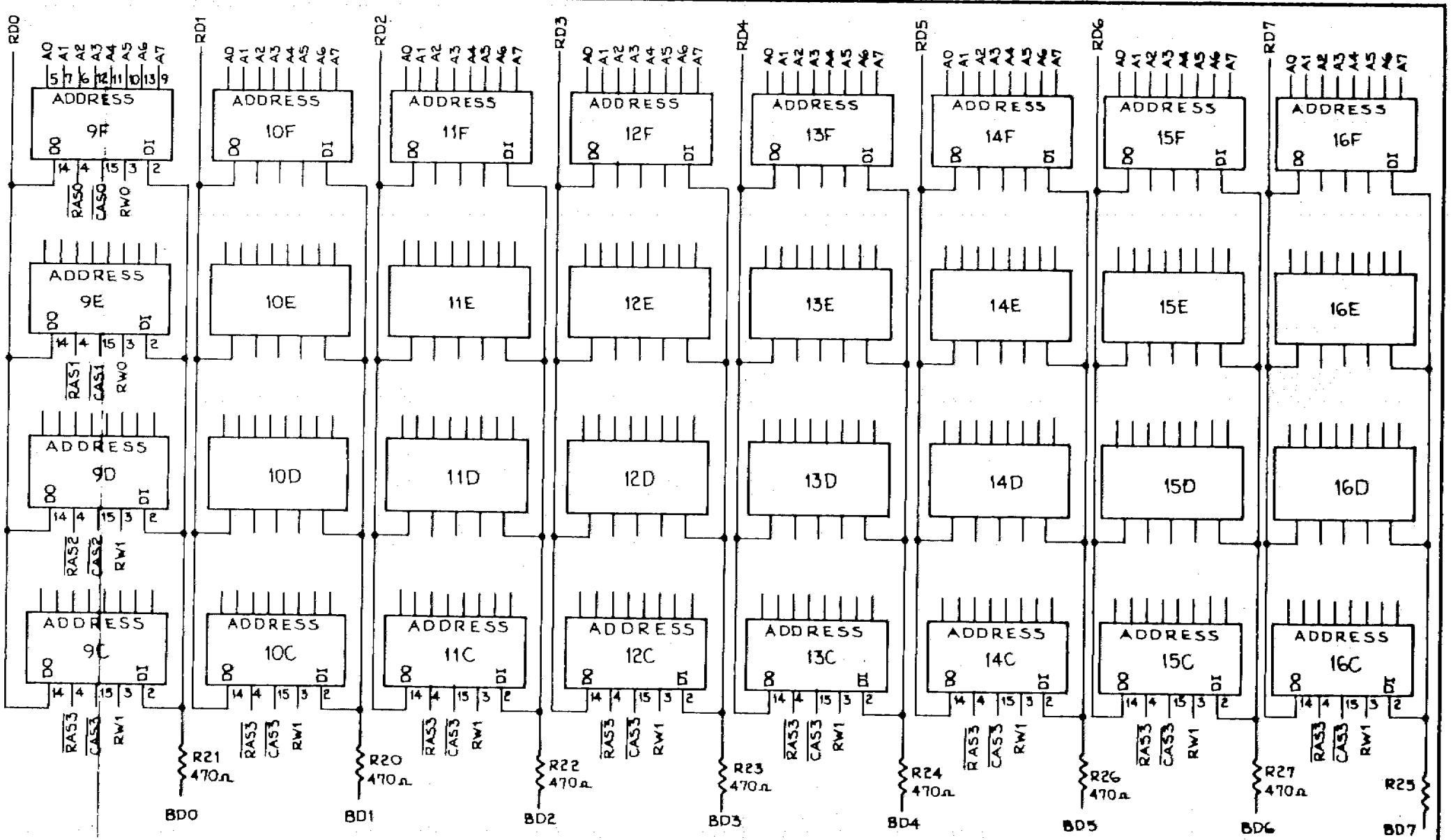


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A3



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
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				27/7/84
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		CHECKED		REV 2 SHEET 5 of 6

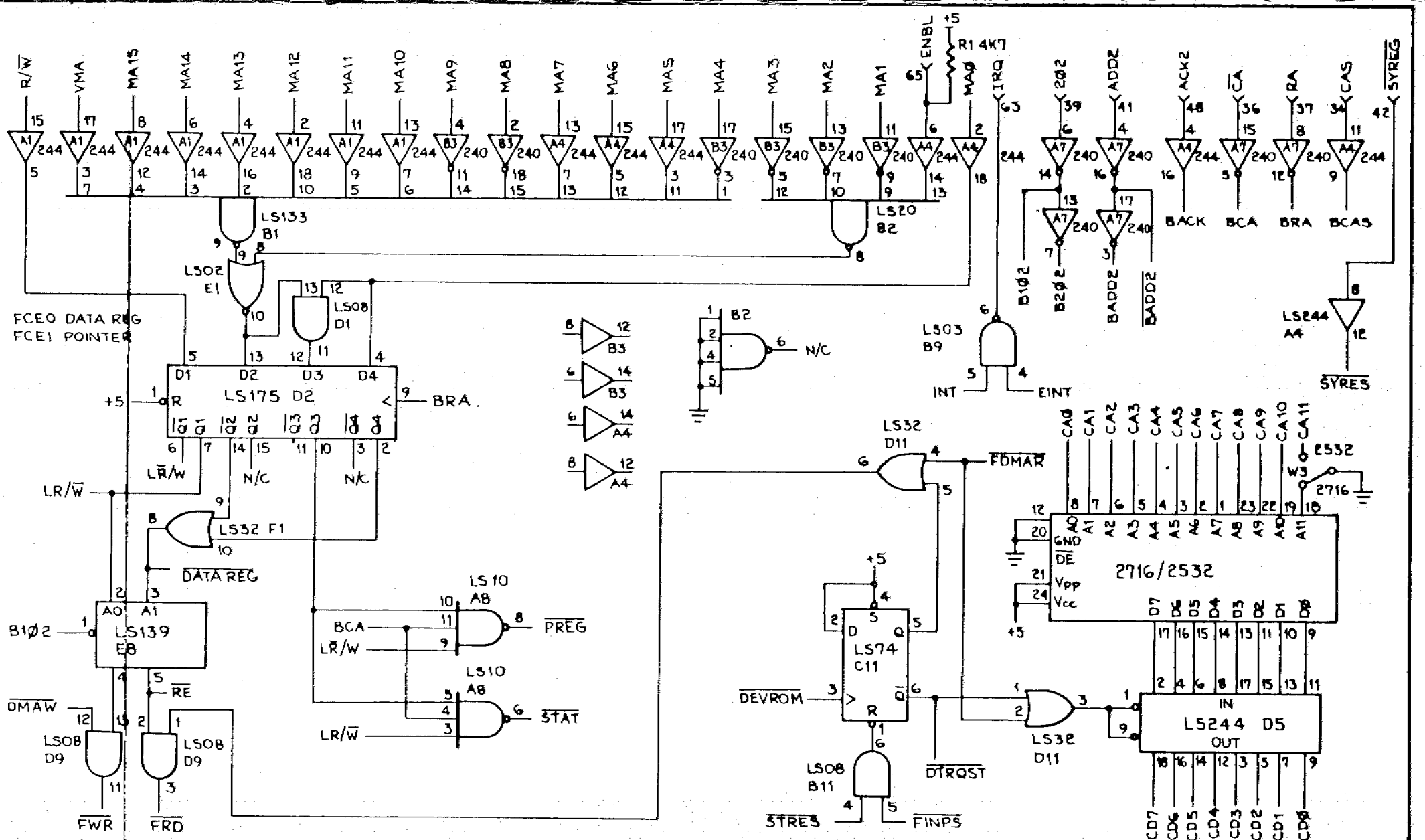


ALL IC's 6665

N.B. Vcc +5V - PIN 8
Vss GND - PIN 16
TIE PIN 1 TO +5V

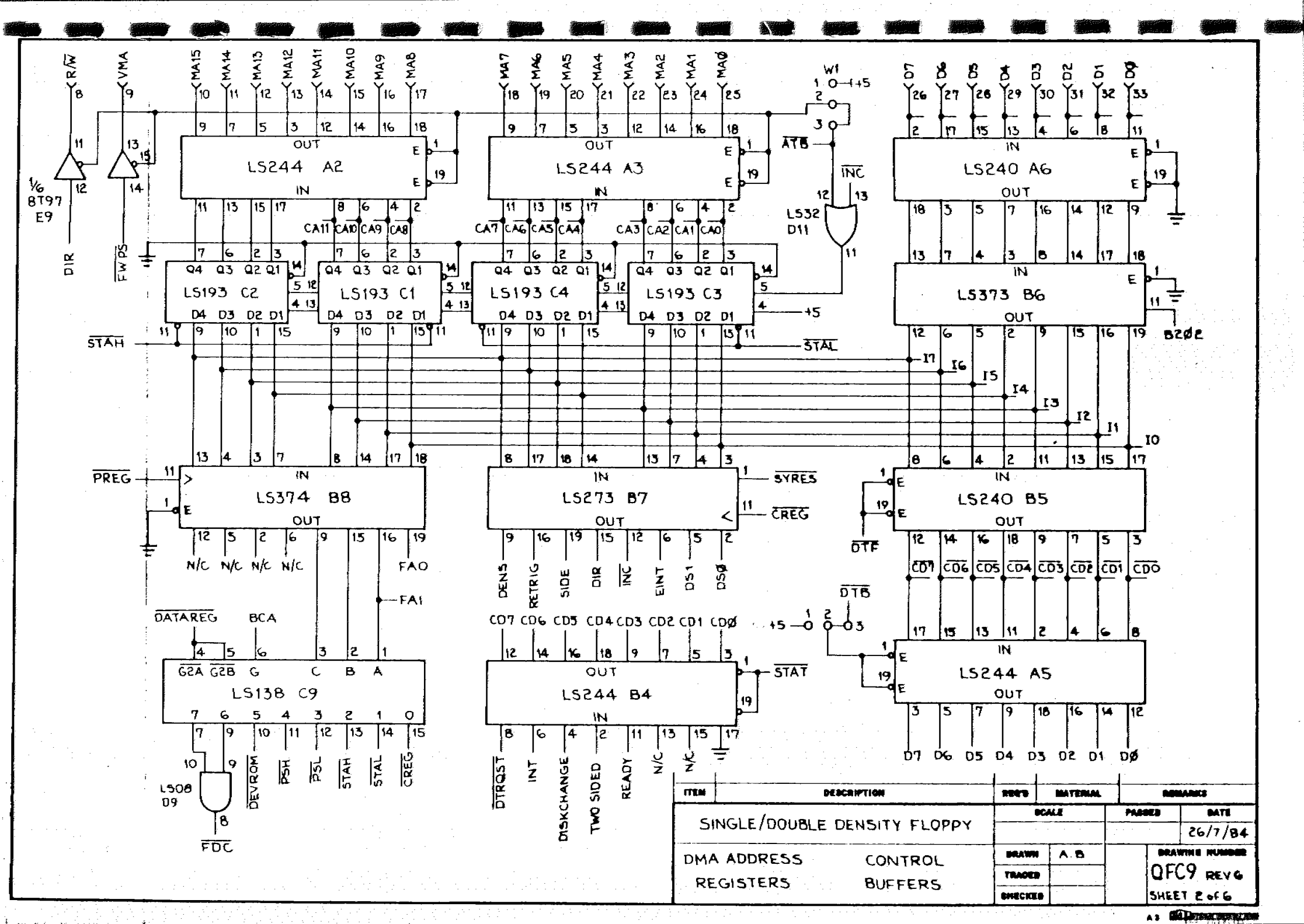
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		CHECKED	REV 2	SHEET 6 of 6

A3



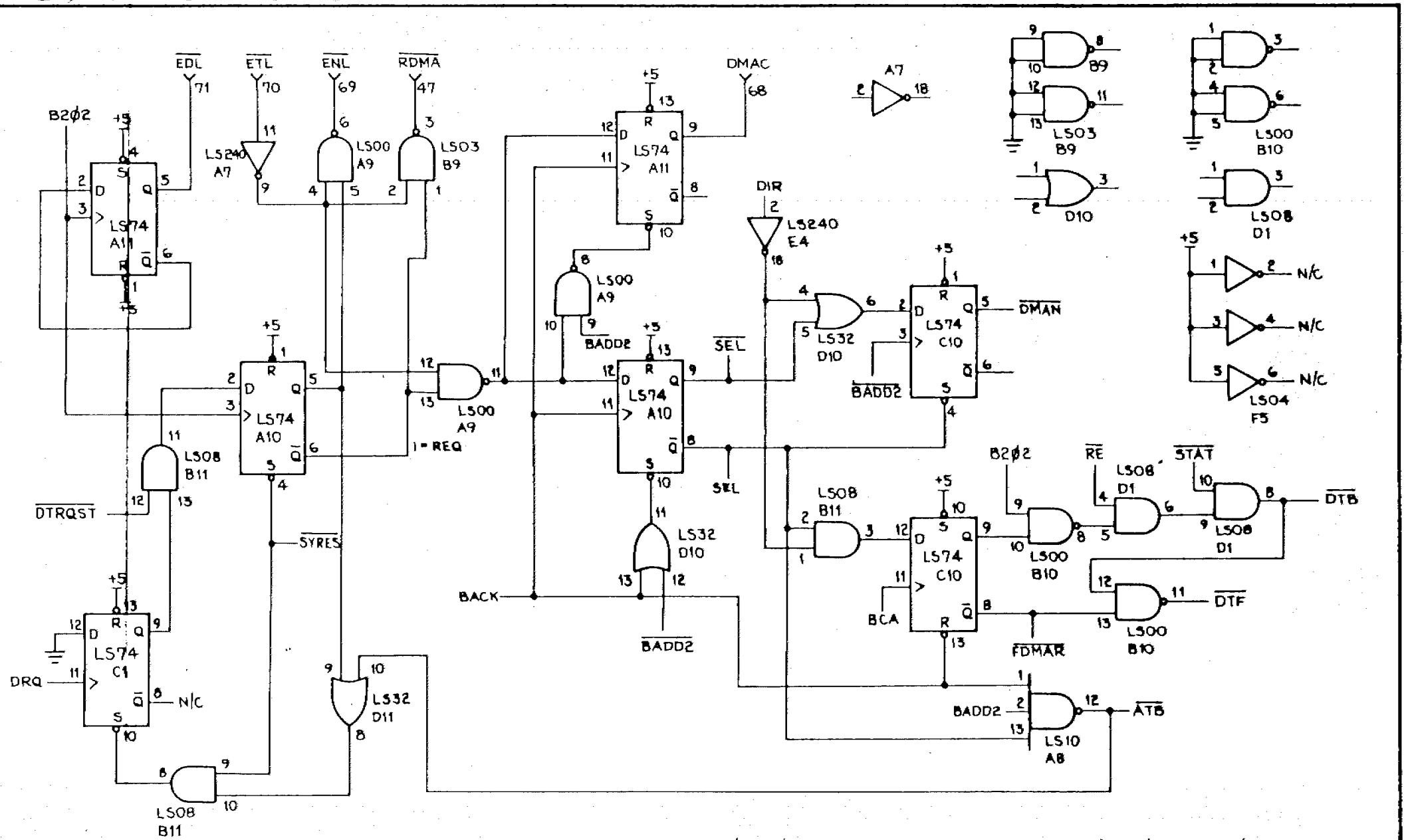
ALL UNMARKED NON INVERTING BUFFERS LS244
" " INVERTING " LS240
WITH PINS 1 AND 19 GROUNDED.

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE / DOUBLE DENSITY FLOPPY		SCALE		PASSED / DATE 26/7/84
ADDRESS / CONTROL BUFFERS DEVICER DRIVER ROM.		DRAWN A.B.		DRAWING NUMBER QFC9 REV6
		TRACED		SHEET 1 of 6
		CHECKED		



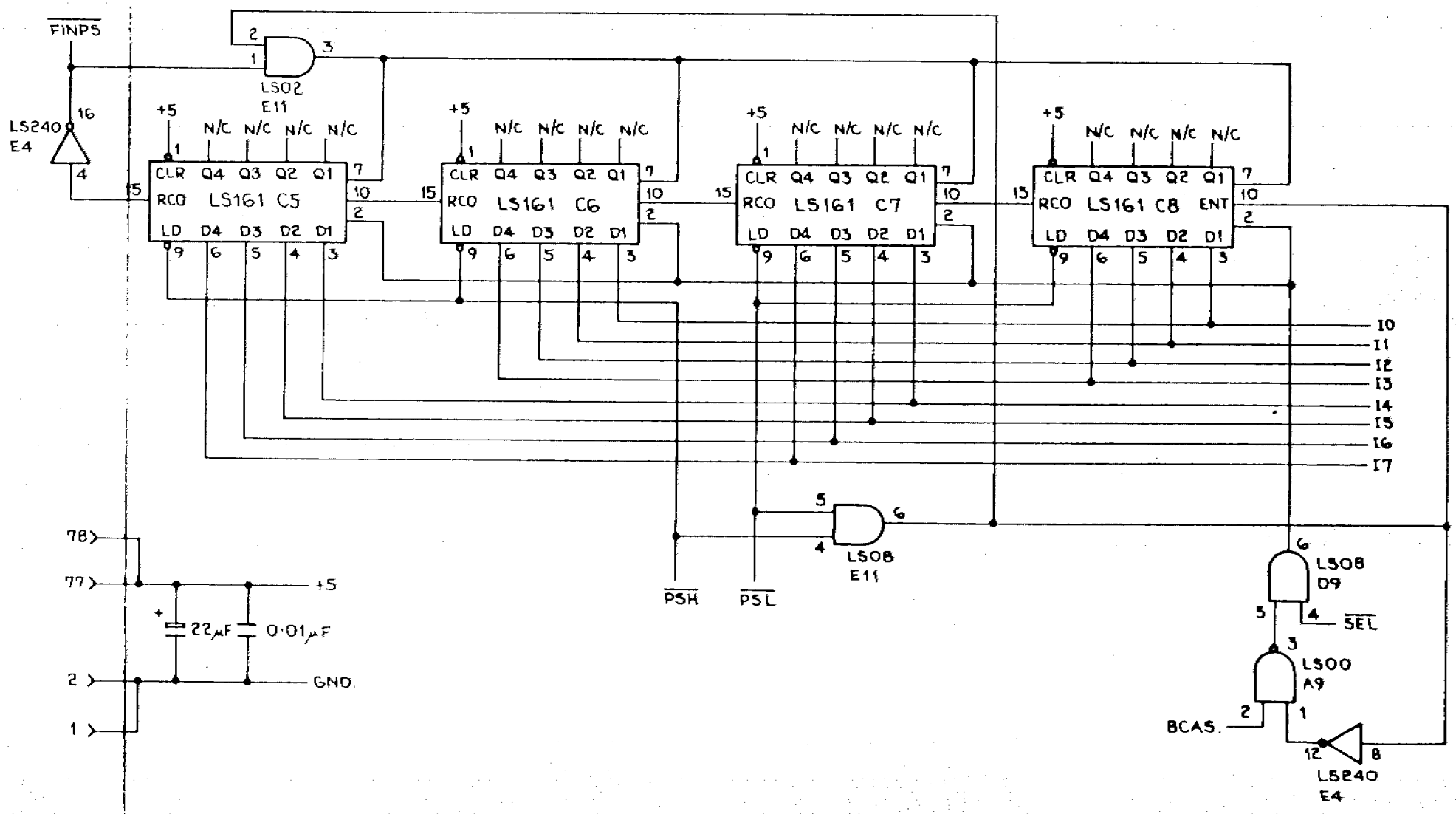
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE/DOUBLE DENSITY FLOPPY		SCALE	PASSED	DATE 26/7/84
DMA ADDRESS REGISTERS CONTROL BUFFERS		DRAWN A.B TRACED CHECKED		DRAWING NUMBER QFC9 REV G SHEET 2 of 6

A3



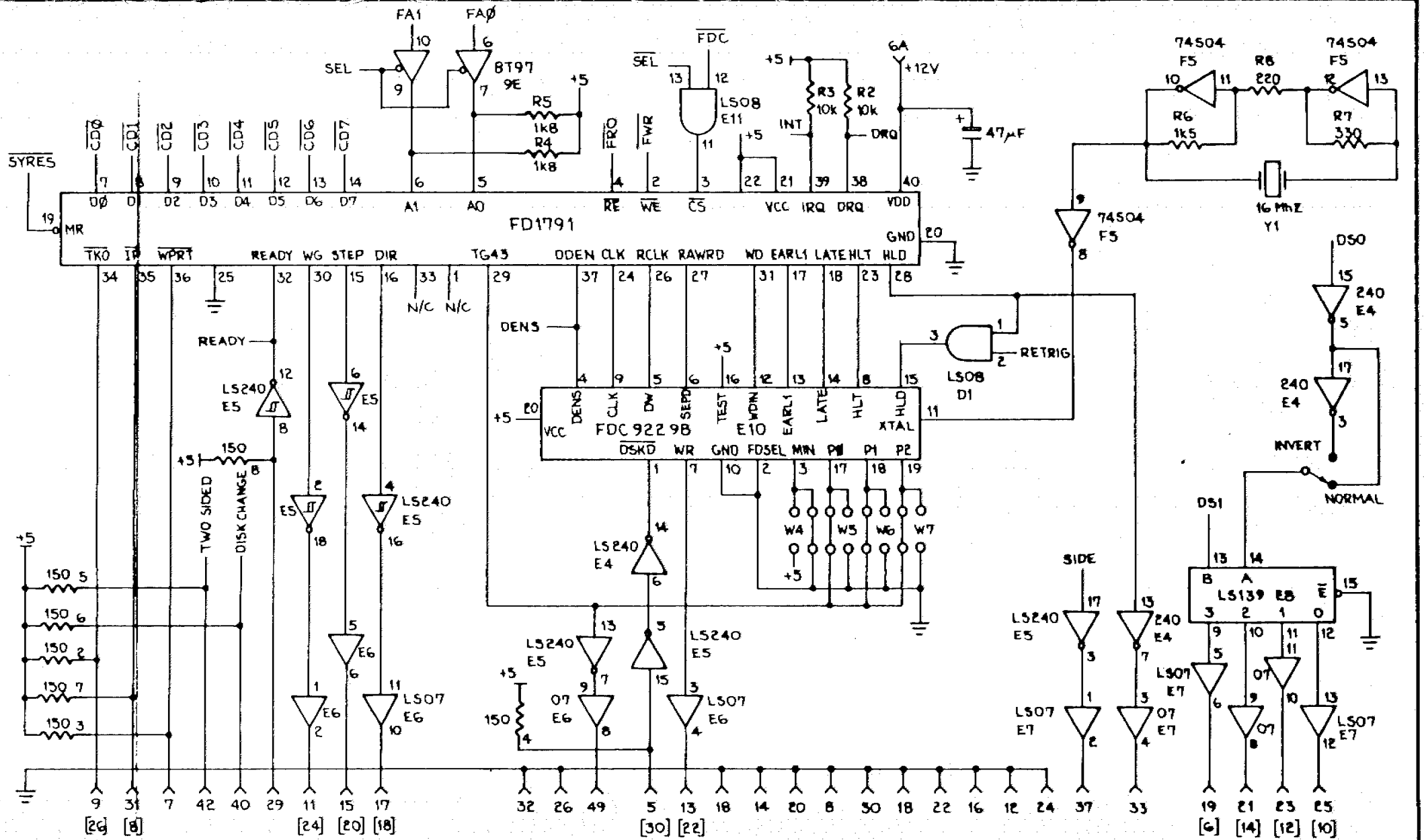
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	SINGLE/DOUBLE DENSITY FLOPPY	SCALE		PASSED / DATE 26/5/84
	DMA LOGIC DAISY CHAIN	DRAWN A.B. / TRACED / CHECKED		DRAWING NUMBER QFC9 REV 6 SHEET 3 of 6

A3



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE / DOUBLE DENSITY FLOPPY		SCALE		PASSED / DATE: 24-7-84
BYTE TRANSFER COUNTER		DRAWN: A.B.		DRAWING NUMBER: QFC9 REV 6
		TRACED		SHEET 4 of 6
		CHECKED		

A3



NUMBERS IN [ ] REFER TO 5¼" DISK 34 WAY CONNECTOR WHICH HAS ALL ODD PINS GROUNDED.

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
SINGLE/DOUBLE DENSITY FLOPPY		SCALE	PAGE NO	DATE
FDC/BUFFERS PLL		DRAWN A.B.		DRAWING NUMBER QFC9 REV 6
		TRACED		SHEET 5 of 6
		CHECKED		

A3

1		2	GND
3		4	HDL3
5	READ DATA	6	HDL2
7	WRITE PROTECT	8	
9	TRACK Ø	10	
11	WRITE GATE	12	
13	WRITE DATA	14	
15	STEP	16	
17	DIRECTION	18	
19	DS4	20	
21	DS3	22	
23	DS2	24	
25	DS1	26	
27		28	HDL1
29	READY	30	
31	INDEX	32	
33	HEAD LOAD	34	HDLØ
35	ALT	36	IN USE
37	SIDE SELECT	38	
39		40	DISK CHANGE
41		42	TWO SIDE
43		44	
45		46	
47		48	
49	LOW CURRENT	50	

ITEM | DESCRIPTION | SHEETS | MATERIAL | REMARKS

SINGLE DOUBLE DENSITY FLOPPY

CABLE CONNECTOR SIGNAL 5

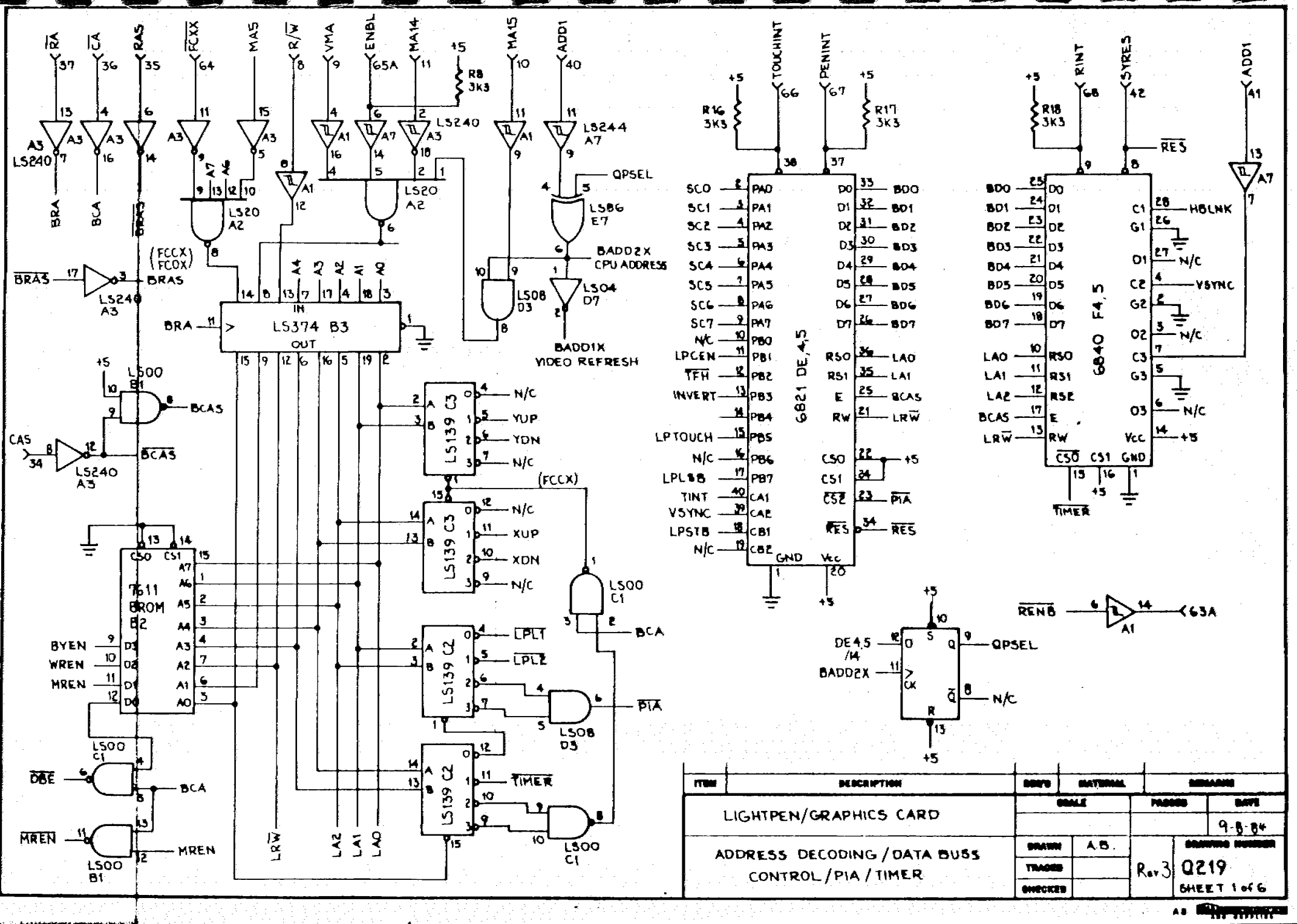
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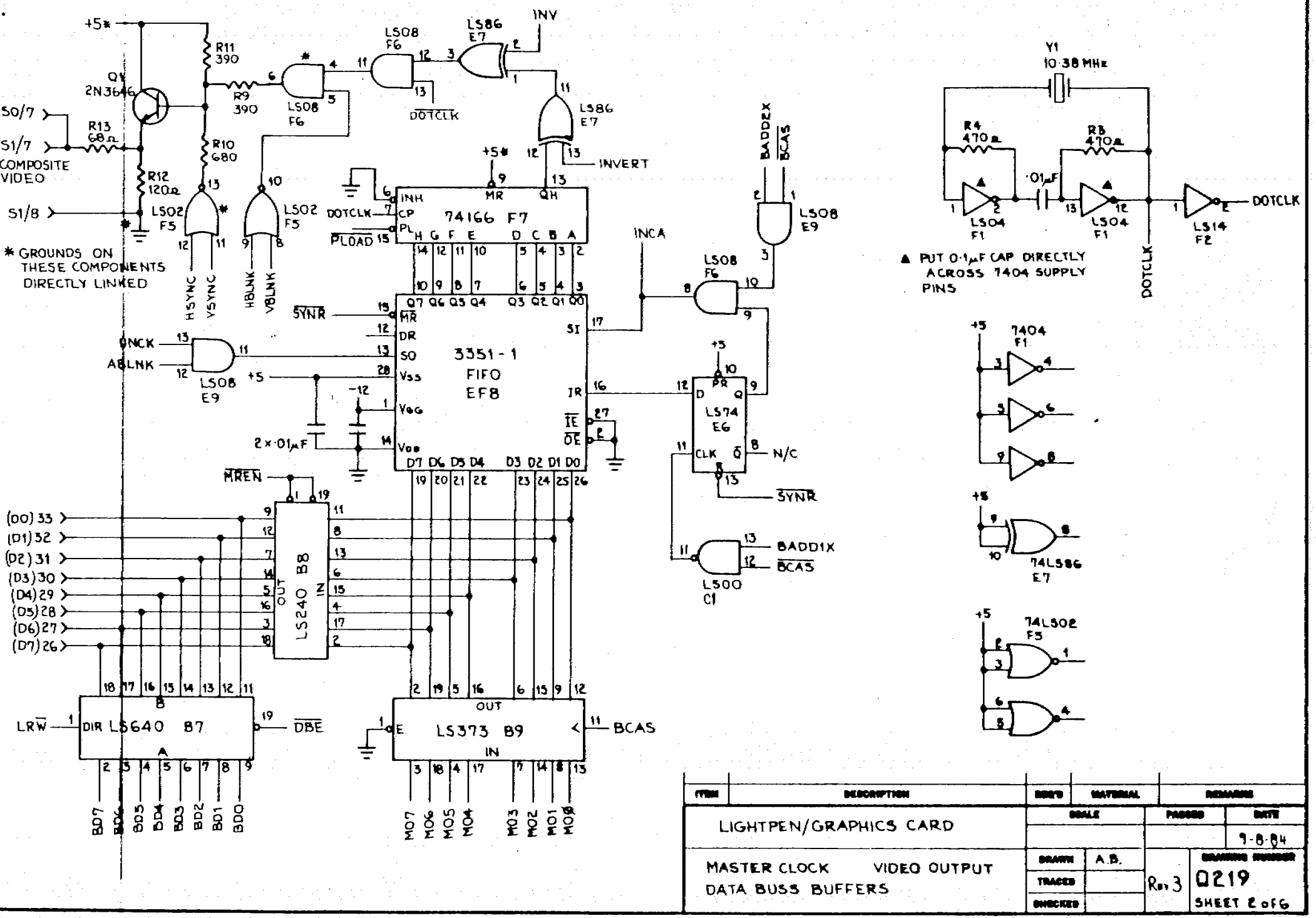
SCALE | DRAWN A.B. | TRACED | CHECKED

PROVED | DATE 24-7-84

DRAWING NUMBER QFC9 REV C

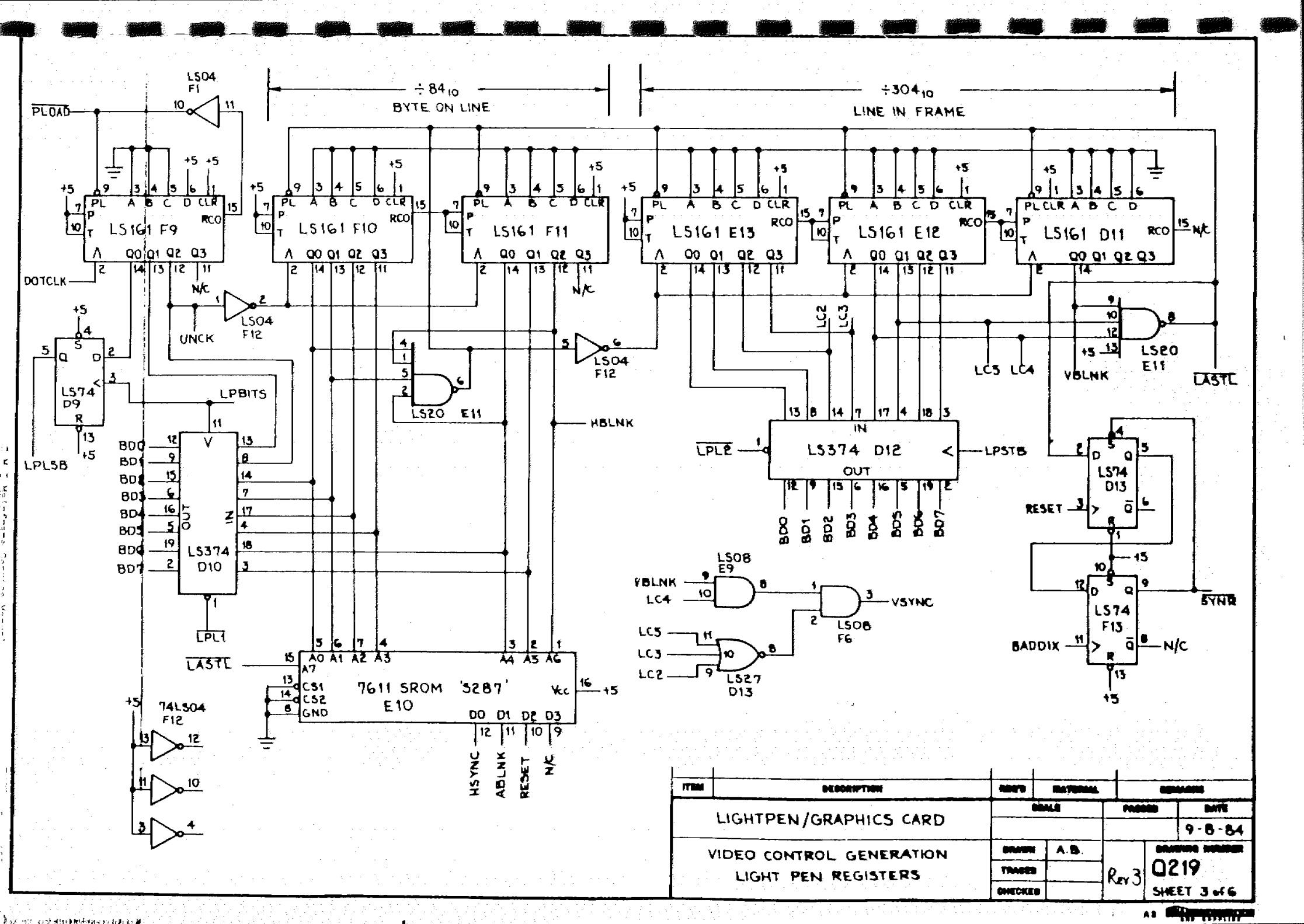
SHEET 6 of 6


LS240 A3
LS240 A2
LS374 B3
OUT
LS139 C3
LS139 C2
LS08 D3
LS00 C1
LS00 B1
LS04 D7
LS86 E7
LS244 A7
6821 DE,4,5
6840 F4,5
7611 BROM B2
R8 3K3
R16 3K3
R17 3K3
R18 3K3
BRA
BCA
BRAS
BCAS
MRAS
MCAS
MREN
BYEN
WREN
QPSEL
BADD2X
CPU ADDRESS
BADD1X
VIDEO REFRESH
TOUCHINT
PENINT
RINT
VSYNC
HBLNK
TIMER
PIA
RES
RENB
LPLT
LPLT2
XUP
XDN
YUP
YDN
LRW
LA2
LA1
LA0
TITLE
LIGHTPEN/GRAPHICS CARD
ADDRESS DECODING / DATA BUSS
CONTROL / PIA / TIMER
A.B.
Rev 3
Q219
SHEET 1 of 6
9-8-84

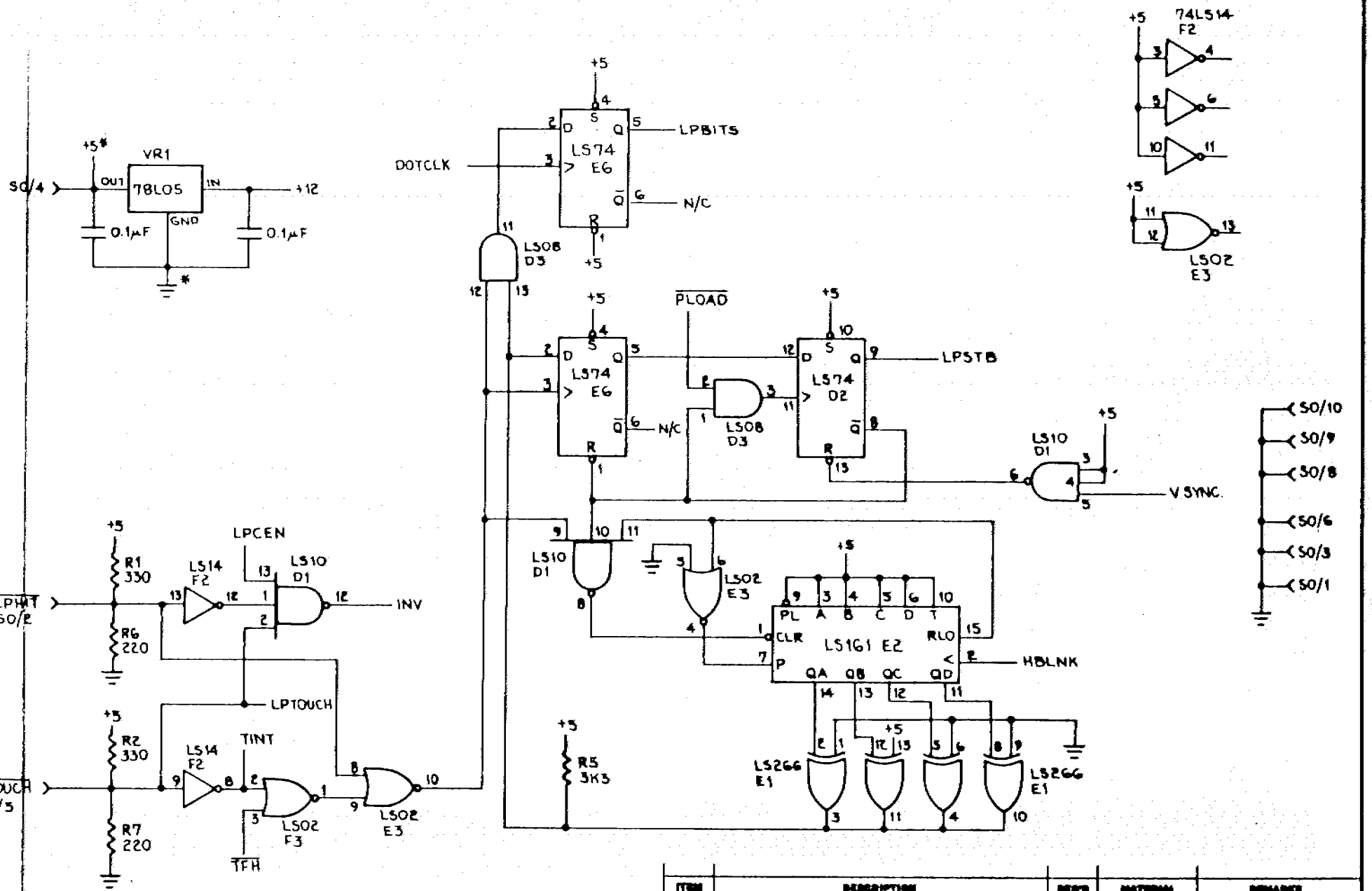


ITEM	DESCRIPTION	QTY	MATERIAL	REMARKS
	LIGHTPEN/GRAPHICS CARD	SCALE		PROJ NO. / DATE 9-8-84
	MASTER CLOCK VIDEO OUTPUT DATA BUSS BUFFERS	DRAWN A.B. / TRACED / CHECKED	Rev 3	DRAWING NUMBER Q219 SHEET 2 OF 6

A3

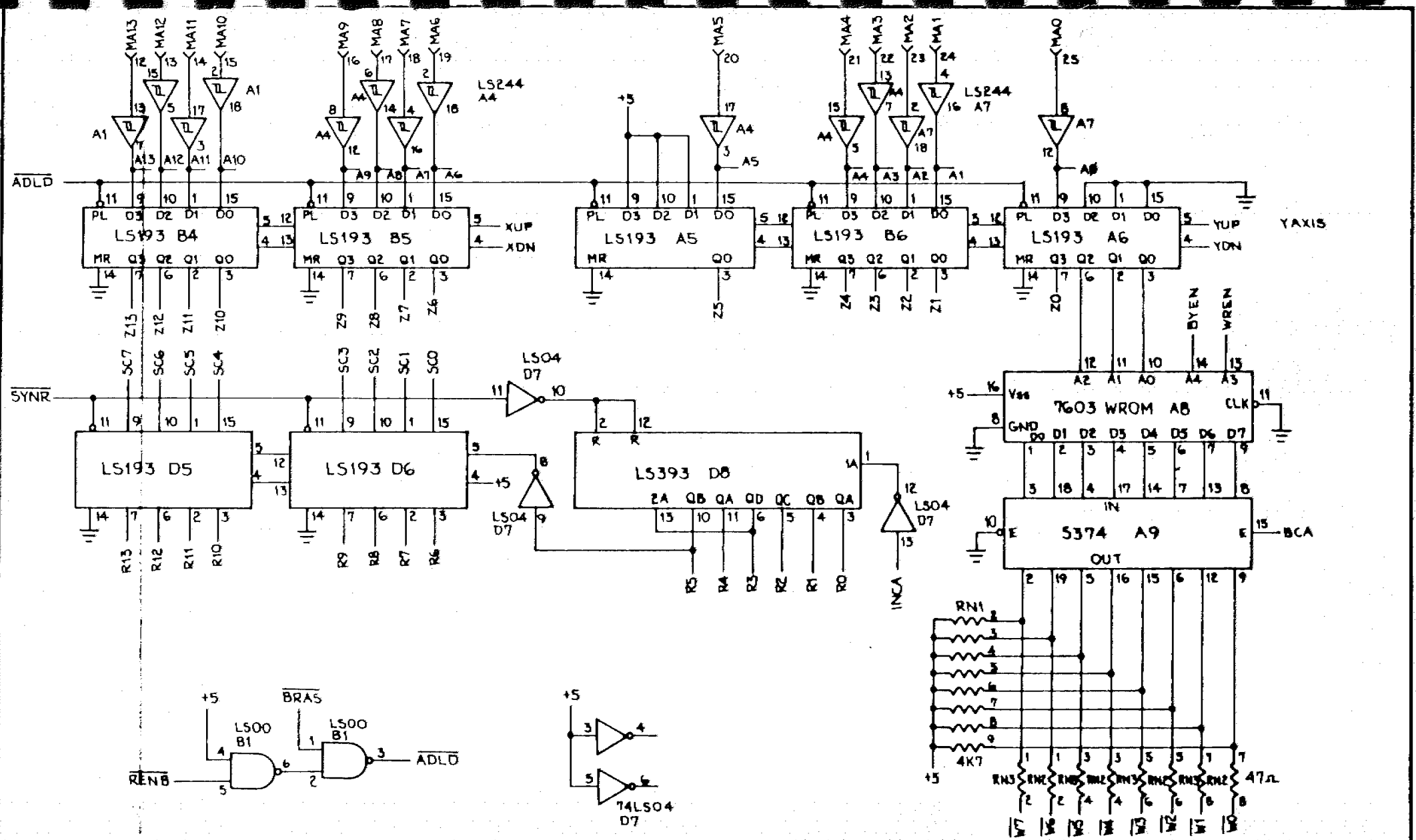


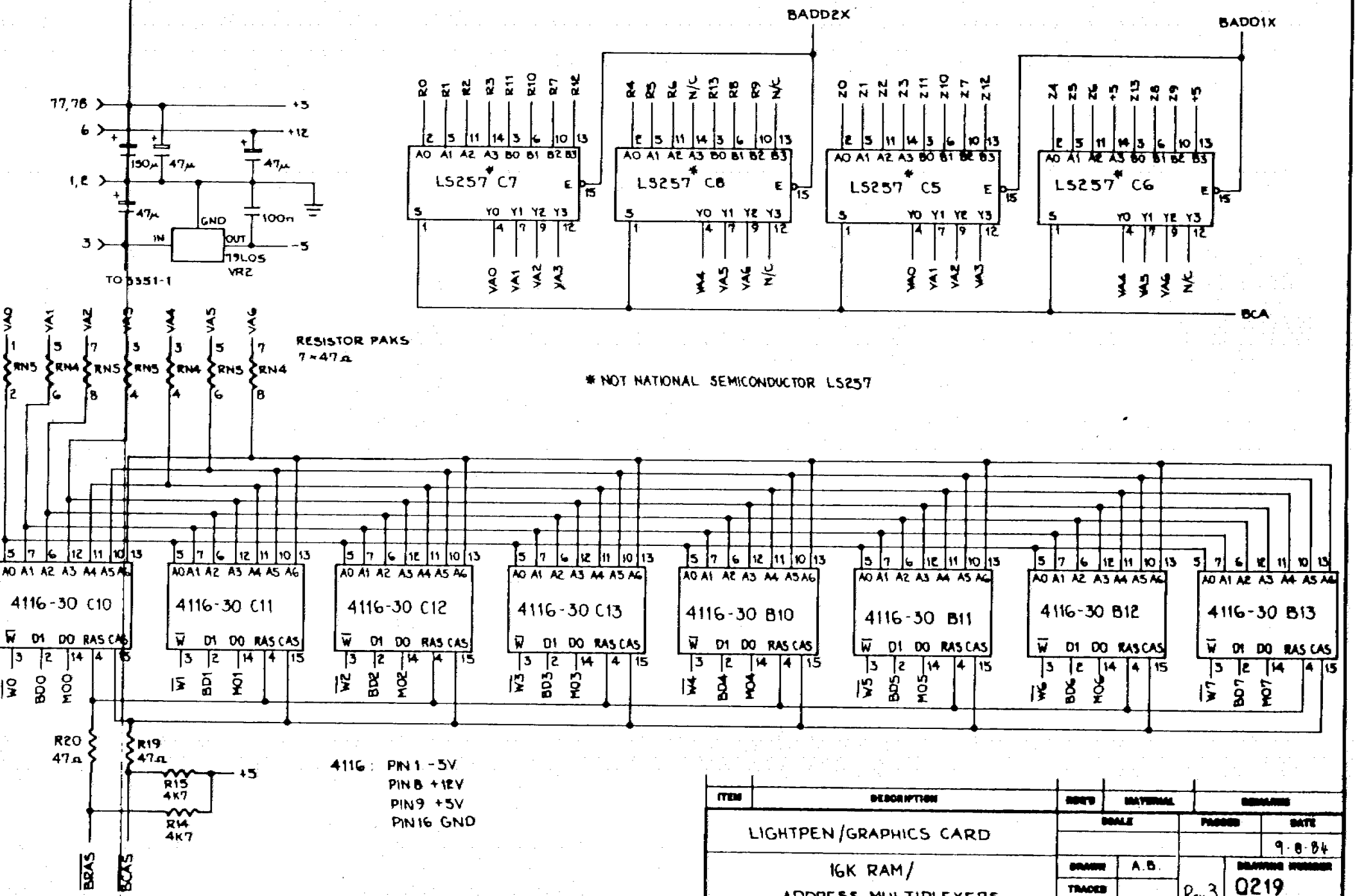
ITEM	DESCRIPTION	REV'D	MATERIAL	REMARKS
LIGHTPEN/GRAPHICS CARD		SCALE	PROJECT	DATE 9-8-84
VIDEO CONTROL GENERATION LIGHT PEN REGISTERS		DRAWN A.B. / TRACED / CHECKED	REV 3	DRAWING NUMBER Q219 SHEET 3 of 6



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
LIGHTPEN/GRAPHICS CARD		SCALE	PROOF	DATE 9/8/84
LIGHTPEN INTERFACE		DRAWN A.B.	Rev 3	DRAWING NUMBER Q219
		TRACED		SHEET 4 of 6
		CHECKED		

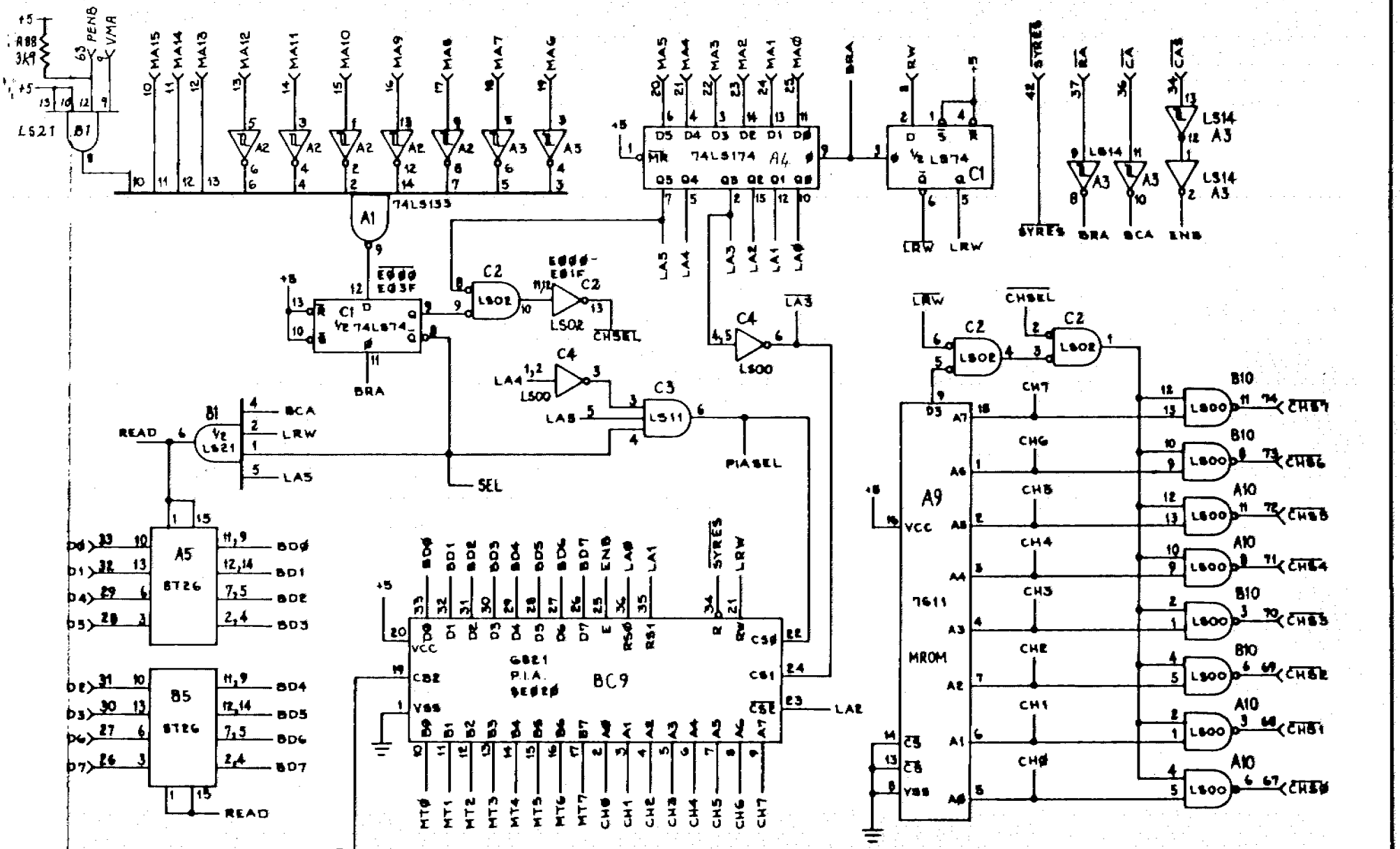
A3

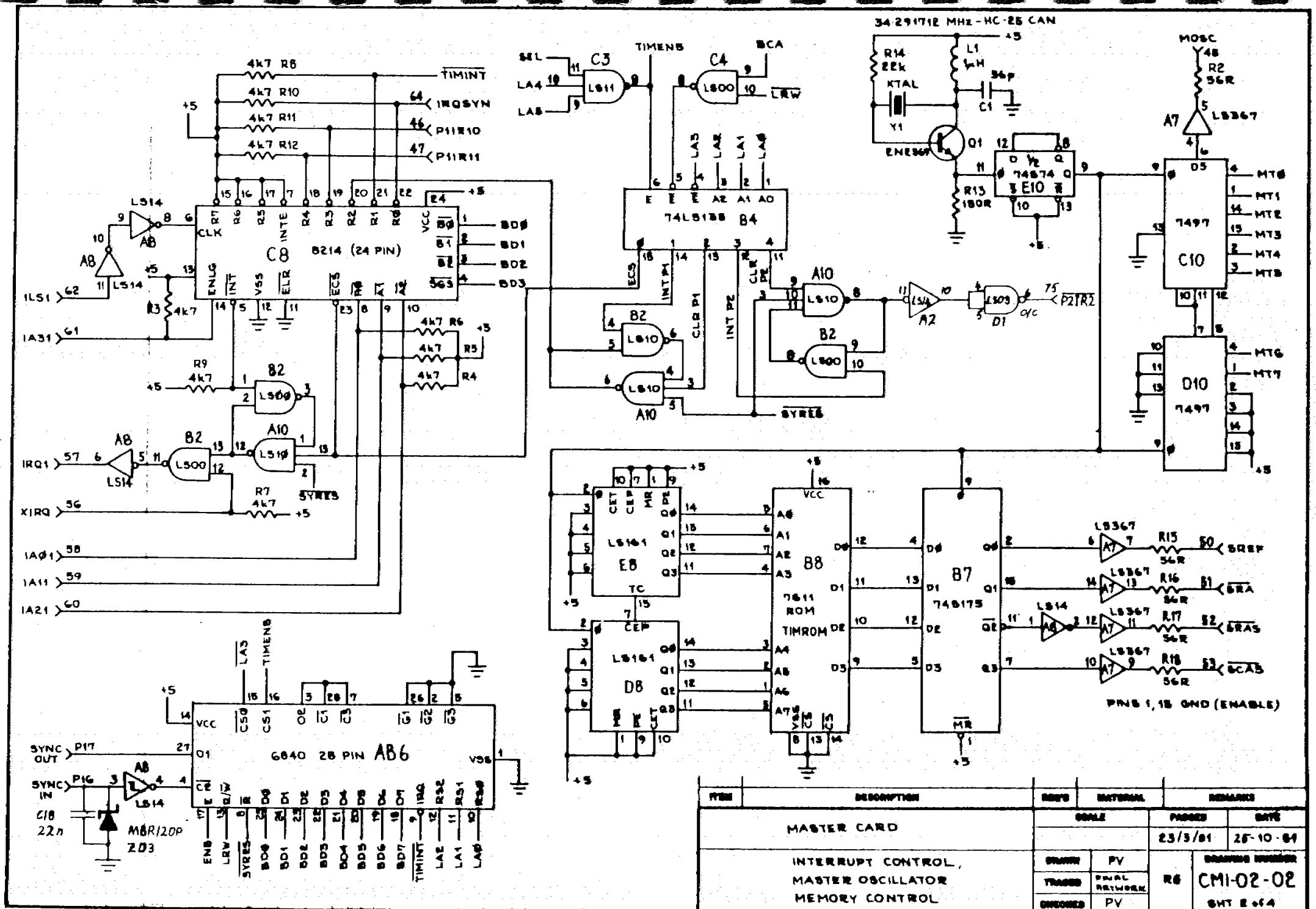

LS193 B4
LS193 B5
LS193 A5
LS193 B6
LS193 A6
LS193 D5
LS193 D6
LS393 D8
7603 WROM A8
5374 A9
LS244 A4
LS244 A7
LS04 D7
LS00 B1
74LS04 D7
ADLD
SYNR
RENB
BRAS
XUP
XDN
YUP
YDN
YAXIS
BYEN
WREN
BCA
INCA
4K7
47Ω
LIGHTPEN/GRAPHICS CARD
VRAM ADDRESSING WRITE CONTROL LOGIC
A.B.
9/8/84
0219
REV 3
SHEET 5 of 6



* NOT NATIONAL SEMICONDUCTOR LS257

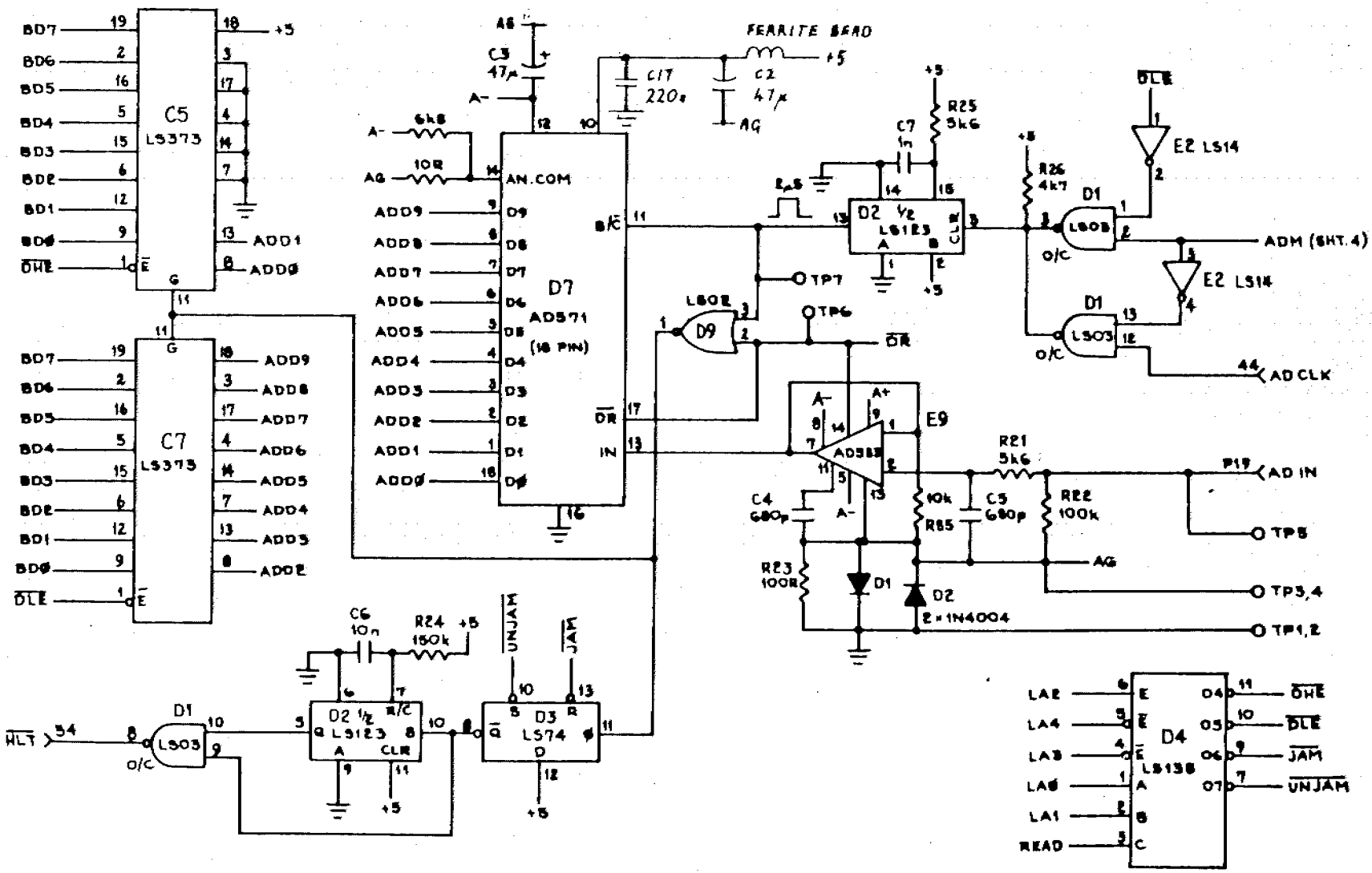
ITEM	DESCRIPTION	QTY	MATERIAL	REMARKS
	LIGHTPEN/GRAPHICS CARD	SCALE		DATE 9-8-84
	16K RAM/ ADDRESS MULTIPLEXERS	DRAWN A.B.		DRAWING NUMBER Q219
		TRACED		Rev 3
		CHECKED		SHEET 6 of 6


MASTER CARD
ADDRESS DECODING; CHANNEL SELECTION
RAM SWITCHING;
MASTER TUNING REGISTER
DRAWN PV
TRACED
CHECKED PV
23/3/81
25-10-84
R6
CM1-02-01
SHT 1 of 4
74LS133
74LS174
LS21
LS02
LS00
LS11
LS14
LS74
8T26
6821
P.I.A.
7611
MROM
BC9
A9
BRA
LRW
SYRES
LA3
LA4
LA5
SEL
PIASEL
CHSEL
READ
RAMEN
R1
4k7



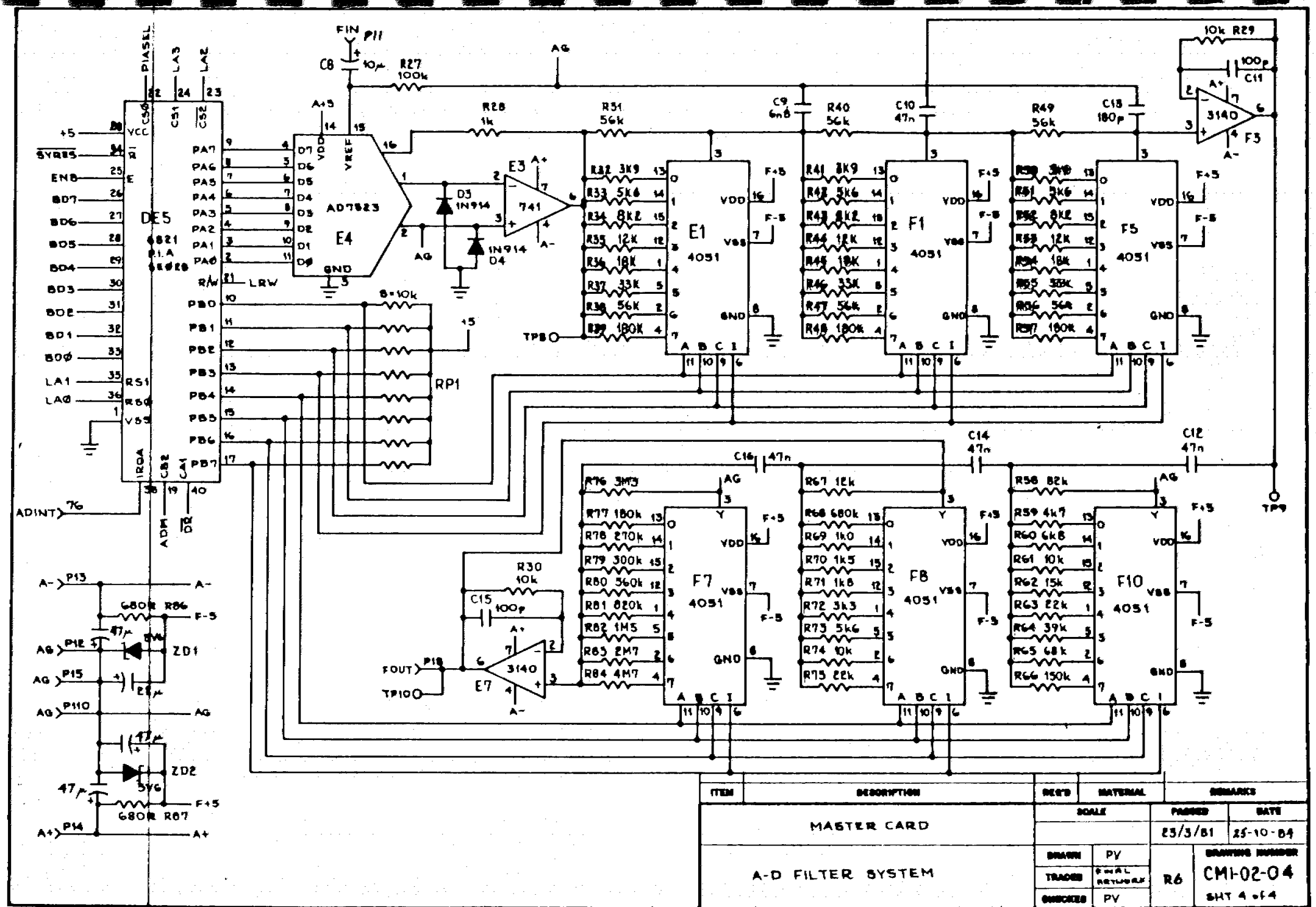
ITEM	DESCRIPTION	DRWG	MATERIAL	REMARKS
	MASTER CARD	SCALE		PRINTED 23/3/81
	INTERRUPT CONTROL, MASTER OSCILLATOR MEMORY CONTROL	DRAWN PV		DATE 25-10-84
		TRACED FINAL ARTWORK	R6	DRAWING NUMBER CMI-02-02
		CHECKED PV		SHT 2 of 4

A3



ITEM	DESCRIPTION	REVS	MATERIAL	REMARKS
MASTER CARD		SCALE	PASSED 23/3/81	DATE 25-10-84
AD CONVERTER		DRAWN PV	R6	DRAWING NUMBER CM1-02-03
		TRACED		SHT 3 of 4
		CHECKED PV		

A3


DE5
6821
P.I.A
AD7523
E4
741
E3
D3 IN914
D4 IN914
E1 4051
F1 4051
F5 4051
F7 4051
F8 4051
F10 4051
E7 3140
RP1
8×10k
ZD1
ZD2
5V6
MASTER CARD
A-D FILTER SYSTEM
DRAWN PV
TRACED
CHECKED PV
R6
CMI-02-04
SHT 4 of 4
23/3/81
25-10-84

****
** **
** **
** NOT FOR PUBLICATION **
** **
** **
****

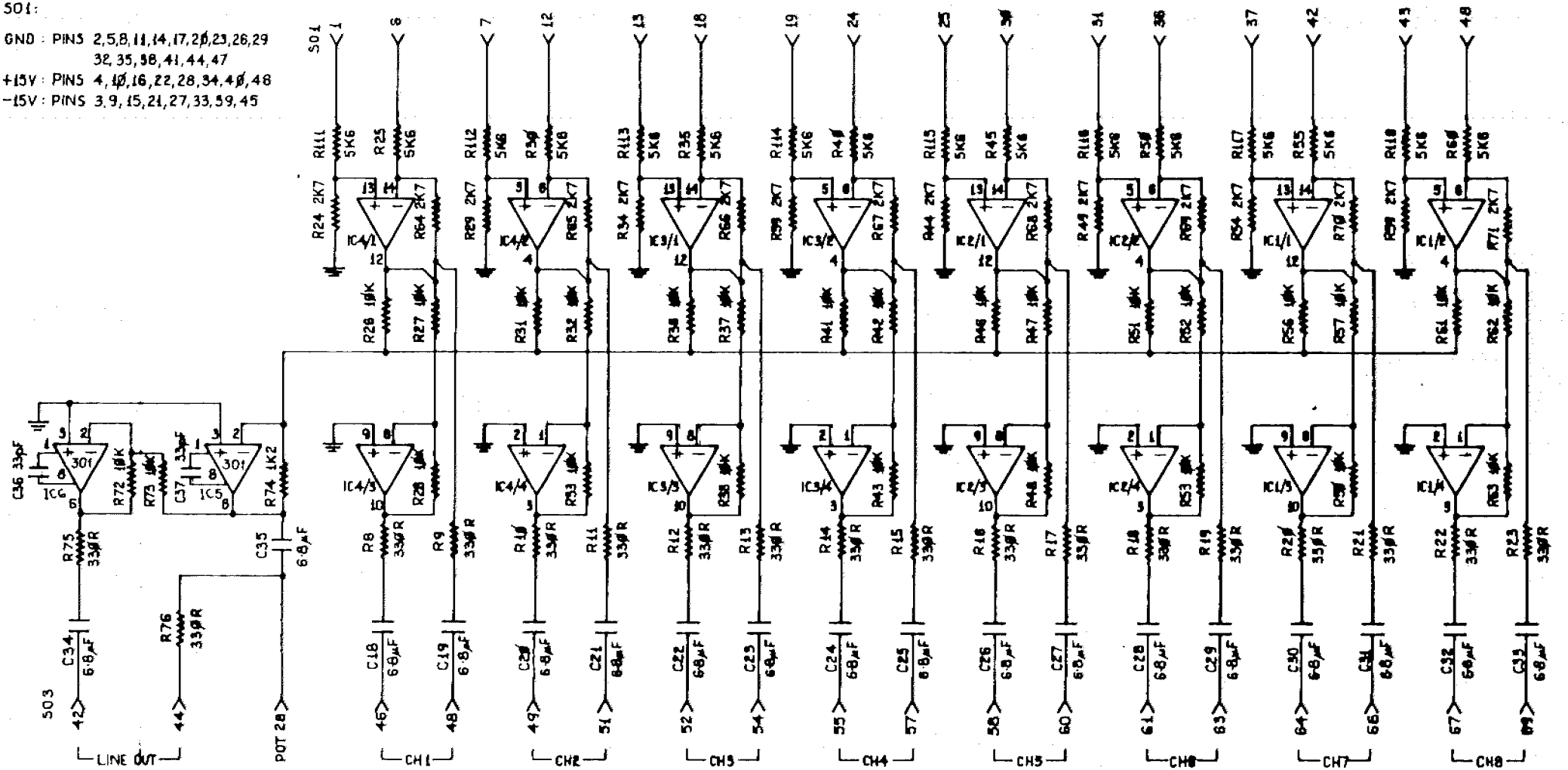
CHANNEL CARD CMI01-A SCHEMATIC

SO1:

GND : PINS 2,5,8,11,14,17,20,23,26,29
32, 35, 38, 41, 44, 47

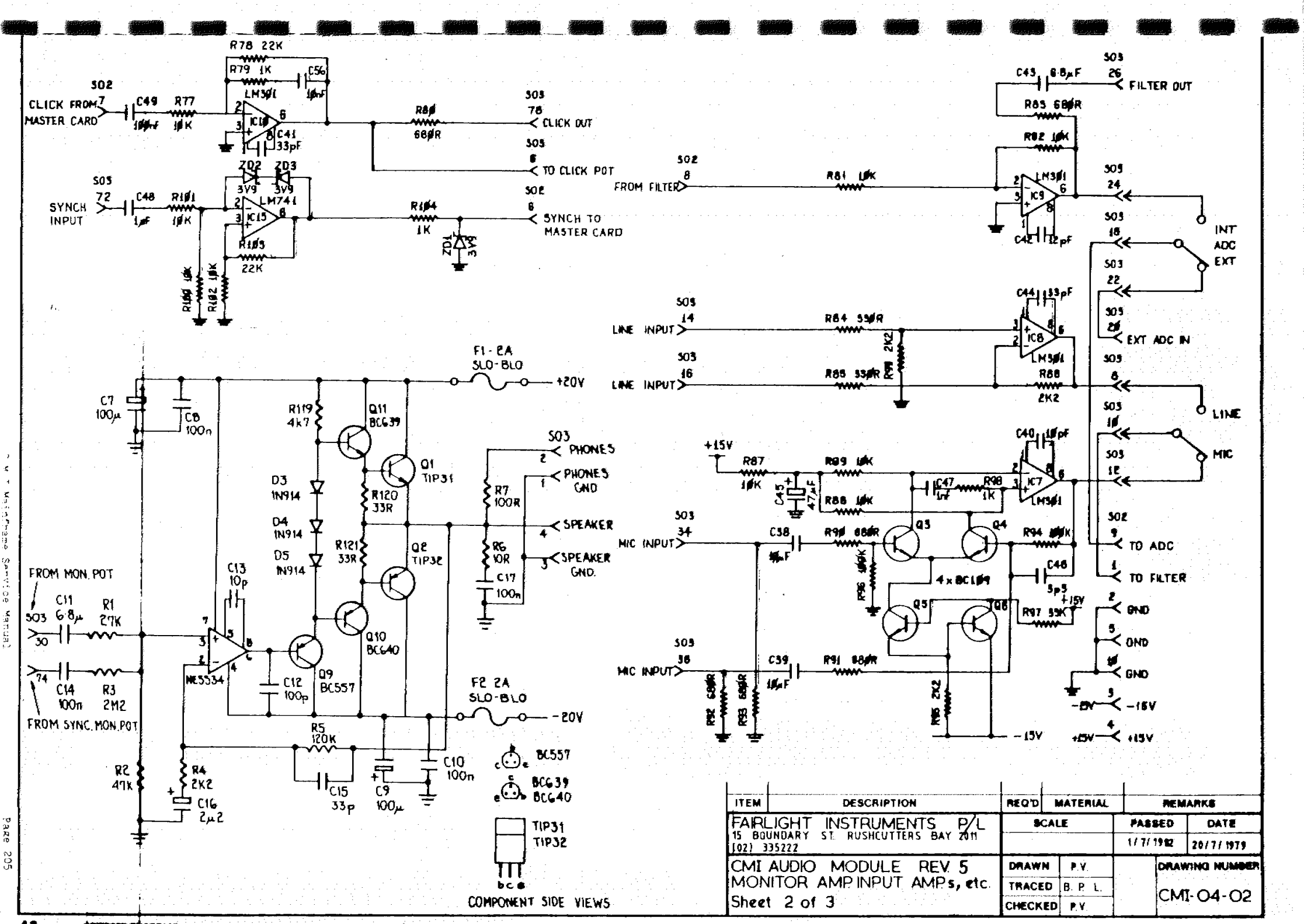
+15V : PINS 4, 10, 16, 22, 28, 34, 40, 46

−15V : PINS 3, 9, 15, 21, 27, 33, 39, 45

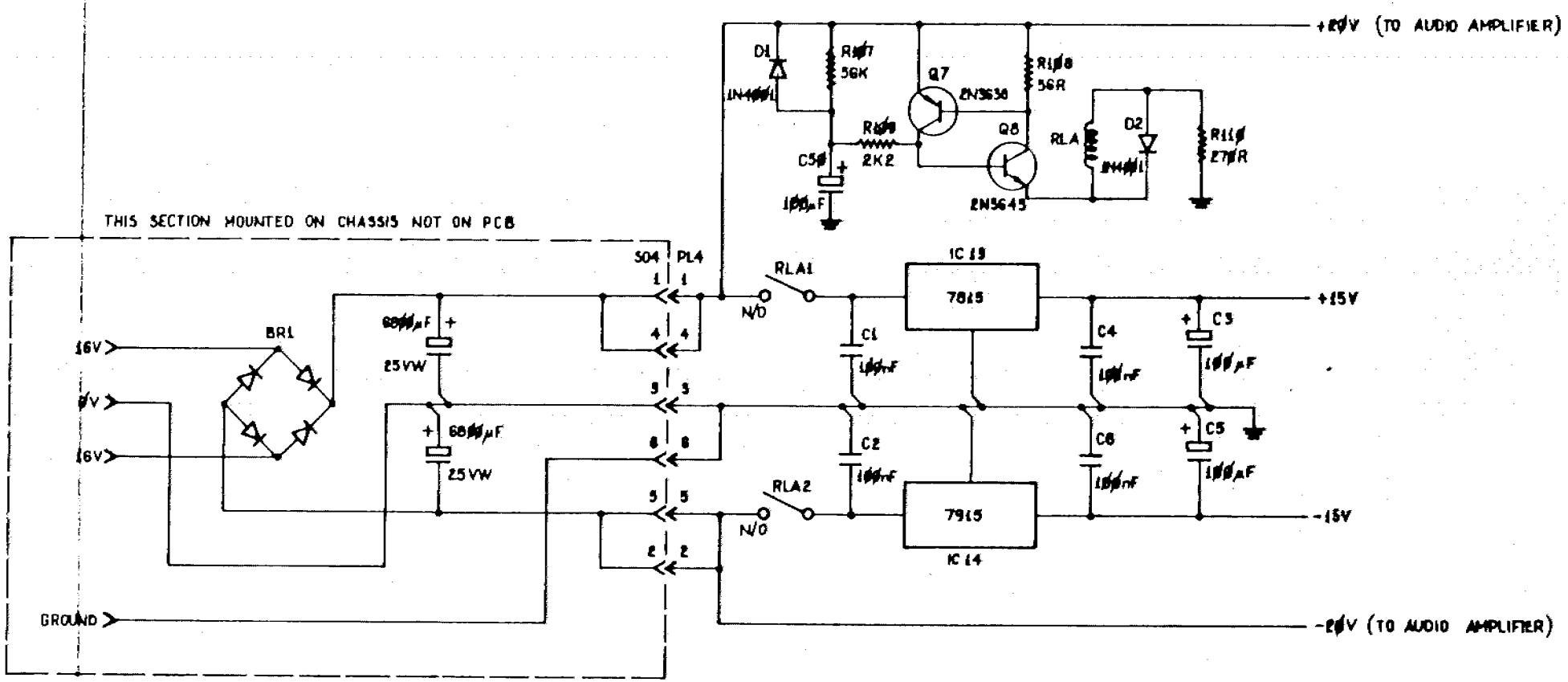


NOTE: IC1 - IC4 : TL084

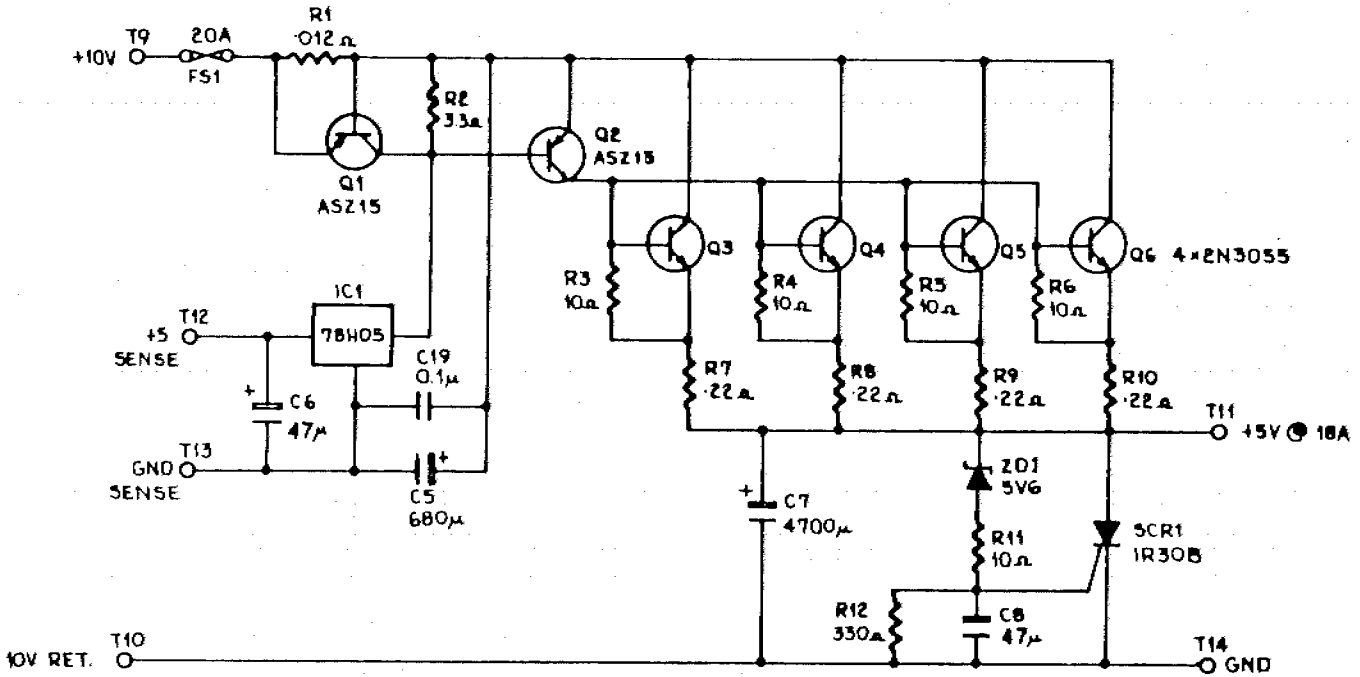
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
FAIRLIGHT INSTRUMENTS P/L 15 BONDARY ST RUSHCUTTERS BAY 2011 (02) 335222		SCALE		PASSED 1/7/1982 DATE 22/07/1979
CMI AUDIO MODULE REV 5 MIXER LINE DRIVERS Sheet 1 of 3		DRAWN P.V. TRACED B.P.L. CHECKED P.V.		DRAWING NUMBER CMI-04-01



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
FAIRLIGHT INSTRUMENTS P/L 15 BOUNDARY ST. RUSHCUTTERS BAY 2011 (02) 335222		SCALE		PASSED 1/7/1982 DATE 20/7/1979
CMI AUDIO MODULE REV 5 MONITOR AMP INPUT AMPs, etc. Sheet 2 of 3		DRAWN P.V. TRACED B. P. L. CHECKED P.V.		DRAWING NUMBER CMI-04-02

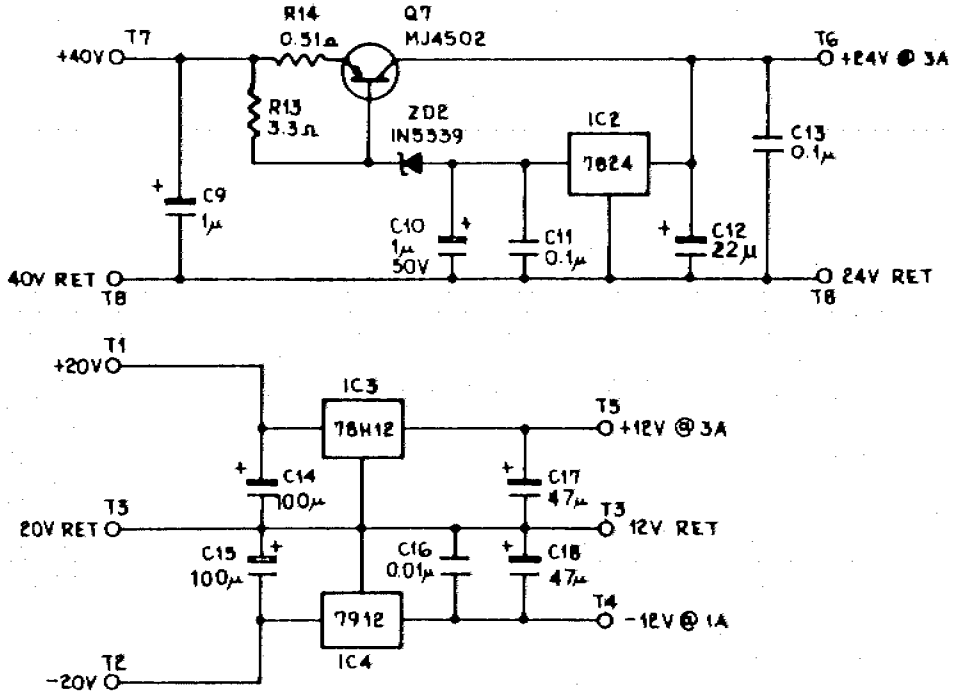


ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
FAIRLIGHT INSTRUMENTS P/L 15 BOUNDARY ST. RUSHCUTTERS BAY 2011 (02) 335222		SCALE		PASSED 1/7/1982 DATE 11/04/1979
CMI AUDIO MODULE REV 5 POWER SUPPLY Sheet 3 of 3		DRAWN P.V. TRACED B.P.L. CHECKED P.V.		DRAWING NUMBER CMI-04-03

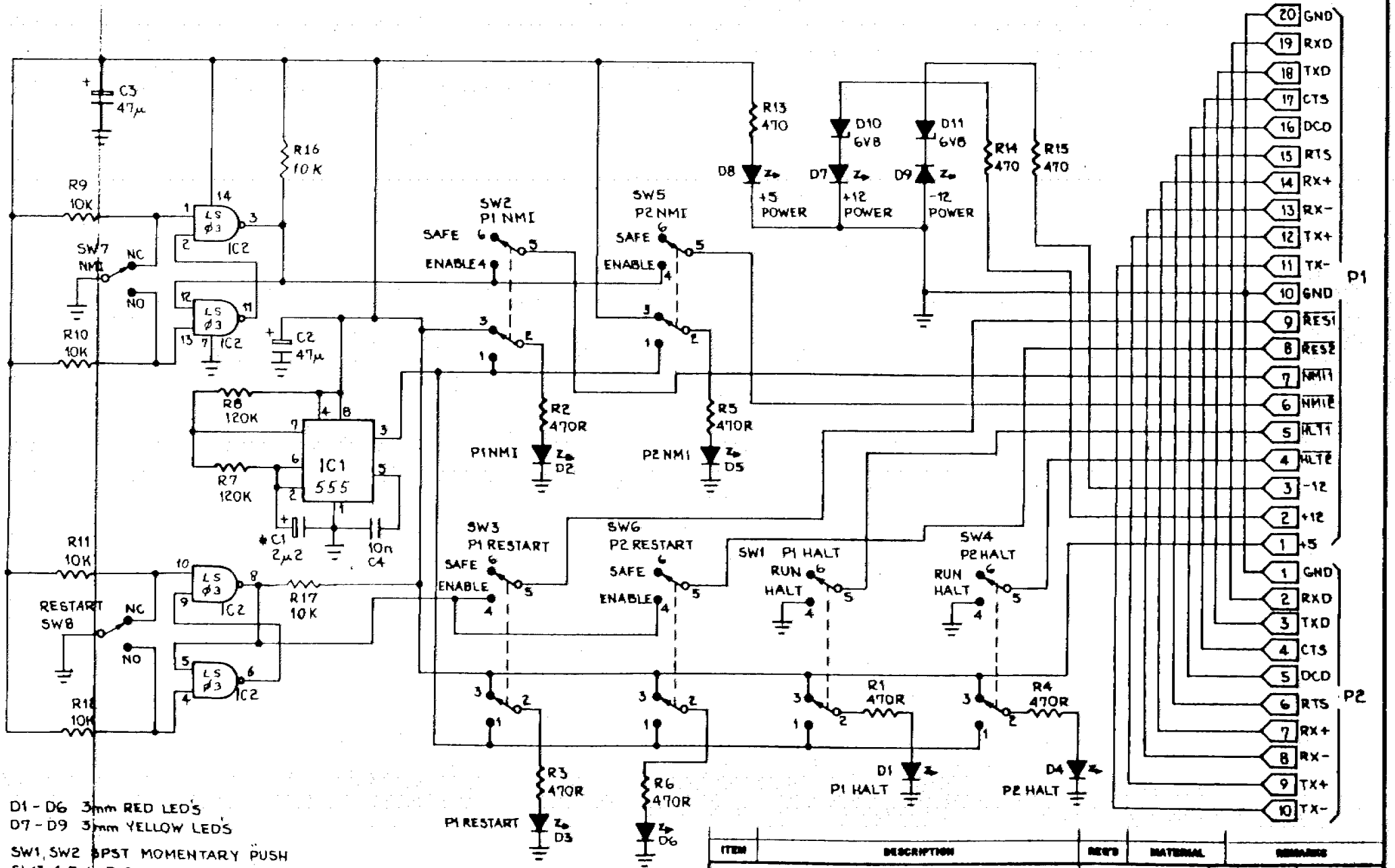


ASZ15 = Hitachi 2SB472

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	C.M.I.	SCALE		PASSED / DATE: 3/2/81
	POWER SUPPLY ASSEMBLY REGULATOR 5V 18A SHEET 1 of 2	DRAWN: DK TRACED: MTB CHECKED: PV		DRAWING NUMBER: QPSA-01



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
C.M.I		SCALE	PASSED	DATE 3/2/81
POWER SUPPLY ASSEMBLY ±12V, 24V REGULATORS SHEET 2 of 2	DRAWN DK TRACED MTB CHECKED PV			DRAWING NUMBER QPSA-02



D1 - D6 3mm RED LED'S
D7 - D9 3mm YELLOW LED'S

SW1, SW2 SPST MOMENTARY PUSH
SW3, 4, 5, 6, 7, 8 DPDT TOGGLE

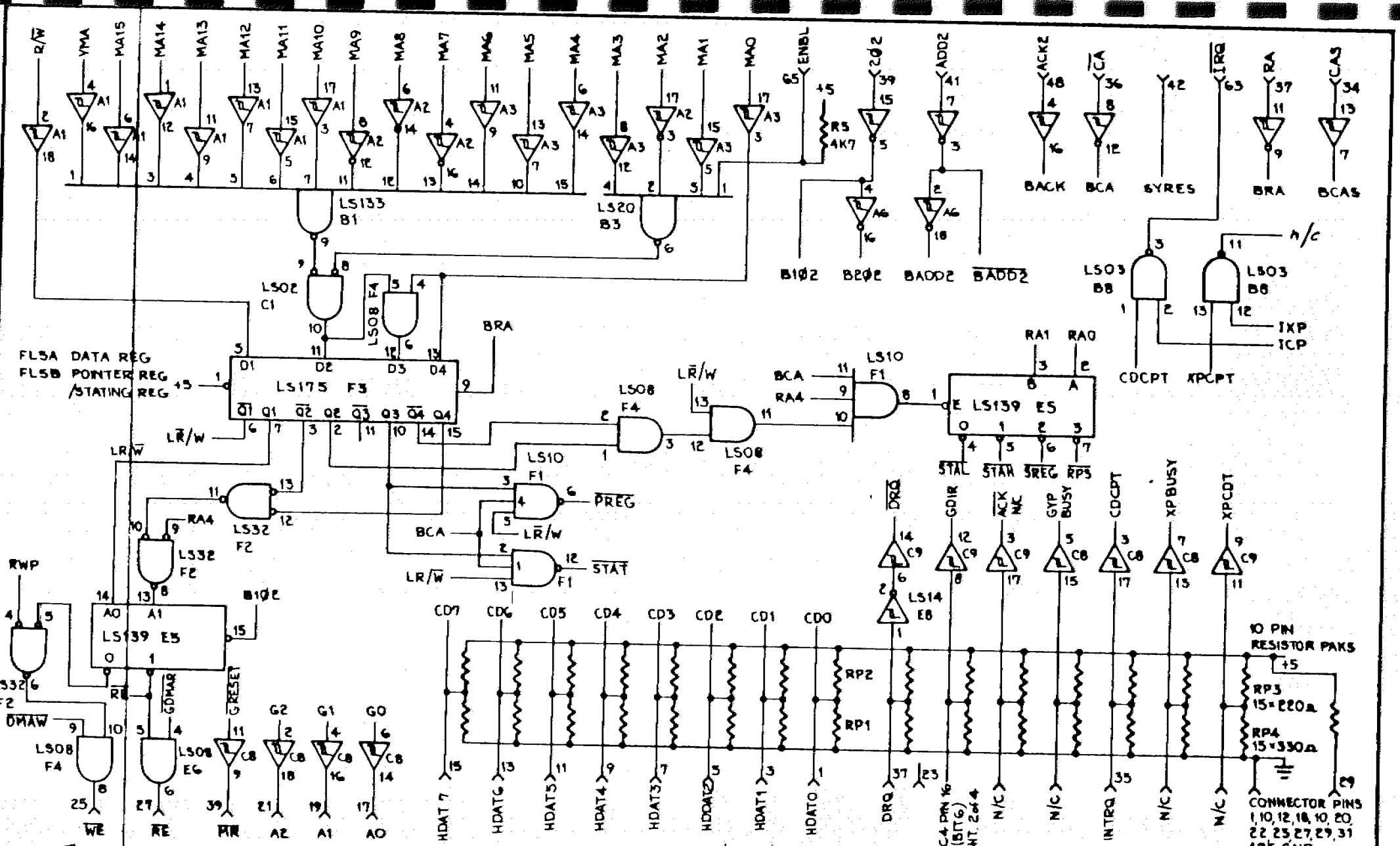
IC1 555
IC2 74LS03

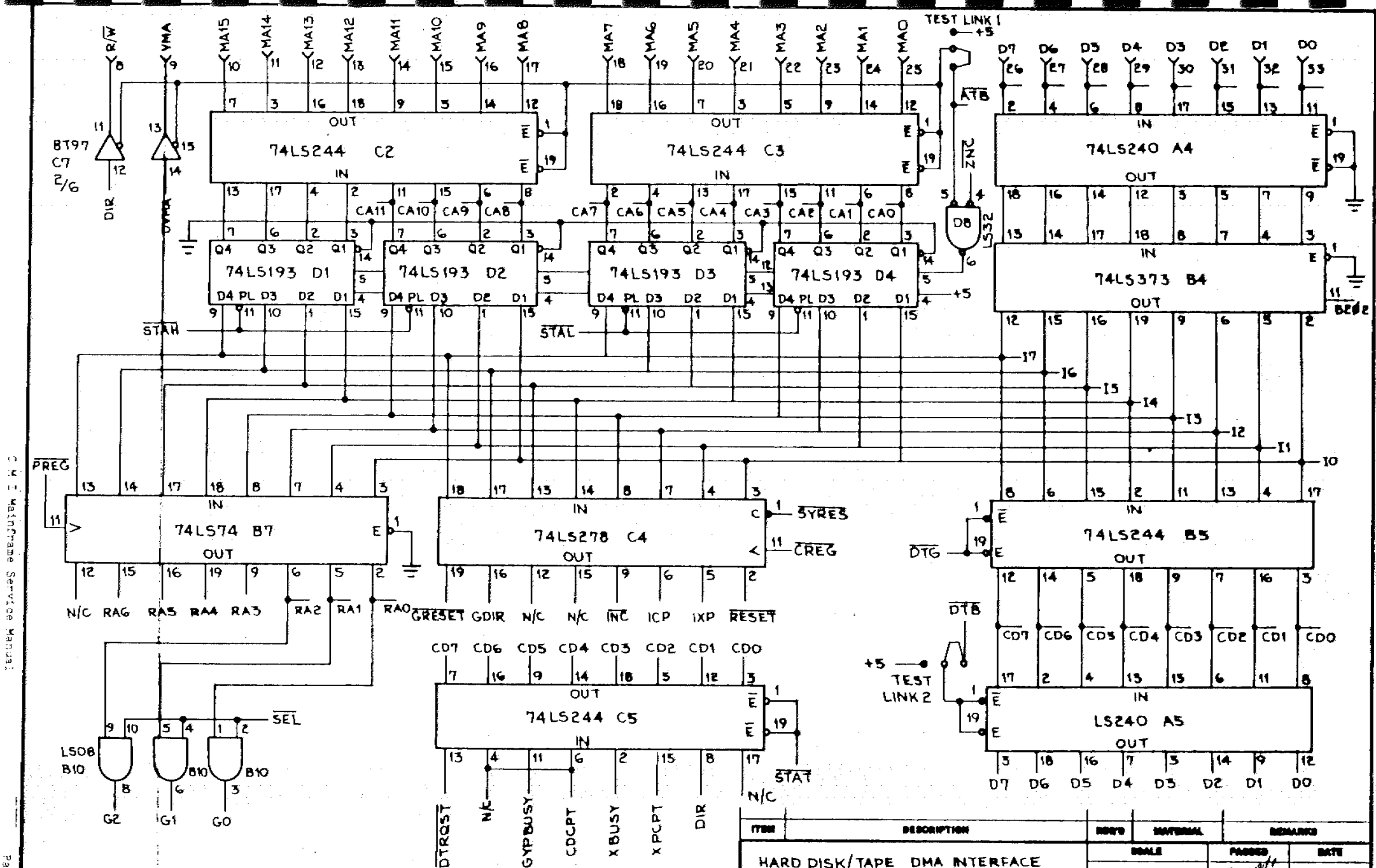
* TAG TANTALUM

ITEM	DESCRIPTION	REV'D	MATERIAL	REMARKS

SCALE		PROOF	DATE
			5/10/84
DRAWN	P.V.	DRAWING NUMBER	
TRACED		0137-02	
CHECKED		SHEET 1 of 1	

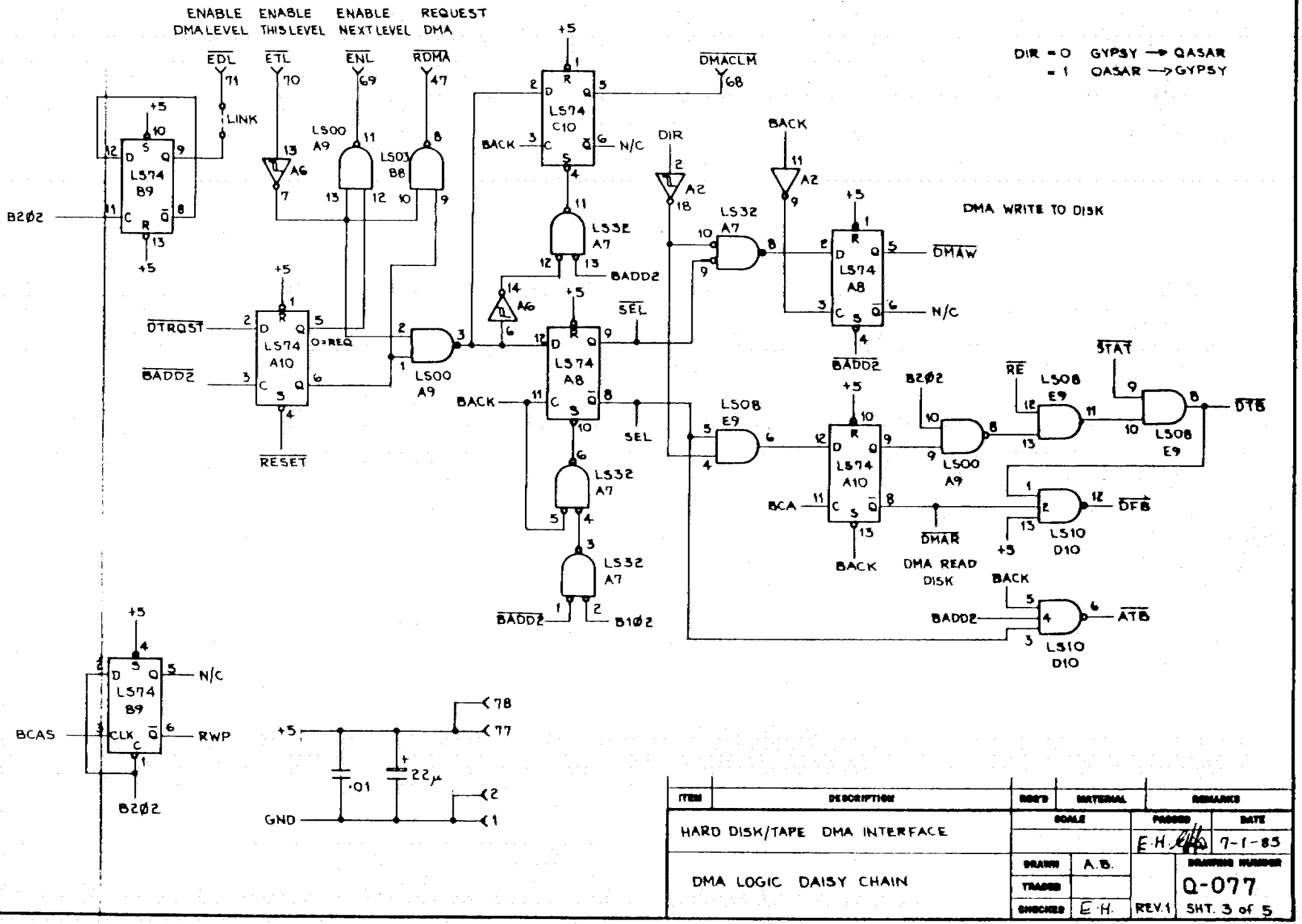
CMI-09 CONSOLE Rev. 2


R/W
YMA
MA15
MA14
MA13
MA12
MA11
MA10
MA9
MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MA0
ENBL
CD2
ADD2
ACK2
CA
SYRES
IRQ
RA
CA3
BACK
BCA
BRA
BCAS
LS133 B1
LS20 B3
B1Ø2
B2Ø2
BADD2
BADD2
LS02 C1
LS08 F4
LS03 B8
n/c
IXP
ICP
CDCPT
XPCPT
BRA
FL5A DATA REG
FL5B PONTER REG /STATING REG
LS175 F3
D1 D2 D3 D4
Q1 Q1 Q2 Q2 Q3 Q3 Q4 Q4
LR/W
LS08 F4
LS10 F1
BCA
RA4
RA1
RA0
LS139 E5
STAL STAR SREG RPS
LS32 F2
PREG
STAT
RWP
B1Ø2
A0 A1
O 0 1
LS139 E5
RE
GDMAR
GRESET
G2 G1 G0
DMAW
LS08 F4
LS08 E6
WE RE MR A2 A1 A0
CD7 CD6 CD5 CD4 CD3 CD2 CD1 CD0
RP2
RP1
HDAT7 HDAT6 HDAT5 HDAT4 HDAT3 HDAT2 HDAT1 HDAT0
DRQ
GDIR
ACK NC
GYP BUSY
CDCPT
XP BUSY
XPCDT
LS14 E8
10 PIN RESISTOR PAKS
+5
RP3 15×220Ω
RP4 15×330Ω
INTRQ
CONNECTOR PINS 1, 10, 12, 18, 10, 20, 22, 25, 27, 29, 31 ARE GND.
40 WAY GYPSY CONNECTOR
ALL UNMARKED NON INVERTING SCHMITT BUFFERS 74LS244
" " INVERTING " " 74LS240
UNUSED GATES HAVE INPUTS TIED TO +5
CONNECTOR N/C TO 33, 34, 35, 36, 37, 38, 39, 40
ITEM
DESCRIPTION
REQ'D
MATERIAL
REMARKS
HARD DISK / TAPE DMA INTERFACE
ADDRESS, DECODING, TERMINATION
SCALE
DRAWN A.B.
TRACED
CHECKED E.H.
PROOFED E.H.
DATE 7/1/85
REV1
DRAWING NUMBER Q-077
SHEET 1 of 5

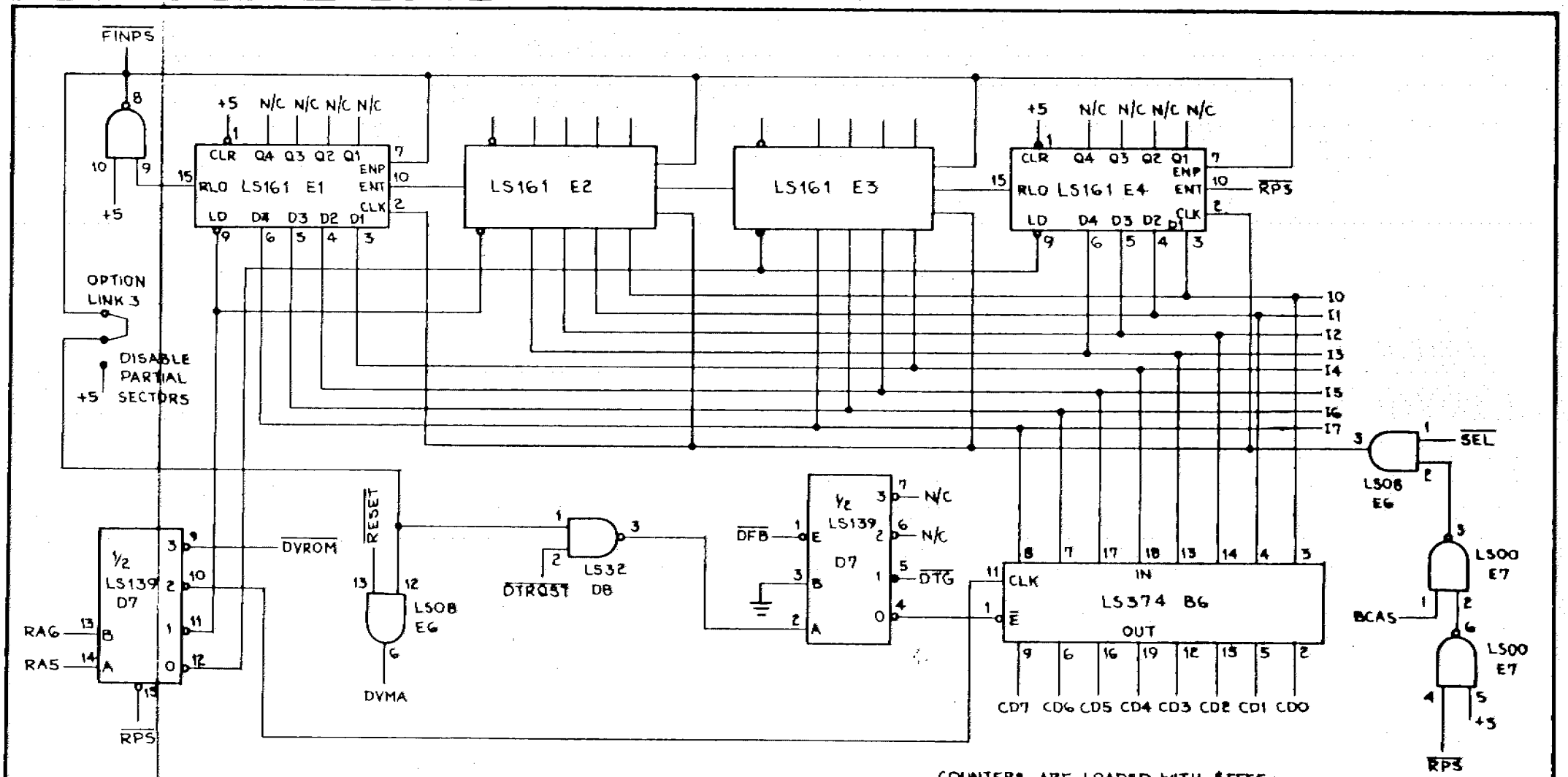


ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
HARD DISK/TAPE DMA INTERFACE		SCALE	PASSED	DATE
			E.H.	7-1-85
DATA BUFFERS DMA ADDRESS COUNTER POINTER REGISTER/STATUS REGISTER	DRAWN A.B.			DRAWING NUMBER
	TRACED			Q-077
	CHECKED E.H.	REV. 1	SHT. 2 of 4	

C.M.I. Mainframe Service Manual



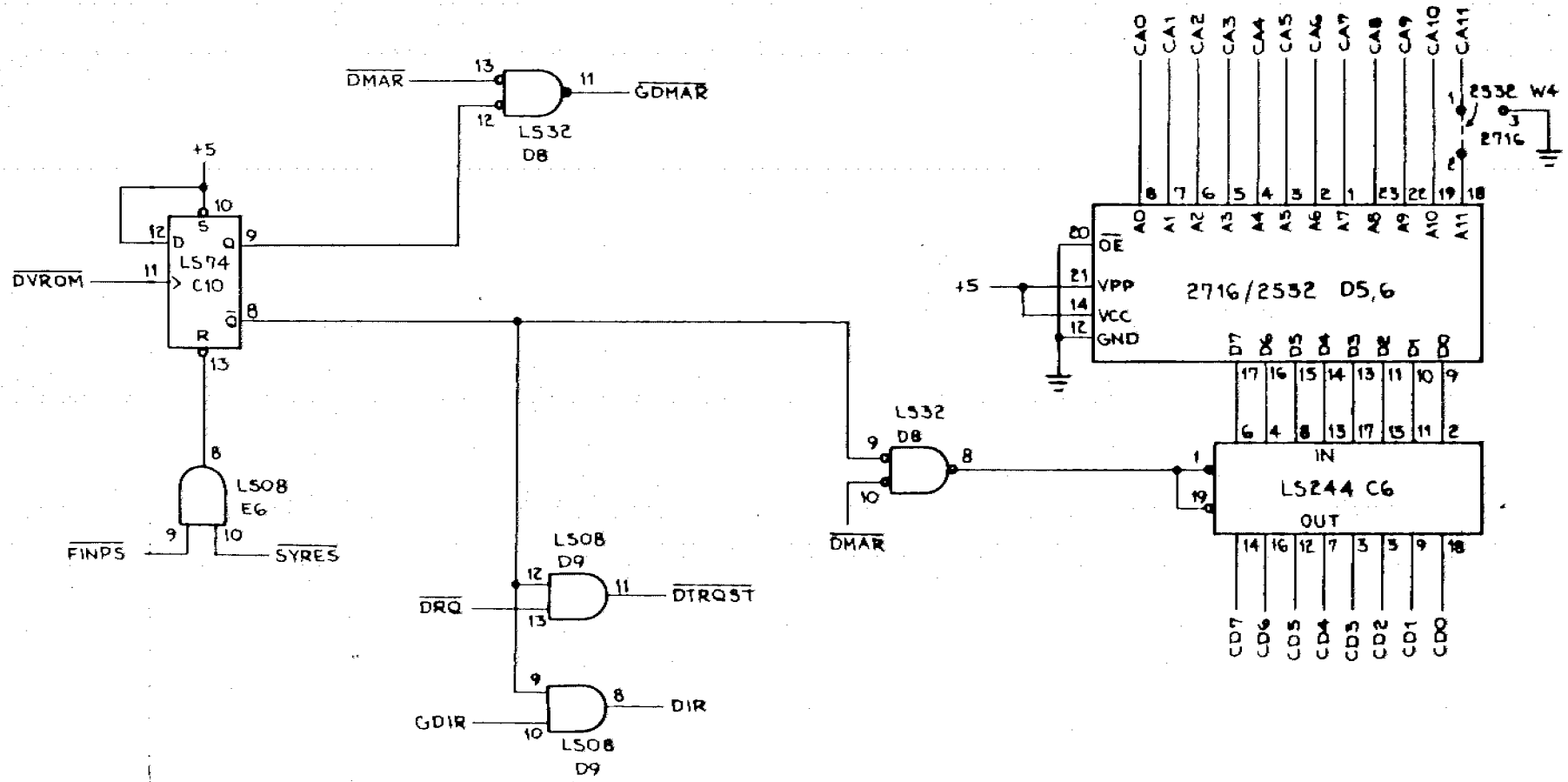
ITEM	DESCRIPTION	QTY	MATERIAL	REMARKS
HARD DISK/TAPE DMA INTERFACE		SCALE		PROOF / DATE
				E.H. 7-1-85
DMA LOGIC DAISY CHAIN		DRAWN	A.B.	DRAWING NUMBER
		TRACED		Q-077
		CHECKED	E.H.	REV.1 SHT. 3 of 5



COUNTERS ARE LOADED WITH $FFFF —
NUMBER OF BYPASS TO
READ/WRITE IN SECTOR

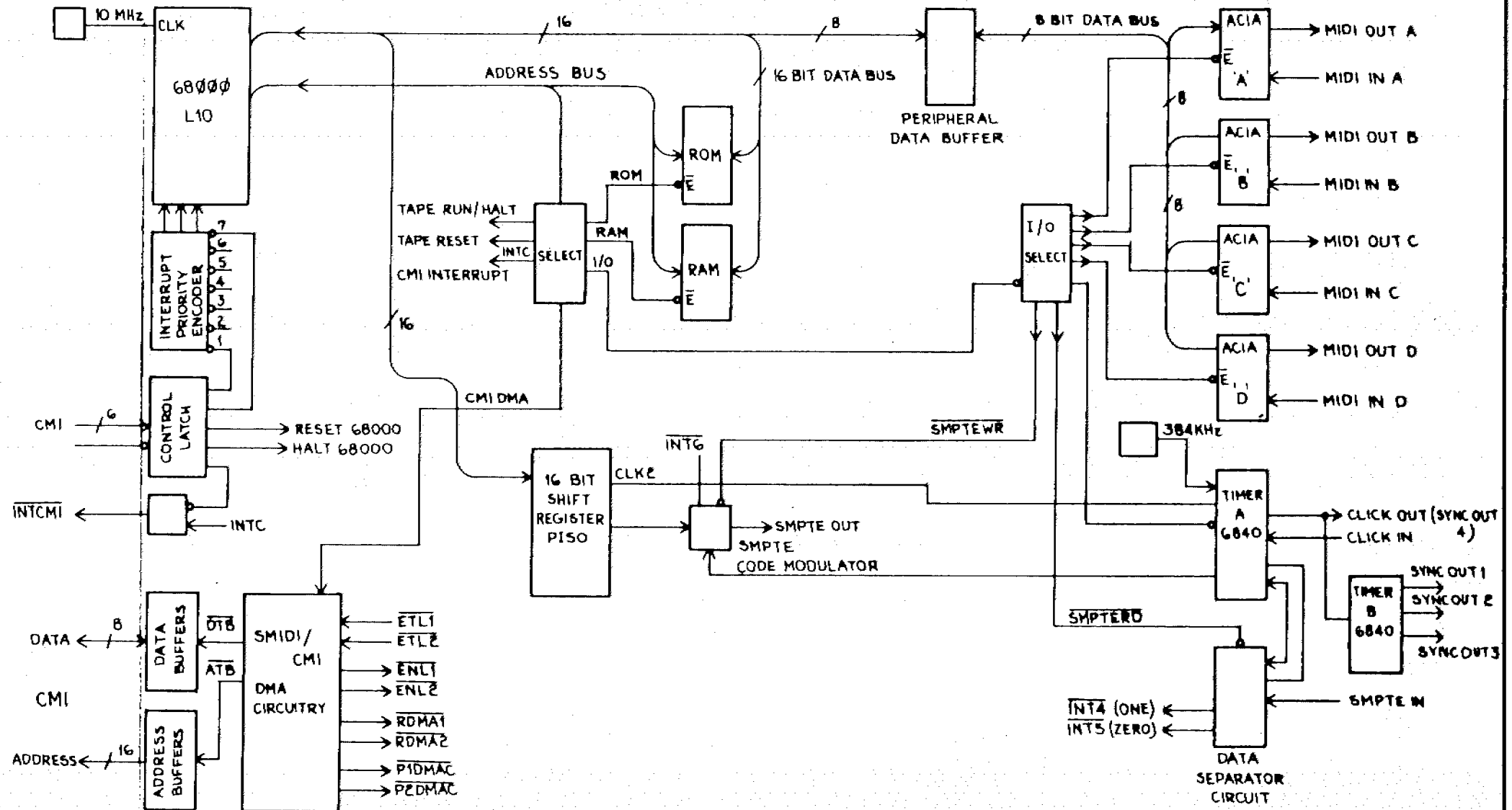
UPPER COUNTER BYTE $33
LOWER " " $13
DATA TO FILL REST OF SECTOR WRITTEN TO $53

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
HARD DISK/TAPE DMA INTERFACE		SCALE		DATE
			E.H.	7-1-85
READ/WRITE PARTIAL SECTOR LOGIC.	DRAWN A.B.			DRAWING NUMBER
	TRACED			Q-077
	CHECKED E.H.	REV. 1		SHT. 4 of 5

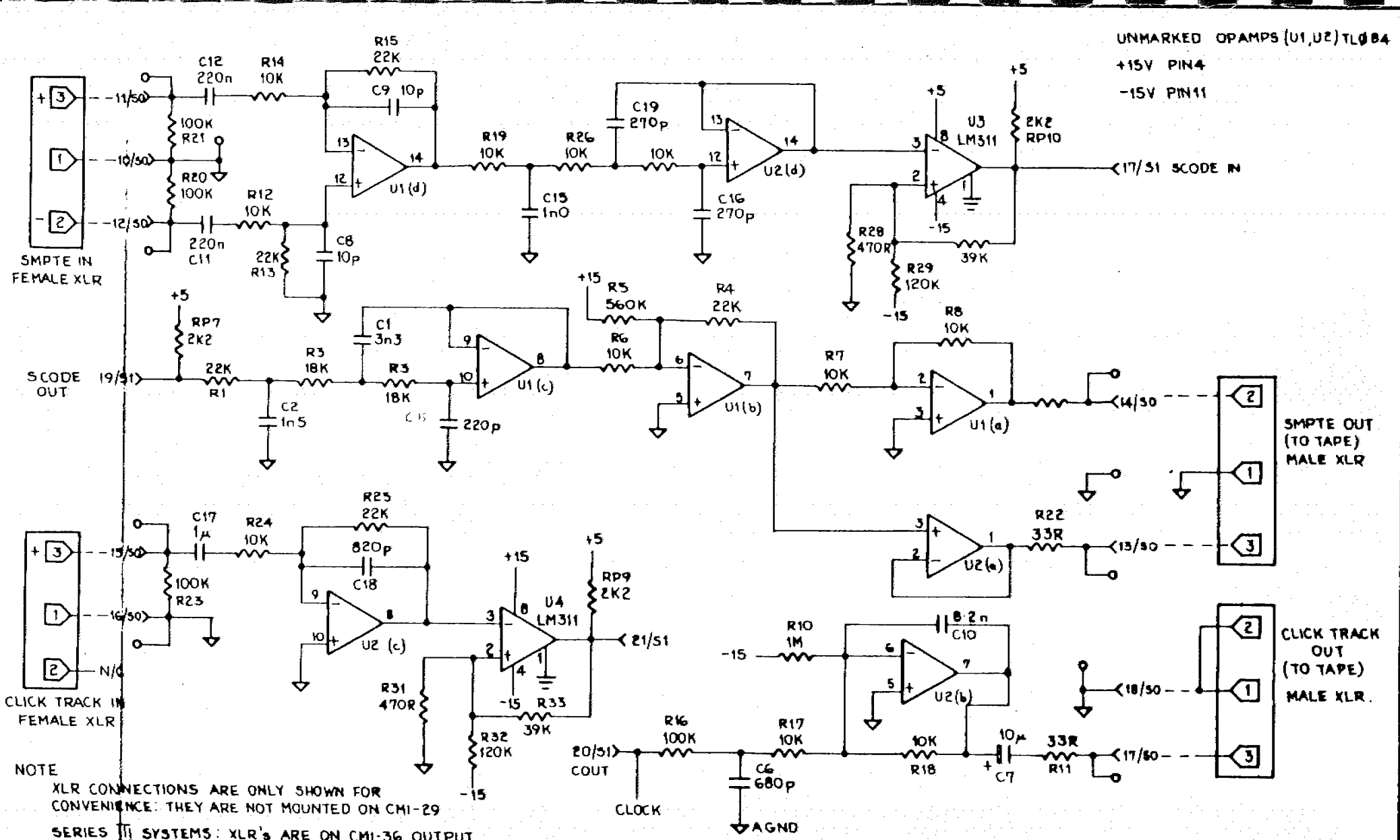


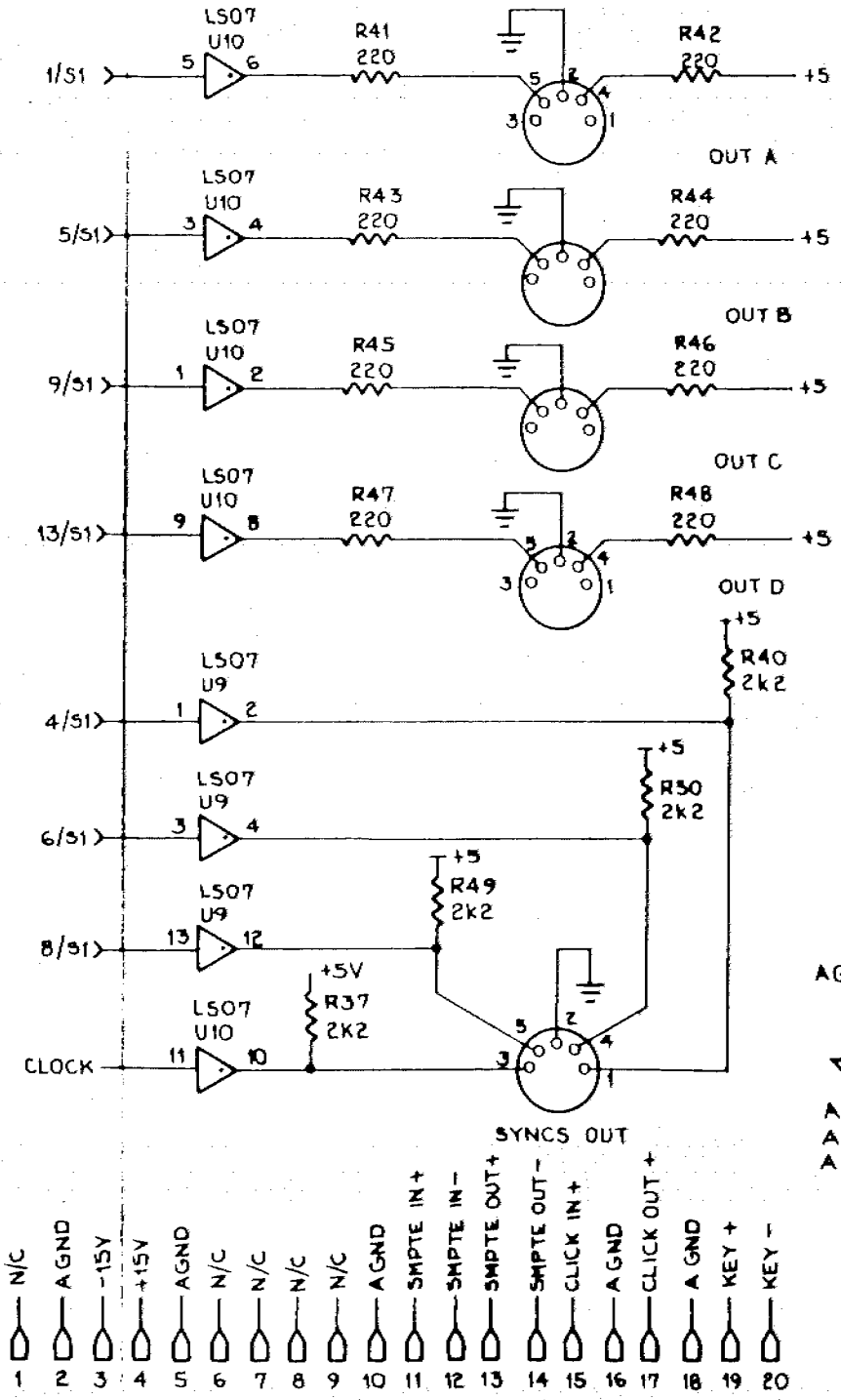
WRITE TO $73 STARTS DMA OF ROM INTO RAM.

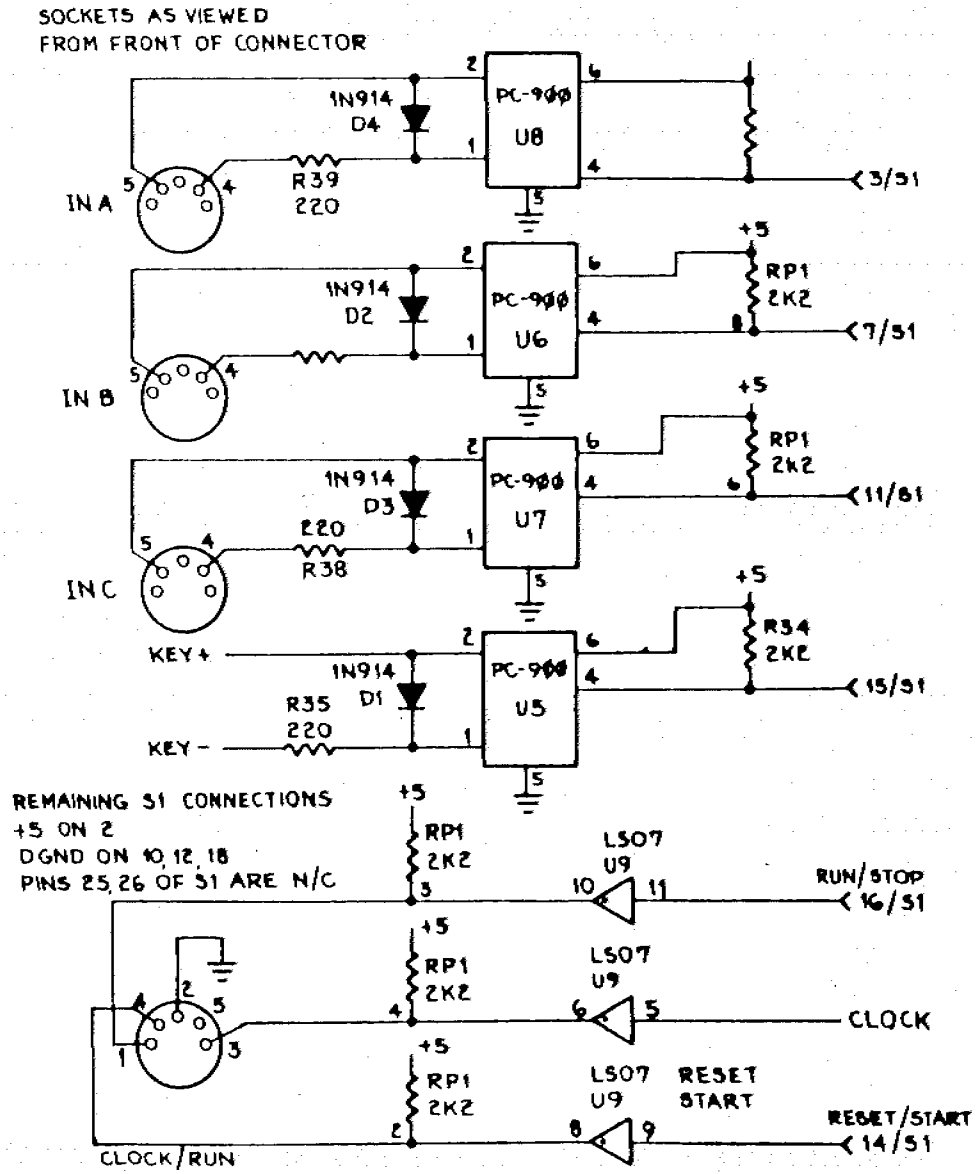
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
HARD DISK/TAPE DMA INTERFACE		SCALE		PASSED E.H. DATE 7-1-85
DEVICE DRIVER ROM.		DRAWN A.B.		DRAWING NUMBER Q-077
		TRACED		
		CHECKED E.H.	REV. 1	SHT. 5 of 5



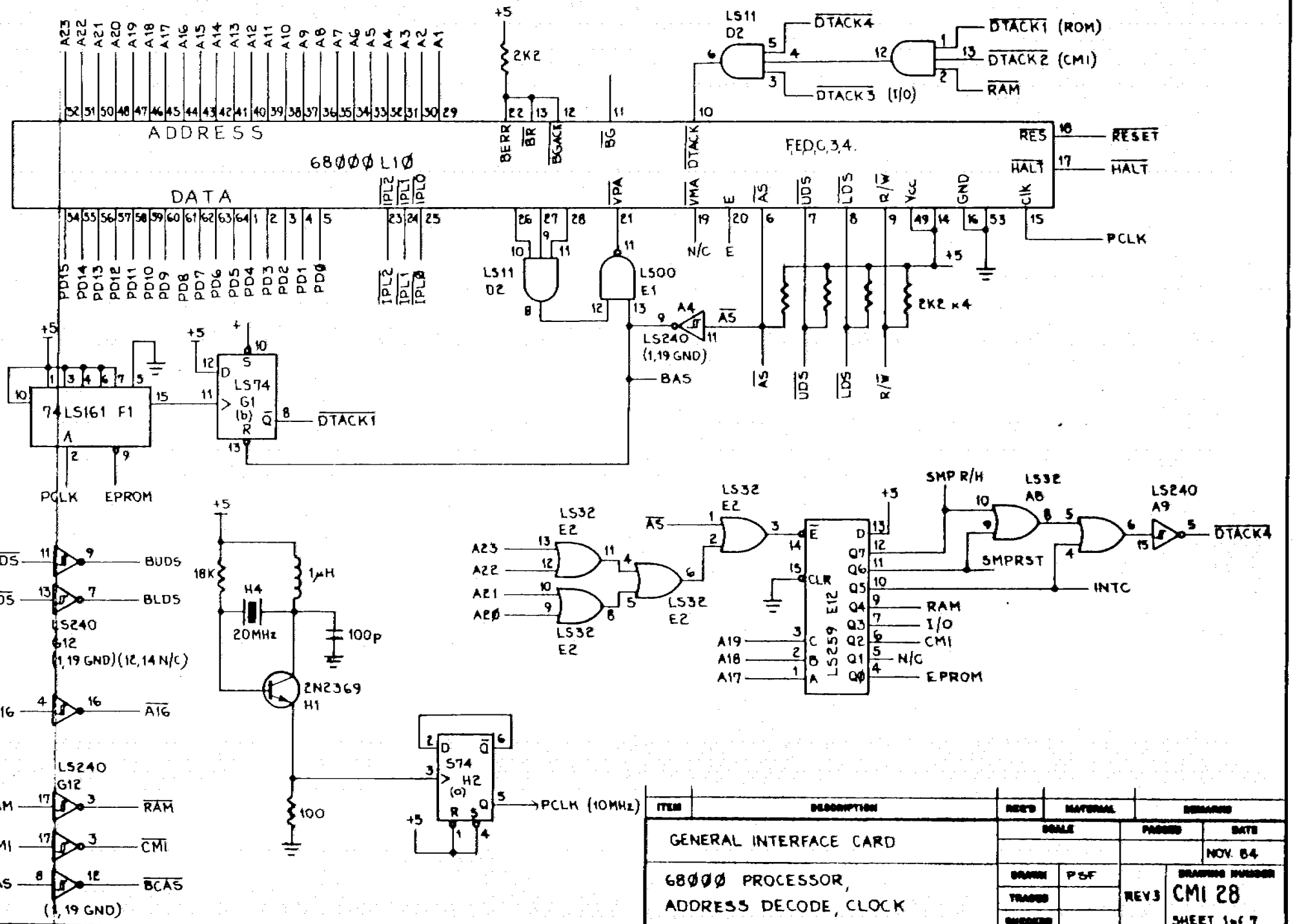
ITEM	DESCRIPTION	QTY	MATERIAL	REMARKS
GENERAL INTERFACE CARD		SCALE		PROOF / DATE
				NOV. 84
BLOCK DIAGRAM.		DRAWN	P&F	REV.3
		TRACED		CMIBD-1
		CHECKED		


UNMARKED OPAMPS (U1,U2) TL084
+15V PIN4
-15V PIN11
SMPTE IN FEMALE XLR
-11/S0
-10/S0
-12/S0
C12 220n
R14 10K
R15 22K
C9 10p
100K R21
R20 100K
R12 10K
220n C11
22K R13
C8 10p
U1 (d)
R19 10K
R26 10K
C19 270p
10K
C15 1n0
C16 270p
U2 (d)
+5
U3 LM311
2K2 RP10
17/S1 SCODE IN
R28 470R
R29 120K
39K
-15
SCODE OUT
19/S1
RP7 2K2
22K R1
C2 1n5
R3 18K
C1 3n3
R3 18K
220p
U1 (c)
+15
R5 560K
R4 22K
R6 10K
U1 (b)
R7 10K
R8 10K
U1 (a)
14/S0
SMPTE OUT (TO TAPE) MALE XLR
U2 (a)
R22 33R
13/S0
CLICK TRACK IN FEMALE XLR
-15/S0
-16/S0
N/C
C17 1µ
R24 10K
R25 22K
820p C18
100K R23
U2 (c)
U4 LM311
RP9 2K2
21/S1
R31 470R
R32 120K
-15 R33 39K
R10 1M
8·2n C10
U2 (b)
18/S0
CLICK TRACK OUT (TO TAPE) MALE XLR.
20/S1 COUT
CLOCK
R16 100K
R17 10K
C6 680p
AGND
10K R18
10µ C7
33R R11
17/S0
NOTE
XLR CONNECTIONS ARE ONLY SHOWN FOR CONVENIENCE: THEY ARE NOT MOUNTED ON CMI-29
SERIES II SYSTEMS: XLR's ARE ON CMI-36 OUTPUT BOARD CONNECTED TO SØ VIA RIBBON CABLE
SERIES I SYSTEMS: XLR's ARE MOUNTED IN EXTERNAL BOX CONNECTED TO SØ DIRECTLY OR TO PCB PINS INDICATED —o
ITEM
DESCRIPTION
REV'D
MATERIAL
REMARKS
GENERAL INTERFACE SUPPORT CARD
SCALE
PASSED
DATE
NOV '84
TIME CODE / CLICK TRACK IN OUT
DRAWN P.F.
TRACED
DESIGNED
DRAWING NUMBER
CMI 29
REV.4
SHEET 1 of 2
A3



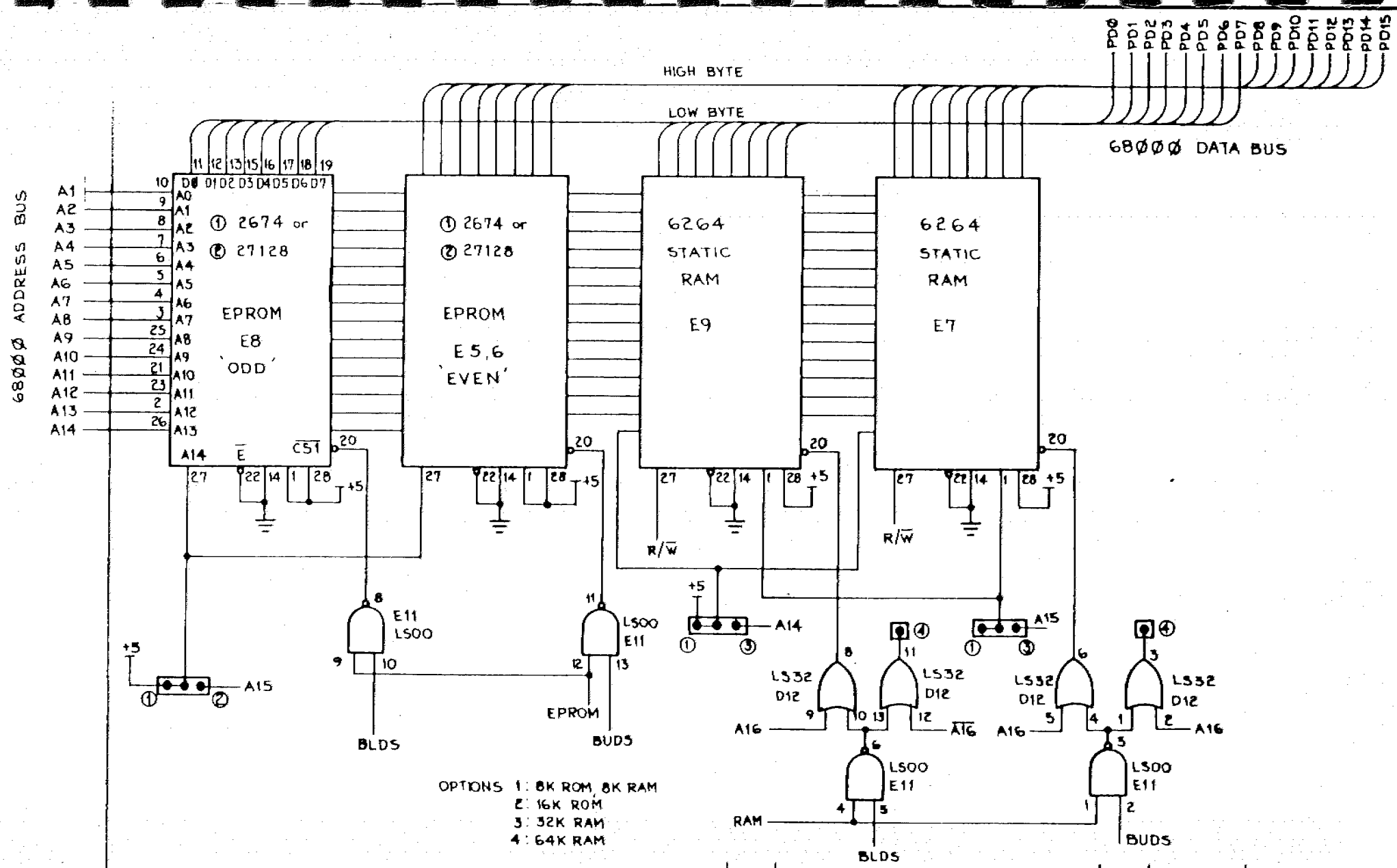


ITEM	DESCRIPTION	QTY	MATERIAL	REMARKS
GENERAL INTERFACE SUPPORT CARD.		SCALE		PASSED / DATE
				OCT. 84
MIDI CLOCK IN OUT		DRAWN PBF	REV. 4	DRAWING NUMBER CMI 29
		TRACED		SHT. 2 of 2
		CHECKED		



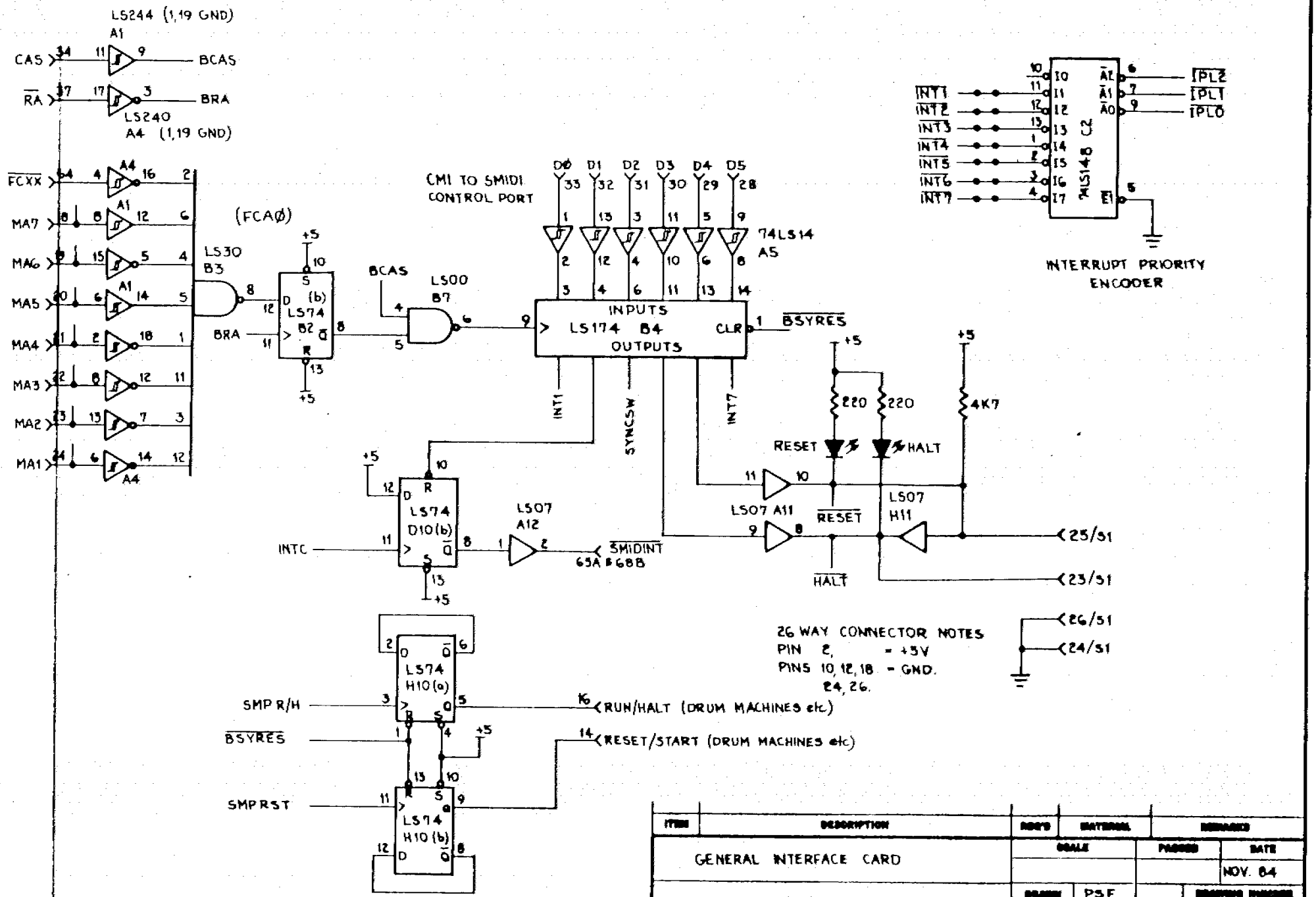
ITEM	DESCRIPTION	REV'D	MATERIAL	REMARKS
GENERAL INTERFACE CARD		SCALE	PROJECT	DATE
				NOV. 84
68000 PROCESSOR, ADDRESS DECODE, CLOCK	DRAWN P&F	REV 3	DRAWING NUMBER CMI 28	
	TRACED		SHEET 1 of 7	
	CHECKED			

A3

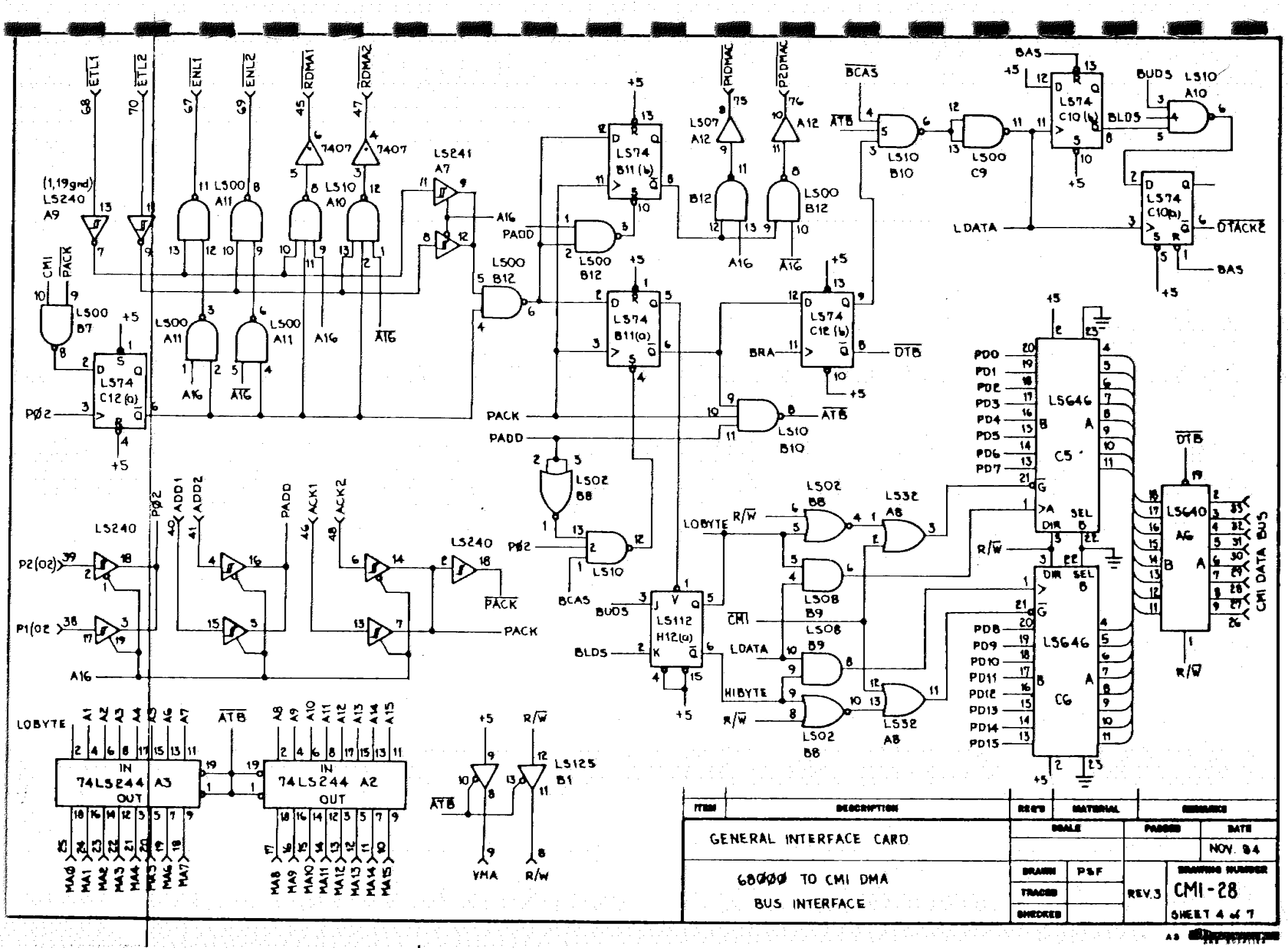


OPTIONS 1: 8K ROM, 8K RAM
2: 16K ROM
3: 32K RAM
4: 64K RAM

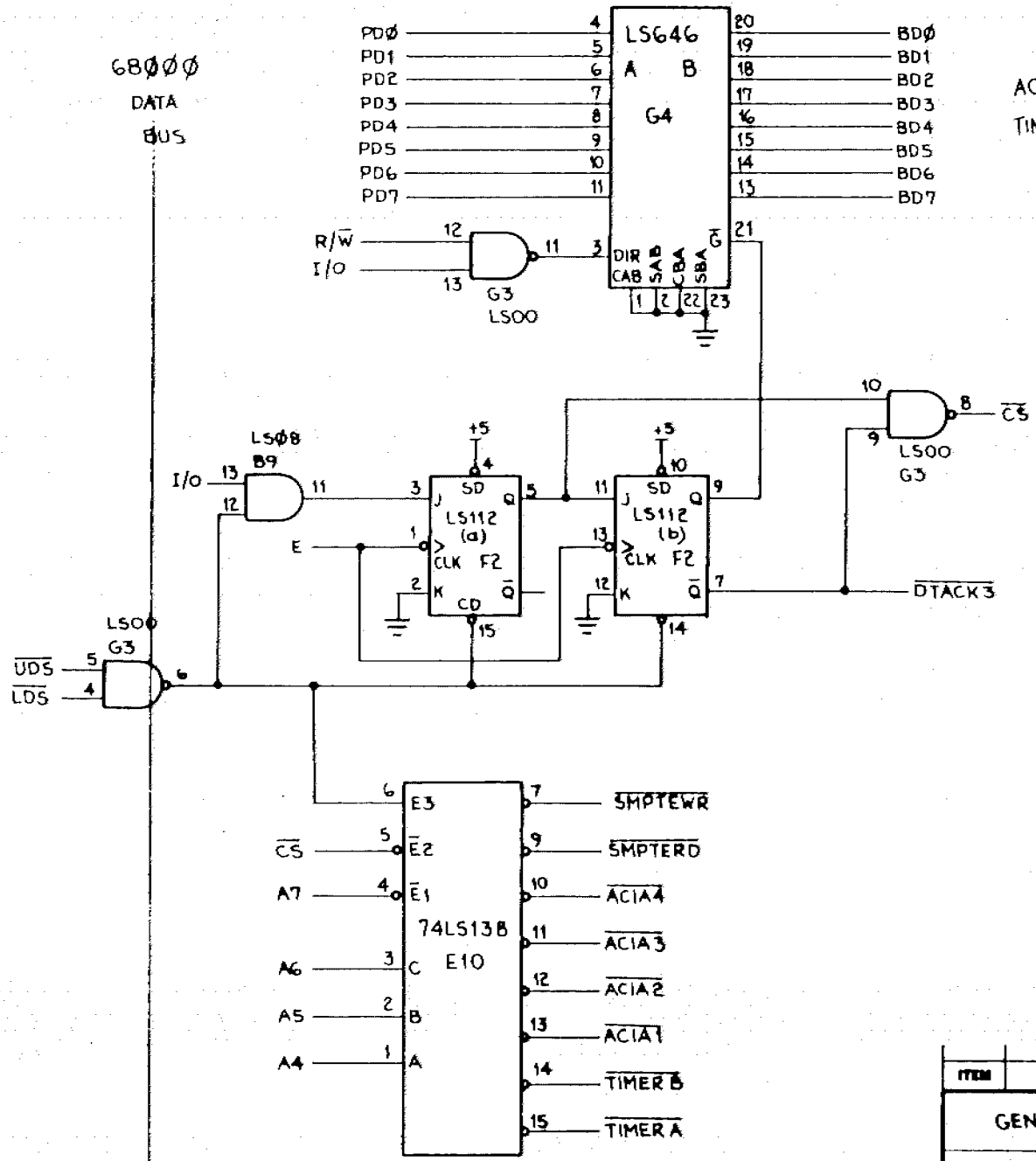
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	GENERAL INTERFACE CARD	SCALE	PAGE NO.	DATE
				NOV. 84
	MEMORY	DRAWN PSF	REV. 3	DRAWING NUMBER CMI-28
		TRACED		SHEET 2 of 7
		CHECKED		



ITEM	DESCRIPTION	NO'D	MATERIAL	REMARKS
GENERAL INTERFACE CARD		SCALE		PROOFED / DATE: NOV. 84
HALT/RESET CONTROL, INTERRUPT PRIORITY		DRAWN: PSF	REV 3	DRAWING NUMBER: CMI 28
		TRACED		SHEET 3 of 7
		CHECKED		

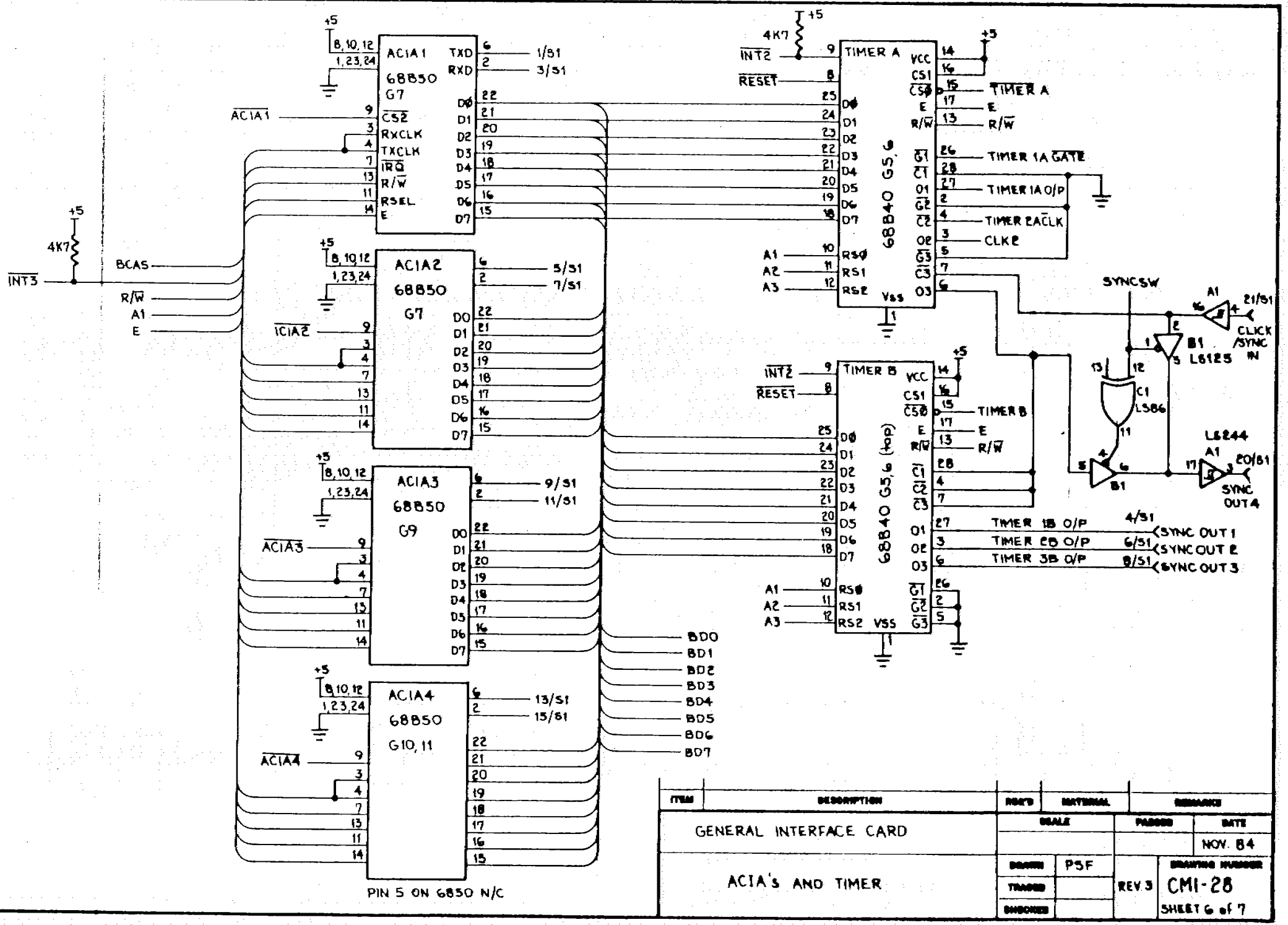


ITEM	DESCRIPTION	REV'D	MATERIAL	REMARKS
GENERAL INTERFACE CARD		SCALE	PAGES	DATE
				NOV. 84
68000 TO CMI DMA BUS INTERFACE	DRAWN P&F	REV.3	DRAWING NUMBER CMI-28	
	TRACED		SHEET 4 of 7	
	CHECKED			



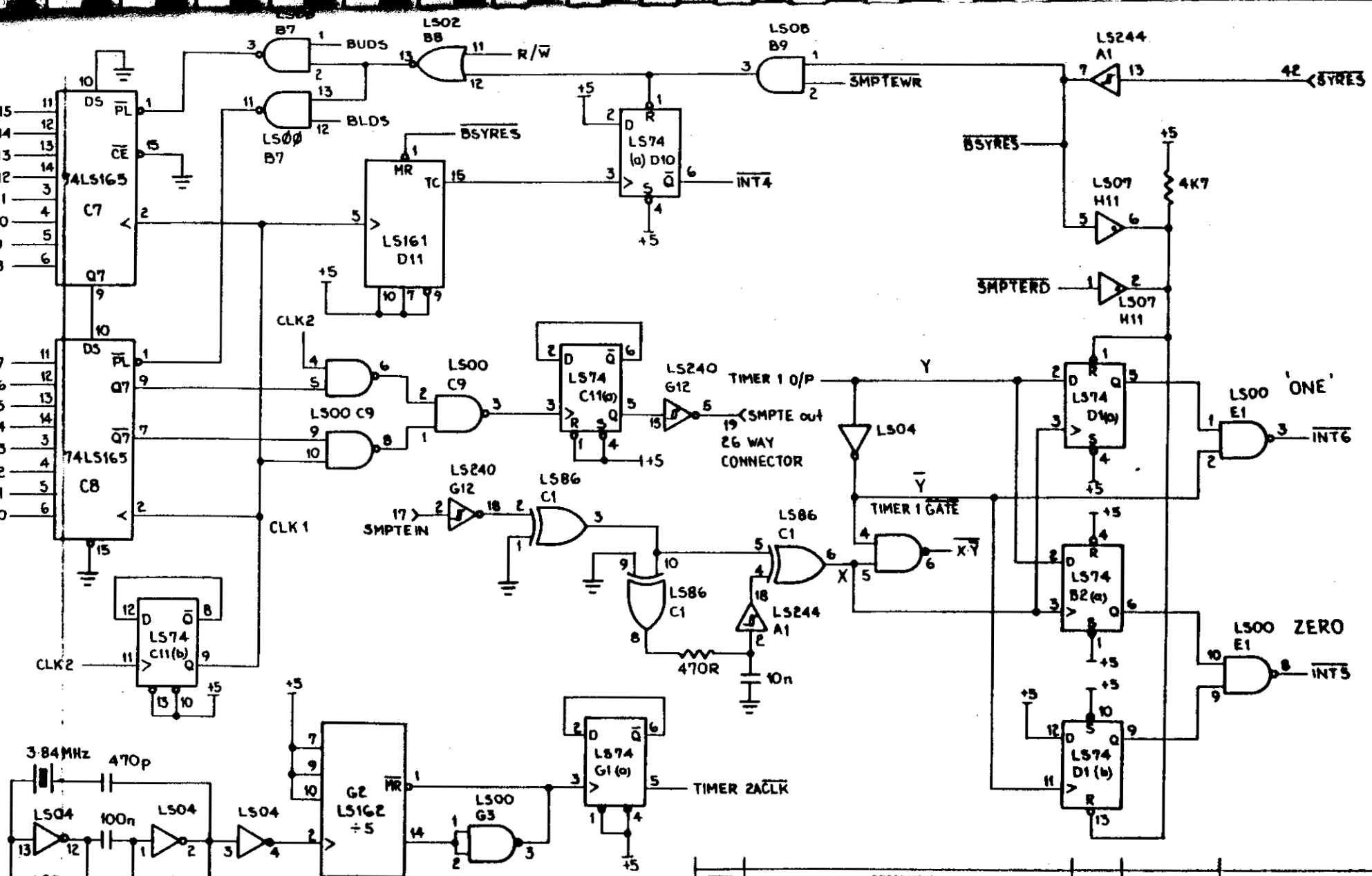
ACIA &
TIMER BUS

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
GENERAL INTERFACE CARD		SCALE		PROJECT / DATE
				NOV. 84
PERIPHERAL SELECT		DRAWN PSF		REV. 3
		TRACED		DRAWING NUMBER CM1-28
		CHECKED		SHEET 5 of 7

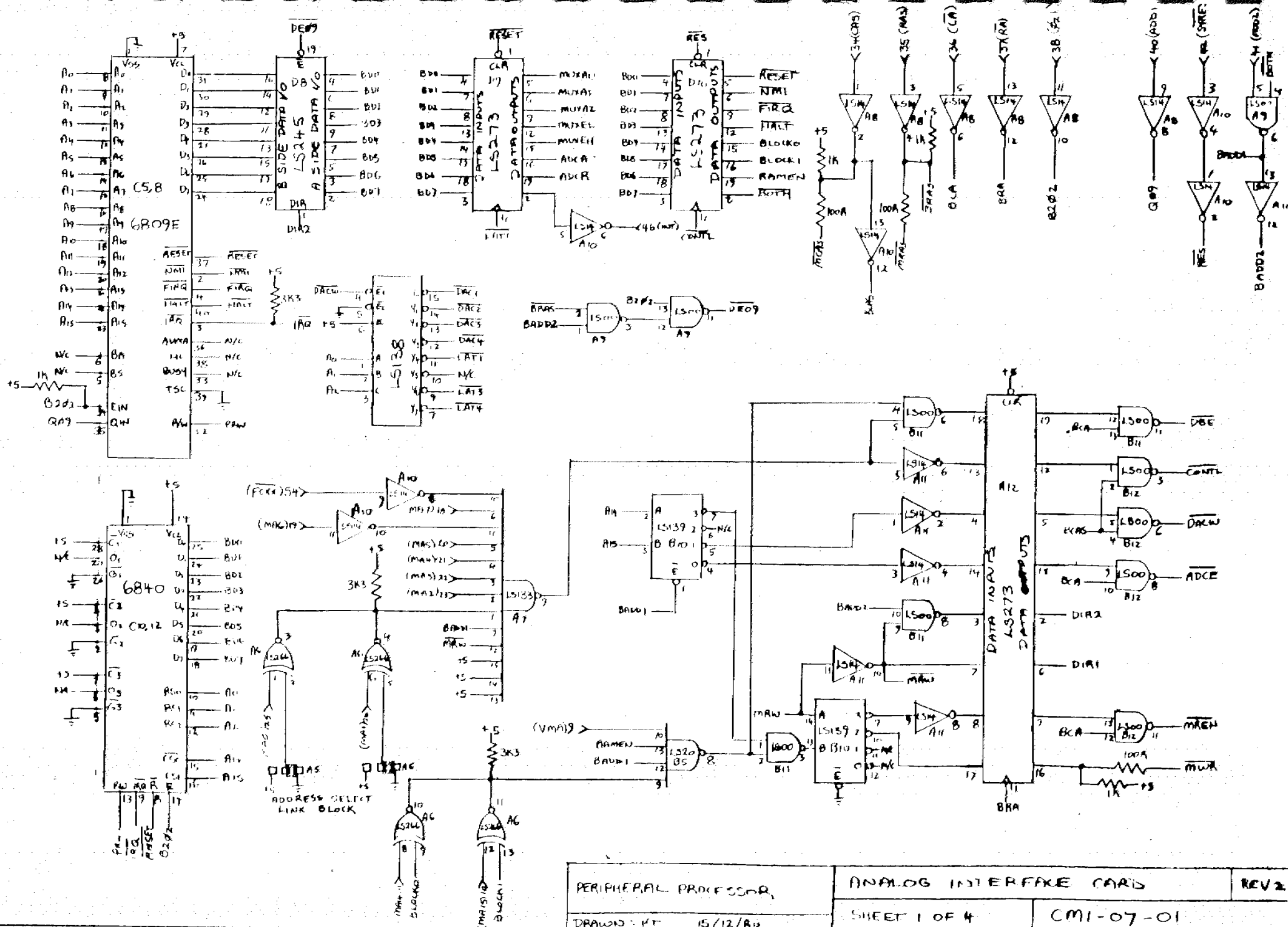


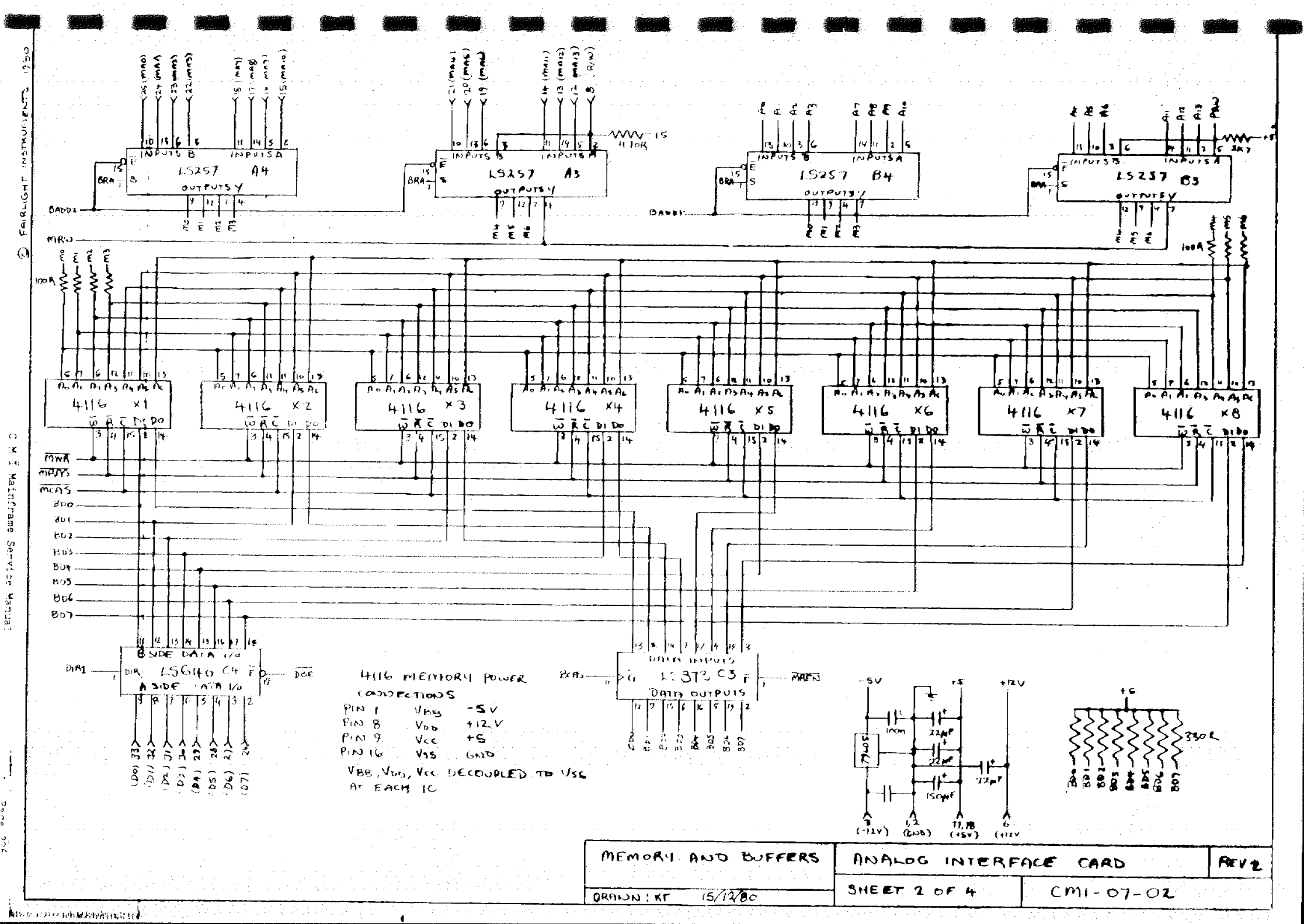
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	GENERAL INTERFACE CARD	SCALE	PASSED	DATE
				NOV. 84
	ACIA's AND TIMER	DRAWN PSF	REV. 3	DRAWING NUMBER CMI-28
		TRACED		SHEET 6 of 7
		CHECKED		

A3

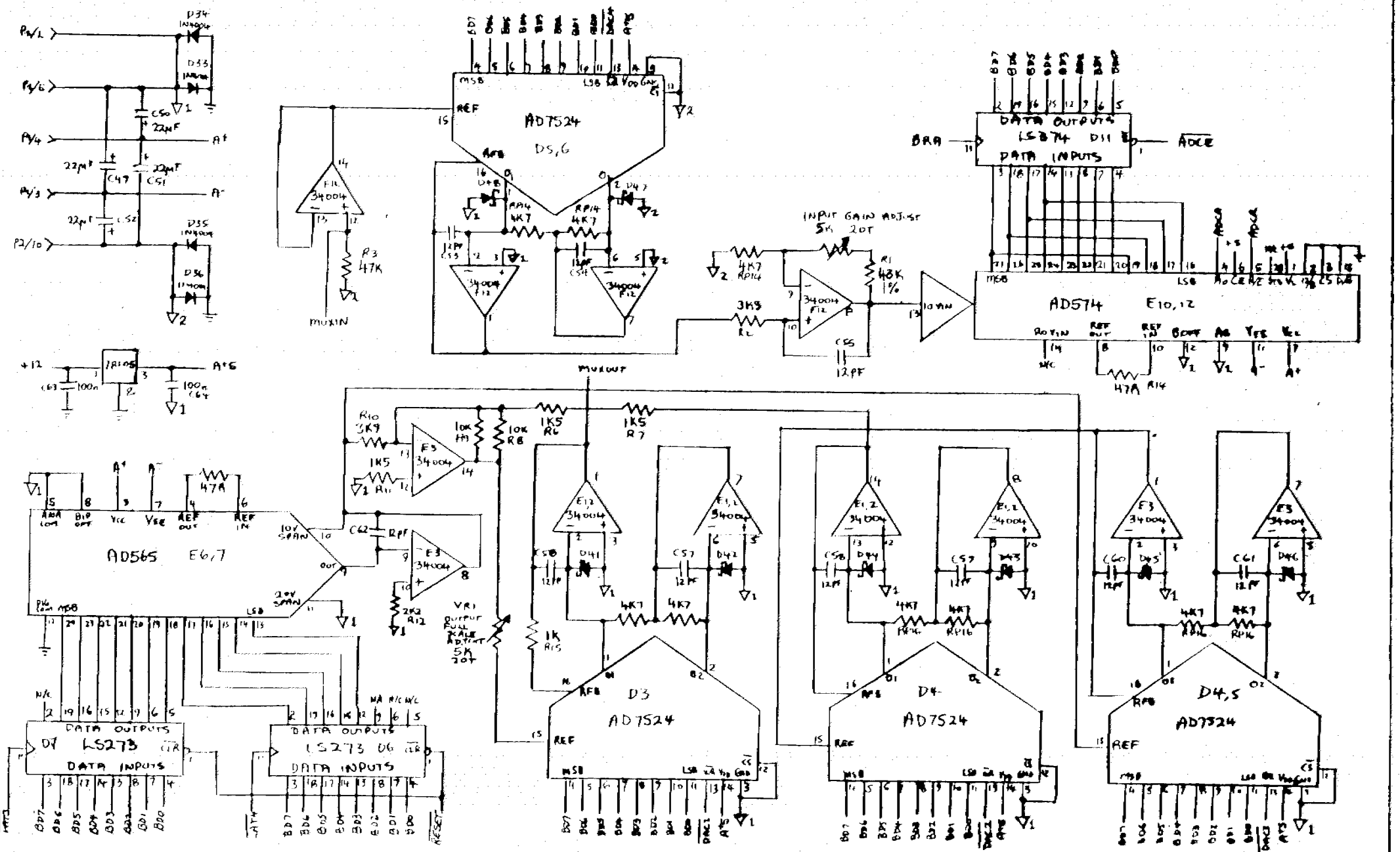


ITEM	DESCRIPTION	NOTES	MATERIAL	REMARKS
GENERAL INTERFACE CARD		SCALE	PROJECTION	DATE: NOV. 84
SMPTE CODE GENERATOR, DATA SEPARATOR AND READER		DRAWN: P&F; TRACED; CHECKED	REV. 3	DRAWING NUMBER: CMI - 28; SHEET 7 of 7

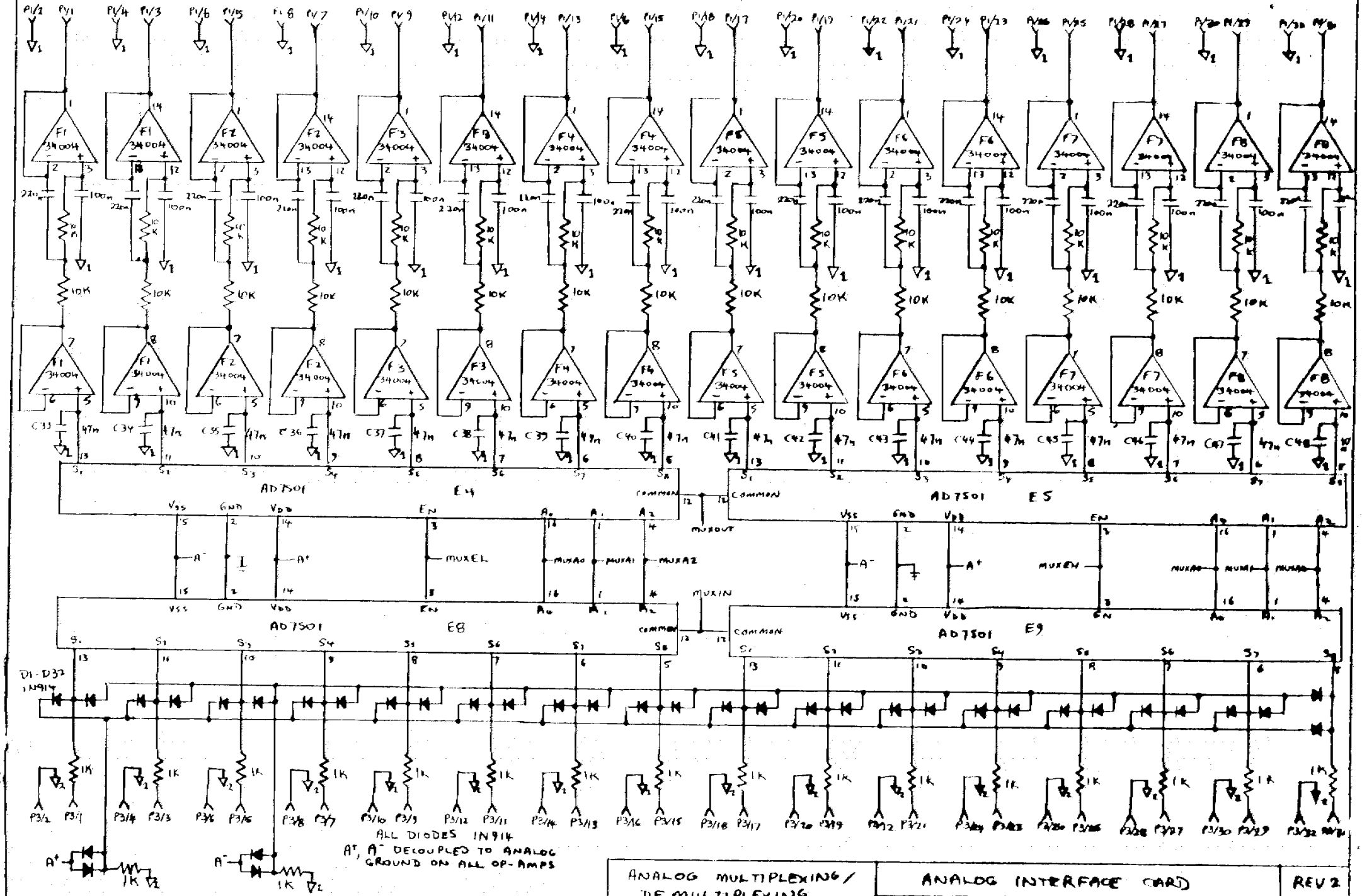

6809E
6840
LS245
LS273
LS373
LS139
LS32
LS244
LS14
LS00
3K3
1K
100R
ADDRESS SELECT LINK BLOCK
PERIPHERAL PROCESSOR
ANALOG INTERFACE CARD
REV 2
SHEET 1 OF 4
CM1-07-01
DRAWN: KT 15/12/80

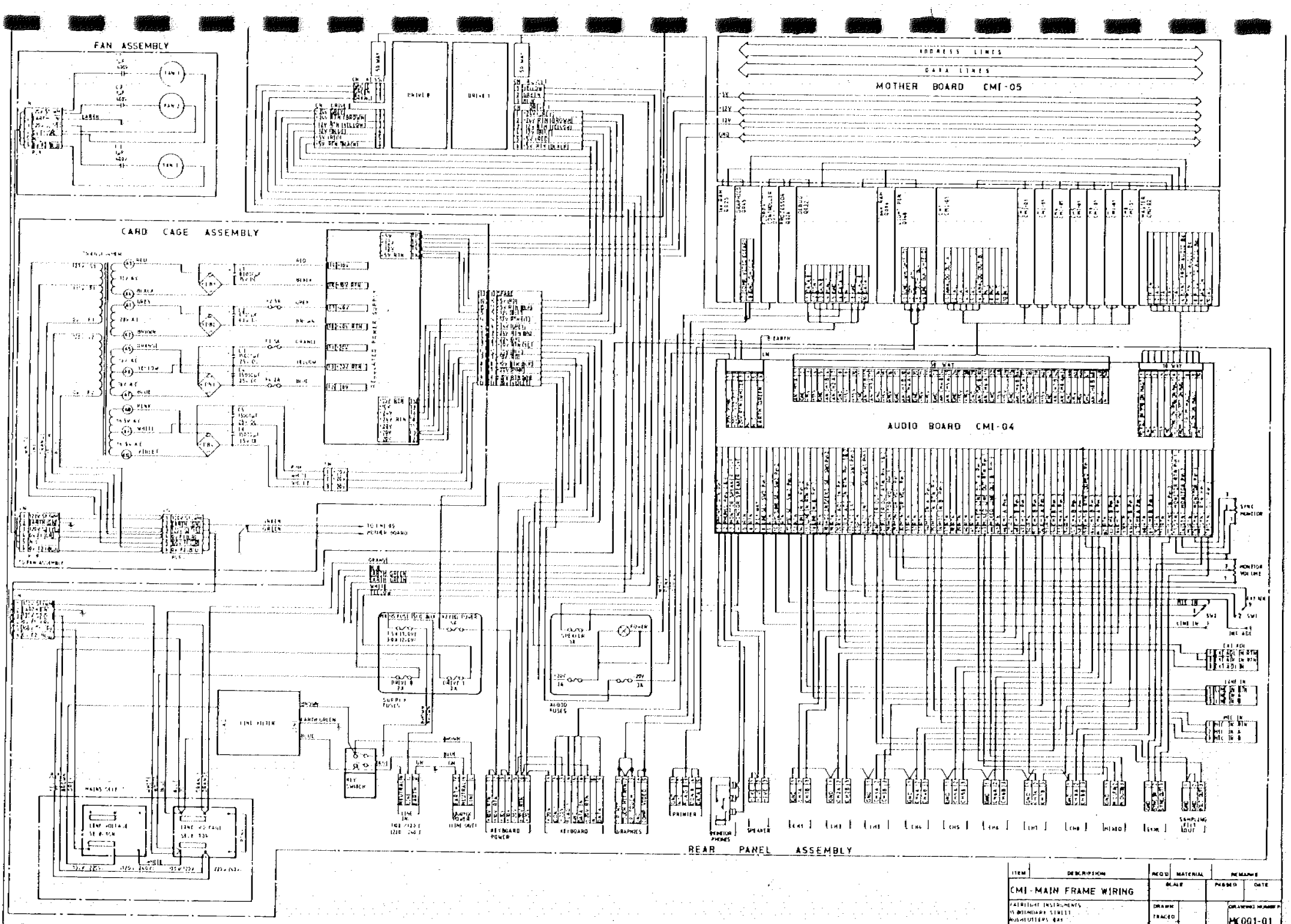


MEMORY AND BUFFERS	ANALOG INTERFACE CARD	REV 2
DRAWN: KT 15/12/80	SHEET 2 OF 4	CMI-07-02



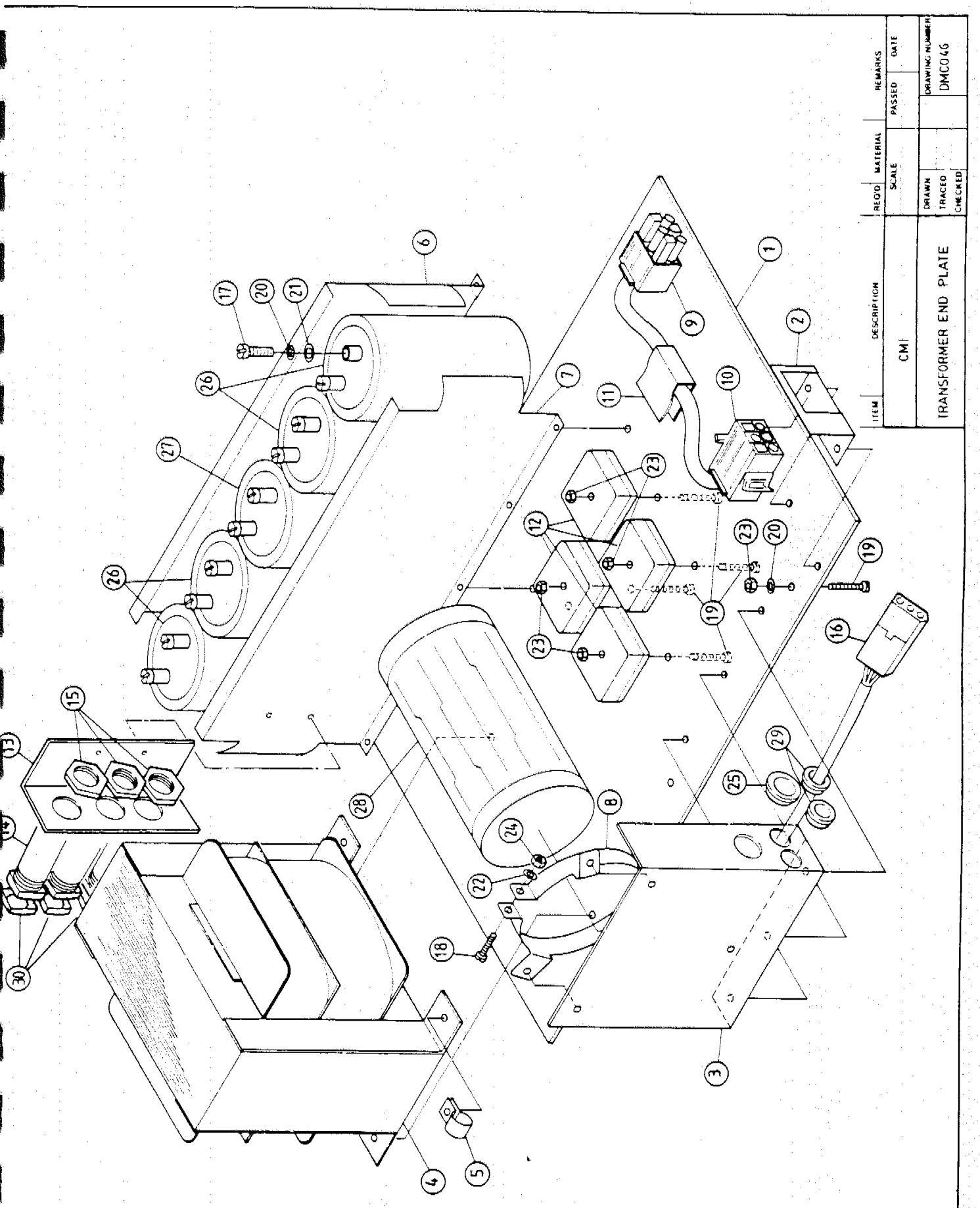
DIGITAL ↔ ANALOG CONVERSION	ANALOG INTERFACE CARD	REV 2
DRAWN: KT 15/12/80	SHEET 3 OF 4	CM1-07-03

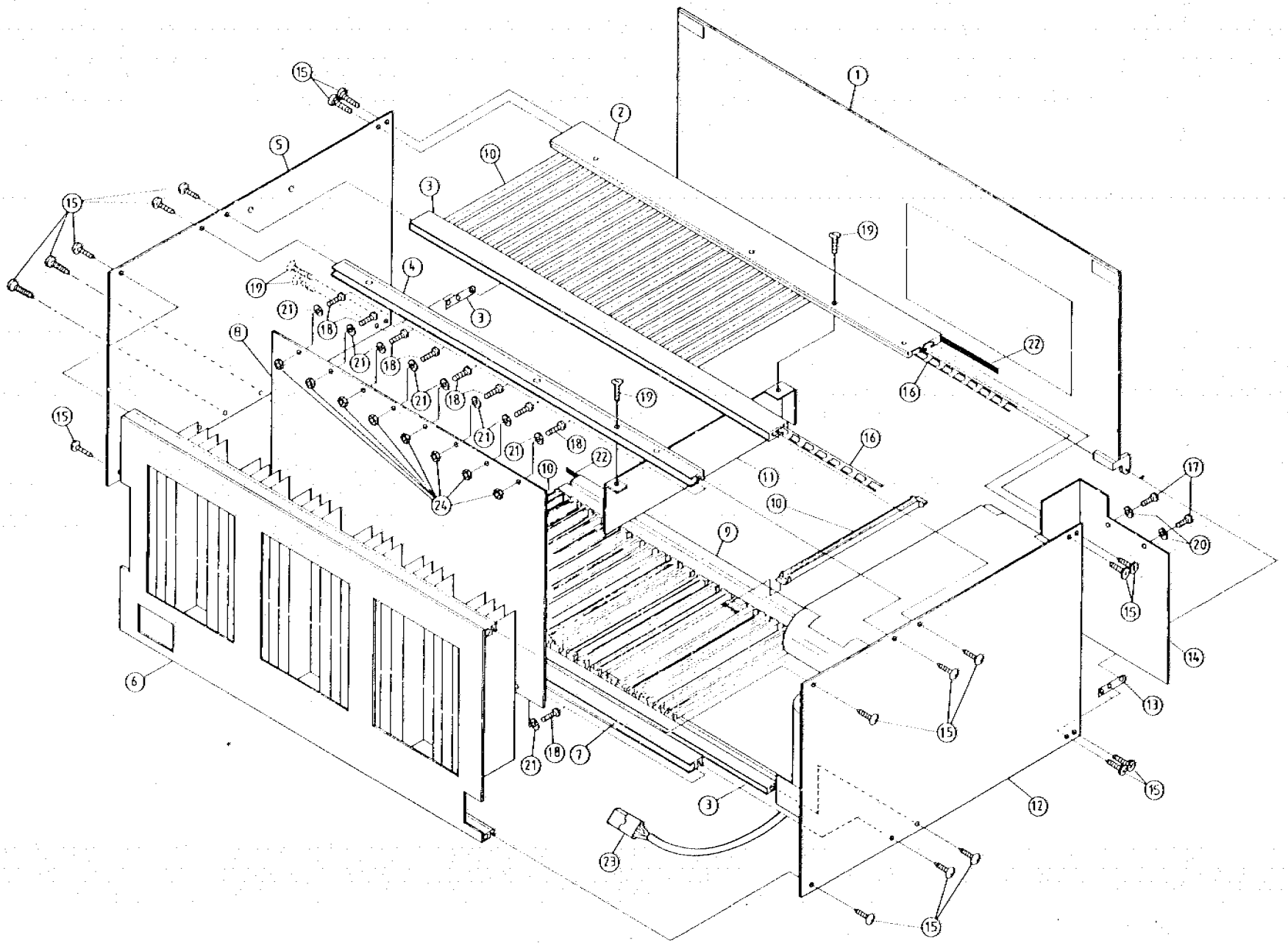

AD7501
E4
AD7501
E5
AD7501
E8
AD7501
E9
MUXEL
MUXIN
MUXOUT
MUXEN
COMMON
ALL DIODES IN914
A+, A- DECOUPLED TO ANALOG GROUND ON ALL OP-AMPS
ANALOG MULTIPLEXING / DE MULTIPLEXING
DRAWN: KT 15/12/80
ANALOG INTERFACE CARD
REV 2
SHEET 4 OF 4
CMI-07-04


FAN ASSEMBLY
CARD CAGE ASSEMBLY
MOTHER BOARD CMI-05
ADDRESS LINES
DATA LINES
AUDIO BOARD CMI-04
REAR PANEL ASSEMBLY
CMI-MAIN FRAME WIRING
PATRICIA INSTRUMENTS
PMK001-01

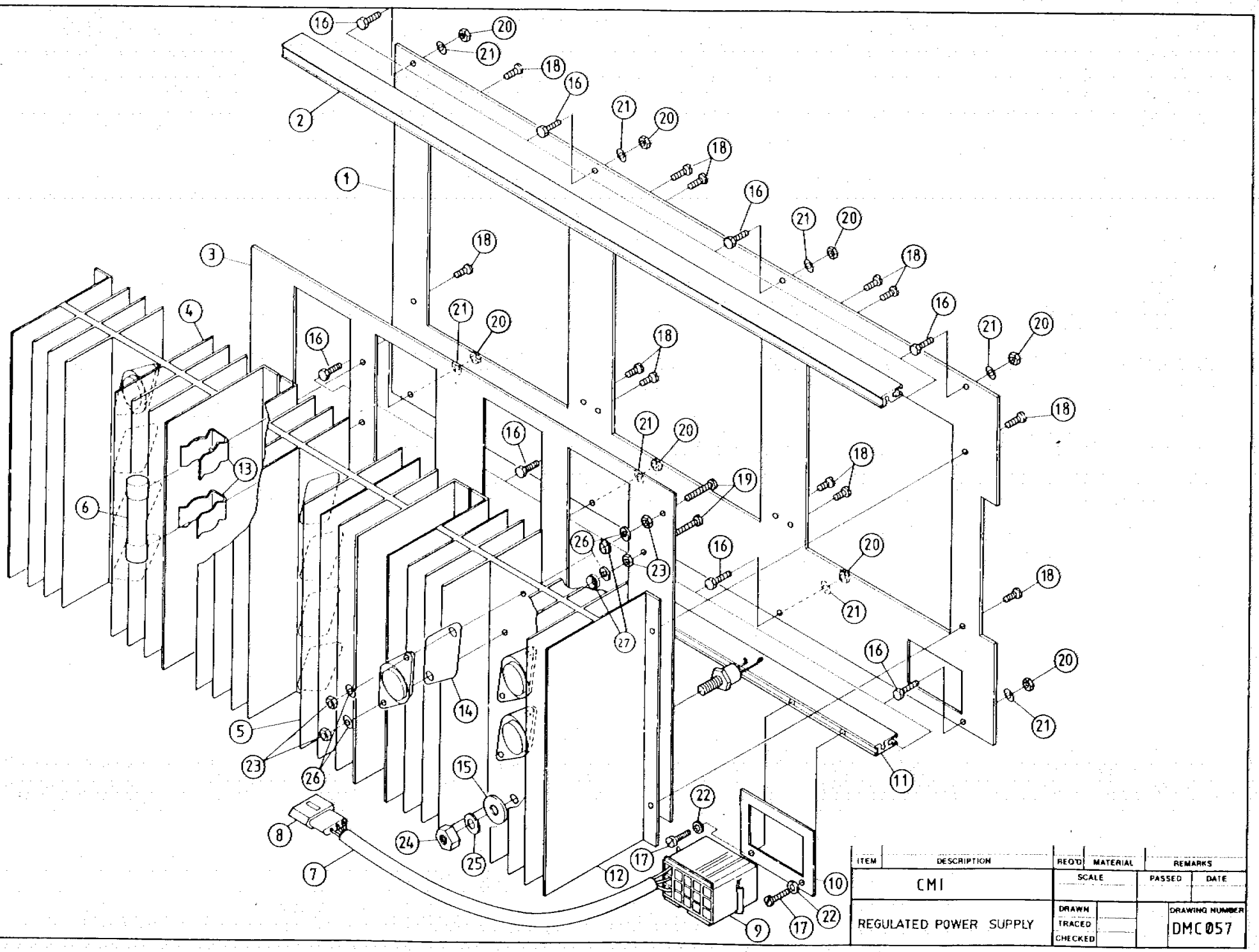
SECTION 13

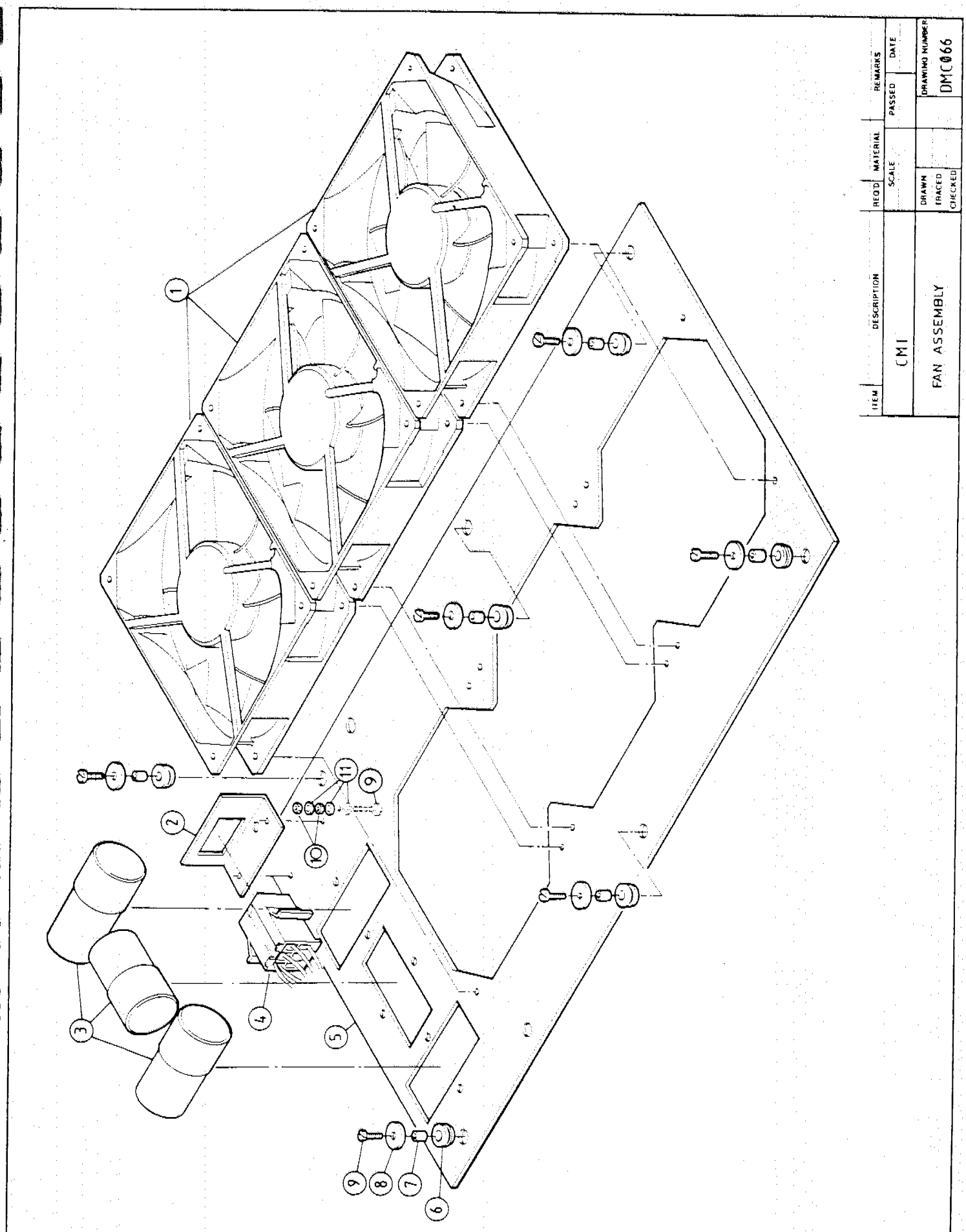
EXPLODED VIEWS

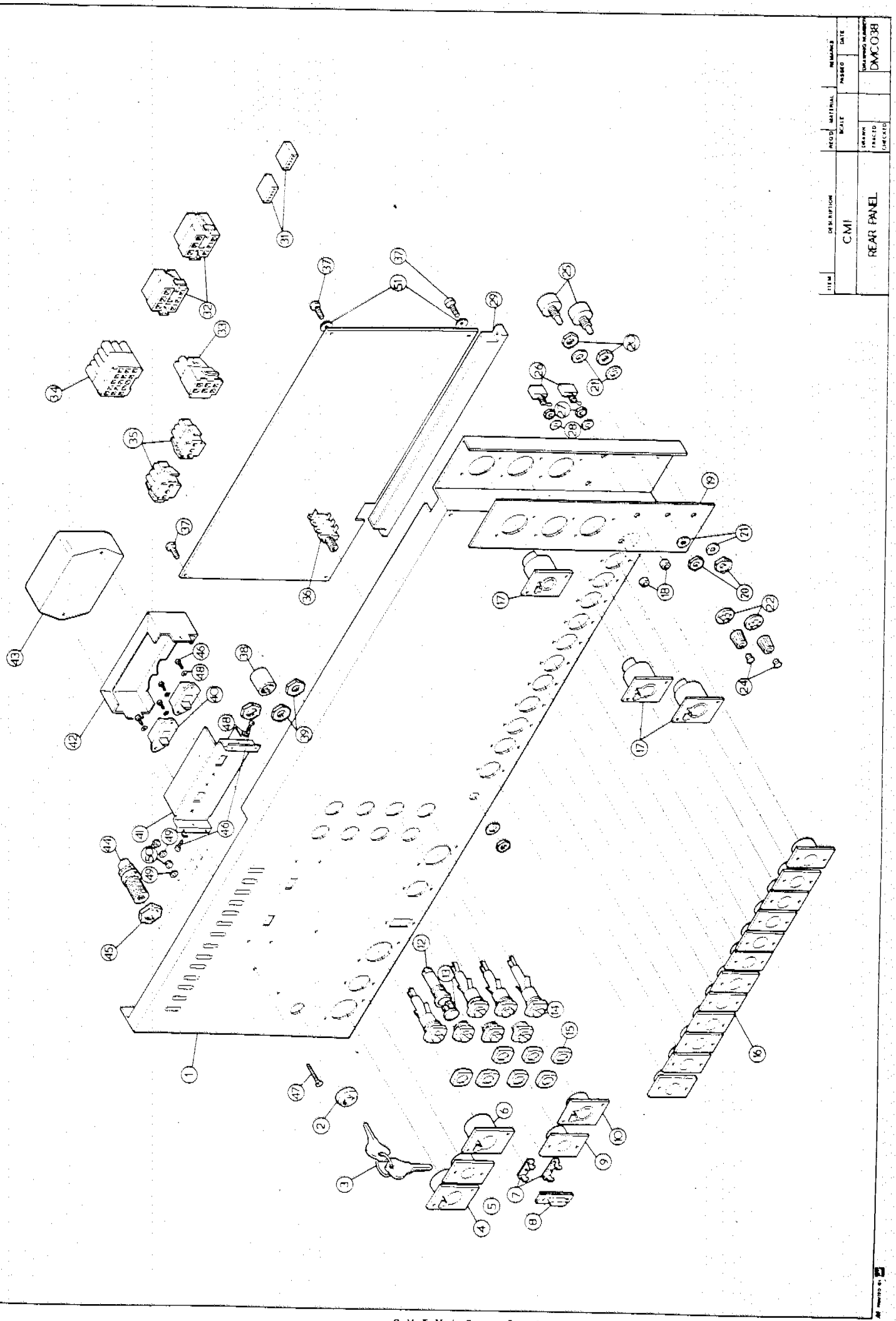

ITEM
DESCRIPTION
REQ'D
MATERIAL
REMARKS
CMI
SCALE
PASSED
DATE
DRAWN
TRACED
CHECKED
TRANSFORMER END PLATE
DRAWING NUMBER
DMC046

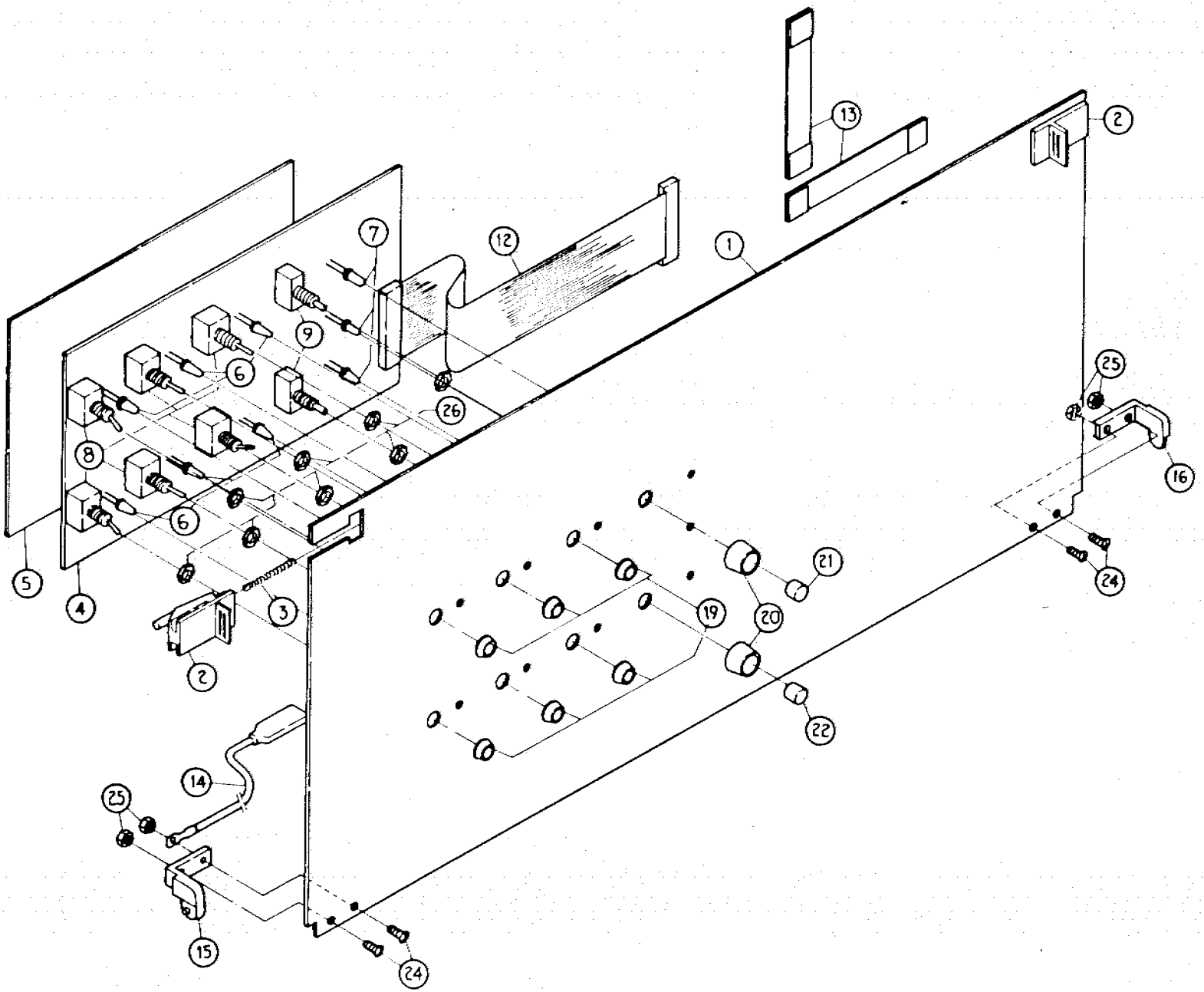


ITEM	DESCRIPTION	REQD	MATERIAL	REMARKS
CMI		SCALE	PASSED	DATE
CARD CAGE ASSEMBLY	DRAWN / TRACED / CHECKED			DRAWING NUMBER: DMC032

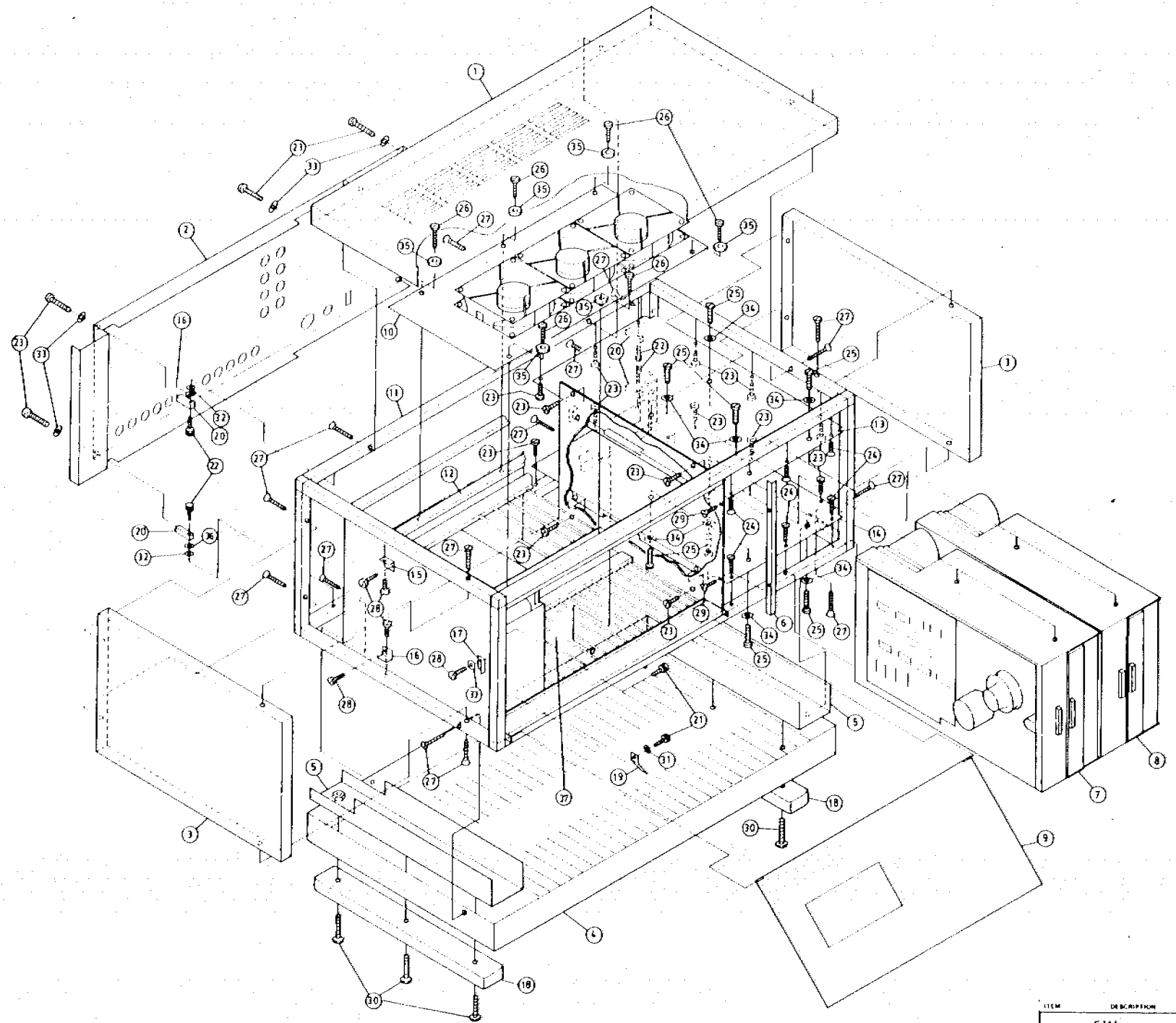

ITEM
DESCRIPTION
REQ'D
MATERIAL
REMARKS
CMI
SCALE
PASSED
DATE
REGULATED POWER SUPPLY
DRAWN
TRACED
CHECKED
DRAWING NUMBER
DMC057


ITEM
DESCRIPTION
REQ'D
MATERIAL
REMARKS
CMI
SCALE
PASSED
DATE
FAN ASSEMBLY
DRAWN
TRACED
CHECKED
DRAWING NUMBER
DMC066
A2 PRINTED BY


ITEM
DESCRIPTION
CMI
REAR PANEL
MOD'D
MATERIAL
SCALE
DRAWN
TRACED
CHECKED
PASSED
RELEASED
DATE
DRAWING NUMBER
DMC038



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	CMI	SCALE	PASSED	DATE
	FRONT PANEL ASSEMBLY	DRAWN TRACED		DRAWING NUMBER DMC042



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CMI		SCALE	PASSED	DATE
MAINFRAME		DRAWN / TRACED / CHECKED		DRAWING NUMBER DMC001

14. MECHANICAL PARTS LISTS

14.1 C.M.I MAINFRAME DRAWING REF.DMC0001

REF.NO	PART NO	DESCRIPTION	REMARKS
01	G0036	PANEL C.M.I TOP BEIGE	
02	MC038	PANEL C.M.I REAR BEIGE	
03	G0035	PANEL C.M.I SIDE BEIGE	
04	G0050	PANEL C.M.I BOTTOM BEIGE	
05	G0069	PANEL SUPPORT BASE	
06	G0090	STRIP C.M.I FRONT B/KG B/K	
07	G5054	DISK DRIVE LEFT (0)	
08	G5055	DISK DRIVE RIGHT (1)	
09	G0089	PANEL C.M.I FRONT	
10	MC066	FAN ASSEMBLY	
11	MC031	FRAME SPEED	
12	G0086	C/CAGE RAIL M/BRD UPPER	
13	G0033	PLATE DISK DRIVE TOP	
14	G0034	PLATE DISK DRIVE BOTTOM	
15	G0082	BRACKET CARD CAGE SUP TOP	
16	G0081	BRACKET CARD CAGE SUP LOWER	
17	G0083	BRACKET CARD CAGE SUP FRONT	
18	G0075	FOOT C.M.I WOOD	
19	G5230	UTH1058 MALE TERM	
20	G0076	SPACER REAR PANEL 1SHT	
21	H0134	SCREW 4BAX3/8" ALLEN	
22	H0135	SCREW 4BAX5/8" ALLEN	
23	H0112	SCREW 4BAX3/8"CHD	
24	H0136	SCREW 4BAX3/8" CSK	
25	H0116	SCREW UNC 3/8"X8/36" PAN	
26	H0112	SCREW 4BAX3/8" CHD	
27	H0101	SCREW 4BAX1" CSK BLACK	
28	H0133	SCREW 4BAX1/4" CHD	
29	H0117	SCREW 6BAX1/4" CSK	
30	H0132	SCREW 1" GUTTER	
31	H0008	WASHER 4BA STAR	
32	H0007	WASHER 4BA FLAT	
33	H0007	WASHER 4BA FLAT	
34	H0000	WASHER STAR INT.4MM ID	
35	H0001	WASHER 3/16" ID FLAT	
36	G0077	SPACER REAR PANEL 2 SHT	
37	MC032	C/CAGE ASSY C.M.I	

14. MECHANICAL PARTS LISTS (continued)

14.2 CARD CAGE ASSEMBLY DRAWING DMC032

REF.NO	PART NO	DESCRIPTION	REMARKS
01	MC042	ASSY C.M.I FRONT PANEL	
02	G0084	RAIL C/CAGE FT UPPER	
03	D9010	RAIL C/CAGE MIDDLE	
04	G0086	RAIL C/CAGE M/BRD UPPER	
05	G0048	PLATE C.M.I C/CAGE RH	
06	MC057	ASSY C.M.I REG PSU	
07	G0087	RAIL C/CAGE M/BRD LOWER	
08	MCMI05	CARD MOTHER CMI	
09	G0085	RAIL C/CAGE FT LOWER C.M.I	
10	D9014	GUIDE CARD V35-1321A	
11	G0068	COVER FILTER CAPACITORS	
12	MC046	ASSY C.M.I TXFORMER END PLATE	
13	D9012	PLATE HINGE V35-0501G	
14	G0063	COVER C.M.I TXFORMER	
15	D9018	SCREW 6GX1/2" V27-1299	
16	D9021	SPACER STRIP V35-0481K	
17	H0124	SCREW 6BAX1/4" CHD	
18	D9015	SCREW M3X10, V41-1374D	
19	H0117	SCREW 4BAX1/2" CSK	
20	H0011	WASHER 6BA FLAT	
21	H0009	WASHER 1/8" ID FIBRE	
22	D9022	STRIP IDENT V41-1660J	
23	G5213	CONNECTOR UTH9373-3R	
24	D9006	NUT M3	

14.3 MAINFRAME REAR PANEL DRAWING DMC038

REF.NO	PART NO	DESCRIPTION	REMARKS
01	G0056	PANEL C.M.I REAR	
02	H0213	NUT DRESS KEY SWITCH	
03	D8014	KEY SWITCH YALE	
04	D6709	CONNECTOR CAN PANEL LINE 3S	
05	D6736	CONNECTOR CAN PANEL LINE 3P	
06	D6739	CONNECTOR CAN PANEL 7S	
07	D6731	LUG DMINI LOC/LATCH	
08	D6727	CONNECT DMINI 9S	
09	D6721	CONNECTOR PANEL 5P	
10	D6710	CONNECTOR PANEL 5S	
11	H0016	WASHER HEAD PHONE SOCKET	
12	G5410	HOLDER LAMP 01030AC	
13	G5412	BEZEL RED 012319 AC	
14	G5309	HOLDER FUSE	
15	G5190	TOP FUSE HOLDER B/K	
16	D6720	CONNECTOR PANEL 3P	
17	D6719	CONNECTOR PANEL 3S	
18	H0205	NUT DRESS SMALL	
19	G0079	ESCUTCHEON C.M.I REAR PANEL	
20	H0020	NUT 10K POT	
21	H0021	WASHER 10K POT	
22	G5403	POINTER KNOB SMALL	
23	G5408	KNOB B/K SMALL	
24	G5409	TOP RED SMALL KNOB	
25	R4009	POT 10K LIN	
26	D8006	SWITCH 7101A	
27	H0207	NUT SWITCH HEX	
28	H0017	WASHER SWITCH STAR	
29	D6726	AMT SOC-78	
30	MCMI04	CARD AUDIO C.M.I-04	
31	D6021	CONNECTOR 10 WAY SHELL	
32	D6744	CONNECTOR AMP 6P	
33	G5222	CONNECT UT 6P	
34	G5224	CONNECTOR UT 15P	
35	D6713	CONNECTOR D/DRIVE LINE	
36	G5171	SOCKET H/PHONE C.M.I	
37	H0133	SCREW 4BAX1/4" CHD	
38	H0211	NUT SWITCH ASC	
39	H0208	NUT FUSE HOLDER	
40	G5159	SWITCH SLIDE	
41	G0098	BRAKET C.M.I A/C SELECT	
42	G0099	COVER C.M.I A/C SELECT	
43	G5155	FILTER MAINS	
44	D8010	SWITCH LINE KEY	
45	H0214	NUT HEX KEY SWITCH	
46	H0124	SCREW 4BAX3/4" CSK	
47	H0106	SCREW 4BAX3/4" CSK	
48	H0011	WASHER 6BA FLAT	
49	H0008	WASHER 4BA STAR	
50	H0202	NUT 4BA HEX	
51	H0010	WASHER 5/32"X3/8" FILTER	
52	H0215	NUT H/PHONE SOCKET	

14. MECHANICAL PARTS LISTS (continued)

14.4 FRONT PANEL ASSEMBLY DRAWING DMC042

REF.NO	PART NO	DESCRIPTION	REMARKS.
01	G0089	PANEL C.M.I FRONT BEIGE	
02	D9003	VERO HINGE BOLT	
03	D9004	VERO HINGE SPRING	
04	MQ137	CARD FRONT PANEL	
05	G0007	INSULATOR FRONT PANEL	
06	D5203	LED YELLOW 5MM	
07	D5202	LED RED 5MM	
08	D8004	SWITCH DPDT 7211C	
09	D8001	SWITCH SPDT 8121C	
12	M3034	CABLE Q137	
13	G5106	CLAMP FLAT CABLE	
14	MC020	CABLE STATIC FRONT PANEL	
15	D9031	VERO HINGE BRACKET LEFT	
16	D9030	VERO HINGE BRACKET RIGHT	
19	H0205	NUT C&K DRESS SMALL	
20	H0206	NUT C&K DRESS LARGE	
21	D8002	TOP C&K SWITCH ORANGE	
22	D8003	TOP C&K SWITCH YELLOW	
23	D8011	SPRING C&K SWITCH	
24	D9005	VERO SCREW M3X8	
25	D9006	VERO NUT M3	
26	H0207	NUT C&K HEX	

14. MECHANICAL PARTS LISTS (continued)

14.5 TRANSFORMER END PLATE DRAWING DMC046.

REF.NO	PART NO	DESCRIPTION	REMARKS
01	G0051	PLATE C.M.I C/CAGE L.H.AND	
02	G0066	BRACKET C.M.I AC CONNECTOR	
03	G0054	BRACKET C.M.I CAP MTG.AND.	
04	G5167	TXFORMER C.M.I 1 ALKAY	
05	G5205	CLAMP CORD UTH906	
06	G0052	BRKT C.M.I CAP MTG TOP AND	
07	G0053	BRKT C.M.I CAP MTG BOT AND.	
08	C7611	CLIP CAP ELECT SIZE 16	
09	G5223	CONNECTOR UTM3191.6R	
10	G5222	CONNECTOR UTM3191.6P	
11	G5122	CLIP CABLE GREY 3M	
12	D2003	RECTIFIER BRIDGE MDA3504	
13	G0064	BRACKET C.M.I C/CAGE FUSES	
14	G5309	HOLDER FUSE FLUSH L2004	
15	H0208	NUT FUSE HOLDER L2004	
16	G5213	CONNECTOR UTH9373-3R	
17	H0128	SCREW CAPACITOR	
18	H0102	SCREW 4BAX1/2" CHD	
19	H0127	SCREW 4BAX3/4" CHD	
20	H0014	WASHER STAR CAPACITOR	
21	H0013	WASHER CAP Elet	
22	H0008	WASHER 4BA STAR	
23	H0202	NUT 4BA HEX	
25	G5113	GROMMET PLASTIC 5/8 DIA	
26	C7603	CAP ELCT 15KUF 25V CAN	
27	C7601	CAP ELCT 4K7UF 63V CAN	
28	C7604	CAP ELCT 68KUF 16V CAN	
29	G5114	GROMMET PLASTIC 3/8 DIA	
30	G5190	TAP FUSE HOLDER L2004	

14.6 REGULATED P.S.U ASSEMBLY DRAWING DMC057

REF.NO	PART NO	DESCRIPTION	REMARKS
01	G1050	PLATE HEATSINKS	
02	D9011	RAIL P.S.U UPPER V	
03	MQPS2	CARD P.S.U	
04	G0111	HEATSINK REG	
05	G0112	HEATSINK TRANSISTOR	
06	G5305	FUSE 15A	
07	MC049	CABLE P.S.U HARNESS	
08	G5213	CONNECTOR 3PIN UTH.	
09	G5227	CONNECTOR 15PIN UTM3191.15R	
10	G0065	BRACKET CONNECTOR DC	
11	G0087	RAIL P.S.U LOWER	
12	G0113	HEATSINK SCR	
13	G5306	HOLDER FUSE	
14	H0003	WASHER MICA T03	
15	H0004	WASHER MICA SCR	
16	D9019	SCREW M3X8 V41-1376E	
17	H0112	SCREW 4BAX3/8" CHD	
18	H0133	SCREW 4BAX1/4" CHD	
19	H0122	SCREW 6BAX3/4" CHD	
20	D9006	NUT M3 V41-0505B	
21	D9016	WASHER M3 VERO	
22	H0008	WASHER 4BA STAR	
23	H0201	NUT 6BAX HEX	
24	H0212	NUT SCR HEX	
25	H0015	WASHER SCR FLAT	
26	H0011	WASHER 6BA FLAT	
27	G0114	BUSH NYLON T03	

14.7 FAN ASSEMBLY DRAWING DMC066

REF.NO	PART NO	DESCRIPTION	REMARKS
01	G5148	FAN EP114H-25	
02	G0066	BRACKET C.M.I AC	
03	C7301	CAP 1UF 440-1200	
04	G5223	UTM3191-6R	
05	G0270	PLATE FAN MOUNTING BM	
06	G5178	GROMMET RUBBER M16	
07	G5111	SPACER 4BA CLEARX1/4"	
08	H0001	WASHER 3/16" ID FLAT	
09	H0112	SCREW 4BAX3/8" CHD	
10	H0202	NUT 4BA HEX	
11	H0008	WASHER 4BA STAR	

MITSUBISHI FLOPPY DISK DRIVE, M2896-63

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. DISK DRIVE OPTIONING AND ALIGNMENT

.1 Disk Drive Optioning

ptioning may only need to be done if the disk drive has been returned to a itsubishi service centre. If returned to a Fairlight service centre, the drive ill be correctly optioned to perform correctly on the C.M.I.

ɔtion blocks to be shorted - Mitsubishi M2896-63 Rev G

JFC, PS, SE, DC, M2, S2, I, R, IT, MS,
MO, RFA, HR, A, HUN, WP, DS, 2S, RM

ıditional wire link option - Y

.l other option blocks to be left open. See Figure 3.1 for option block ɔcations.

.2 Disk Drive Alignment

.sk drives may require checking to account for any maladjustments which may ɔcur during shipment. This requires the Fairlight Disk Diagnostic Diskette ɔntaining the command **DSKTST.CM.**

ıe disk drive under test should be able to load test programs, however if the ɔndition of the disk drive under test is suspect then another known good disk ·ive should be used to load the test program and used to run the tests on the .ulty disk drive.

2.1 Radial Alignment

cause disk drives utilize double density disk format, radial alignment is itical and is best performed by Fairlight or Mitsubishi. To ascertain whether ive alignment is correct, run the DSKTST command from the Fairlight agnostic disk.

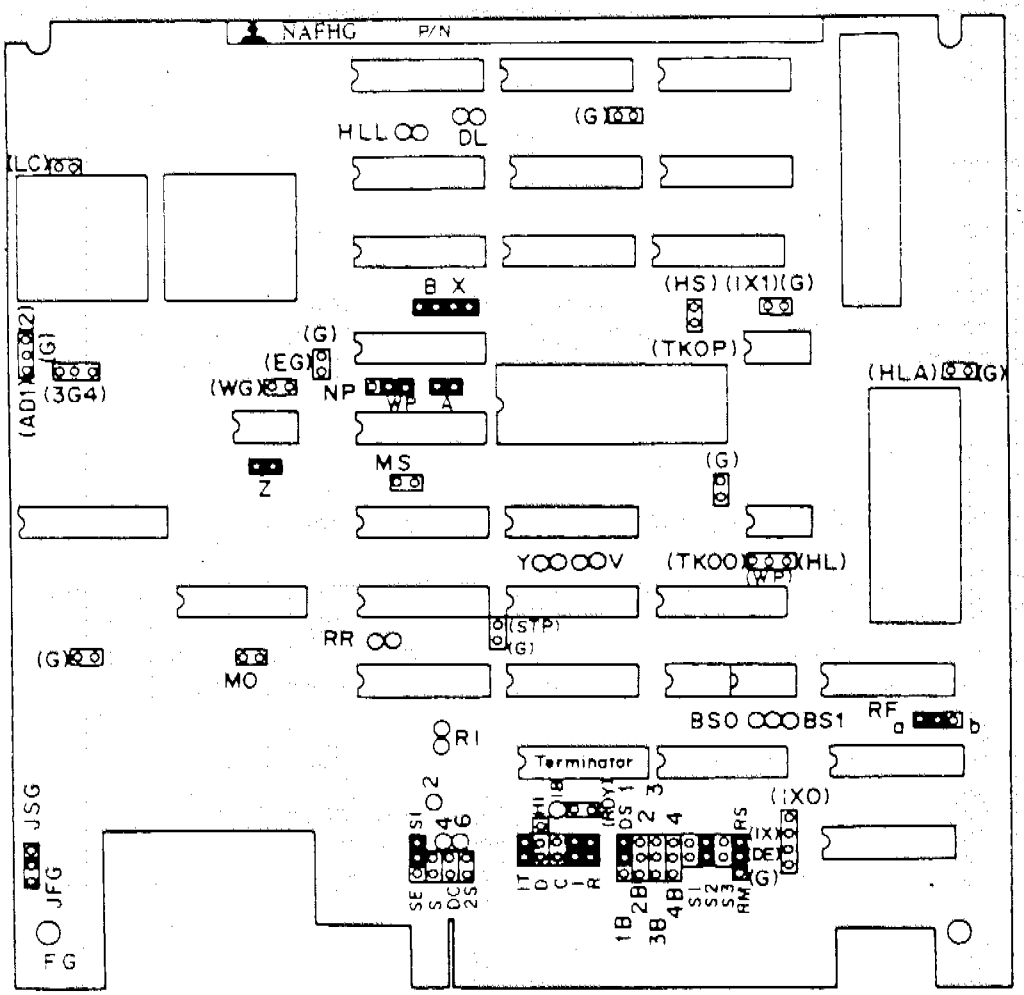


Figure 3.1 Printed Circuit Board Option Block Location

4. DISK DRIVE MAINTENANCE

Under normal circumstances preventive maintenance is not required on the M2896. If severely dirty environments are encountered, an occasional cleaning of the drive may be performed to assure continued reliable performance.

Only basic corrective maintenance is documented here. If it is determined that a disk drive requires more extensive repairs than are described in this section, return the unit to Fairlight Instruments for service. This document should provide sufficient information to determine whether return of the unit is necessary.

4.1 Preventative Maintenance

4.1.1 Visual Check

Visual inspection is the first step in any maintenance operation. Always look for corrosion, dirt, wear, binds, and loose connections. Noticing these items may save downtime later.

4.1.2 Cleaning

Cleanliness cannot be overemphasized in maintenance of the M2896.

Caution: The head/carriage assembly is a factory-adjusted and tested assembly. Do not try to adjust or repair this internal component. Do not, for any reason, clean the read/write heads. To do so would cause severe damage to the head surfaces or head spring supports.

Parts	Observe	Procedure
1. Main Frame	Inspect for loose screws, connectors, switches, etc.	Clean main frame

5. FLOPPY DISK SYSTEM DIAGNOSIS

The Floppy Disk System comprises of the QFC-9 Floppy Disk Controller as well as the disk drives themselves. The first step in servicing the system with an apparently faulty disk system is to establish in what subassembly the fault actually lies.

The general procedure to follow in disk system fault tracing is:

(1) Check all disk system cables, especially the 50 way flat cable for open circuits or shorts and ensure all connections are secure.
(2) Use the system test program CHECK to determine if the fault is in the drive itself (or the diskette) or the disk controller/DMA data transfer system.
(3) If the disk drive is faulty, use DSKTST to further analyse the fault.
(4) Otherwise, refer to the CMI Mainframe manual to trace the fault in the QFC-9 controller.

5.1 Test Program CHECK

Allows checking of;

- Cyclic Redundancy Check (CRC) errors
- Data transfer between memory and disk
- RAM bit corruption errors

Command Syntax

CHECK <UNIT>,<HEXNUM>;<OPTIONS>

where <UNIT> = <COLON><NUMBER>

<HEX DIGIT> = number 1 to 9 and/or letter A to F

e.g., CHECK<return> performs CRC on DRIVE 0.
CHECK :1<return> performs CRC on DRIVE 1.
CHECK :1;V<return> performs CRC on DRIVE 1 with V option.

(1) Disk Integrity Check

Options: none required

This is the default CHECK routine. Entire disk in specified drive is read to check for CRC errors.

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

(2) Read Data D.M.A. Verify

Option: V

Reads entire disk in specified drive twice, into separate blocks of memory and verifies data against itself.

(3) Write Data D.M.A. Verify

Options: W,D (May be used together)

The W option creates a file, writes distinctive data to each sector of the file and reads each sector of the file back, twice, into different areas of memory for verification. All unfree disk space will be allocated to the file.

The D option is a destructive (to the disk contents) test which writes a unique "ADD -29" pattern to each sector in an interleaved fashion, reads it back, and verifies the data.

Interleaving of blocks ensures track boundaries are continually being crossed. A delay can be introduced using the "T" option (see below) to isolate head-load timing problems.

(4) Other Options

Option	Use with	
R	W	use random number pattern instead of "29" pattern
P=XX	W	use pattern XX where XX = <hex number> write the pattern to disk, read back and verify
E=XX	all	print error if total recoverable disk errors exceed XX where XX = <hex number>. Default value is 0.
T=XX	all	delay XX*10 ms. after a read/write where XX = <hex number>
C	all	test continously alternating between 'add-29' and a random number pattern
L	all	all error messages printed on printer

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

(5) Error messages

(a) Disk Read/Write Errors
These are of the form;

**PROM I/O ERROR -- STATUS = <status byte> AT h DRIVE i - PSN j

where h is not significant
i = drive number
j = physical sector number at which the error occurred

and the status byte can be interpreted as follows:

31 data C.R.C. error
32 disk is write protected
33 disk is not ready for some reason
34 deleted data address mark read
35 abnormal command termination
36 invalid sector address
37 seek error (track not found)
38 data mark read error
39 address mark read error

(b) Verify Errors

When a verify error is encountered the offending disk sector is re-read into the QDOS sector buffer and matched against system RAM to determine where the error came from. The program then reports the corresponding address in RAM, the data expected, the erroneous data, the physical sector number of the disk where the error occured, and the byte offset within the sector.

(6) Termination

Test is terminated by -
ESC key (sets system error status word)
More then 20 errors logged
User supplied iteration counter expired (default 1)

System error status word will be set if any error condition has been reported.

5.2 Test Program DSKTST

DSKTST comprises of five main test routines and a number of utility commands. The main routines are as follows -

#1 Write/read test	(destructive)
#2 Read C.R.C. test	(non-destructive)
#3 Worst case seek test	(non-destructive)
#4 Worst case data pattern R/W	(destructive)
#5 Sector/drive uniqueness	(destructive)

NOTE: DESTRUCTIVE TESTS WILL OVERWRITE THE DISKETTE IN THE DRIVE UNDER TEST WITH A 'TESTING PATTERN'.

Tests can be run separately or in destructive/non-destruct groups by typing as follows -

DN,(0 or 1 or B) [,X]<return> (Do all non-destruct tests)

DD,(0 or 1 or B) [,X]<return> (Do all destructive tests)

ST#<tests>,(0 or 1 or B)[,X]<return>
where <tests> = up to 10 test numbers separated by '-'

The extended test option X accumulates error counts over a number of passes.

ESC key will abort test in progress.

Typing OS<return> will return the user to QDOS and reboot the system.

Examples: DN,0<return> does all non-destructive tests on drive 0 only.

ST#1-3-5,B,X does tests 1,3 and 5 on both drives with error count accumulation.

If stop on error option is selected (in answer to a prompt) the user may choose -

C continue
L loop
R reset stop on error

if an error stop occurs.

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

5.2.1 Error reporting

Error printouts take the following form :

<drive no.> <error type> <track no> /<physical sector no> <*>

Presence of '*' indictes a "hard" disk error,

e.g. 1 E3 1F /0325 *

means :- drive no 1
error type 3 (E3)
track no 1F
p.s.n 0325
error was not recoverable on retry (*)

If after three retries the error persists, it will be logged as a hard error (indicated by *).

Error types are as follows (per QDOS ROM codes) :-

E1 data CRC error
E2 disk is write protected
E3 disk is not ready for some reason
E4 deleted data address mark read
E5 abnormal command termination
E6 invalid sector address
E7 seek error (track not found)
E8 data mark read error
E9 address mark read error

Additional error types are :-

E@ data read back is not the same as data written

Additional error types from the drive uniqueness test are :-

EA body of data buffer is not zero after test data
EB unique data for this drive/sector is incorrect.

5. FLOPPY DISK SYSTEM DIAGNOSIS (continued)

5.2.2 Error Graphs

Errors may be summarised by use of the 'PG' command. This summary plots the track no. as the vertical ordinate and the number of errors as the horizontal ordinate.

A horizontal line may contain up to 11 error types (codes) with each character representing (n*horizontal scale) errors.

The error graph is divided into two blocks. The left hand block relates to drive 0 errors, the right hand block to drive 1.

The graph is printed starting at the first track with errors logged and finishes with the last track with errors logged.

To stop the display rolling off the screen, <control W> can be used to stop printing. Subsequent carriage returns will print a little at a time, an escape will terminate the 'PG', and any other character will resume continuous printing.

In the case of double sided systems, each disk 'cylinder' is considered as two tracks, so even track numbers correspond to side 0 of the disk and odd track numbers correspond to side 1.

5.2.3 Utility Commands

Commands for utility programmes are as follows

HD,d,hhhh	Head load timing test on drive d at speed hhhh (100 mS = D8F0)
IX,d	Index sensor alignment test on drive d. t1=tk 1. t2=tk 76.
AT,d,s	Read data amplitude test on drive d. s is optional side select (0 or 1). t1=tk 0. t2=tk 76.
RA,d,s	Radial alignment test on drive d. s is optional side select (0 or 1) t1=0-38. t2=77-38. t3=39-38. t4=37-38.
AZ,d,s	Head azimuth test on drive d. s is optional side select. t1=0-76. t2=75-76.
TO,d	Track zero sensor alignment test on drive d. t1=1-2 lp. t2=0-1 lp. t3=0-2 lp.
SK,d,s	Head skew test on drive d. s is optional side select (0 or 1). t1=1-76 lp.
RS,d,hhhh	Read sector hhhh from drive d to buffer
WS,d,hhhh	Write buffer to sector hhhh on drive d
DB	Display buffer in hex and ascii
FB,hhhh	Fill buffer with repeating pattern hhhh

The running test may be aborted by escape key.
The next test of the sequence is entered by depressing space key.
Tests followed by letters "lp" move head between tracks shown.

Some tests require the appropriate alignment diskette and ask that it be inserted. Other tests require a scratch diskette and ask that it be inserted.

Typing OS<return> will return the user to the operating system (reboot).

CMI MUSIC KEYBOARDS, #MC004 & #MC005

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1. INTRODUCTION

The CMI has provision for one Master keyboard and an optional Slave keyboard which operates in parallel with the Master. The CMI mainframe has only one keyboard input port, to which is connected the Master keyboard. The Slave keyboard, Alpha-numeric keyboard, and other attachments such as pedal controls, all connect to the Master keyboard. The latter contains an intelligent communications interface which monitors all attached devices and routes information from them through the single channel to the CMI.

In addition to the piano type music keyboard, the Master keyboard provides three slider pot analog controls and two switch controls (one momentary on, the other on/off) with lamp indicators whose purpose may be defined by the user by means of the CMI system software. A 12 character LED alpha-numeric display and 16 switch keypad constitutes a simple user interface to the mainframe so that during a live performance, operations such as loading voices may be performed directly from the Master keyboard.

The Slave keyboard serves only as an extra music keyboard and contains none of the extra facilities of the Master keyboard.

Related Documents: The following drawings are either referred to directly in this manual or will be of use in servicing the CMI music keyboards -

Exploded diagrams	DMC004 Master Keyboard
	DMC004B Master Keyboard with cover
	DMC015 Keyboard switches subassembly
	DMC005 Slave Keyboard
Drawing	DMC004C Bottom panel screw positions
Schematic Diagrams	MC004-01 Master keyboard wiring
	CMI10-00 Master controller to CMI10-02
	CMI11-01 Switch module
	CMI12-01 Display/keypad
	CMI14 Slave keyboard interface.

1. INTRODUCTION (continued)

1.1 OPERATING PRINCIPLES

Control over all keyboard functions is centralised upon the CMI-10 Keyboard Controller which is located within the Master Keyboard. Keyboard scanning, of both master and slave keyboards, is accomplished by analog multiplexing of the voltages on all key switches. The key switch mechanism consists of two brass buss bars running the full length of the keyboard which are supplied with +5 and -5 volts, and a delicate spring contact on each key which is allowed to move between the two buss bars as the key is pressed. By measuring the time it takes the spring contact voltage to change from -5V to +5V, the velocity with which a key is pressed may be calculated.

The analog multiplexing is performed by the CMI-11 switch modules, each of which has provision for 24 or 25 spring contacts. Each module provides one analog output which is the state of the contact currently addressed by the select lines from the controller, and each keyboard contains three modules. Six analog comparators (three for the master and three for the slave) on the master controller receive these analog signals and determine the state of the currently addressed key.

The user keypad and off/on switches are scanned in the same way although the multiplexed states are read directly as a digital signal.

The wipers of the three slider controls on the master keyboard and three plug-in pedal pots are similarly multiplexed and fed to a single analog to digital converter on the master keyboard controller. A change detected in any analog level read by this converter is reported to the CMI provided that change is greater than a certain tolerance set by a 6-pole DIL switch.

All information reflecting the state of the master and slave keyboards, and attached pedal controls plus characters received from the alpha-numeric keyboard are sent to the CMI through a single serial communications channel. User information received from the CMI through the same link is displayed on the LED display. The display modules accept ASCII characters directly from the keyboard controller.

2. KEYBOARD DIS ASSEMBLY AND REASSEMBLY

2.1 MASTER KEYBOARD DISASSEMBLY

2.1.1 Removal of Wooden cover.
(Refer to drawings DMC-004C and DMC-004B)

(1) Switch off CMI power and remove all cable connections to the keyboard.

(2) Place keyboard upside-down on a soft surface.

(3) Remove the six screws marked "A" and the five screws marked "B" on the drawing DMC-004C from the bottom panel of the keyboard. Do not remove any screws other than these from the bottom panel at this stage.

(4) Return the keyboard right way up and remove the five back panel screws attaching the wooden cover to the panel, marked "C" on DMC-004C.

(5) Lift the cover from the rear about 5 cm. then slide the cover forward while continuing to raise the rear as illustrated in Fig 2.1.

With the cover off, the CMI-10 Keyboard Controller circuit module may now be observed, along with the wiring from the rear panel connections to the module. To remove the module, follow steps 6-9.

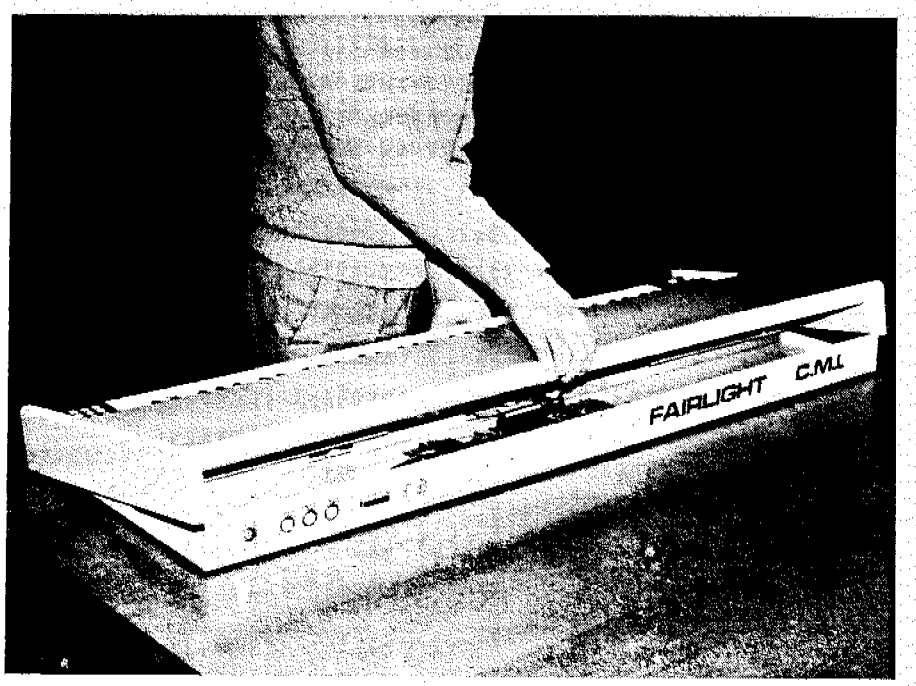


FIGURE 2.1

2. KEYBOARD DIS ASSEMBLY AND REASSEMBLY (continued)

2.1.2 Removal of CMI-10 Keyboard Controller
(Refer to drawing DMC-004)

(6) Remove all cable connections to the CMI-10 module.

(7) Unscrew three nuts and bolts attaching the CMI-10's heatsink to the back panel.

(8) Six plastic standoffs secure the module to the base of the keyboard. With a small screwdriver, press the catch of each standoff while gently prising the module up.

(9) Lift the module off the standoffs.

2.1.3 Access to Keyboard Switch Mechanism
(Refer to drawings DMC-004C and DMC-015)

(10) Slide the keyboard forward so the five screws marked "D" in drawing DMC004C may be accessed from underneath. Remove these screws to release the retaining strip which secures the keyboard assembly to the bottom panel.

(11) The entire key assembly may now be swung up on its own hinges by lifting from underneath the keys. Support the assembly from behind on a piece of soft foam to avoid scratching the keys.

At this point the three CMI-11 switch modules may be viewed with the spring switch contacts gently stretched across the brass -5V buss bar and engaged in the plastic "keyhole grips" extending from underneath each key. Each grip has two keyholes: the spring contact should always be engaged with the lower one (closest to the underside of the key).

2.1.4 Removal of CMI-11 switch modules
(Refer to drawing DMC-015)

The following steps should be followed for each module to be removed:

(12) Remove the 10-way cable plug from its socket.
CAUTION: This cable should never be plugged or unplugged with the keyboard power applied or damage will result to the switch module circuitry.

(13) Using tweezers or fine pliers, gently grip each spring switch contact and stretch it just enough to release it from its keyhole catch. Tuck it down underneath the lower brass buss supply bar (-5V).

(14) Use a 6BA nut driver to remove the 9 nuts and star washers securing the switch module to the underside of the key assembly.

(15) Unscrew the 3 screws which pass through the buss bar support blocks to the underside of the key assembly.

(16) Lift the module off its supports.

2.1.5 Removal of Control Panel and Display/Keypad
(Refer to drawing DMC-004)

(17) Slide the keyboard forward again as in step 10, and remove the four screws numbered 31 and 32 on the left in drawing DMC004 for the control panel, and/or the corresponding screws on the right for the display/keypad.

(18) Lower the keyboard and remove the 20-way flat cable from the display/keypad or release from its cable clips the 10-way ribbon cable leading from the CMI-10 module to the control panel. This cable is attached to the control panel.

(19) Lift the desired assembly out.

2.2 MASTER KEYBOARD REASSEMBLY

Reassembly of the Master keyboard is essentially a matter of reversing the procedures of Section 2.1. Care should be exercised while replacing the CMI-11 switch modules not to damage the delicate spring switch contacts. Tighten the nine nuts and three buss bar support screws evenly to ensure the module is not warped or distorted in any way and that the buss bars are not bent.

2.3 SLAVE KEYBOARD DISASSEMBLY AND REASSEMBLY

To remove the wooden cover and the CMI-11 switch modules from a slave keyboard, follow the same procedures as specified for the master keyboard in sections 2.1.1 and 2.1.3 respectively.

2.3.1 Removal of CMI-14 Slave Interface
(Refer to drawing DMC-005)

(1) With CMI power off, remove the flat cable connecting the master and slave keyboards, if not already done.
CAUTION: Always turn off CMI power to the master keyboard before connecting or disconnecting the external cable between the master and slave. Omission to do this will cause damage to the switch modules in the slave keyboard.

(2) The CMI-14 module is item 7 on DMC-005. Release the 25-way flat cable leading to the CMI-11 switch modules (item 8).

The same caution applies to this cable as to the external cable.

(3) Remove the three screws marked 13 which secure the module to the back panel of the slave keyboard.

Reassembly of the slave keyboard is the reverse of the disassembly procedures.

3. TROUBLE SHOOTING

3.1 FAILURE OF MASTER KEYBOARD TO POWER-UP

Successful power-on sequence of the Keyboard Controller is indicated by the control panel switch lights flashing on for approximately 1 second, off for another second, then on again. A "- POWER ON -" message is then written to the LED display. If this does not occur and the CMI does not respond when the keyboard is played or the keypad operated, follow the procedure below.

(1) Check that all power supplies (+10V, +20V and -20V) are present on the Music Keyboard cable from the CMI. Refer to drawing MC004-01. If not, check CMI fuses, the Cannon connector on the back panel of the keyboard, and the cable itself.

(2) Remove the cover of the keyboard according to section 2.1.1.

(3) Ensure all cables are firmly connected and that the correct power supplies are present on the six pin Utilux connector to the CMI-10 Keyboard Controller. If not, look for the faulty connection between the back panel sockets and the CMI-10, referring to drawing MC004-01.

(4) Check that both DIL switches on the CMI-10 are set correctly. SW3 (4-way) should have switches 2 and 3 only closed, SW4 (6-way) should have switches 3 and 4 only closed. Refer to sections 4.1.1 and 4.1.3.

(5) Verify the voltages on each power supply regulator output on the CMI-10. Refer to section 4.3.1.

(6) Check that the power-on restart circuitry holds the processor in reset for approximately 0.4 secs. Refer to section 4.1.1.

(7) Check that the processor crystal is operating and that the processor ø2 output signal is present.

(8) Check that the processor is not receiving spurious interrupts due to a faulty SW3. Refer section 4.1.1

(9) Establish whether the controller is running its program by examining the VMA, data and address lines, and checking peripherals which are accessed in the processor idle loop (refer to section 4.4). If it is, then the controller is powering up but a major I/O problem is preventing all normal indications of this. Otherwise, a fault in the processor itself, the address decoding system, the ROMs or RAM is causing the controller to crash. In both cases, carefully check each of the functions described in section 4 to isolate the fault.

3. TROUBLE SHOOTING (continued)

3.2 INDIVIDUAL KEY FAILURE (Master and Slave)

The failure of a single key to operate will usually be caused by a mechanical problem in the spring switch contact mechanism. Remove the cover of the keyboard according to section 2.1.1 and hinge the key assembly up as described in section 2.1.3.

Common causes of failure are damaged, loose or dirty spring contacts, or inadequate contact between the spring and the brass buss bars.

3.3 FAILURE OF GROUPS OF KEYS (Master and Slave)

If all the 24 or 25 keys scanned by a particular switch module fail to operate then the fault lies either in that module (check the voltages on both buss bars) or in the path from it to the analog key data multiplexor in the Keyboard Controller (incuding the cable). The source of such a fault may be isolated by swapping around the flat cable connectors to the switch modules.

Failure of certain keys belonging to each module is most likely to be caused by incorrect scanning addresses arriving at the switch module: either a cable fault or an I/O problem on the keyboard controller. In this case it is unlikely that the keypad or display will work either.

If no such module-related pattern to the faulty keys exists, then the problem is mechanical. Check that all spring contacts bend across the -5V buss bar by approximately 20 degrees from the horizontal when the keys are released and across the +5V bar by the same angle (in the opposite direction) when the keys are depressed. A tension spring in the back of each key returns it to the original position when it is released.

3.4 SLAVE KEYBOARD MALFUNCTIONS

Failure of groups of keys or individual keys on the slave keyboard can be diagnosed following the same guidelines as for the master keyboard. However two additional possible sources of faults exist: the cable from the master keyboard to the slave, and the CMI-14 slave interface. Since the slave scan address lines are the same as the master scan address lines, faults in the slave keyboard which corrupt those lines can cause the master to malfunction. Section 7.1.1 describes the use of the 4-pole DIL switch on the CMI-14 to disable individual switch module outputs when isolating slave keyboard faults. Ensure that all switches are open to enable the full keyboard velocity sensing prior to reassembling the slave.

CAUTION: Always turn off CMI power to the master keyboard before connecting or disconnecting the external cable between the master and slave. Omission to do this will cause damage to the switch modules in the slave keyboard.

4. MASTER KEYBOARD CONTROLLER, CMI-10

The function of the CMI-10 Master Keyboard Controller card is to execute all keyboard facilities of the CMI and communicate the status of those facilities through a single serial link to the central processor. The facilities are -

Master keyboard scanning (with CMI-11 multiplexor).
Slave keyboard scanning (with CMI-14 slave interface and CMI-11 multiplexor).
Data link to CMI for the alpha-numeric keyboard.
Master keyboard keypad.
Keypad display of information from CMI.
Three slider pots.
Two on/off switches.
Three pedal controls with switches.

This section describes the operation of the CMI-10 board.

4.1 MPU,DECODING,RAM AND RESTART.
(Refer to drawing CMI10-00)

4.1.1 Microprocessor Unit

The central driver of the Keyboard Controller is the 6802 microprocessor unit (MPU) at location E567 which is activated by a 4MHz crystal. At power-up the MPU reset line is held low for approximately 0.4 seconds at which time it is released to begin execution. It is important that this restart time is less than the CMI's Central Processor restart interval to ensure that no characters sent to the Keyboard Controller are lost. The MPU may also reset manually by depressing SW1 (nearer the heatsink). This switch is debounced through the pair of open-collector NAND gates D12.

While the restart line is held low, the MPU places FFFE (hex) on the address buss and its first operation is to fetch the restart vector from locations FFFE/F. Execution is then transferred to the initialization routines in ROM. Successful completion of this power up phase is indicated by the keyboard switch lamps switching on for about one second, off for another second, then on again. A " - POWER ON - " message is then written to the keypad display.

A 4-pole dual-in-line (DIL) switch, SW3, is used to select the source of Non-Maskable Interrupts to the MPU. This may be either from the manual switch SW2 or a clocked timing signal. The DIL switch functions as follows:

Switch	Effect if closed
1	Select BRCK signal from Baud rate gen. as timing reference.
2	Select ø2 from MPU as timing reference.
3	Select SW2 as NMI
4	Select timing rerence as NMI

Clearly, switches 1 and 2 are mutually exclusive and must not be closed simulataneously, as are switches 3 and 4. Before feeding to switch 4, the high frequency reference selected by switches 1 or 2 is divided by 512, 1024, 2048 or 4096 by the binary counter C5. This division ratio is determined by the p.c.b. link next to C5 (normally 2048). The divided reference (signal SCND) is used as a control line signal to the PIAs, in addition to optioning as an NMI source.

With "KBDIOA" and "VELKEYD" ROMs, switches 2 and 3 only should be closed. This selects SW2 as NMI source, and has the same effect as restart SW1 except that NMI vector FFFC/D is used. Switch 1 of the DIL switch is nearest the edge of the p.c.b. with the heatsink.

The 6802 MPU contains 128 bytes of internal RAM. This is permanently enabled by tying the Ram Enable signal (pin 36) high.

4.1.2 Address Decoding

Selection of all ROMS, external RAM and peripheral devices is performed by four LS139 1-of-4 decoders in ICs E12 and E34. Addresses are decoded when both the ø2 and VMA (Valid Memory Address) signals from the MPU are high.

The address map of the Keyboard Controller is as follows:

Address (Hex)	Function
0 - 7F	Internal RAM. 23 bytes only used, for software variable storage.
80 - 83	Active key input/AD conv. input PIA (K34)
90 - 93	Key address output PIA (F34)
A0 - A1	Alpha-numeric keyboard comms. ACIA (C67)
B0 - B1	CMI communications ACIA (D67)
C0	Software readable switch
4000 - 43FF	External RAM #1 (L67, N67)
5000 - 53FF	External RAM #2 (K67, M67, not normally installed)
9000 - 9400	ROM #1 (J67, not normally installed)
A000 - A400	ROM #2 (HI67, not normally installed)
B000 - B400	ROM #3 (G67, "VELKEYD")
FC00 - FFFF	ROM #4 (F67, "KBDIOA")

4.1.3 Software Readable Switch

The six-pole dual-in-line (DIL) switch SW4 provides adjustment to the sensitivity of the analog controls. It is read whenever an A/D conversion detects a changed analog level. Bits 4 and 5 (switches 1 and 2, nearest the heatsink) are ignored and the 4-bit number remaining gives the minimum change in the converted level required before the change will be reported to the CMI.

The switch is read through buffer N8 whose inputs are pulled high, unless grounded by a closed switch. Thus a binary '1' corresponds to an open switch.

Normally, sensitivity is set to 3 digital levels so switches 3 and 4 only are closed.

4.1.4 External RAM

Provision is made on the CMI-10 p.c.b. for 2K of static RAM but normally only 1K is installed: 2114s L67 and N67. Each chip contains 1K x 4 bits storage. The upper nybble is stored in L67, and the lower nybble in N67.

4.2 ROMs and PERIPHERALS
(Refer to Drawing CMI10-01)

4.2.1 ROMs

Provision is made on the CMI-10 printed circuit board for four 2708 ROMs. Normally only two of these are installed: "KBDIOA" at location F67, and "VELKEYD" at G67. The first ROM contains the initialization and I/O firmware for the Keyboard Controller and the second contains firmware responsible for scanning the velocity sensitive keyboard and analog and switch controls.

4.2.2 Serial Communications ACIAs

Serial communication with the Alpha-numeric keyboard is accomplished through the 6850 Asynchronous Communications Interface Adaptor (ACIA) at C67, while communication with the CMI utilises the 6850 ACIA at D67. The Baud rate for both ACIAs is derived from the Baud rate generator at B12 driven by a 1.8432 MHz crystal and a p.c.b. link at C12 normally selects 9600 Baud operation (pin 1 of B12). The Baud rate generator also provides the BRCK signal, normally linked to 1200 Baud at B45.

Both ACIAs are normally linked via LK1 and LK2 to the common interrupt request (IRQ) buss signal. D67 generates IRQs when transmitting to and receiving from the CMI, while C67 generates IRQs when receiving from the Alpha-numeric keyboard.

4.2.3 Peripheral Interface Adapters (PIAs)

Two PIAs are used, each containing two 8-bit parallel I/O ports and four control outputs/IRQ input lines. The PIAs are configured during initialization and used as follows:

PIA F34

I/O port A PA0 - PA1	Peripheral address outputs. Buffered through G23 to address to provide: CMI-11 switch module addresses CMI-12 keypad mutiplexor addresses LED display module data Data inputs to flip-flops (G4) which switch control button lamps. Analog control input multiplexor addresses.
CA1	Scan Not Done (SCND) timing flag input
CA2	Strobe output to update lamp flip-flops
I/O port B PB0 - PB1 PB2 - PB7	LED display digit select lines LED display all-segments-on (CU) and module select (CS) signals.
CB1	Input flag from keypad multiplexor. Does not generate IRQs.
CB2	Strobe output to update a LED display (DWS)

PIA K34

I/O port A PA0 - PA5	Inputs from music key threshold comparators
PA6	Input from control switch multiplexor enabled by BKA7
PA7	Input from keypad multiplexor, also enabled by BKA7
CA1	Inverted timing reference input. Does not generate IRQs.
CA2	Threshold select output
I/O port B PB0 - PB7	Data inputs from A/D converter (ADC)
CB1	$\overline{DR}$ (Data Ready) flag from ADC
CB2	B/C (Begin Conversion) strobe to ADC

4.3 POWER SUPPLIES AND ANALOG INTERFACE SECTION
(Refer to drawing CMI-10-02)

4.3.1 Power Supplies

The Keyboard Controller receives +20V, -20V and +10V from the CMI through a 6-pin Utilux connector. Six on-board regulators are used to generate three independant +5V supplies, in addition to +12V, -12V and -5V supplies. These power the Controller itself plus the keypad display, slider and pedal pots and switches.

The supply designated "+5V" powers all circuitry on drawings CMI-10-00 and CMI10-10-01 except the ROMs, which are powered separately from "+RV". The analog multiplexors, A/D converter and RS-232 drivers on CMI-10-02 receive power from "+XV" and where necessary, the -5V supply.

"+XV" also leaves the Controller board to power the CMI-11 keyboard switch multiplexors, and the keypad display.

4.3.2 Threshold Detection

MD1-3 and SD1-3 are the multiplexed signals representing the position of music keys addressed by the three master keyboard CMI-11 modules and the slave keyboard interface CMI-14, respectively. These signals are compared by the six MLM311s to a known threshold to determine when a key begins to be pressed, and when it is fully depressed.

The THLD signal from PIA K34 sets up one of two thresholds through the 741SC level shifter. If THLD is low, a -2.7V threshold is applied to the comparators. With THLD high, the threshold is +2.3V.

Initially, THLD is low. An unpressed key rests against the -5V buss bar so the corresponding comparator output will be high. When the key is first depressed and the spring contact leaves the -5V buss bar, the output of the module when that key is selected is pulled to just below zero volts by a 10k resistor to ground on the switch module and a 100k resistor to -5V on each comparator input. This causes the comparator to change state to a low. The change is read from the PIA whereupon THLD is switched high to select the +2.3V threshold, setting the comparator high again. It will return low when the key reaches the +5V buss bar at its full depression. The time taken between the two falling edges of the comparator output is noted by the MPU, and this mechanism forms the basis of the velocity sensitive keyboard.

The key continues to be compared to the +2.3V threshold until its release is detected.

4.3.3 Control Signal Multiplexors and A/D Convertor

User control signals enter the Keyboard Controller from several possible sources: two control panel switches, three pedal switches, three control panel slider pots and three pedal pots. The switch controls are analog multiplexed by H3 and read directly as KD6 when gated by a high level on BKA7.

The analog controls (slider and pedal pots) are multiplexed by I3, buffered by 741SC I4, and fed to the AD570 A/D converter at J4. The low frequency signals used do not require a sample and hold. The converter is strobed to begin a conversion by the B/$\overline{C}$ signal from the CB2 output of PIA K34 and flags the end of conversion to CB1 of the same PIA.

The sensitivity of the analog controls may be set by DIL switch SW4. Refer to section 4.1.3 for further details.

4.3.4 RS-232 Interface

ICs A5 and A6 are the RS-232 drivers for the two ACIAs described in section 4.2.2.

4.3.5 Lamp driver

The control panel lamps are supplied with 20V and switched on when the MC75452 driver at J2 pulls the appropriate line to ground. The driver is activated by signals LP1 and LP2 latched from PIA F34.

4.3.6 Connections

The Keyboard Controller requires four external connections as follows:

SO1 50-Way flat cable connector.

Pins 1-5	Master switch module 1 scan address
6	N/C
7	-5V to Master switch module 1
8	"+XV" 5V to module 1
9	Ground to module 1
10	MD1 module 1 multiplexed output
11-20	Master switch module 2 connections as for 1
21-30	Master switch module 3 connections as for 1
31-37	Scan address to keypad and data lines to LED display
38	All segments on, display module 0 (CU)
39	Module select, module 0 (CS)
40-41	CU and CS lines, display module 1
42-43	CU and CS lines, display module 2
44-45	LED display digit select
46	Digit write strobe
47	Keypad multiplexed output
48	$\overline{BKA3}$, selects keypad multiplexor 2
49	Ground to display/keypad
50	"+XV" +5V to display/keypad

SO2 10-Way rainbow cable connector

Pins	1-2	Button lamps switched returns
	3	Switch 2 (momentary on)
	4	Switch 1 (push on/push off)
	5	Slider pot 3 wiper
	6	+20V to lamps
	7	-5V to pots
	8	"+XV" +5V to pots
	9	Slider pot 2 wiper
	10	Slider pot 1 wiper

SO3 26-Way rainbow cable connector

Pins	1	Pedal 1 pot wiper
	2	Pedal 1 switch
	3	Pedal 2 pot wiper
	4	Pedal 2 switch
	5	Pedal 3 pot wiper
	6	Pedal 3 switch
	7-11	Slave keyboard scan address
	12	Slave keyboard ground
	13-15	Slave switch module outputs
	16	RTS flag to alpha-numeric keyboard
	17	CTS flag to A/N keyboard
	18	A/N keyboard ground
	19	Data to A/N keyboard
	20	Data from A/N keyboard
	21	Ground
	22	CTS flag from CMI
	23	RTS flag to CMI
	24	Ground
	25	Data from CMI
	26	Data to CMI

SO4 6-Way Utilux Connector

Pin	1	+10V return
	2	+10V
	3	+20V
	4	-20V
	5	Ground
	6	+/-20V return

4.4 SOFTWARE LOOP AND INTERRUPT ROUTINE

A useful clue when fault finding ROM-based equipment such as the CMI-10 is the main software loop which the processor normally executes in the "steady state": that state which exists after a successful power-on initialisation, but before any special functions have been called upon by key presses, changed A/D values, etc.
This software loop may also be referred to as the "idle loop". Knowledge of what happens in the idle loop allows a service person to establish, for example what peripherials are not being regularly accessed as they should.

The program flow of the idle loop in "VELKEYD" is as follows:

```
begin loop

    for keyselect = 1 to 32

       read key-pressed pattern from comparators

       for module select = 1 to 6 (3 master, 3 slave)

           update statuses in RAM of keys pressed

       end for

    end for

    read one of the control functions and update status
    (slider pots, pedal pots and switches)

    scan entire keypad for a keystroke

    wait for rising edge of SCND flag

end loop
```

The key scan loop executes 32 times because there are 5 key select lines but there are only 24 or 25 keys on each module so some iterations of the inner loop do not correspond to any real key. A different control function is monitored and updated on each iteration of the main loop.

A knowledge of the sources of interrupts and the functions performed in the interrupt service routine(s) can be similarly useful when fault tracing. In the KBDIOA firmware, there are three possible sources of interrupts (IRQ's):

1. A character has been received from the CMI.
2. A character previously transmitted to the CMI has completed transmission from the ACIA.
3. A character has been received from the alpha-numeric keyboard.

Characters received from the CMI are written to the LED display immediately. A transmit-complete interrupt causes the processor to check the output character queue and send another character if it is not empty. A character received from the alpha-numeric keyboard is placed on the output character queue unless the received character is actually a BREAK level, in which case a BREAK level is transmitted to the CMI.

The short piece of code which places characters on the output queue (and enables the transmitter interrupt) is actually a software interrupt routine, called by the SWI instruction rather than a subroutine call.

5. KEYBOARD SWITCH MODULE CMI-11

Three Keyboard Switch Modules are installed in each master and slave keyboard used with a CMI. Each module provides a single signal out which represents the state (pressed, released, or in flight) of one of the 24 or 25 keys addressed by the multiplexor inputs. This section describes the operation of the CMI-11.

5.1 KEYBOARD SWITCH MODULE OPERATION
(Refer to drawing CMI-11-01)

Five key address bits are provided provided by the Keyboard Controller CMI-10 as inputs to the CMI-11. The lower three of these are bussed across three 4051 analog multiplexors (ICs 2-4) so that each 4051 selects one of eight spring key contacts as its analog input. Normally, a key rests against a -5V buss bar, but when fully depressed, it contacts a +5V buss bar. In between, it contacts neither.

The outputs of ICs 2-4 are fed to another multiplexor, IC1, whose select inputs are the upper two bits of the key address. Thus the output of IC1 may be any of the 24 key contacts accessed by ICs 2-4. It may alternatively be the 25th key contact which is fed directly to IC1 as a fourth analog input.

Each CMI keyboard has a total of 49 keys so the 25th key is only used on the extreme right hand switch module. Provision is made on the switch module p.c.b. for a 10k resistor (R1) pulling to ground. This is to ensure that if the 25th key is not installed, it appears to the multiplexor as a key which is never pressed. However, the resistor must be removed if the 25th key is installed or the velocity sensing mechanism will not work on that key.
The output of IC1 is fed directly to the Keyboard Controller in a master keyboard or to the Slave Interface in a slave keyboard. Its unused inputs are grounded.

5.2 EXTERNAL CONNECTIONS

SO1 10-Way flat cable

Pins	1-5	Key scan address inputs
	6	N/C
	7	-5V supply
	8	+5V supply
	9	Ground
	10	Multiplexed analog output

6. KEYBOARD DISPLAY AND KEYPAD MODULE, CMI-12

The Display and Keypad Module provides a simple user interface with the CMI from the master music keyboard. A 16-switch keypad is scanned by the Keyboard Controller for commands to be sent to the CMI and a 12 digit LED display receives simple messages from the CMI to the user. This section describes the operation of the CMI-12.

6.1 DISPLAY AND KEYPAD OPERTION
(Refer to drawing CMI-12-01)

6.1.1 LED Display

The DL-1416 LED display modules, containing four digits each, accept 7 bit ASCII codes from the data lines to display the desired character. The key scan addresses are used as data inputs. Data is latched into the modules whose chip select line ($\overline{CS}$) is low on the falling edge of $\overline{DWS}$. The DA lines select which digit within the selected module(s) is written to. The $\overline{CU}$ line is a test enable line which causes every segment in each digit to light up.

6.1.2 Keypad

The keypad is simply an array of 16 momentary switches which connect to the common (+5V) line when pressed. Two 4051 1-of-8 analog multiplexors scan the keypad. Their select and inhibit inputs are taken from the key scan address lines. Only enabling one multiplexor at a time allows the outputs to be wired together on the same KPAD signal.

6.2 EXTERNAL CONNECTIONS

SO1 20-Way Ribbon cable connector

Pins	1-2	Digit select
	3,5,7	Display module select
	4,6,8	Display module test (all segments on)
	10	Digit write strobe
	9,18, 11-16	Key scan address and data to display modules
	17	Keypad multiplexed output
	19	Ground
	20	"+XV" +5V supply

7. SLAVE KEYBOARD INTERFACE, CMI-14

The Slave Keyboard Interface provides regulated power supplies to the CMI-11 switch modules in a slave keyboard and buffers the analog outputs of the switch modules before feeding them to the master keyboard controller. This section describes the operation of the CMI-14.

7.1 OPERATION

(Refer to drawing CMI-14)

7.1.1 Scanning and Buffering

The five slave key scan address lines from the master keyboard controller are fed straight through to the CMI-11 switch modules. The output from each module is buffered by a 741SC in a non-inverting configuration and fed to the master controller. A 4-pole dual-in-line (DIL) switch allows the input of each buffer to be pulled to nearly -5V for testing purposes. In the event of a switch module being unplugged, closing the switch corresponding to that module simulates all keys released. Two or more floating buffer inputs result in the keyboard controller going into overflow due to sensing too many keys pressed. All switches should normally be open, otherwise the velocity sensing system will not work.

7.1.2 Power Supplies

The CMI-14 is supplied with +20V and -20V from the CMI via the master keyboard. A 4V7 zener is used on each supply side to provide +12V and -12V to the 741 buffers, and 7805 and 7905 regulators send +5V and -5V respectively to the switch multiplexors.

7.2 EXTERNAL CONNECTIONS

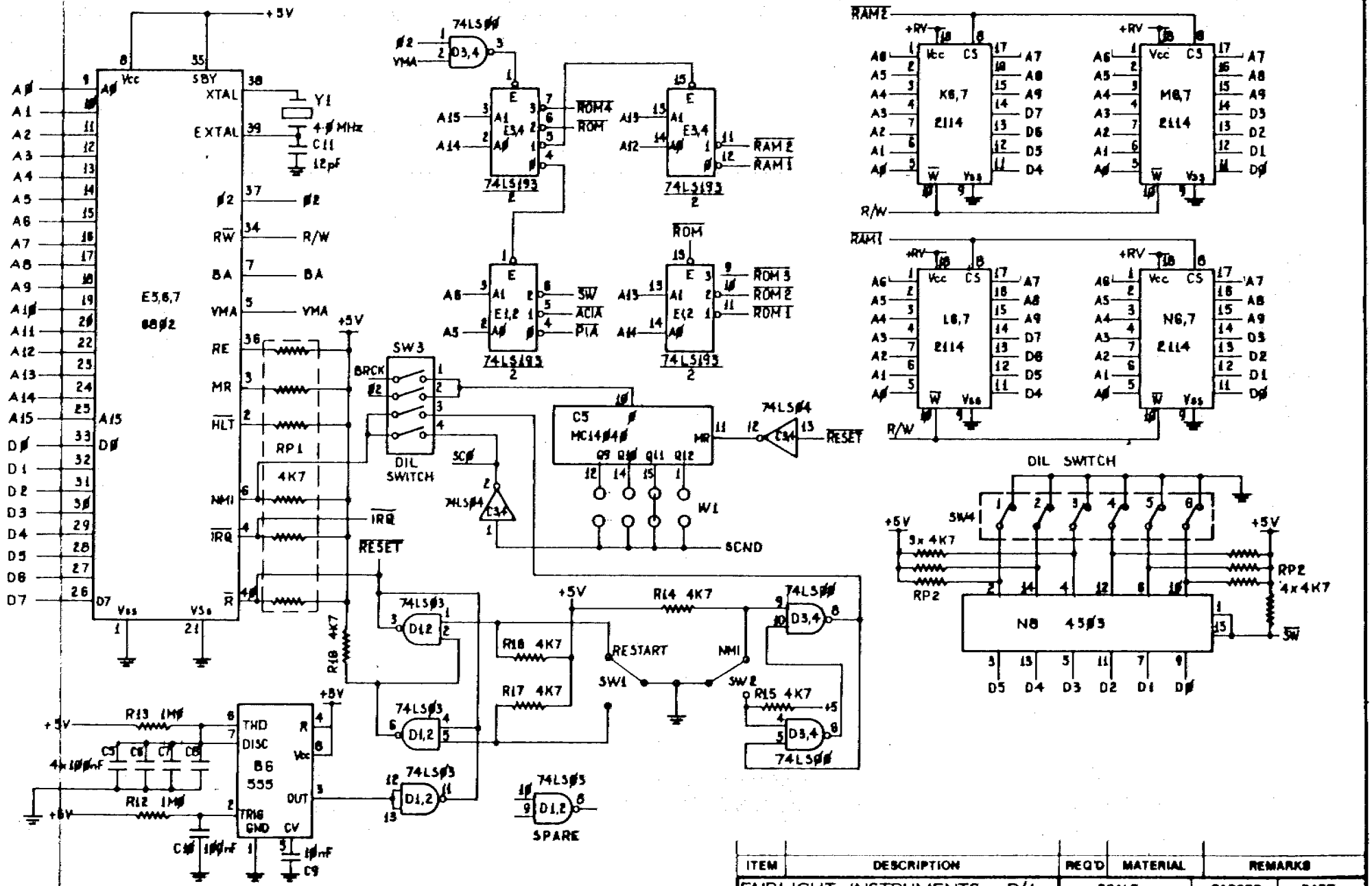
SO1 30-Way flat cable connector

Pins 1-5	Slave switch module 1 scan address
6	N/C
7	-5V to Slave switch module 1
8	"+XV" 5V to module 1
9	Ground to module 1
10	MD1 module 1 multiplexed output
11-20	Slave switch module 2 connections as for 1
21-30	Slave switch module 3 connections as for 1

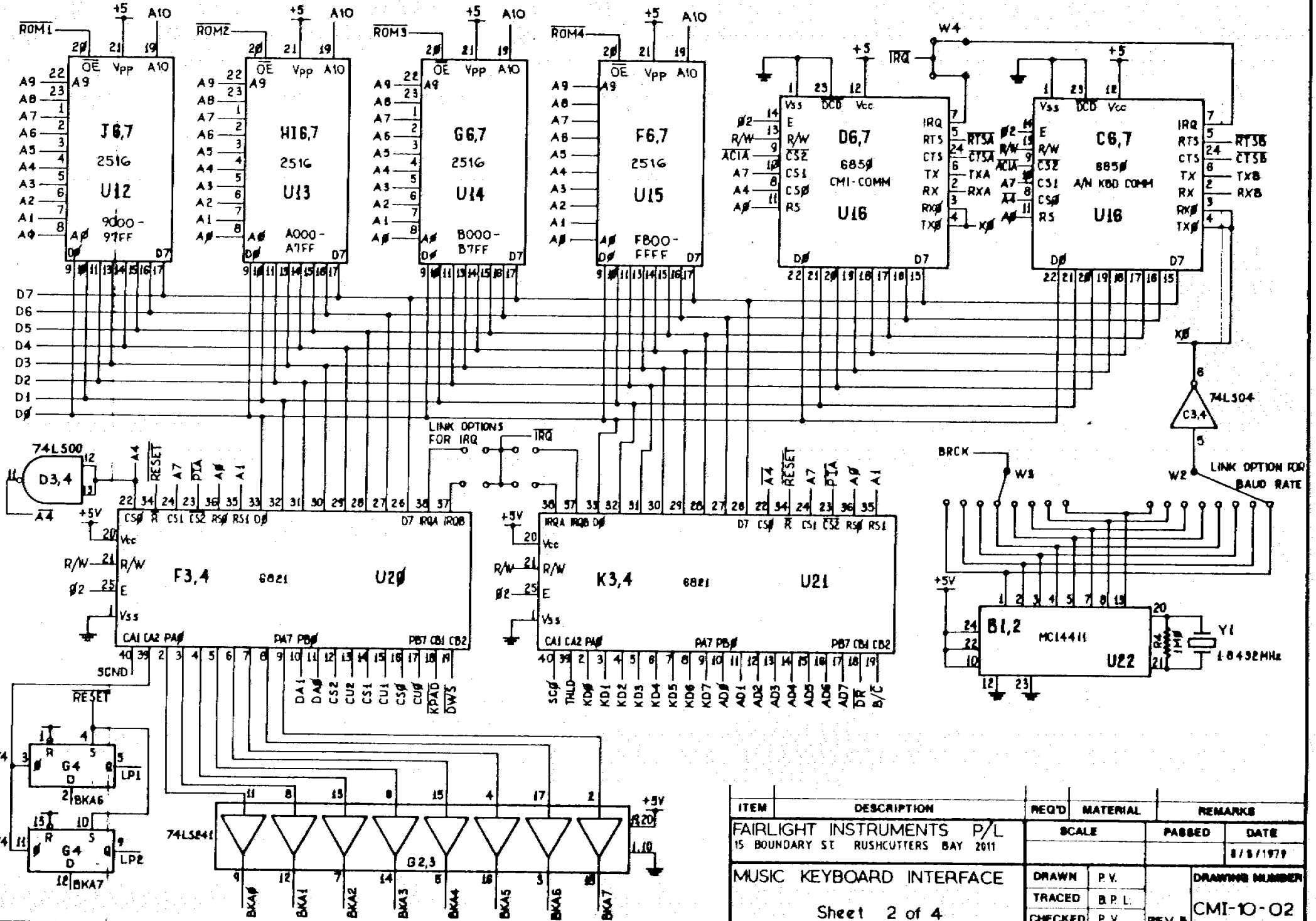
7. SLAVE KEYBOARD INTERFACE, CMI-14 (continued)

SO2 25-Way D series external connector

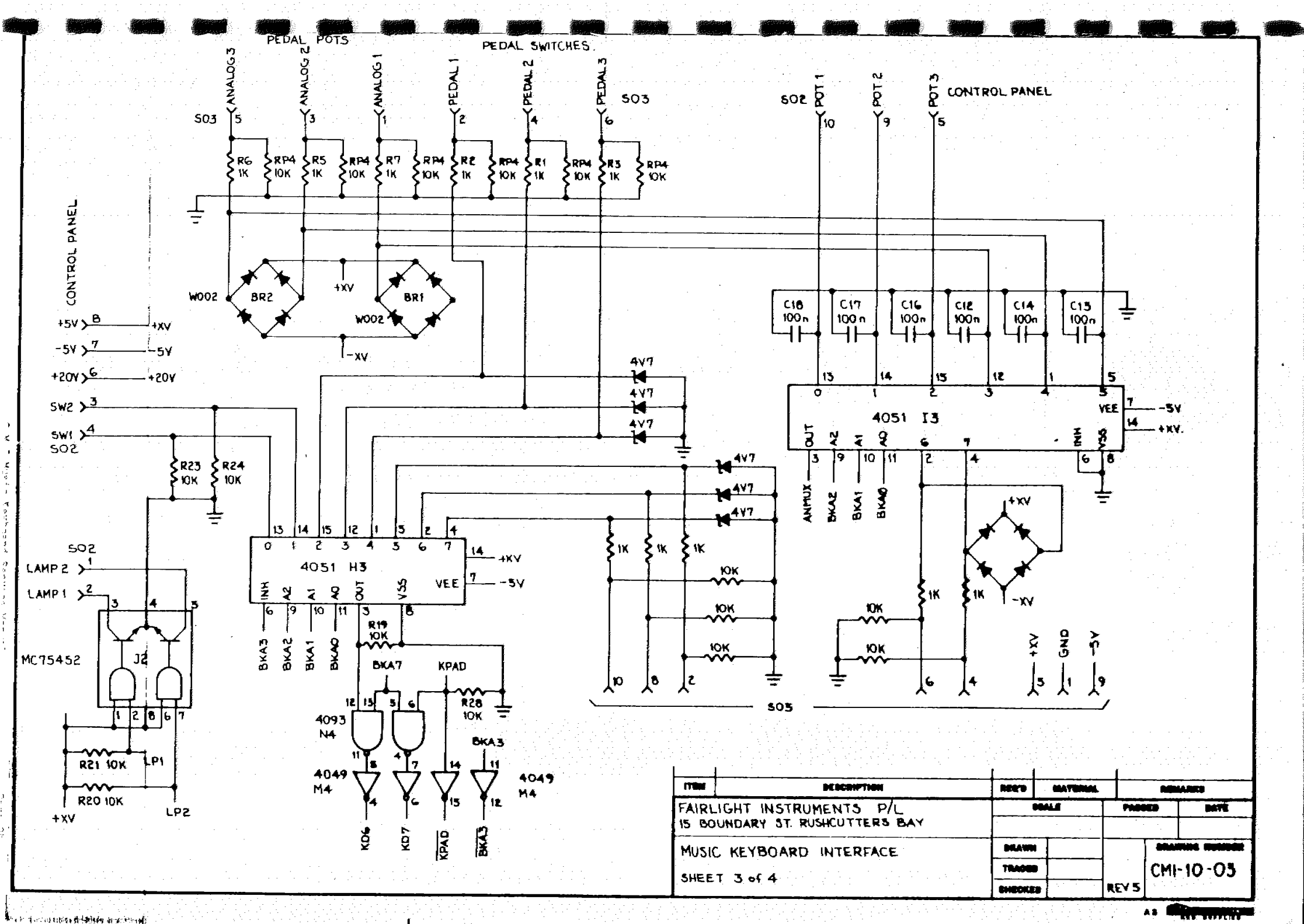
Pins	1-2	Ground
	3-7	Slave keyboard scan addresses
	8	Ground
	9-11	Slave multiplexor outputs
	12-21	N/C
	22-23	-20V supply
	24-25	+20V supply



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
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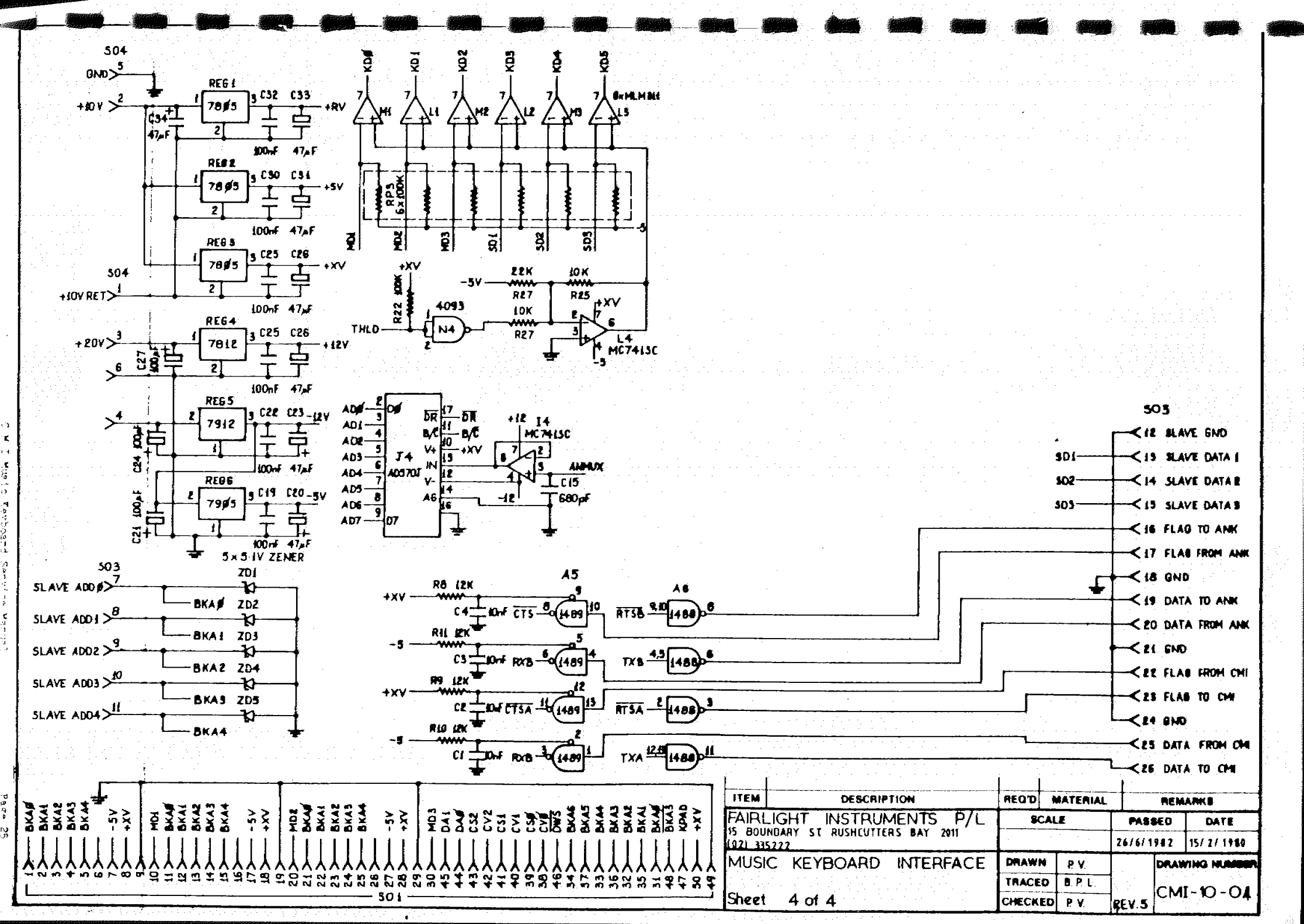


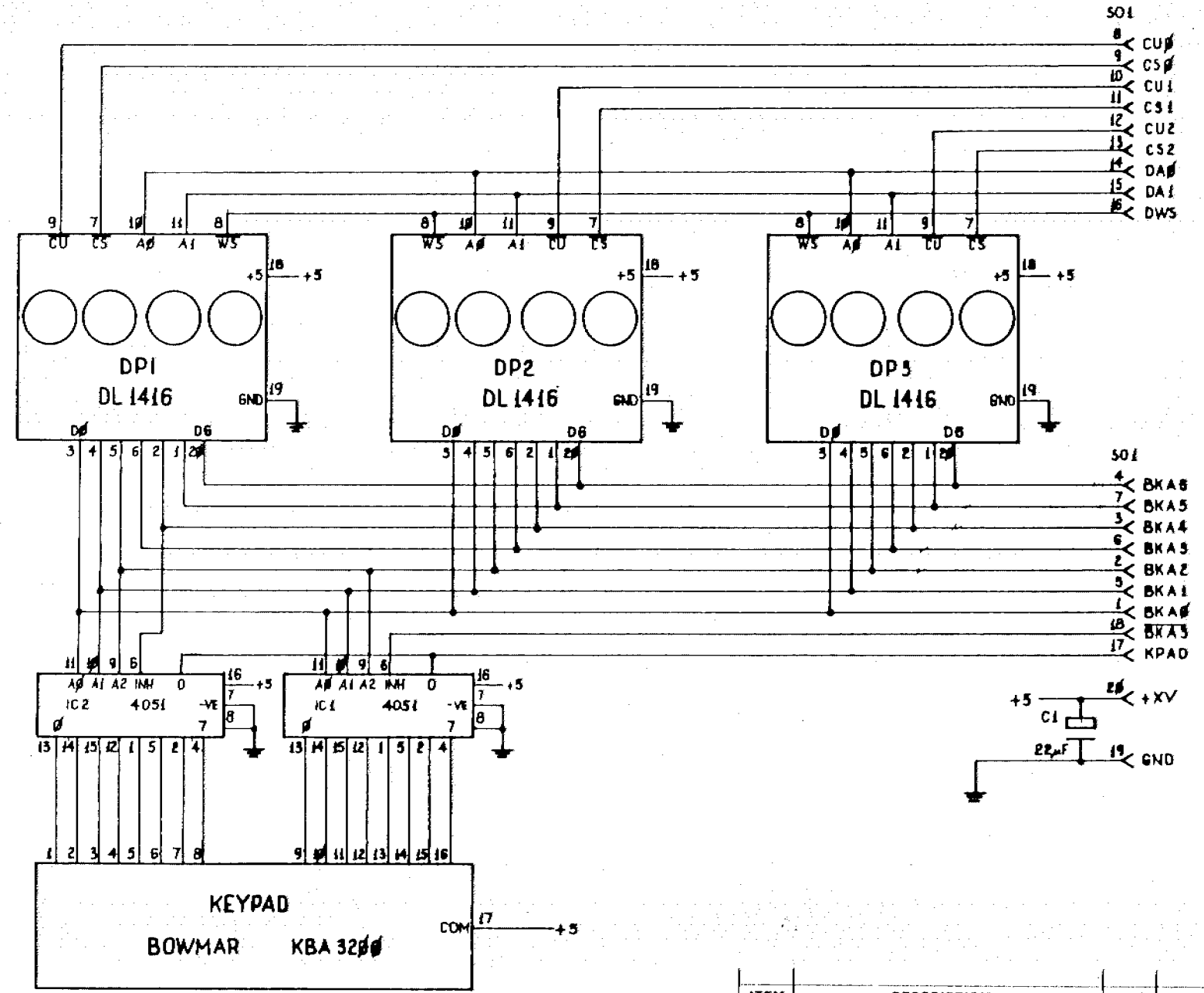
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MUSIC KEYBOARD INTERFACE Sheet 2 of 4		DRAWN P.V. TRACED B.P.L. CHECKED P.V.	REV. 5	DRAWING NUMBER CMI-10-02



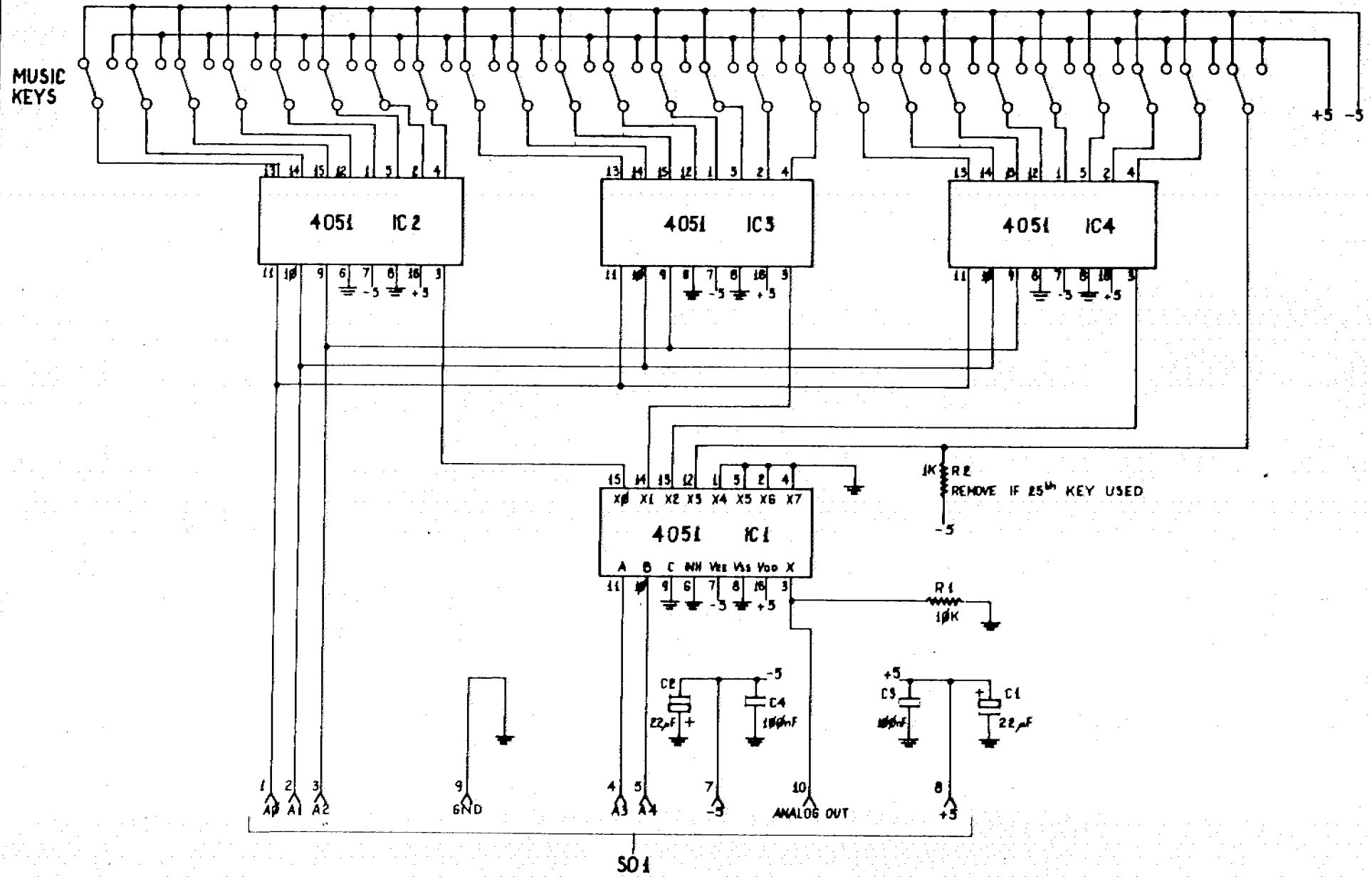
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MUSIC KEYBOARD INTERFACE		DRAWN		DRAWING NUMBER
SHEET 3 of 4		TRACED	REV 5	CMI-10-03
		CHECKED		

A3

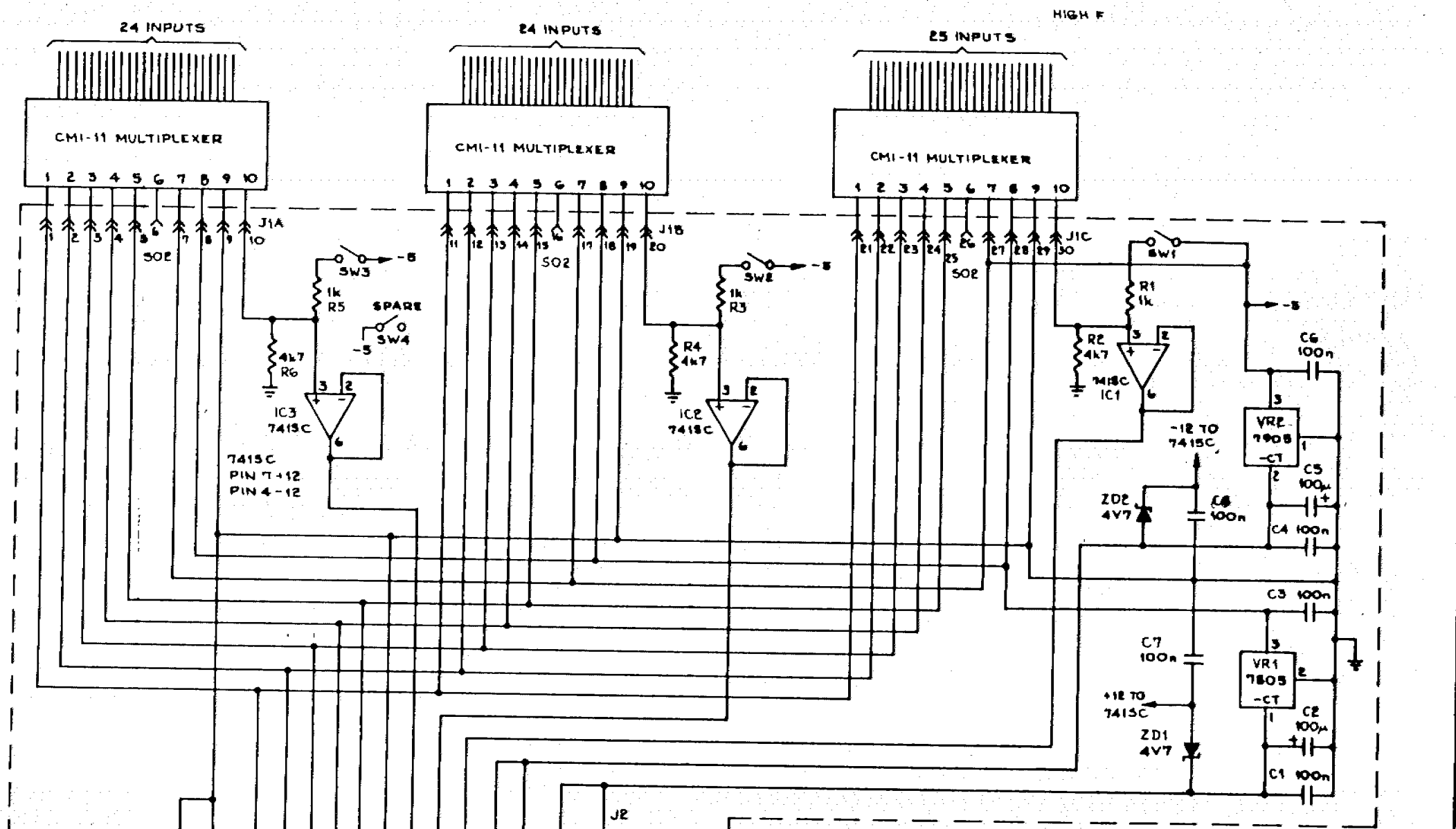

S04
GND
+10V
+10V RET
REG1
REG2
REG3
REG4
REG5
REG6
7805
7812
7912
7905
C32
C33
C34
C30
C31
C25
C26
C27
C22
C23
C24
C19
C20
C21
100nF
47µF
100µF
+RV
+5V
+XV
+12V
-12V
-5V
5x5.1V ZENER
KD0
KD1
KD2
KD3
KD4
KD5
RP5
6x100K
MD1
MD2
MD3
SD1
SD2
SD3
THLD
R22 100K
4093
N4
22K
10K
R27
R25
L4
MC7413C
J4
AD570J
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
DR
B/C
V+
IN
V-
A6
I4
ANMUX
C15
680pF
S03
SLAVE ADD0
SLAVE ADD1
SLAVE ADD2
SLAVE ADD3
SLAVE ADD4
ZD1
ZD2
ZD3
ZD4
ZD5
BKA0
BKA1
BKA2
BKA3
BKA4
A5
A6
R8 12K
R11 12K
R9 12K
R10 12K
C4
C3
C2
C1
10nF
CTS
RXB
CTSA
RXB
1489
1488
RTSB
TXB
RTSA
TXA
SLAVE GND
SLAVE DATA I
SLAVE DATA II
SLAVE DATA III
FLAG TO ANK
FLAG FROM ANK
GND
DATA TO ANK
DATA FROM ANK
GND
FLAG FROM CMI
FLAG TO CMI
GND
DATA FROM CMI
DATA TO CMI
S01
-5V
+XV
MD1
MD2
MD3
DA1
DA2
CS2
CV2
CS1
CV1
CS0
CV0
DWS
KPAD
ITEM
DESCRIPTION
REQ'D
MATERIAL
REMARKS
FAIRLIGHT INSTRUMENTS P/L
15 BOUNDARY ST RUSHCUTTERS BAY 2011
(02) 335222
SCALE
PASSED
DATE
26/6/1982
15/2/1980
MUSIC KEYBOARD INTERFACE
Sheet 4 of 4
DRAWN P.V.
TRACED B.P.L.
CHECKED P.V.
REV.5
DRAWING NUMBER
CMI-10-04



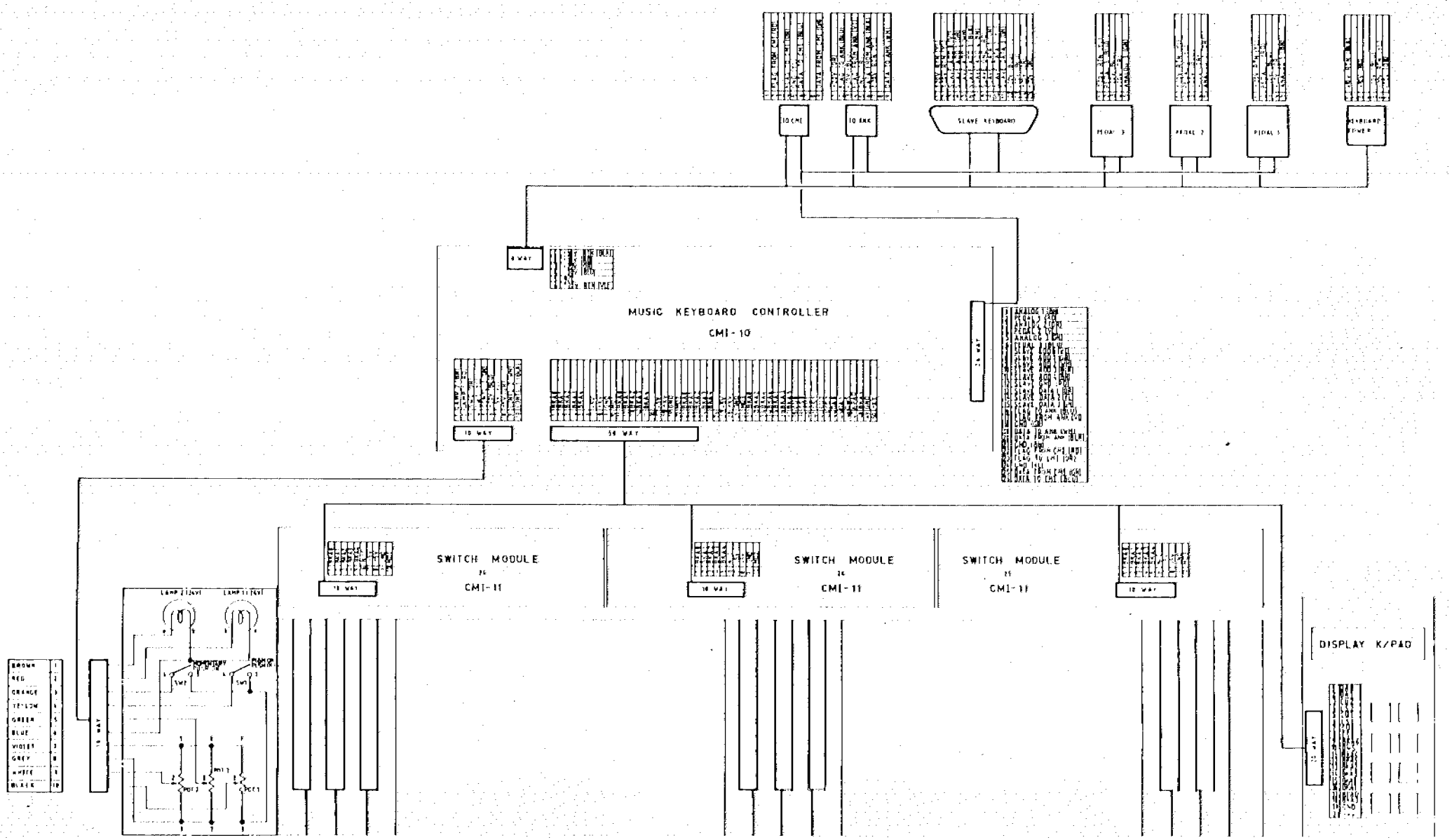
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FAIRLIGHT INSTRUMENTS P/L 15 BOUNDARY ST. RUSHCUTTERS BAY 2011 (02) 335222		SCALE	PASSED 26/6/1982	DATE 10/8/1979
KEYPAD / DISPLAY MODULE		DRAWN P.V.		DRAWING NUMBER
Sheet 1 of 1		TRACED B.P.L.		CMI-12-01
		CHECKED P.V.		



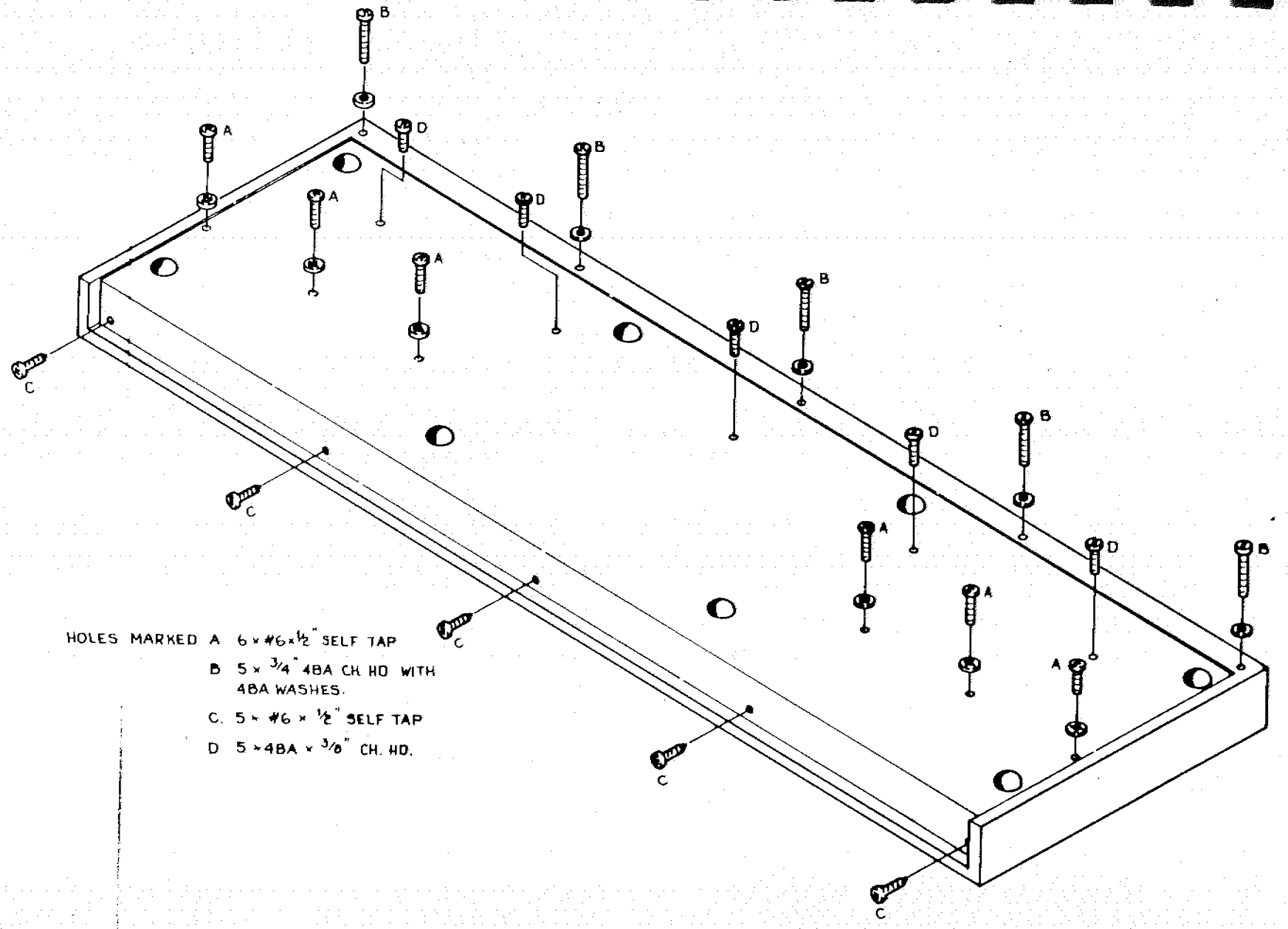
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FAIRLIGHT INSTRUMENTS P/L 15 BOUNDARY ST. RUSHCUTTERS BAY 2011 (02) 335222		SCALE		PASSED 26/6/1982 DATE 6/8/1979
KEYBOARD SWITCH MODULE REV. 3, 4 Sheet 1 of 1		DRAWN P.V. TRACED B.P.L. CHECKED P.V.		DRAWING NUMBER CMI-11-01



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
CMI		SCALE		PASSED / DATE: 10/6/81
SLAVE INTERFACE SHEET 1 of 1		DRAWN: PV		DRAWING NUMBER: CMI-14-01
		TRACED: MTB		
		CHECKED: PV		



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
MASTER COPY	CMI MUSIC KEYBOARD	SCALE		PASSED / DATE
	SIGNAL & POWER WIRING DIAGRAM	DRAWN / TRACED / CHECKED		DRAWING NUMBER MC004-01



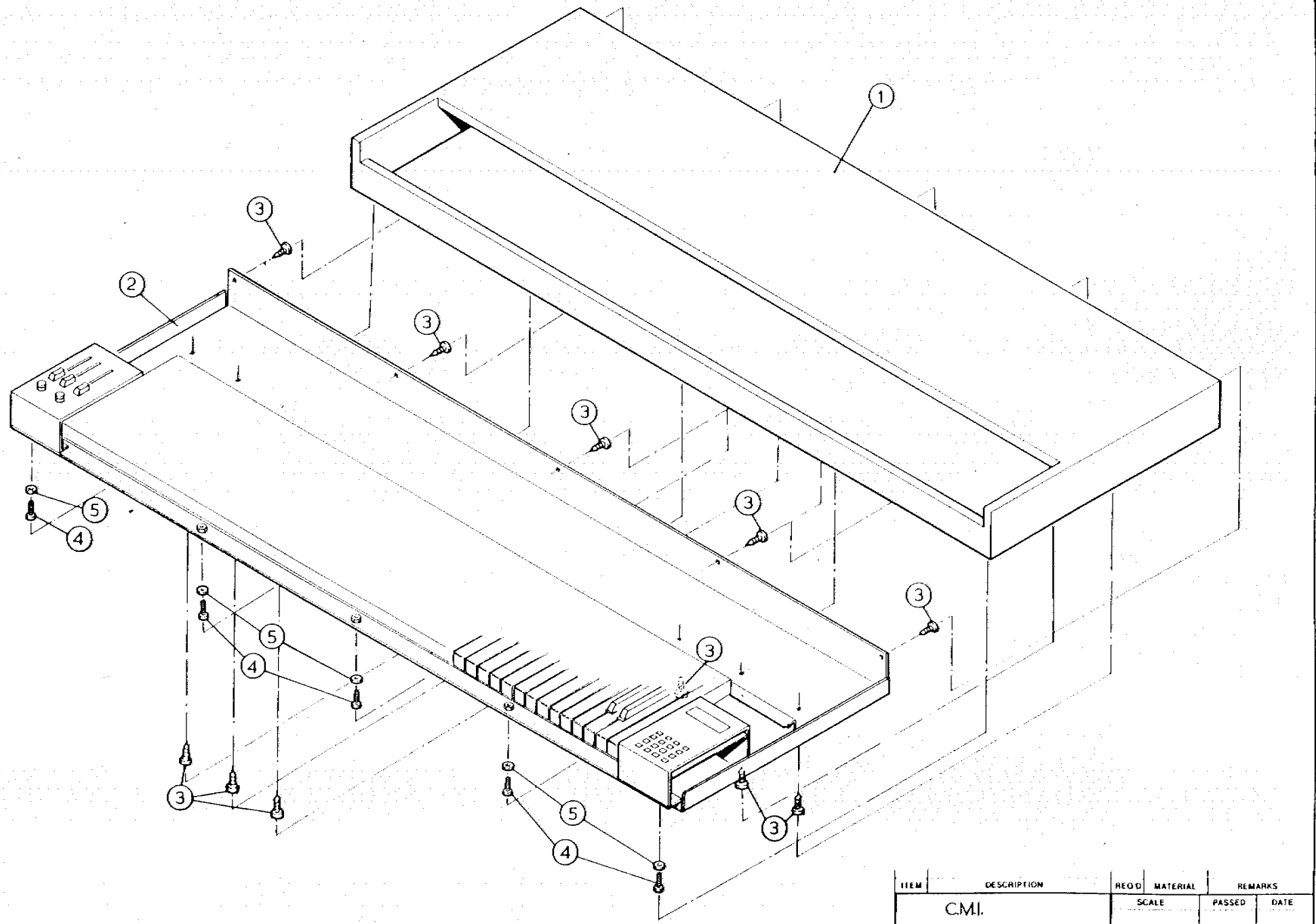
HOLES MARKED A 6 × #6 × ½" SELF TAP

B 5 × ¾" 4BA CH HD WITH 4BA WASHES.

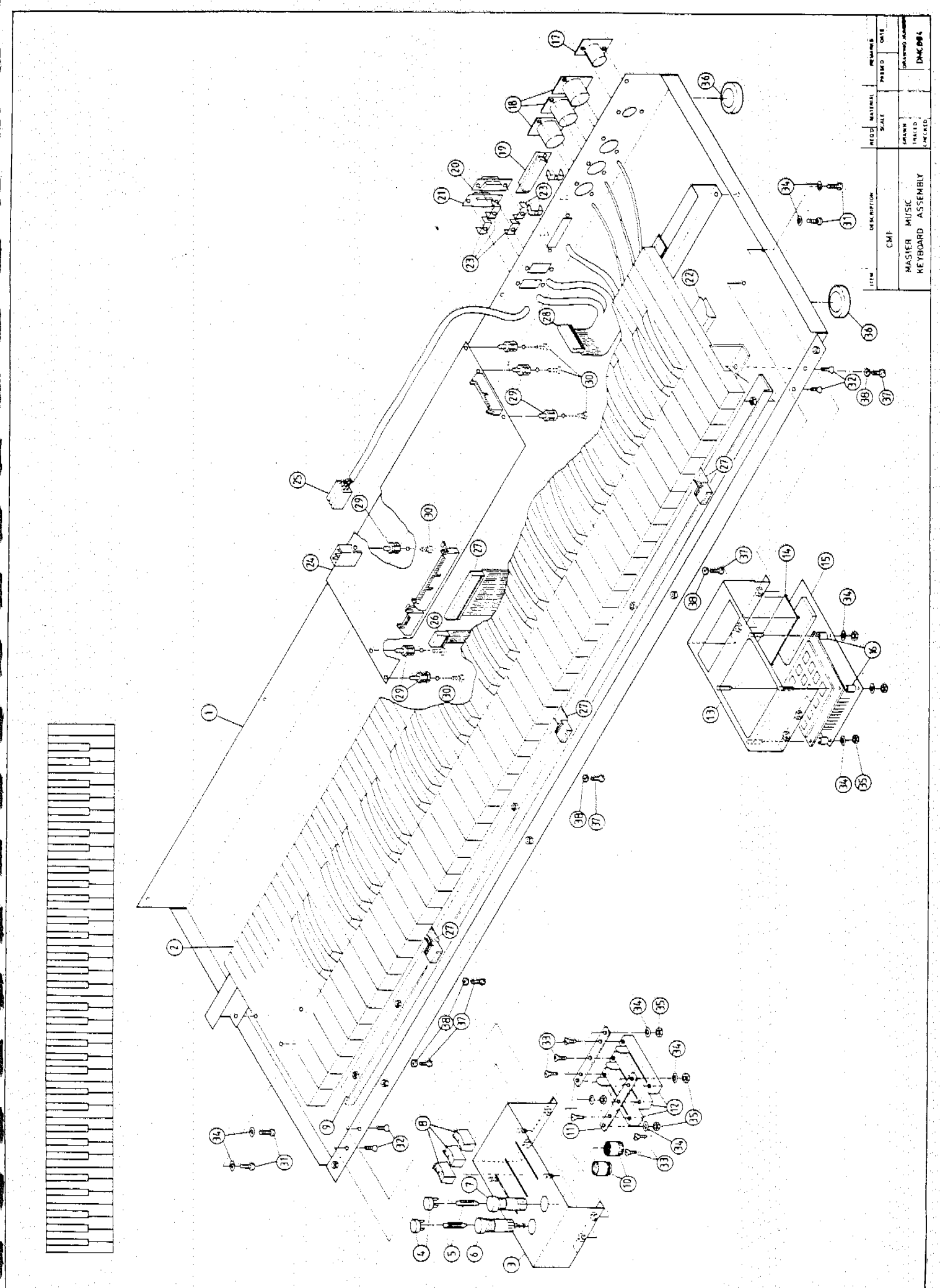
C. 5 × #6 × ½" SELF TAP

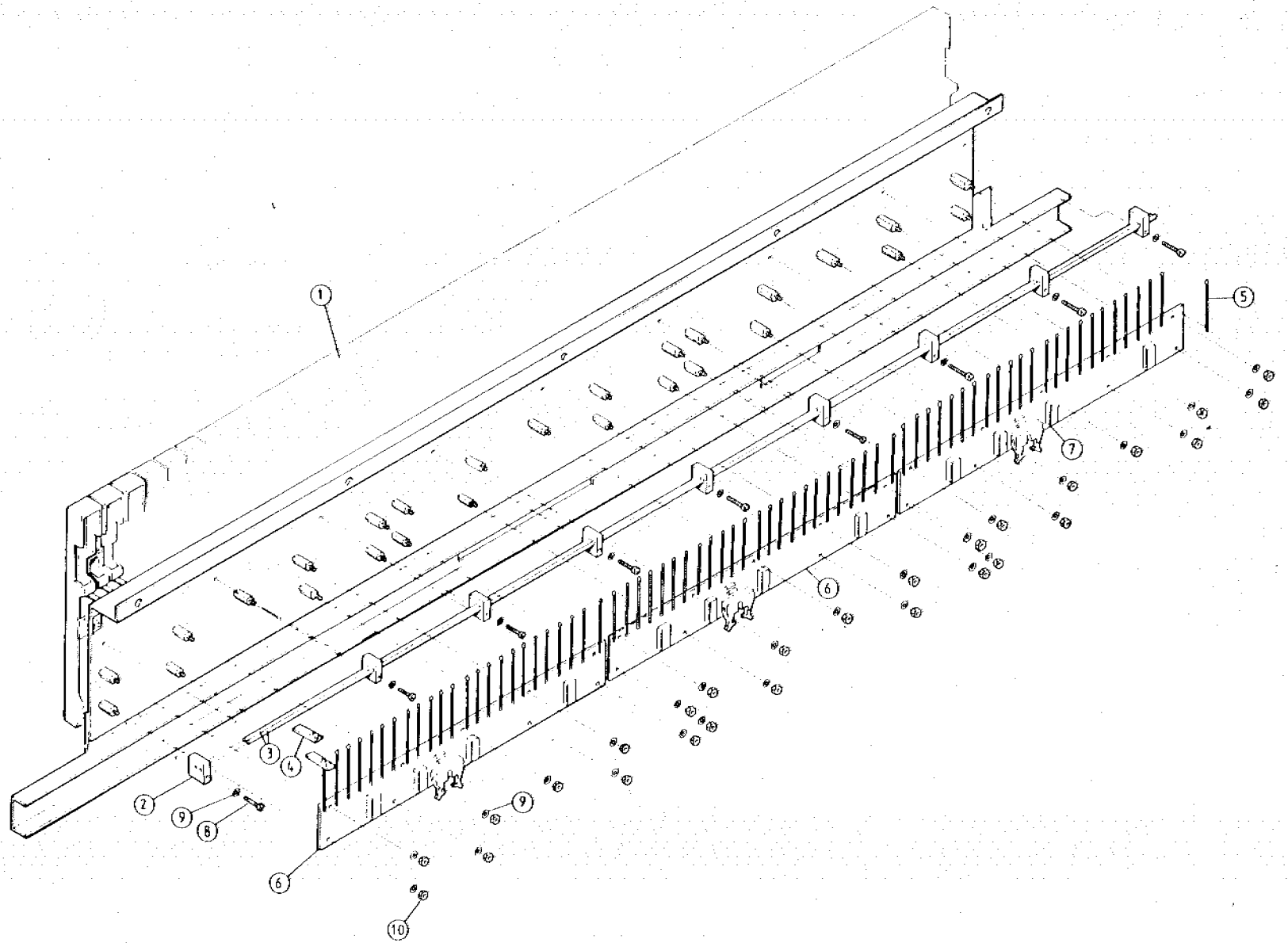
D 5 × 4BA × ⅜" CH. HD.

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	C.M.I.	SCALE	PASSED	DATE
				5/12/80
	EXPLODED VIEW OF FIXING SCREWS ON MASTER KEYBOARD TOP COVER	DRAWN MTB		DRAWING NUMBER
		TRACED		DMC004C
		CHECKED C.T.		

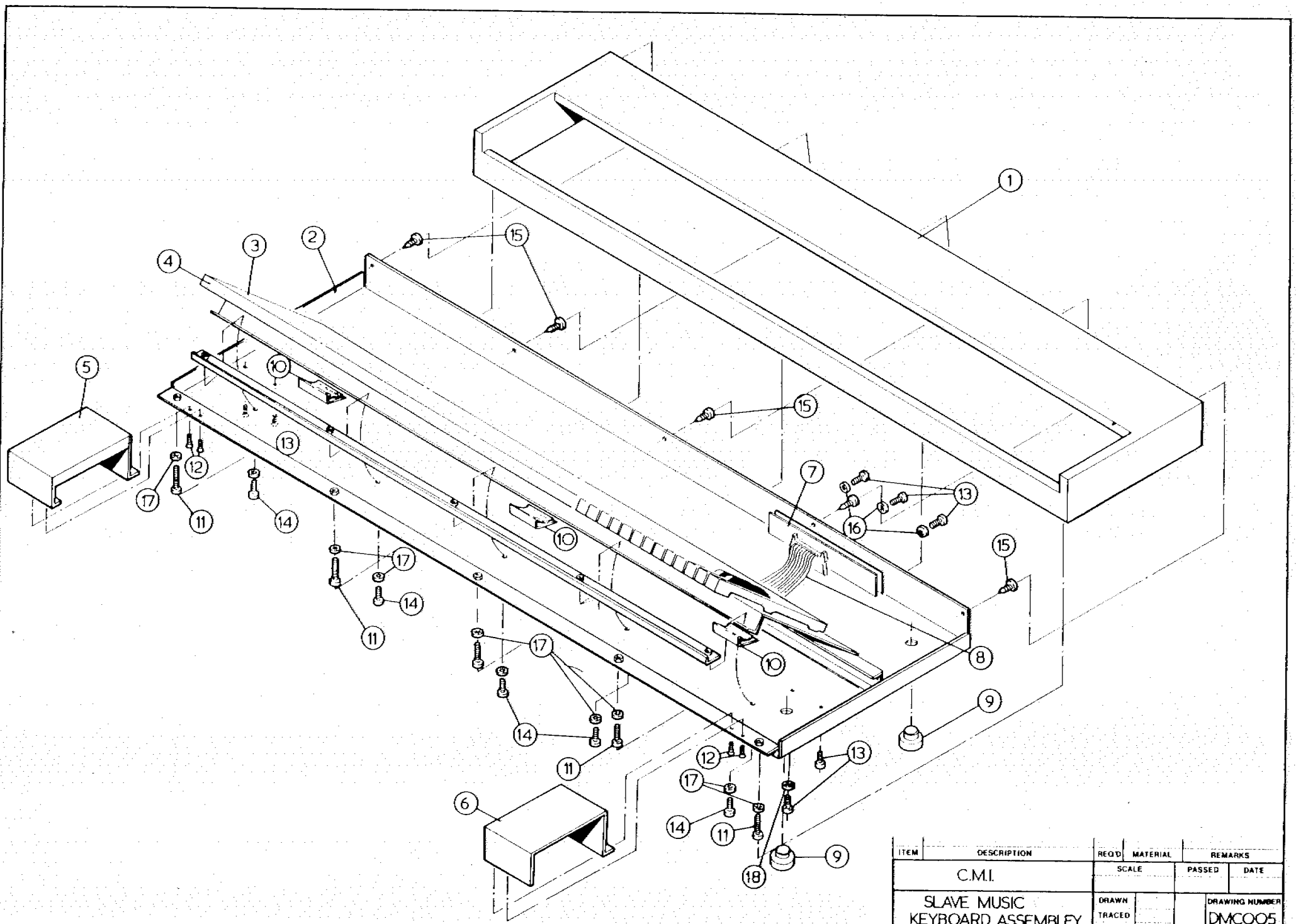


ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
C.M.I.		SCALE	PASSED	DATE
MASTER MUSIC KEYBOARD COMPLETE		DRAWN / TRACED / CHECKED		DRAWING NUMBER DMC00-1B


CMI
MASTER MUSIC
KEYBOARD ASSEMBLY
DRAWING NUMBER
DMC 004



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	CMI	SCALE		PASSED / DATE
	MUSIC KEYBOARD SUBASSEMBLY	DRAWN / TRACED / CHECKED		DRAWING NUMBER OMC 015



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
C.M.I.		SCALE	PASSED	DATE
SLAVE MUSIC KEYBOARD ASSEMBLEY		DRAWN / TRACED / CHECKED		DRAWING NUMBER DMC005

C.M.I. Music Keyboard Service Manual

11. MECHANICAL PARTS LIST

11.1 DMC004B MASTER KEYBOARD

REF. NO	PART NO	DESCRIPTION	REMARKS
1	G0028	COVER MUSIC WOOD	BEIGE
2	G0027	PANEL MUSIC BASE	BEIGE
3	H0114	SCREW 6GX1/2" PAN	
4	H0127	SCREW 4BAX3/4" CHD	
5	H0008	WASHER 4BA STAR	

11.2 DMC004 MASTER KEYBOARD ASSEMBLY

1	G0027	PANEL MUSIC K/BD BASE
2	MC015	KEYBOARD MECHAISM ASSY
3	G0023	CHEEK LH MASTER
4	G5406	BEZEL WHITE
5	G5407	LAMP
6	G5404	SWITCH #1
7	G5405	SWITCH #2
8	G5146	KNOB SLIDER POT
9	G0105	STRIP CLAMP MUSIC K/BD
10	H0211	NUT SWITCH
11	G0024	STRIP SLIDER POT
12	G5161	POT SLIDER
13	G0025	CHEEK RH MASTER
14	G5165	BEZEL DISPLAY RED
15	MCMI12	CARD MUSIC DISPLAY
16	G5142	SPACER 6BAX1/4" ROUND
17	D6738	CONNECTOR CANNON 7P
18	D6710	CONNECTOR CANNON 5S
19	D6729	CONNECTOR DMINI 25S
20	D6727	CONNECTOR DMINI 9S
21	D6728	CONNECTTOR DMINI 9P
22	G5122	CLIP CABLE
23	D6731	LUG DMINI
24	MCMI10	CARD C.M.I-10
25	G5219	CONNECTOR UTH9356-6R
26	MC070	CABLE SLIDER POT ASSY
27	MC063	CABLE KEYBOARD ASSY
28	MC071	CABLE REAR PANEL
29	G5107	STANDOFF
30	H0125	SCREW 6GX1/4" CHD
31	H0124	SCREW 6BAX1/4" CHD
32	H0117	SCREW 6BAX1/4" CSK
33	H0130	SCREW 6BAX3/16" CSK
34	H0012	WASHER 6BA STAR
35	H0201	NUT 6BA HEX
36	G5183	FOOT RUBBER
37	H0112	SCREW 4BAX3/8" CHD
38	H0008	WASHER 4BA STAR

REF. NO	PART NO	DESCRIPTION	REMARKS

11.3 DMC015 MASTER/SLAVE KEYBOARD SUBASSEMBLY

1	G5156	KEYBOARD MUSIC 73 KEYS	
2	G5154	BRACKET A/N/ K/BD MTG	
3	G5153	BAR PLATED	
4	G5187	RETAINER SPRING MUSIC K/BD	
5	G5158	SPRING KEYBOARD MUSIC	
6	MCM11A	CARD K/BD MUSIC 24SW	
7	MCM11B	CARD K/BD MUSIC 25SW	
8	H0122	SCREW 6BAX3/4" CHD	
9	H0012	WASHER STAR 6BA	
10	H0201	NUT 6BA HEX	

11.4 DMC005 SLAVE KEYBOARD

1	G0030	COVER MUSIC SLAVE WOOD BEIGE	
2	G0029	PANEL MUSIC SLAVE BASE BEIGE	
3	G5156	KEYBOARD MUSIC 73 KEYS	
4	G0105	STRIP CLAMP MUSIC K/BD.	
5	G0002	CHEEK SLAVE LH B/K	
6	G0003	CHEEK SLAVE RH B/K	
7	MC014	SLAVE KEYBOARD INTERFACE CARD	
8	MC019	CABLE MUSIC SLAVE K/BD INTERNAL	
9	G5183	FOOT RUBBER	
10	G5122	CLIP CABLE	
11	H0122	SCREW 6BAX3/4" CHD	
12	H0117	SCREW 6BAX1/4" CSK	
13	H0124	SCREW 6BAX1/4" CHD	
14	H0112	SCREW 4BAX3/8" CHD	
15	H0114	SCREW SELF TAPPER NO6X1/2" SLOTTED PAN HEAD	
16	H0012	WASHER 6BA STAR	
17	H0007	WASHER 4BA FLAT	

ALPHA NUMERIC KEYBOARD - #MC003

SERVICE MANUAL

FAIRLIGHT INSTRUMENTS - FEBRUARY 1985

Revision 2.1

4. DISASSEMBLY

4.1.BOTTOM COVER REMOVAL

1. Disconnect the Power/Signal cable from the computer before proceeding.
2. Place keyboard face down on smooth surface.
3. Using 'locking type' bladed screwdriver, remove the 4 screws from the base cover. Access is gained through the 4 clearance holes in the bottom cover.
4. Lift off the cover and slide the cord grip out from the bottom cover cut-out.

4.2. CABLE REMOVAL

1. Remove bottom cover as in 4.1.
2. Spread cord grip open to release cable.
3. Remove the cable from the Printed Circuit Card by spreading the connector locking lugs apart.

4.3. PRINTED CIRCUIT CARD REMOVAL

1. Remove bottom cover as in 4.1.
2. Leave keyboard laying face down, remove the 4 hexagon nuts and washers from each corner of the card.
3. Lift out the card from the top cover.

4.4.EPROM UPGRADE

1. Remove the Printed Circuit Card as in 4.3.
2. Place the card down on a flat surface with the keytops facing upwards.
3. Locate the EPROM near the heatsink bracket, refer to exploded view drawing #DMKB2.
4. NOTE THE POSITION OF PIN 1 ON THE EPROM WITH RESPECT TO ITS SOCKET BEFORE REMOVING THE EPROM. USE THE EPROM'S LABEL AS YOUR GUIDE TO THE POSITION OF PIN 1. Carefully lift out the EPROM from its socket.
5. To replace the EPROM, position its pins over its socket *NOTE POSITION OF PIN 1 BEFORE INSERTING* and push-down on the EPROM until its bottom is sitting flat on its socket.

4.5. KEYSWITCH MODULE REMOVAL

1. Remove the bottom cover as in 4.1.
2. Remove the keytop from the module being replaced and as many adjacent buttons as required to allow adequate working space. The keytop can be removed by pulling or prying upward with a padded tool from their under side. FAIRLIGHT INSTRUMENT recommends to use the 'Keytop Puller' tool,(Part #SW-10485). Refer to figure 1.

1. INTRODUCTION

The FAIRLIGHT Intelligent Alpha-Numeric Keyboard has been designed to be used as the primary input console for the Fairlight range of microcomputers. It has 64 keys, which include all the usual 'typewriter' functions plus cursor control keys.

It is a completely self-contained unit using a microprocessor for maximum flexibility and adaptability for custom applications. By changing the 2716 EPROM in the keyboard, any special key function can be programmmed.

High-reliability Hall-Effect switches are used which means no contact wear. The keytops are of a 'double-shot' moulded type, giving permanent keytop legends which will not wear away.

Connection between the keyboard and the computer is made via a 7-core cable. This cable provides power to the keyboard plus the serial link between the two devices.

2. SPECIFICATION

Switch Module Type:	Hall-Effect (no contact wear)
Total ket travel:	4.1mm
Key actuating force:	71 grams
Reliability:	100,000,000 operations/station
Keytop type:	Double-shot moulded
Data format:	RS-232C ASCII format
Baud rate:	110 to 9600. Factory set to 9600
Power requirements:	+16 to 18 volts at 500mA -16 to 18 volts at 100mA
Connector type:	9 pin 'D Mini' socket
Dimensions:	415mm(W) x 75mm(H) x 170mm(D)
Weight:	2.75kg

3. FUNCTIONAL DESCRIPTION

3.1 MPU, DECODING, RAM, RESTART, INTERRUPT CLOCK and OPTION SWITCHES (refer to drawing #IKB1-01).

3.1.1 Microprocessor Unit.

All keyboard functions are performed by the 6802 microprocessor unit (MPU) at location D2. This is activated by the 3.840MHz crystal which results in a MPU cycle time of 1.04 microseconds. At power-up the MPU is held reset by the 555 IC at location H2, to satisfy the 6802's reset requirements. After reset the MPU obtains its restart vector from ROM 2 at location C1 and starts program execution.

The 6802 MPU contains 128 bytes of internal RAM. This is permanently enabled by tying the Ram Enable signal (pin 36) high. This is the only RAM in the keyboard.

3.1.2 Address Decoding.

Selection of both ROMs, the Option switch and the PIA is performed by the LS139 1-of-4 decoders at location B1. The devices are selected when the devices' address(es) is on the address bus and both VMA and E are active (high). Not all address lines are used in the decoding so the devices appear in several places in the 6802's address space. See the following address map.

The address map of the keyboard is as follows:

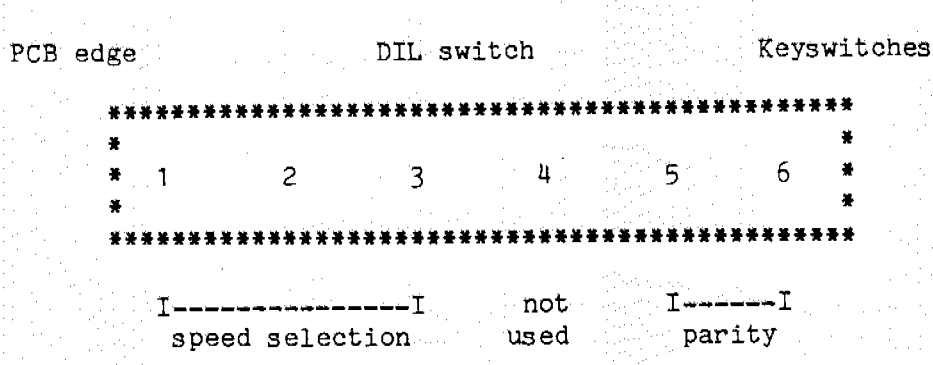
Address (Hex)	Function
4000-7FFF	Option switch
8000-BFFF	PIA
E000-FFFF	ROM 1 (optional)
F000-FFFF	ROM 2

Restart and other vectors must be stored in the last locations of ROM 2.

3.1.3 Software Readable Switch

The six-pole dual-in-line (DIL) switch provides for the selection of baud rate and parity, as follows :-

0 refers to switch on (closed).
1 refers to switch off (open).



3.1.4 DIL Switch selection

Speed selection (baud)

1	2	3	
0	0	0	9600
0	0	1	600
0	1	0	2400
0	1	1	150
1	0	0	4800
1	0	1	300
1	1	0	1200
1	1	1	110

Parity selection

5	6	
0	0	even parity
0	1	odd parity
1	0	no parity bit 7 set to 0
1	1	no parity bit 7 set to 1

The standard switch setting is:

1	2	3	4	5	6
on	on	on	on	on	off

3. FUNCTIONAL DESCRIPTION (continued)

3.1.5 Interrupt Clock

The 6802's E output is divided by 100 by the dual CMOS counter 4518 at location A2 to provide a 9.6KHz interrupt source. This clock is connected to the PIA's CA1 pin which in turn is programmed to generate an interrupt to the MPU. This is used by the software in determining the serial output baud rate.

3.2 PIA, VOLTAGE REGULATORS, CLICKER AND RS-232C SIGNAL
(refer to drawing #IKB1-02).

3.2.1 Parallel Interface Adapator (PIA)

The two 8 bit ports in the PIA at location D1 are used to scan the keyswitch matrix. The remaining lines are used to generate RS-232C controls and the data line. The ports and control line functions are as follows:-

Port A	input	- from keyswitch columns
Port B	output	- to keyswitch rows
CA1	input	- receives 9.6KHz clock
CA2	output	- CTS flag
CB1	input	- RTS flag
CB2	output	- keyboard data

3.2.2 Voltage Regulators

The keyboard receives +/- 20 volts from the main computer's power supply along the same cable as the keyboard's data signals. These voltages are regulated to -12, +12 and +5 by the three terminal regulators located on the heat sink along the edge of the PCB. A 10 ohm 5 watt resistor is in series with the +20 volts and the 7812 +12 volt regulator to reduce power dissipation in the regulator.

3.2.3 Clicker

Audible feed back in the keyboard is provided by a relay driven by a discrete monostable. The monostable is triggered by any serial output data. This monostable is configured around the CMOS 4001 at location G2 and capacitors C15, 16 and resistors R6, 7. A LED is connected across the relay and flashes when the relay is activated.

3.2.4 RS-232C Levels

The TTL signal outputs are converted to RS-232C levels by the driver in location H1 and inputs are converted to TTL by attenuators feeding LS14 inverters in location F1.

3.3 KEYBOARD OPERATION

The keyboard is scanned by the MPU by setting successive rows to "1" using the PIA, and seeing if any columns go to "0". Each key has a unique row and column number thus allowing the MPU to access each of the 64 keys individually.

The HALL EFFECT keyswitches do not "bounce", so repetitive reads of a depressed key do not have to be made to distinguish if a key is pressed or released. The keyboard scanning is the main program loop. When keys are found depressed and later released, their state is noted in a 64 bit 'key state' table and the appropriate ASCII code is looked up, taking into account any other simultaneous depression of keys (such as shift or control). The character to be sent is put in a queue. One key can be handled each scan.

The characters in this queue are then outputted, one bit at a time in the interrupt routine. The transmission rate is determined by the setting of the option switch and the 9.6KHz interrupt clock. This results in N key roll-over.

4. DISASSEMBLY

4.1.BOTTOM COVER REMOVAL

1. Disconnect the Power/Signal cable from the computer before proceeding.
2. Place keyboard face down on smooth surface.
3. Using 'locking type' bladed screwdriver, remove the 4 screws from the base cover. Access is gained through the 4 clearance holes in the bottom cover.
4. Lift off the cover and slide the cord grip out from the bottom cover cut-out.

4.2. CABLE REMOVAL

1. Remove bottom cover as in 4.1.
2. Spread cord grip open to release cable.
3. Remove the cable from the Printed Circuit Card by spreading the connector locking lugs apart.

4.3. PRINTED CIRCUIT CARD REMOVAL

1. Remove bottom cover as in 4.1.
2. Leave keyboard laying face down, remove the 4 hexagon nuts and washers from each corner of the card.
3. Lift out the card from the top cover.

4.4.EPROM UPGRADE

1. Remove the Printed Circuit Card as in 4.3.
2. Place the card down on a flat surface with the keytops facing upwards.
3. Locate the EPROM near the heatsink bracket, refer to exploded view drawing #DMKB2.
4. NOTE THE POSITION OF PIN 1 ON THE EPROM WITH RESPECT TO ITS SOCKET BEFORE REMOVING THE EPROM. USE THE EPROM'S LABEL AS YOUR GUIDE TO THE POSITION OF PIN 1. Carefully lift out the EPROM from its socket.
5. To replace the EPROM, position its pins over its socket *NOTE POSITION OF PIN 1 BEFORE INSERTING* and push-down on the EPROM until its bottom is sitting flat on its socket.

4.5. KEYSWITCH MODULE REMOVAL

1. Remove the bottom cover as in 4.1.
2. Remove the keytop from the module being replaced and as many adjacent buttons as required to allow adequate working space. The keytop can be removed by pulling or prying upward with a padded tool from their under side. FAIRLIGHT INSTRUMENT recommends to use the 'Keytop Puller' tool,(Part #SW-10485). Refer to figure 1.

4. DISASSEMBLY (continued)

3. Unsolder the 4 terminals of the Key Switch Module from the PCB using a temperature controlled soldering iron set to 750F degrees. Use a solder removal tool to remvove all the solder from the pin hole in the PCB. Refer to figure 2.
4. Insert the 'Module Removal' tool, (Part #SD-10101) at each end of the module. With the Module Removal tools in position, grip the switch module with a pair of pliers and pull straight out.Refer to figure 4.
5. Replace the module with same part number type as the one being replaced.

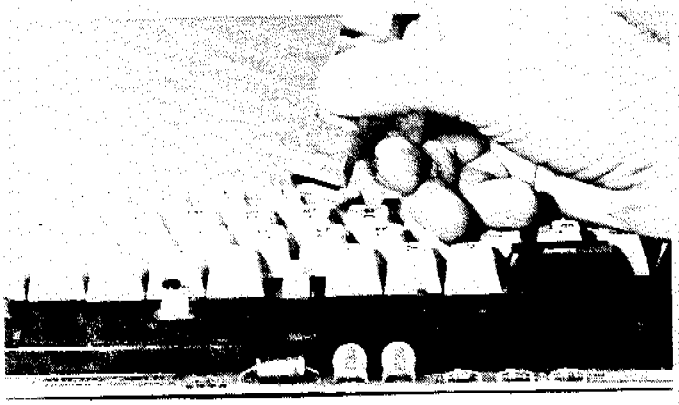


Figure 1 Button Removal

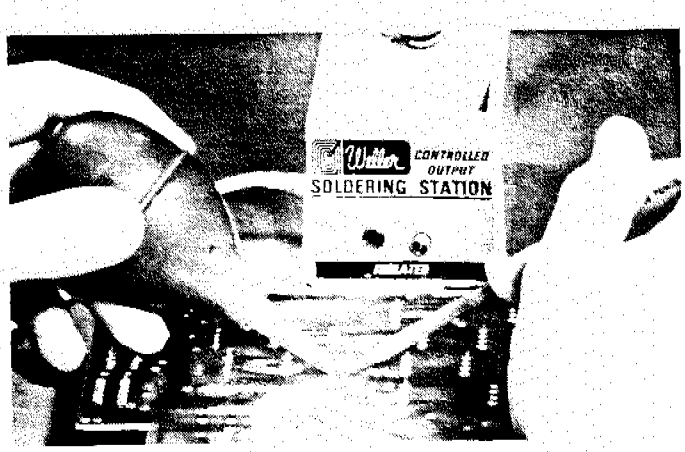


Figure 2 Unsoldering Terminals

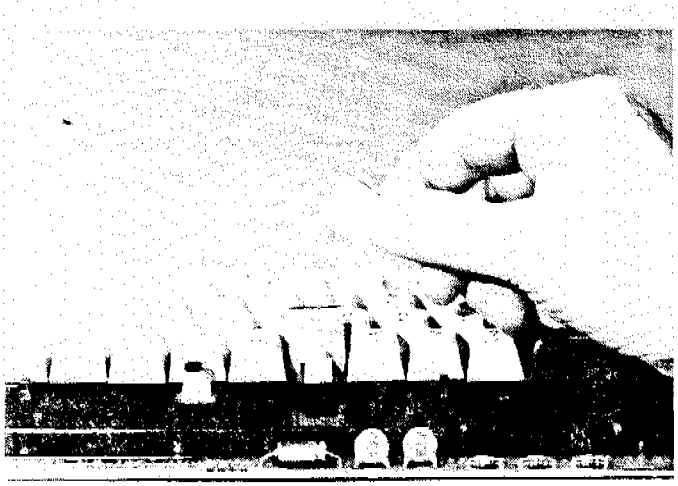


Figure 3 Inserting Removal Tools

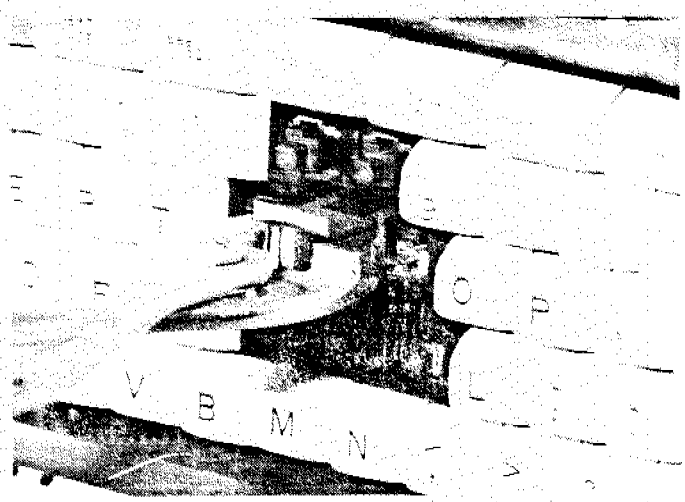
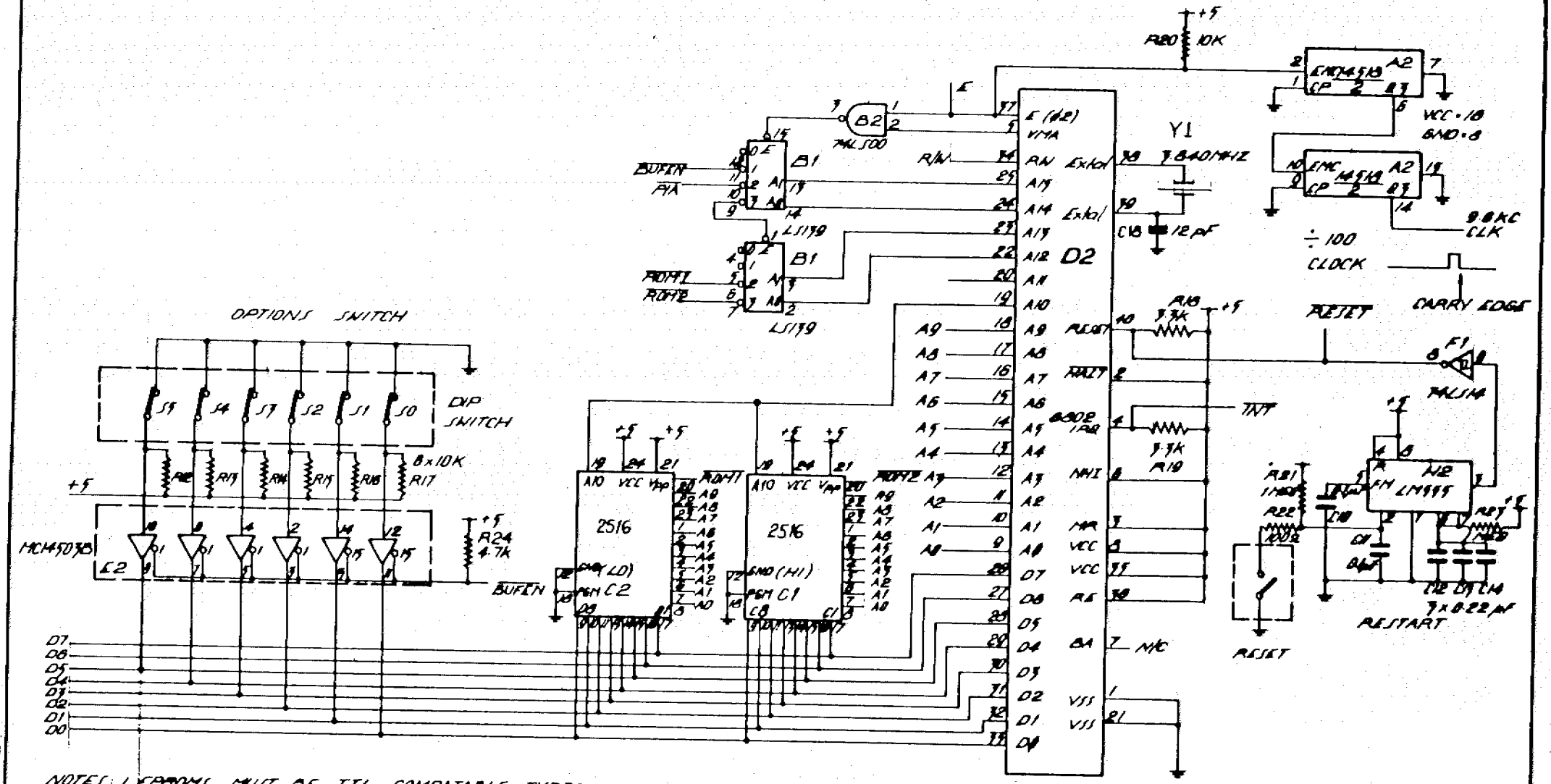


Figure 4 Module Removal



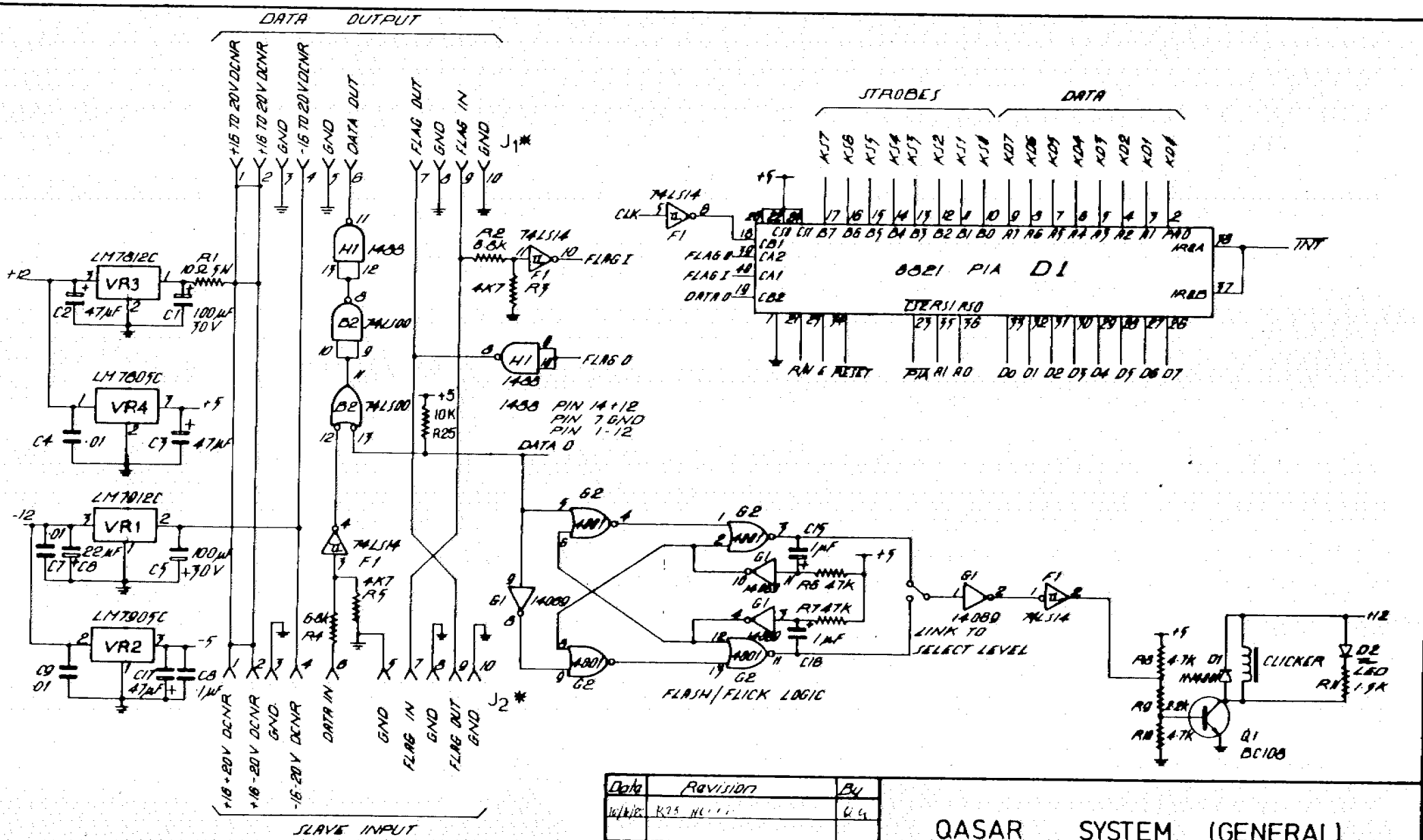
Date	Revision	By
0.6/81	1.24 LIC UNCELLED	GG

QASAR SYSTEM (GENERAL)

INTELLIGENT KEYBOARD UNIT PROCESSOR (ROM) OPTIONS

Sheet 1 of 3

Drawn	Checked	Scale	Drawing No.
BINOPI Pty.	P.V.		IkB1- 01
NOV. 1981	REV. 3	NIL	



* CONNECTOR PINS ON J_1 + J_2 ARE NUMBERED ACCORDING TO POSITION IN 10 WAY STRIP CABLE. PIN 1 ON ARROW END OF CONNECTOR

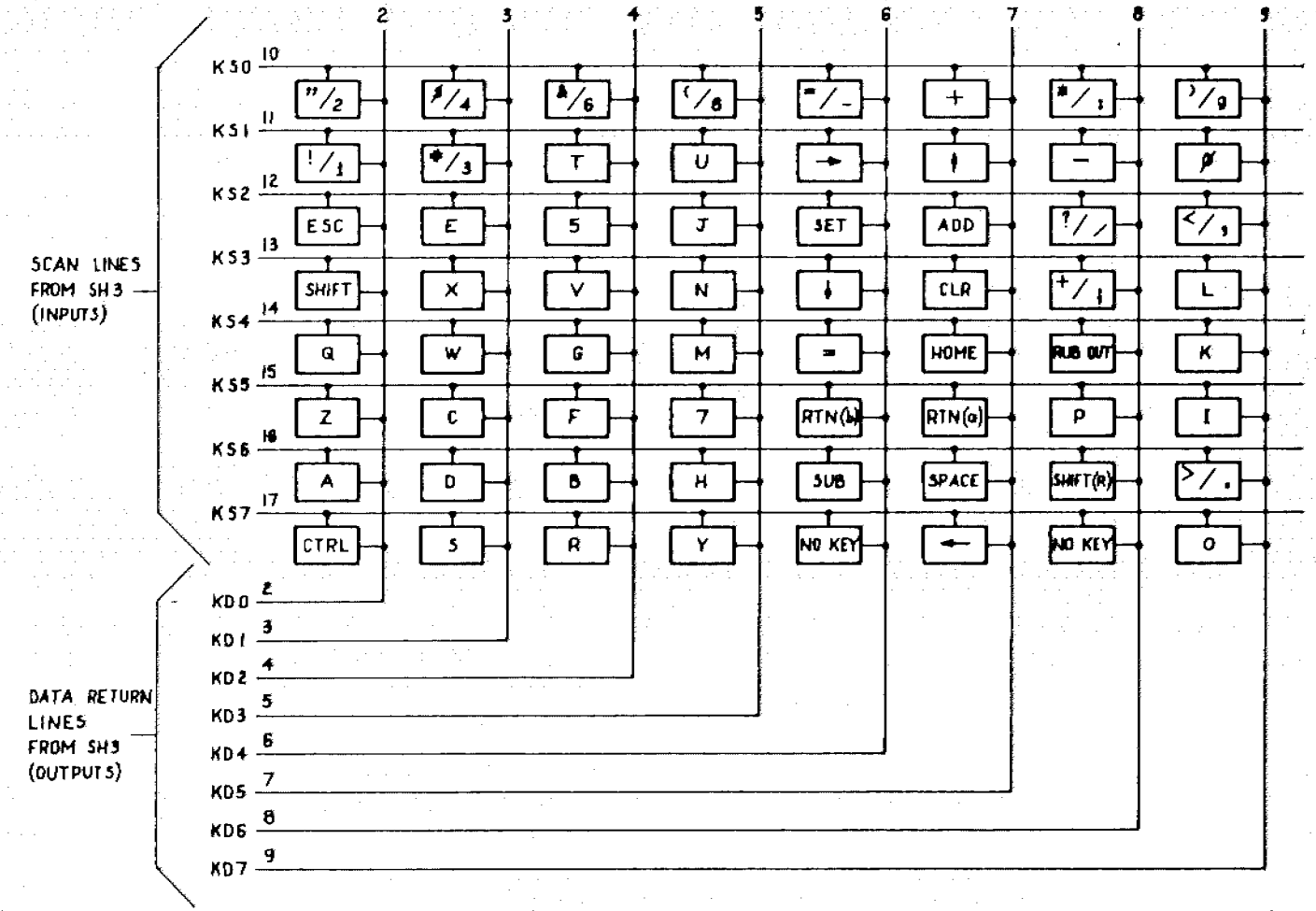
Date	Revision	By
16/11/81	R25 NOW 10K	G.G.

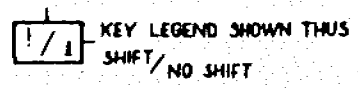
QASAR SYSTEM (GENERAL)

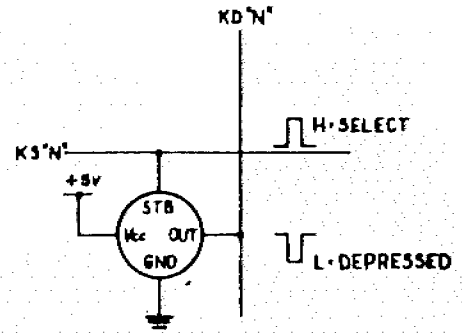
INTELLIGENT KEYBOARD UNIT
DATA PORTS & MISCELLANEOUS LOGIC

Sheet 2 of 3

Drawn	Checked	Scale	Drawing N°
BINOPI Pty.	P.V.	NIL	IkB1 – 02
NOV. 1981	REV. 3		





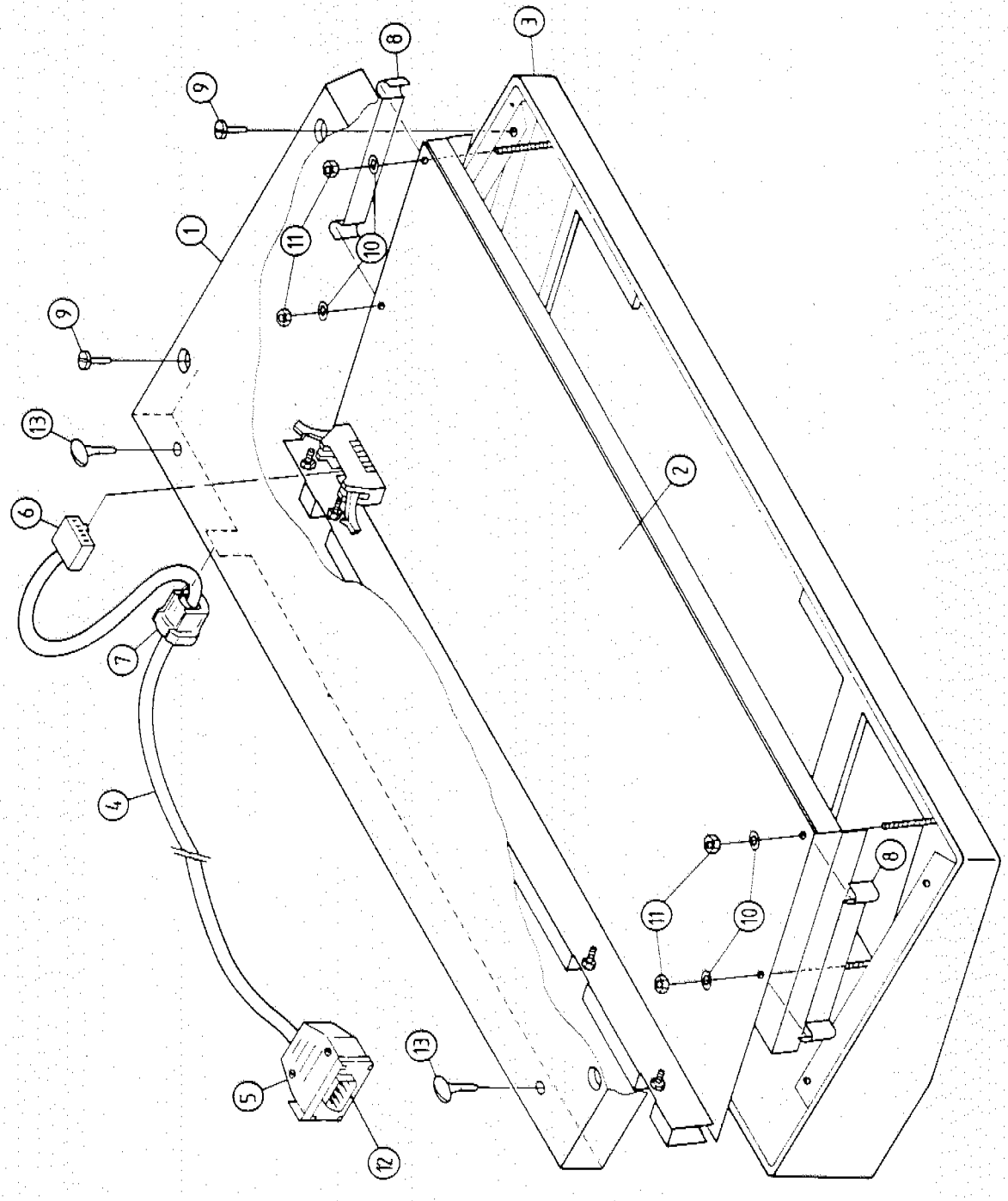


TYPICAL KEY WIRING

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
FAIRLIGHT INSTRUMENTS P/L 15 BOUNDARY ST RUSHCUTTERS BAY 2011 (02) 335222		SCALE	PASSED	DATE 22/4/1978
INTELLIGENT KEYBOARD SWITCH ARRAY (64 KEY) SHEET 3 of 3		DRAWN A.G.F TRACED B.P.L CHECKED P.V.	REV.3	DRAWING NUMBER IKB1-03-

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5.3.6 Focus Adjustment	7
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ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	CMI	SCALE	PASSED	DATE
	ALPHA/NUMERIC KEYBOARD ASSEMBLY	DRAWN / TRACED / CHECKED		DRAWING NUMBER DMC 003

7. MECHANICAL PARTS LIST

7.1 DMKB2 ALPHA NUMERIC KEYBOARD MODULE

Drawing ref.	Part #.	Description.
1	G1046	Heatsink
2	EQKB1	PCB
3	G0042	Switch Module 4B3S
4	G4008	Support Module SD10438
5	G4009	Tension bar
6	G0061	Felt pad
7	G4006	Switch Module 6A1D
8	G4005	Switch Module 4A1S
9	G4004	Switch Module 6B1D
10	G4003	Switch Module 4B1S
11	H0123	Screw 6BAx1" CHD
12	H0201	Nut 6BA Hex.
13	H0110	Screw 4BAx1/4" nylon
14	H0202	Nut 4BA Hex.
15	H0002	Washer Mica TO220

7.2 DMC003 ALPHA NUMERIC KEYBOARD ASSEMBLY

1	G1049	Bottom cover
2	MQKB1	Card assembly
3	G1017	Top cover
4	MC013	Cable assembly
5	D6753	Cover assembly D-Mini
6	D6021	Connector shell 10 Way
7	G5215	Cord grip
8	G1048	Spacer
9	H0112	Screw 4BAx3/8" CHD.
10	H0008	Washer 4BA Star
11	H0202	Nut 4BA Hex.
12	D6753	Connector 9 pin D-Mini
13	G5180	Rubber foot

8. SIGNAL LIST

8.1 POWER/SIGNAL CABLE #MC013

9 Pin "D-Mini" Connector end.

Pin 1 +18 to +22 volts unregulated supply to keyboard.

Pin 2 Not Connected.

Pin 3 -18 to -22 volts unregulated supply to keyboard.

Pin 4 Not Connected.

Pin 5 SIGNAL GROUND.Ground for data paths.

Pin 6 DATA OUT. Serial data from keyboard. Format is RS-232C. Normally at -10 volts. Each time a key is depressed a burst of +10 volts pulses lasting approx. 1mS should be seen.

Pin 7 POWER RETURN. Return (Ground) for + and - supplies.

Pin 8 Not Connected.

Pin 9 Not Connected.

10 Pin PCB connector end.

Pin 1 -18 to -22 volts unregulated supply to keyboard.

Pin 2 Same as Pin 1.

Pin 3 POWER RETURN.

Pin 4 -16 to -22 volts unregulated supply to keyboard.

Pin 5 SIGNAL GROUND.

Pin 6 DATA OUT.

Pin 7 FLAG OUT.

Pin 8 SIGNAL GROUND.

Pin 9 FLAG IN.

Pin 10 SIGNAL GROUND.

GRAPHICS MONITOR, #MQ215L

SERVICE MANUAL

FAIRLIGHT INSTRUMENTS, FEBRUARY 1985

Revision 2.1

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1. SAFETY WARNING

CAUTION: Unqualified persons should not attempt to repair or adjust this equipment. High voltages are present inside the unit.

1.1 Picture Tube Handling

A large amount of mechanical potential energy is stored in the picture tube by virtue of its vacuum.

The strength of the glass envelope will be impaired by surface damage, such as scratches or bruises (localised surface cracks caused by impact). When a tube is not in its equipment or original packing, it should be placed faceplate downwards on a pad of suitable ribbed material which is kept free from abrasive substances. Stress on the neck of the tube must be avoided. Handle by the following methods:-

(1) Tube on one edge

To lift a tube from the edge down position, one hand should be placed around the parabola section of the cone and the other hand should be placed near (slightly below) the centre of the faceplate as shown in Figure 1.

UNDER NO CIRCUMSTANCES SHOULD ANY FORCE BE APPLIED TO THE NECK OF THE TUBE.

(2) Tube face-down

To lift a tube from the face-down position, the hands should be placed under the areas of faceplate close to the fixing lugs at diagonally opposite corners of the faceplate as shown in Figure 2. The tube must not be lifted from this position by the lugs themselves.

UNDER NO CIRCUMSTANCES SHOULD ANY FORCE BE APPLIED TO THE NECK OF THE TUBE.

(3) Tube face-up

To lift a tube from the face-up position, the hands should be placed under the areas of cone close to the fixing lugs at diagonally opposite corners of the cone as shown in Figure 3. The tube must not be lifted from this position by the lugs themselves.

UNDER NO CIRCUMSTANCES SHOULD ANY FORCE BE APPLIED TO THE NECK OF THE TUBE.

If the handling procedures for the tube prior to insertion in the chassis is such that there is a risk of personal injury as a consequence of accidental damage to the tube, then it is recommended that protective clothing should be worn, particularly eye shielding.

1. SAFETY WARNING (continued)

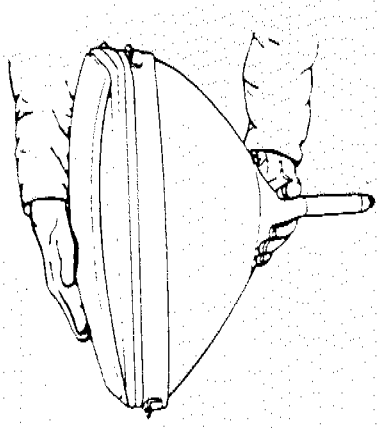


Fig.1 — Lifting picture tube from edge-down position

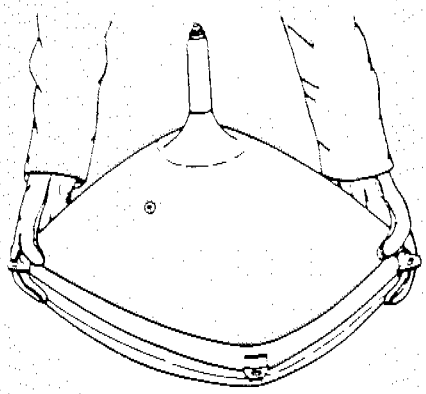


Fig.2 — Lifting picture tube from face-down position

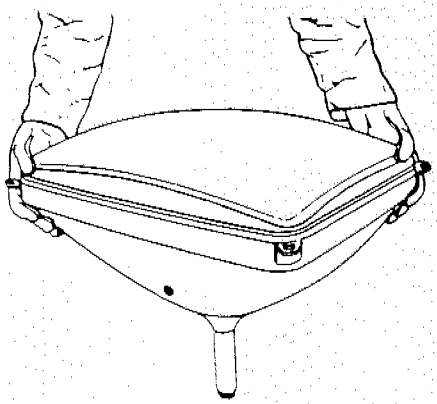


Fig.3 — Lifting picture tube from face-up position

Attention is called to the fact that high voltage may be carried by the internal conductive coating which is connected to the final anode connector and also by the external coating if not earthed, even after the tube has been removed from the unit. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts).

2. SPECIFICATIONS

Picture tube type:	15 inch P31 green phosphor with anti-reflective bonded face-plate. 110 degree deflection angle.
Video Response (Typical):	5Hz to 20MHz(-3db)
Video output risetime (Typical):	30V in 18nS
Horizontal Linearity:	better than 3%
Field Linearity:	better than 1.5%
Geometric raster distortion:	within 1%
Scanning frequency:	Horizontal, 15,625Hz Vertical, 50Hz
Horizontal Flyback time:	10.5uS
Horizontal blanking time:	10.5uS
Field blanking time:	800uS
Anode voltage (eht):	17KV at zero beam current
Input Signal:	1V pk-pk composite video (negative sync) 75ohms
Controls:-	
External:	a) Contrast, Brightness
Internal:	b) H.frequency, H.phase, H.linearity. c) V.frequency, V.height, V.linearity. d) Focus e) Video black level. f) 24V supply adjust.
Power Requirements:	100V,120V,220V,240V -5% +10% 50Hz/60Hz
Power Consumption:	35W (nominal)
Dimensions:	490mm(W) x 345mm(H) x 380mm(D)
Weight:	approximately 30kg

3. INTRODUCTION

The FAIRLIGHT Graphics Monitor is a high resolution CRT monitor for use with the Fairlight range of microcomputers. It is designed to accept composite video from the Graphics/Lightpen Card Q219 and interface the lightpen. The Q219 card is located in the microcomputer mainframe.

The display tube is a high-resolution 15" diagonal P31 type which gives a crisp, green image. The large format results in a highly readable display, which means low operator fatigue.

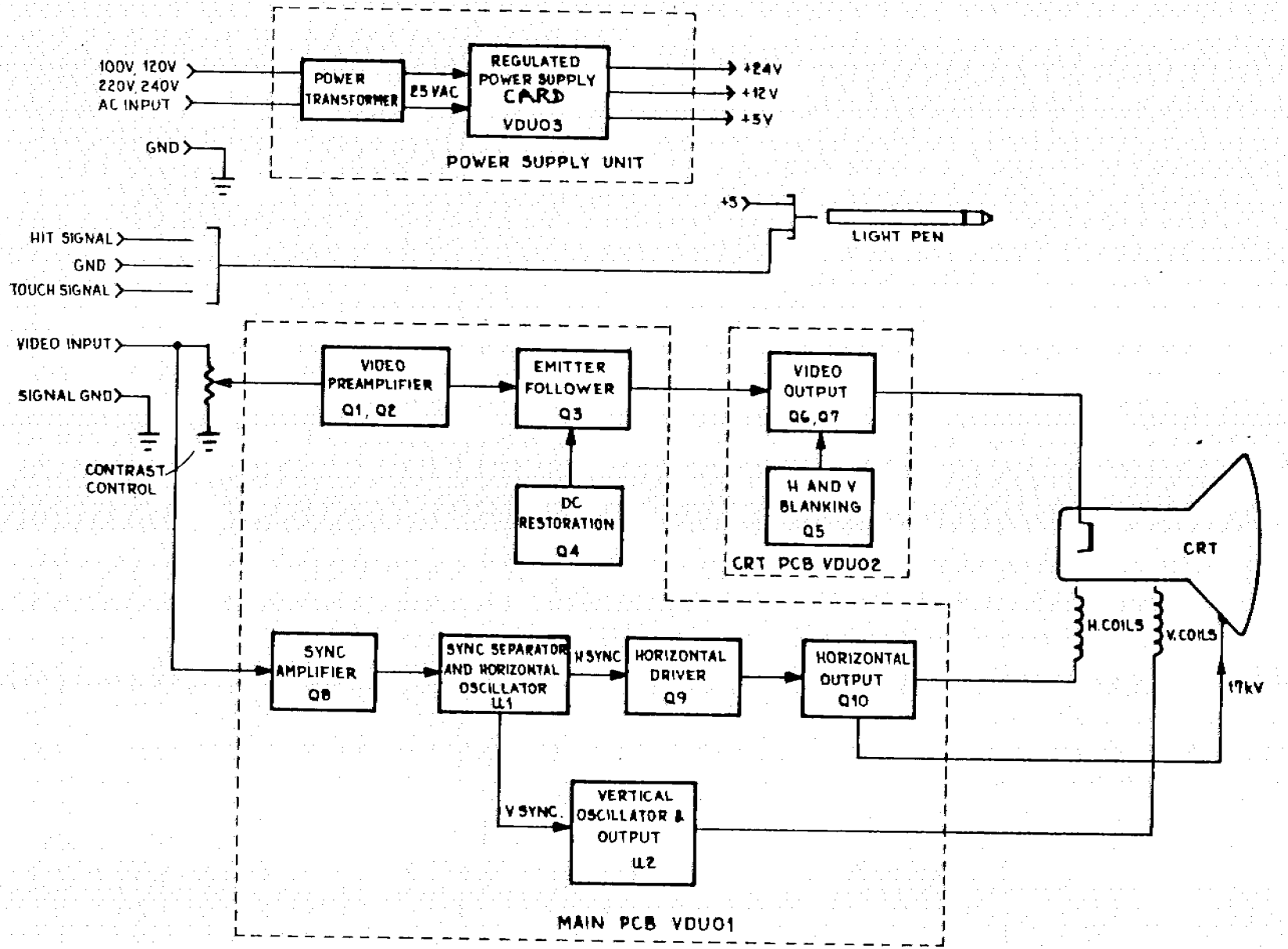
An optional high-performance Light Pen is used with the monitor. The lightpen is used for inputting graphical data, selecting options from a menu or cursor positioning in word-processing.

The lightpen is of high quality metal construction. Connection to the monitor is by means of a flexible spiral retractable cord and miniature connector.

When the pen is pointed at the screen, a bright cursor is displayed to show the exact point it is 'seeing'. The pen is activated by touching the insulated end with a finger, at which time a T.T.L. 'Touch' signal is sent to the computer.

A single cable, containing 3 co-ax cables, makes the signal connection between the monitor and computer. It carries the video information from the computer plus the Light Pen HIT and TOUCH signals back to the computer. Mains power for the monitor is supplied via the computer, to allow the mains keyswitch to turn both Monitor and computer On and Off together.

A block diagram of the Graphics Monitor is shown on the next page.



BLOCK DIAGRAM OF GRAPHICS TERMINAL * MQ215L

5. CIRCUIT ADJUSTMENT

5.1 Preliminary Set-up

1. Check that mains selector on rear of Graphics Monitor is selected to suit local mains voltage.
2. Apply 1V pk-pk composite video signal.
3. Connect mains supply.
4. Adjust contrast and brightness controls for optimum picture.

5.2 Power Supply Card, VDU03

5.2.1 24V adjust.

1. Connect a voltmeter to pins 3 and 1 on connector P9 on the power supply card VDU03.
2. Check output is +23.1V DC.
3. Adjust using RV1, if necessary.

5.3 Main Card, VDU01

5.3.1 Horizontal Frequency.

1. Short point 'fo' (refer to circuit diagram) to ground.
2. Adjust H. freq control VR3 for near stable picture.
3. Remove shorting strap from 'fo'.

5.3.2 H. Phase.

1. Increase brightness control until picture background can be seen.
2. Adjust H. Phase control VR4 to centre picture horizontally within background raster.

5.3.3 H. Linearity.

1. Adjust H. Lin coil L2 to obtain optimum horizontal linearity at the start and end of the horizontal scan.

5.3.4 Vertical Frequency.

1. Turn V. Frequency control VR40 until picture starts rolling down the screen and the blanking bar is seen.
2. Slowly turn VR40 back so that bar rolls up and locks in.
3. Turn VR40 a few more degrees to ensure stable locking.

5. CIRCUIT ADJUSTMENT (continued)

5.3.5 Vertical Height & Linearity.

1. Connect CMI and load a page with defined edges e.g. Page 6.
2. Turn V. Height control VR56 until there is approximately 15mm gap between picture edge and top and bottom of screen.
3. Adjust V. Lin control VR47 for optimum vertical linearity at the top and bottom portions of the picture.
4. Repeat step 2. if necessary.

5.3.6 Focus Adjustment.

1. Adjust contrast and brightness controls for optimum picture.
2. Adjust Focus control VR9 for optimum picture focus.

5.4 CRT Card, VDU02

5.4.1 Black Level

1. Turn contrast control to maximum.
2. Connect staircase generator signal to input.
3. Check video level at P4 pin 5 is approx. 4.5V p-p.
4. Adjust VR2 so that lower grey levels appear.
5. Ensure lowest level (black) actually stays black.

6. DISASSEMBLY

6.1 Top Cover Removal
(Refer to Exploded View #MQ215L/02)

1. Remove the 4 counter-sunk screws marked 6 from both sides of cover.
2. Remove the 3 dome headed screws marked 7 from the rear panel.
3. Lift off top cover.

6.2 Picture Tube Replacement
(refer to Exploded View #MQ215L/01)

Caution: Refer to SAFETY WARNING Section 1 before proceeding.

1. Remove light pen as in 7.4.1.
2. Remove top cover as in 6.1.
3. Remove 10-way cable from the VDU03 card.
4. Discharge and disconnect the red high voltage cable from the picture tube.
5. Remove the CRT card VDU03 and defletion yoke from the neck of the picture tube.
6. Remove the six cheese-head screws holding the front panel/CRT brackets, marked 16 on drawing.
7. Tilt Front panel forward and down until face of the picture tube is laying face down in front of Graphics monitor
8. Remove 4 outer hexagon nuts and washers from front panel studs, and slowly withdraw picture tube from front panel.

7. LIGHT PEN

7.1 General Description

The light pen is completely self-contained and requires only a 5V supply. The pen is activated by touching the end with a finger, at which time a T.T.L. touch signal is sent to the computer. The 'touch' signal only with the 'hit' signal is connected to the computer via the 5 pin Cannon connector located on the rear of the V.D.U. 5V for the light pen is obtained from the P.S.U. card located on the Power Supply Unit (refer to Section 8).

7.2 Light pen adjustments

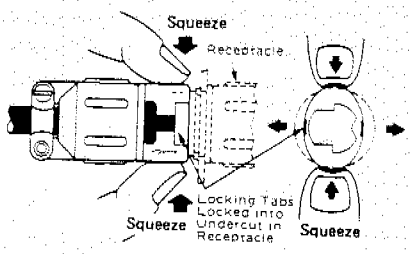
7.2.1 Sensitivity.

The pen sensitivity is factory set, to provide good performance in most applications. If necessary, the sensitivity main the body. CLOCKWISE rotation DECREASES the sensitivity. The pen may be set for maximum sensitivity (without a light source) by increasing the sensitivity until the pen free-runs (dots all over the screen) and then backing off until the dots disappear.

7.3.1 Operation check.

Operation of the pen may be checked by using a laboratory oscilloscope both as signal source and display. Set the scope for a line triggered sweep at a speed of one centimeter per uSec. Connect the vertical input to the pen light pulse output. When the tip of the pen is positioned over the trace a 1uSec pulse should appear about 300nSec to the right of the pen. Increasing the sensitivity should reduce the delay.

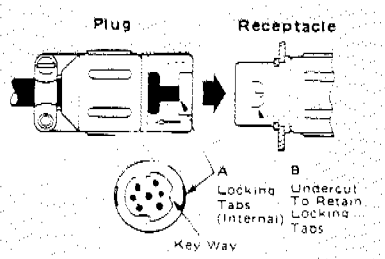
Light Pen Removal/Replacement.



Don't Turn or Twist.
Don't use Hand Tools.

1. Squeeze finger grips to flex plastic coupling area. The locking tabs will deflect outward and unlock.
2. Pull plug from receptacle.

Figure 1 - Removal.



1. Turn plug so "keyed" insulator faces align.
2. Push plug onto receptacle until locking tabs (A) snap into undercuts (B).

Figure 2 - Replacement.

7.4 Lightpen Removal and Replacement

The light pen connector is mated to the connector on the Graphics monitor front panel via a locking type connector.

7.4.1 Removal.

The connector cannot be unmated until the sides of the plug are squeezed (Figure 1).

7.4.2 Replacement.

Connection is made by pushing the plug, on the light pen spiral cord, onto the connector on the Graphics Monitor front panel until the locking tabs snap into the locked positon (Figure 2).

8. VDU03 POWER SUPPLY UNIT

8.1 General Description

The power supply unit is located behind the front panel Light Pen cut-out. The unit consists of the power transformer, voltage selector switches and the regulated DC power supply card VDU03. The unit provides 24V and 12V for the Main Card VDU01 and 5V for the Light Pen.

A multi-tapped primary power transformer is used. It has low magnetic leakage to prevent picture tube interference. The secondary output is connected via 3 pin connector to the Power Supply Card.

8.2 Circuit Description.

The bridge rectifier DB1 and the filter capacitors C1 and C2 provide the DC supply for the IC regulators U1 and U2. U1 is the adjustable regulator used for the 24V DC. Its output is actually adjusted using VR1 to **23.1V** to accommodate variations in mains voltage in different countries. However it should only need readjusting if U1 or its associated components have been replaced.

DB1 also supplies DC to the 12V regulator U2. To reduce the power dissipation in the 12V regulator two 5.6V zener diodes are used in series. The 24V and 12V are connected to the VDU01 card via the 3 pin connector.

U2 also supplies 12V to the 5V regulator U3. U3 is used for the light pen supply and is connected via the 10 way connector where connections for the Light Pen's 'Hit' and 'Touch' signals are also made.

9. VDU01 MAIN CIRCUIT CARD FUNCTIONAL DESCRIPTION

Note: A reasonable knowledge of the technology involved and the dangers of working with high voltages is essential.

9.1 VIDEO/BLANKING

This is where the signal enters the VDU. The functions of this section are:

Video input
Video preamp
DC restoration
Mixed blanking

Two outputs, video and mixed blanking are supplied to the tube support card. There is an external contrast control. The necessary blanking signals are derived from both the horizontal and vertical circuitry.

9.1.1 Video input

Res:	VR1	500R	Contrast control
	R1	82R	
Cap:	C1	470 uF	25 V
Connect:	P3	10 way	Input and contrast

The signal appears on pin 2 of connector P3. First it is DC isolated by C1 and R1. It is then sent in two directions; one is to the sync separator which we will treat later. The other is to the contrast pot via pin 4 of P3. This divides the signal down to set the size of the luminance signal as desired. This signal then returns thru pin 6 of P3 to pass into the buffer stage.

It is rare to encounter problems at this stage.

9.1.2 Video preamp

Res:	R2	18k	R5	100R	
	R3	4k7	R6	470R	
	R4	100R	R14	47R	
Cap:	C2	4.7 uF 16 V	C5	100 uF	25 V
	C4	10 nF			
Tran:	Q1	BC549	Q2	BC559	

The preamp is simply a non-inverting stage with a gain of 6. The output at Q2's collector passes into the next stage via C3. The 12 volt supply to this is decoupled by R14, C4 and C5.

Problems in this stage usually affect the brightness or contrast.

9.1.3 DC restoration

Res:	R7	100k	R10	2k2
	R8	1k	R13	68R
	R9	10k	R15	68k
Cap:	C3	470 nF		
Tran:	Q3	BC559	Q4	BC549
Diode:	D1	BAW62	D5	BYV96E

This section removes non-luminance information from the video signal during horizontal retrace. The horizontal blanking signal is extracted from the horizontal flyback pulses by D5, R9, R10 and R15. Each pulse turns Q4 on, which clamps the video signal via D1.

The blanked video is then buffered by emitter follower Q3. R13 in series on the output corrects the impedance and protects the buffer. There is an optional link for selecting an external luminance signal (no sync). The selected signal passes to the tube support card via P4 pin 5. This section shares the same decoupled supply as the preceding video buffer.

Loss of blanking is apparent when extra horizontal lines appear on the screen in between the normal raster traces. These would be unaffected by the contrast control. It is also possible in this stage to lose luminance. Because Q3's bias is partially set by C3, an out-of-tolerance capacitor here could affect the black level of the picture.

9.1.4 Mixed blanking

Res:	R11	47k	R141	3k9
	R12	18k		
Diode:	D2	BAW62	D3	BAW62

This section provides a mixed blanking signal to the tube support card. The horizontal blanking signal extracted in the previous section is mixed with the treated vertical sync pulses taken from the vertical section. R11 and R12 also provide biasing for Q5 on the tube support card. The final mixed blanking signal passes to the tube support card via P4 pin 2.

9.2 HORIZONTAL SECTION

This section takes care of everything necessary for getting the horizontal trace working:

Sync amplifier
Horizontal oscillator
Decoupling/sync separation
Horizontal driver
Horizontal output
Feedback
Output conditioning
Dynamic focus

9.2.1 Sync amplifier

Res:	R25	560R	R29	3k3
	R26	3M3	R32	2M2
	R27	1M8	R36	33k
	R28	3k3	R76	3K3
Cap:	C12	4.7 nF	C57	470 nF
	C19	6.8 nF	C61	100 nF
	C56	100 pF		
Tran:	Q8	BC559		
Diode:	D13	1N914		

This section extracts both horizontal and vertical sync from the video signal. R25, R26, R27, C12, C61 and D13 form a network at the base of Q8. The effect of the RC time constants and the diode is to pass only negative going pulses of a certain duration (horizontal sync pulses). Vertical sync pulses appear as a rapid string of horizontal pulses.

Q8 forms a high gain inverter stage, and the output is divided down to TTL levels by R28 and R29. There is an optional link for selecting an external sync signal at this point. R76 provides some two-way protection for the external line.

Next is a conditioning network formed by R36, C19, C56 and C57, which further reduces unwanted video information. R32 pulls up the average DC level before the signal enters the horizontal combination IC via pin 9.

The resultant combined sync information should be reasonably clean. Any problems would affect the output of the horizontal combination IC, TDA2591 pin 3; if this shows very stable, clean pulses then there should be no problem with this section (assuming the timebase generation section has no problems).

9.2.2 Horizontal oscillator

Res:	R30	1k2		R34	82k
	R31	3k3		R35	120k
	R33	12k 2%			
	VR3	47k	Horizontal frequency adjust		
Cap:	C14	680 nF		C17	4.7 nF
	C15	22 uF	16 V	C18	100 nF
	C16	10 nF			

Most of this section is the network required by the horizontal combination IC for timebase generation and compensation. The base frequency is set by C18; quite often problems with stability or frequency adjustment can be solved by replacing this. VR3 enables adjustment either side of the base frequency and can also cause problems. The trimpots are ceramic and rough treatment can fracture them. Be warned - a fracture is not always visible.

The frequency and stability of the horizontal trace depend largely on the accuracy of this section; component value drift can cause problems.

9.2.3 Decoupling/sync separation

Res:	R39	12R		R40	10R
Cap:	C20	100 uF	25 V	C60	470 uF 25 V
Diode:	D12	1N4004			
IC:	U1	TDA 2591	Horizontal combination		

Due to the stability required of the horizontal oscillator, the 12 V supply is decoupled first by D12 and C60, and then separated by R39 and R40. R39 provides output power to pin 2 of the IC. R40 feeds pin 1 and also the input and timebase sections, and is further bypassed via C20. Instability of the horizontal timebase may be caused by too much noise on these supplies.

Further decoupling is provided by the separate ground connections to both timebase and output sections (pins 16 and 4). This IC also outputs vertical sync pulses via pin 8, which it separates from the combined sync fed to its input.

9.2.4 Horizontal driver

Res:	R38	220R	R43	68R 5W
	R41	120R	R46	220R
Cap:	C24	100 nF	C52	100 nF
	C25	1 nF	C53	47 uF
	C26	47 nF		
Tran:	Q9	BD131		
Xform:	TX2			

The output of the horizontal IC is fed thru R38, R46, C24 and C25 to Q9, which drives the primary of TX2. R41 and C26 are connected across TX2 to reduce ringing, and R43, C52 and C53 decouple the 24 V supply to this section.

9.2.5 Horizontal output

Res:	R44	1R 0.5W	R71	2R2 5W
	R45	68R		
Cap:	C27	1 nF	C33	1 uF
	C28	12 nF 1.5 kV	C54	100 nF
	C32	1 uF 400 V	C55	100 uF 40 V
Tran:	Q10	BU246		
Diode:	D6	BYW96E	D8	BY229/400
Xform:	TX1	Horizontal flyback transformer		

Here is what can be called the heart of the circuit, as so much depends on its proper operation. The horizontal flyback transformer drives not only the horizontal trace, but all the HT supplies, the EHT for the tube anode and the heater supply. It also does all this from a single 24 V supply.

Q10 is set up as a switch between ground and one end of TX1's primary. The other end of the primary is connected via D8 and C33 to a decoupled 24 V supply. When Q10 is turned on, current flows thru the primary via D8, setting up a magnetic field in TX1. When Q10 is turned off, this field collapses, and its energy appears in the form of a large voltage across the primary (better known as the "flyback" pulse).

This corresponds with the horizontal retrace on the screen. The flyback voltage is boosted by C33 due to the "lever action" of the primary around the "fulcrum" of D8. This is known as a "series efficiency diode circuit". Decoupling of the 24 V supply is provided by R71, C32, C54 and C55. R44 limits the base current of Q10 and prevents ringing. R45 and C27 provide bias and high frequency bypass, and D6 protects Q10 from reverse transients.

C28 forms an LC network with TX1's primary. The value of C28 has a large effect on the behaviour of the flyback waveform, and changes in value can vary the retrace time relative to the horizontal trace time. For example, a larger value would result in a longer horizontal trace.

Transformer faults such as internal cracks or winding problems can affect the stability of the trace, and create electrical and acoustic noise, e.g. " dirty hissing". Another sort of noise is the loud whistle which indicates a poor connection in the energy flow. This could be a dry joint, faulty winding, or fractured component.

Quite often a monitor that does absolutely nothing when turned on has a problem in this area. Also, what can seem to be a failed Q10 can turn out to be a dubious contact upsetting the flow of energy.

9.2.6 Feedback

Res:	R42	82k			
	VR4	47k	Horizontal phase adjust		
Cap:	C21	220 nF	C23	82 pF	630 V
	C22	270 pF			

This network derives a voltage from the horizontal flyback pulses to control the mark/space ratio of the horizontal timebase. This is adjusted by VR4 (horizontal phase) and fed to pin 6. The effect of this is to move the screen image horizontally on the raster (left and right).

Again, the ceramic trimpot used here can fracture and cause problems.

9.2.7 Output conditioning

Res:	R47	1k8	R48	1k8	
Cap:	C29	1 uF 400 V	C30	470 nF	400 V
Coil:	L1	Horizontal width			
	L2	Horizontal linearity			

This section conditions the horizontal drive to ensure linearity and width are correct. The two coils form an adjustable series LC with the capacitors and deflection coils, and the current waveform determines deflection behaviour. Only the linearity coil is adjustable; the width coil was found to work better without its tuning slug. Thus there may be small differences in the screen width of different monitors, but this has not been a problem.

Faint vertical stripes on a bright raster would indicate ringing around the coils, which can be caused by open or faulty damping resistors R47 and R48. Lack of picture can be caused by open circuits in this chain; this crashes the energy cycle of the flyback transformer which provides the important supplies.

9.2.8 Dynamic focus

Res:	R74	68R			
Cap:	C31	1 nF 1 kV	C59	1 nF	1 kV
Xform:	TX3	Dynamic focus			

Dynamic focus is necessary because of the wide angle of deflection (110 degrees). The beam path at the edge of the tube is much longer than the path at the centre. Focussing the whole horizontal trace would be a compromise without some means of compensating for the different path lengths. This is accomplished by adjusting the focus voltage according to the horizontal deflection.

TX3 supplies this adjustment signal; its primary is in series with the deflection coils. The signal appearing at the secondary is passed thru C31 and mixed with the fixed focus voltage thru R57. If this is not working, it will be impossible to focus adequately along the whole trace length.

9. VDU01 MAIN CIRCUIT CARD FUNCTIONAL DESCRIPTION (continued)

9.3. VERTICAL SECTION

Like the horizontal section, this provides everything necessary to maintain a sweep on the screen. It can be broken up into the following sections:

Sync conditioning
Vertical oscillator
Vertical IC decoupling
Output/feedback

9.3.1 Sync conditioning

Res:	R137	4k7
Cap:	C132	10 nF
Diode:	D108	BAW62

This network cleans up the sync from either the sync separator or the optional sync input, which is then fed to TDA 2653 pin 2.

9.3.2 Vertical oscillator

Res:	R139	39k		R150	18k
	R148	270R		R154	68k
	R149	220k			
	VR40	50k	Vertical frequency adjust		
Cap:	C133	100 uF		C139	470 nF
	C136	47 uF			

This network is required by the vertical combination IC to generate the vertical timebase. It can be separated into four smaller networks as follows:

Pin 1: VR40 in series with R139.

Pin 7: RC network (C133, R148) between 24 V and ground.

Pin 10: RC network (R149, R150, C136) between 24 V and gnd.

Pin 13: Parallel RC (R154, C139) to ground.

The problems common to this area are similar to those of the horizontal timebase network. The stability of the trace depends on these networks operating correctly; faults may also affect linearity or size.

9.3.3 Vertical IC decoupling

Res:	R146	6R8 1W		
Cap:	C134	1000 uF	C143	1000 uF
	C135	100 nF		
Diode:	D110	BYV96E		
IC:	U2	TDA 2653A	Vertical combination	

For stable operation, this section needs good decoupling. C135 and C143 bypass the supply to pin 9 for the timebase. The output driver supply to pin 5 is decoupled by R146, C134 and D110. Ground is connected to pin 8. Longterm stability problems can start here, e.g. intermittent flicker or jumping.

9.3.4 Output/feedback

Res:	R73	270R	R157	120R
	R143	39k	R158	18k
	R144	68k	R159	820R
	R145	3k3	R161	22k
	R151	22k	R162	1R5
	R152	2M7	R163	1R5
	R153	1M5	R164	5R6 1W
	R155	4k7		
Cap:	C137	100 nF	C141	1000 uF
	C138	100 nF	C142	100 nF
	C140	2.2 uF		
Diode:	D111	BAW62		

This mass of circuitry provides the feedback and adjustment for linearity and level. The output is driven directly from the IC (hence the heatsink) via pin 6. The return current flows thru C141 and then R162 and R163 which act as current sense resistors. R73 provides damping for the deflection coils, and the RC network of R164 and C142 provides further output "tuning".

Voltage feedback is taken from the coil return thru R161 and R158 with a series RC to ground (C140, R159). Current feedback is taken from R162 and R163 via R157 and trimpot VR56, providing vertical amplitude adjustment. These two feedback signals are mixed by R155 and R158 at pin 4 of the IC. This combined feedback also feeds R143, R145, pin 3 and VR47 (vertical linearity). It then passes thru the network consisting of R144, C138, C137, R151, D111, R152 and R153 to finally enter pin 11 of the IC.

Faultfinding in this area is difficult. Probably the best way to remove suspicion is to check all components for faults or changes in value. The main feedback paths should also be looked at for obvious faults. Further than this, another monitor should be used to compare signals.

9.4 HT AND EHT VOLTAGES

These voltages are generated by the horizontal flyback transformer to supply the tube.

Cathode/brightness supplies
Focus/G2 supply
EHT tripler supply
Tube heater supply

9.4.1 Cathode/brightness supplies

Res:	R51	1k		R53	2M2
	R52	1M			
	VR8	1M	Brightness adjustment		
Cap:	C34	10 uF 350 V		C58	2.2 uF 160 V
Diode:	D9	BYV96E		D11	BY584

The winding between pins 3 and 5 supplies +85 V, rectified by D9 and C58. This is used to supply both the cathode circuit on the tube support card (P5 pin 5) and one leg of the brightness control (via R52).

The winding between pins 6 and 7 provides two supplies; the focus/G2 supply (described in the next section), and -155 V, rectified by R51, D11 and C34. This connects via R53 to the other leg of the brightness control. The connections to this control pass thru P1 as follows:

Pin 4	+85 V
Pin 5	Adjustment voltage return
Pin 6	-155 V

The voltage returned is then sent to the tube support card via P5 pin 4. C34 on the negative supply is deliberately large to prevent spot burn, by maintaining bias on the grid after switch-off.

Overvoltage is possible, and can be dangerous, especially if component ratings are exceeded (capacitors do explode if provoked). This section should always be checked in a repair or test situation.

9.4.2 Focus/G2 supply

Res:	R50	1k8	R57 1M8
	R54	1M5	High voltage type (blue)
	R56	1M5	High voltage type (blue)
	VR9	2M7	Focus adjustment pot
Cap:	C35	10 nF	1.6 kV
Diode:	D10	BY584	

This is a +800 V supply derived from the winding between pins 6 and 7, rectified by R50 and D10. The G2 +400 V supply is divided down by special high voltage resistors R54 and R56, passing to the tube support card via P5 pin 7. The focus adjust pot is connected directly across the +800 V supply. The static focus voltage is mixed thru R57 with the dynamic focus signal at C31, the composite then passing to the tube support card via P5 pin 9.

This section can be lethal due to the high voltages present. It should be checked (carefully) to avoid the possibility of dangerous overvoltage.

It is essential that high voltage resistors be used for R54 and R56; normal resistors are likely to fail within a year or two. This will cause the screen to either go blank or to full brightness, depending on which resistor fails.

9.4.3 EHT tripler supply

Diode: Internal stack in horizontal xformer

This is hermetically sealed within the transformer. A special high insulation cable takes the voltage out to a point on the back of the tube. The return end of the winding is grounded thru pin 13. The voltage developed is approx 17 kV, which for obvious reasons should be treated with great care.

If any part of this connection is exposed to air, the voltage will start to "bleed off" which sounds like white noise or hissing. The sharp edges of the transformer may also do this if too close enough to another component. Usually the smell of ozone appears as well.

```
**********************************************************
**                                                      **
**  WARNING - DO NOT ATTEMPT THE FOLLOWING PROCEDURE    **
**  IF YOU ARE NOT EXPERIENCED IN DEALING WITH E.H.T.    **
**  VOLTAGES (17 kV).                                   **
**                                                      **
**********************************************************
```

To discharge and disconnect the lead from the back of the tube, follow these instructions strictly:

1. Disconnect video signal from monitor. This prevents spikes propagating into the CMI and crashing the system.

2. Turn mains power off at the switch. It is important to leave the power lead connected to ensure chassis grounding. Otherwise the energy liberated by discharging can cause the chassis to float up to a dangerous voltage. Make sure the mains is actually off though.

3. Discharge the EHT to the chassis. This can be done by connecting a clip lead between the chassis and a screwdriver, and inserting the tip of the screwdriver under the plastic cap which protects the tube connection. Obviously use a long enough screwdriver with a well insulated handle for safety. The voltage will spark over as the tip is brought near; it should then be touched to the connector to completely discharge it.

4. While the screwdriver tip is in this position, the connector can be "unhooked" by applying pressure to push the hook clear of the lip which forms the tube connection.

5. It is now possible to remove the lead, holding it by the back of the protective plastic cap and disengaging it from the rear of the tube. However, avoid touching either of the exposed parts of the connection as residual charge may still be present.

6. When reconnecting the EHT lead to the tube, avoid touching either contact as residual charge may still be present. Ensure that the "hook" is properly engaged and the connection is firm. Sometimes this involves a bit of force; perhaps using a screwdriver to push the hook back under the lip would make this easier.

9.4.4 Tube heater supply

Res: R49 10R 5W

The winding between pins 1 and 2 is a 6.3 V floating heater supply, and passes to the tube support card via P5 pins 2 and 3. R49 limits the current.

To check the operation of the heater, look for the glow towards the back of the tube neck.

10. VDU02 TUBE SUPPORT CARD FUNCTIONAL DESCRIPTION

This combines the video and blanking signals and provides an output stage to drive the cathode. It also supplies and limits the necessary voltages to the rear of the tube:

Video output/blanking
Supplies/signals
Overvoltage spark gap

It also has a black level adjustment.

10.1 Video output/blanking

Res:	R18	680R	R22	470R
	R19	56R	R72	39R
	R20	1k2 5W		
	VR2	1k	Black level adjustment	
Cap:	C51	270 uF		
Tran:	Q5	BC549	Q7	BSX20
	Q6	BF337		

A 7.5 V reference is supplied to the base of Q6. Q6's emitter therefore can set the current flowing through the cathode chain: R19, R20, R72, Q6, Q7 and C51. R20 varies the voltage on the cathode as this current varies, thus changing the beam current.

Three things can influence Q6's emitter: VR2 sets the no-signal beam current i.e. black level. The mixed blanking signal turns Q5 on which shuts down Q6, cutting off the beam current. Video signals turn Q7 on, saturating Q6 and increasing beam current. This circuit mixes the three signals and provides output drive. R22 provides some current limiting.

The flying ground lead which clips into the chassis ground lead can cause problems if not soldered properly at the board. A dry joint can create a fuzzy or jittery picture.

10. VDU02 TUBE SUPPORT CARD FUNCTIONAL DESCRIPTION (continued)

10.2 Supplies/signals

Res:	R17	680R	R24	220k
	R21	47R	R33	22k
Cap:	C6	10 nF	C9	100 nF
	C7	22 nF	C10	100 nF 400V
	C8	22 uF	C11	10 nF 1kV
Diode:	D4	7.5 V Zener		

This section covers six areas:

12 V supply to Q5, decoupled by C6.

7.5 V ref. to Q6, generated from 12 V by R17, D4 and C7.

85 V supply to cathode chain, decoupled by R21, C8 and C9.

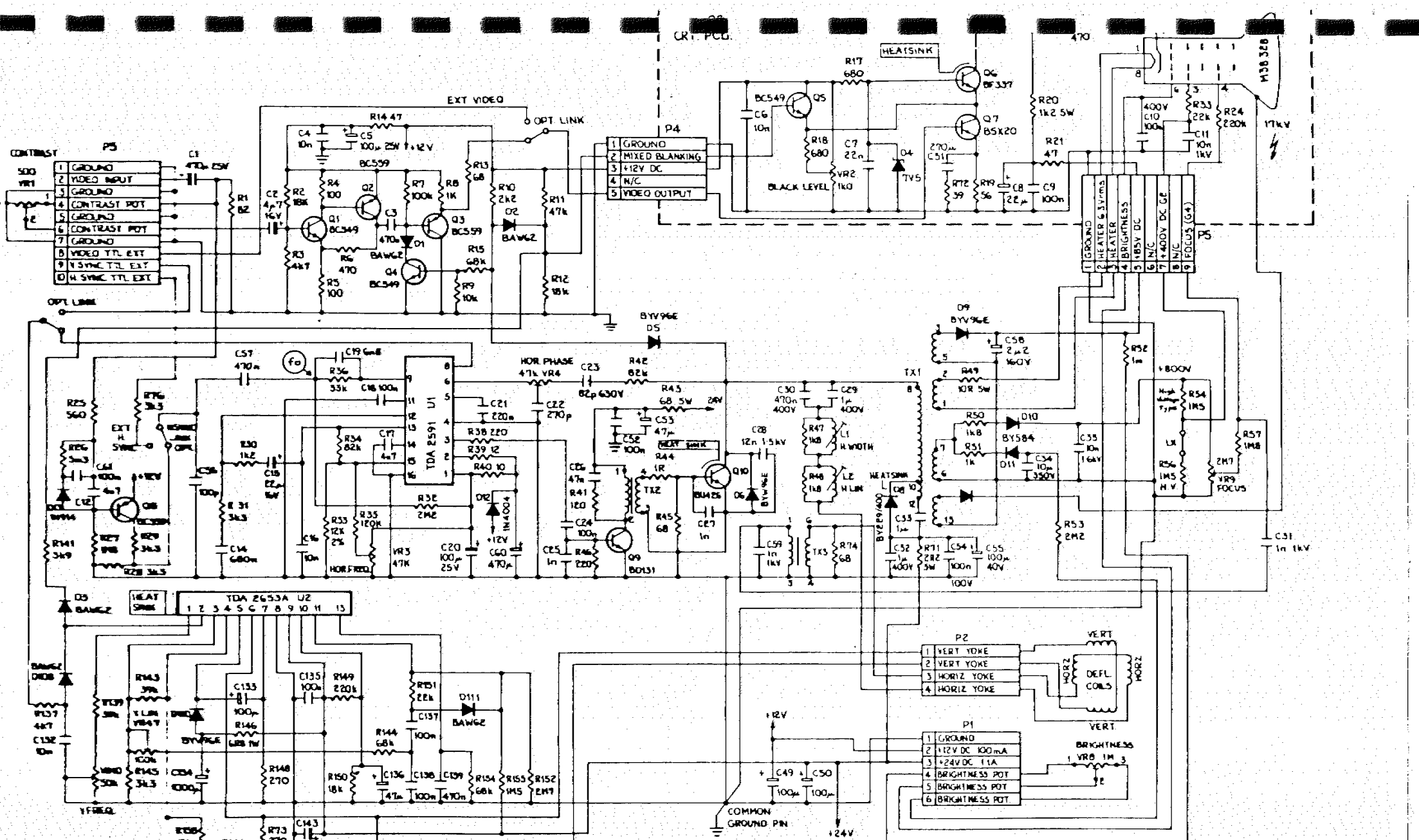
Brightness control voltage, bypassed by C10.

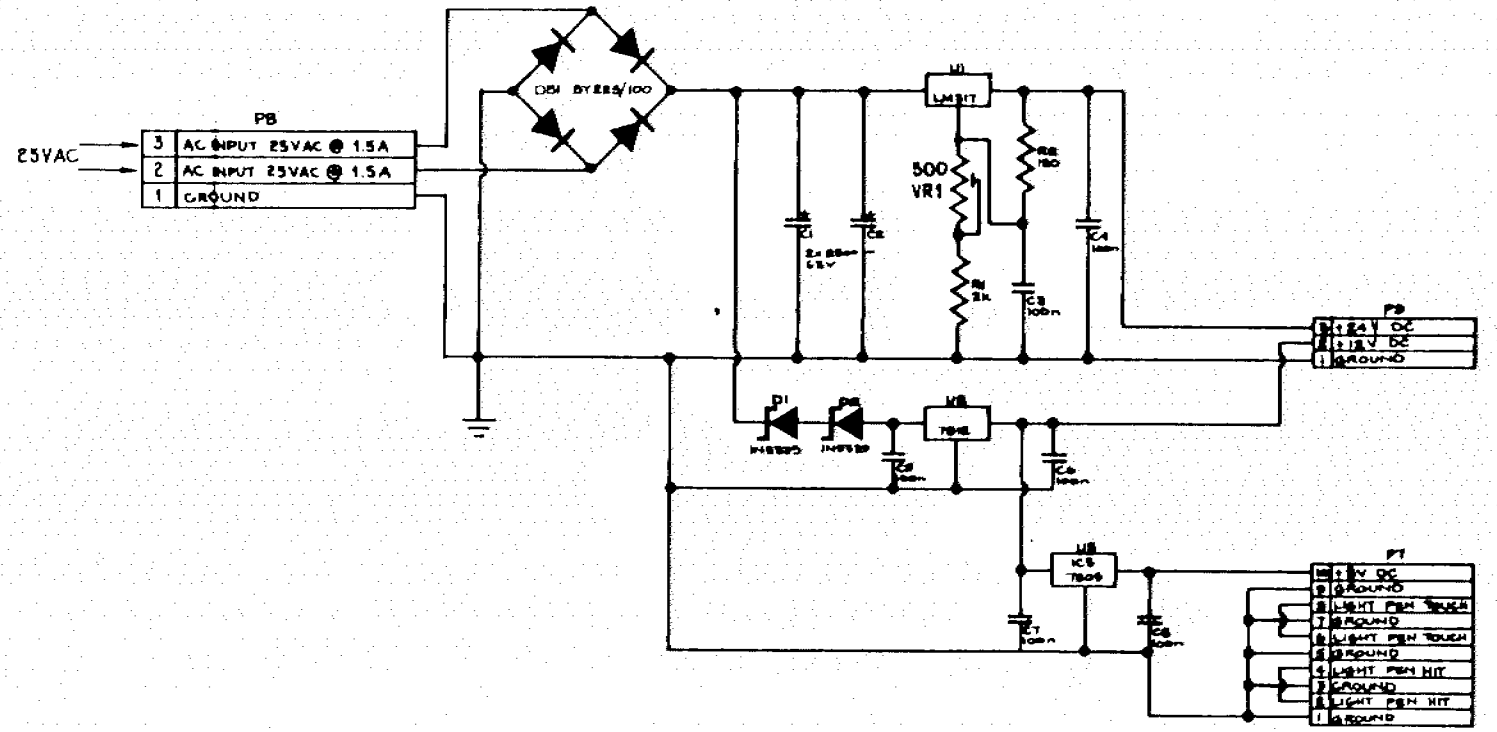
400 V (G2) supply via R33 and C11.

Focus voltage via R24.

10.3 Overvoltage spark gap

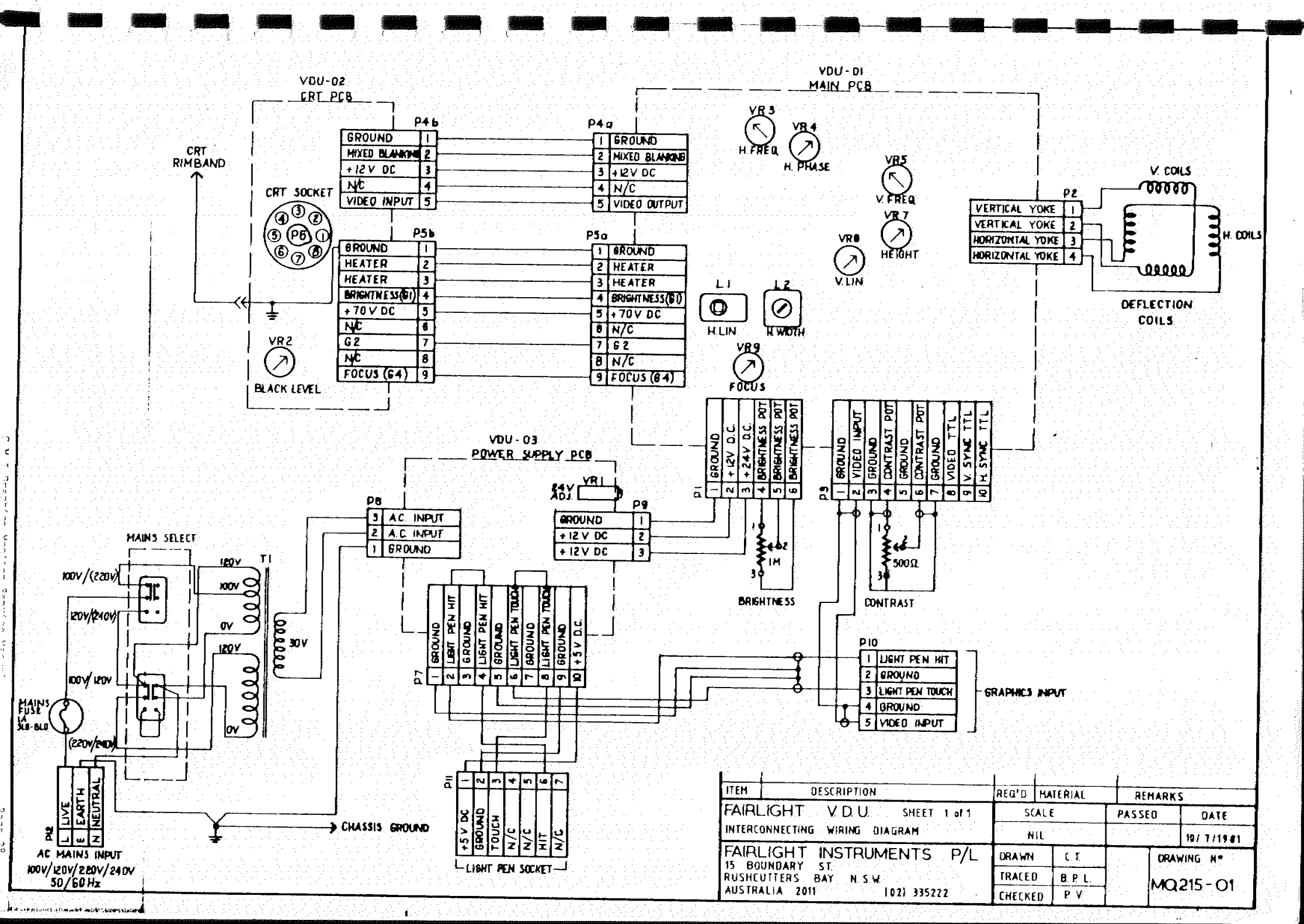
Incorporated into the board layout is a ground ring around the inside of all the tube connections. If any voltage goes dangerously high, the excess energy will arc over and be dissipated.


CRT PCB
P5
P4
P2
P1
TDA 2591 U1
TDA 2653A U2
TX1
TX2
TX3
EXT VIDEO
OPT LINK
HEATSINK
BLACK LEVEL
HOR PHASE
COMMON GROUND PIN
+12V
+24V
+800V
VERT
HORZ
DEFL COILS
BRIGHTNESS
FOCUS
110° GRAPHICS MONITOR
VDU-01-01
4/12/84
E.H.
REV 5
SHEET 1 of 1



POWER SUPPLY CARD VDU03

ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
POWER SUPPLY CARD VDU03		SCALE ——	PASSED ——	DATE 14/7/81
SHEET 1 of 1		DRAWN JL.		DRAWING NUMBER VDU 03-01
FAIRLIGHT INSTRUMENTS 15 BOUNDARY St RUSHCUTTERS BAY NSW AUSTRALIA 2011		TRACED		
		CHECKED C.T.		



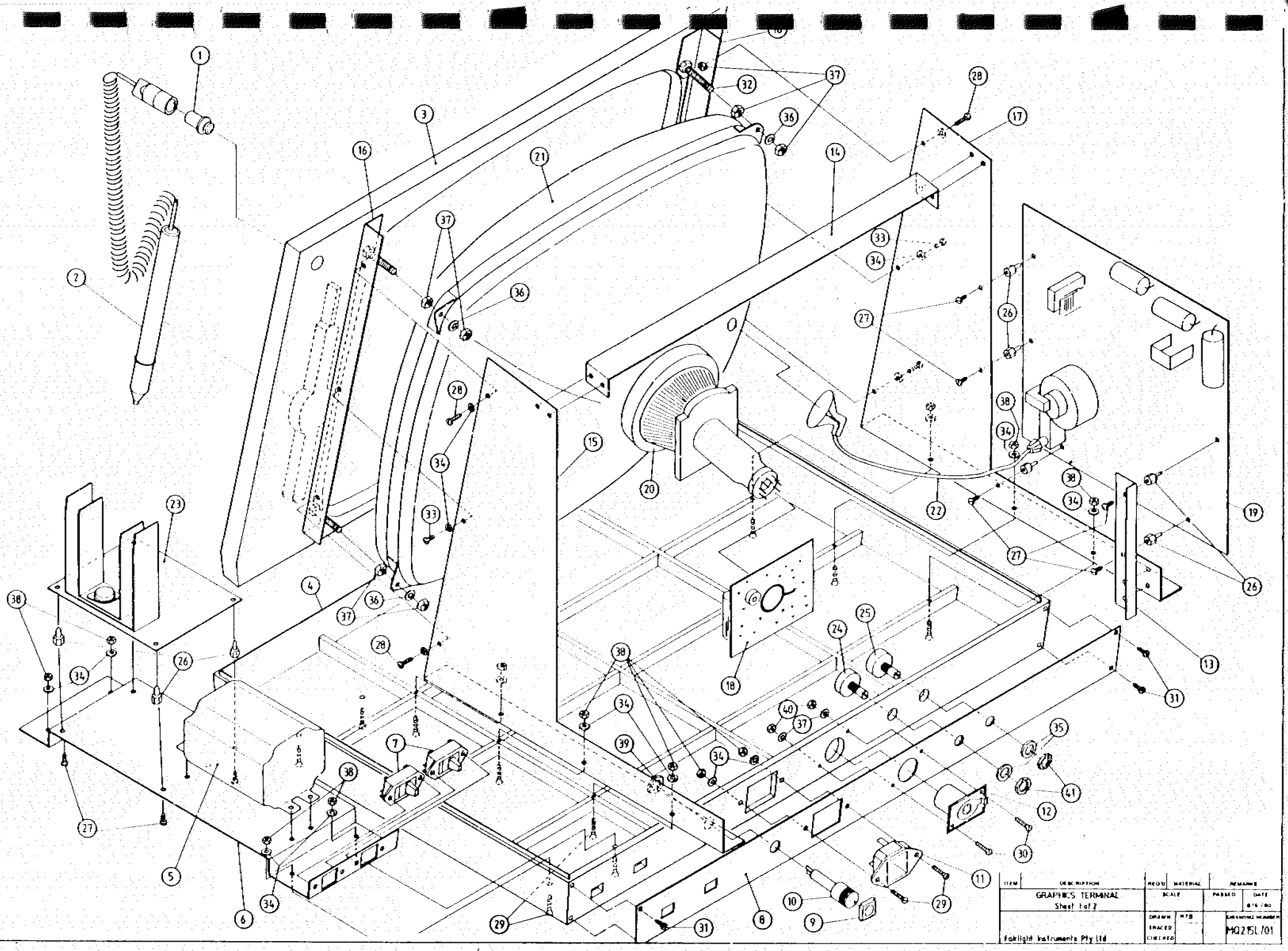
ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS

FAIRLIGHT V.D.U. SHEET 1 of 1
INTERCONNECTING WIRING DIAGRAM

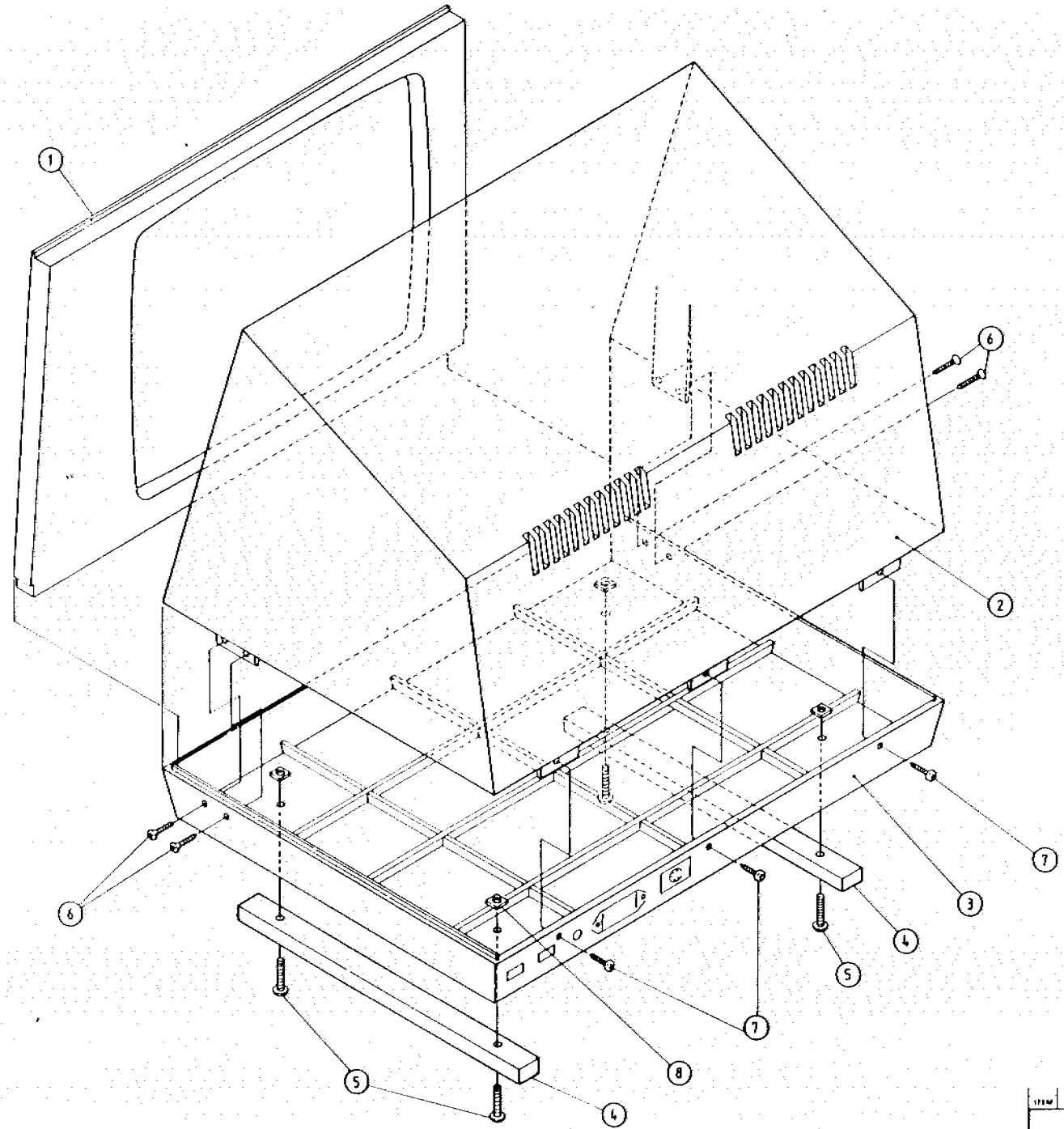
SCALE	PASSED	DATE
NIL		10/7/1981

FAIRLIGHT INSTRUMENTS P/L
15 BOUNDARY ST.
RUSHCUTTERS BAY N.S.W.
AUSTRALIA 2011 (02) 335222

		DRAWING N°
DRAWN	C.T.	MQ215-01
TRACED	B.P.L.	
CHECKED	P.V.	



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	GRAPHICS TERMINAL Sheet 1 of 2	SCALE	PASSED	DATE
		DRAWN MTB		DRAWING NUMBER
	Foxlight Instruments Pty Ltd	TRACED		MG215L/01
		CHECKED		



ITEM	DESCRIPTION	REQ'D	MATERIAL	REMARKS
	GRAPHICS TERMINAL Sheet 2 of 2	SCALE NIL		PASSED DATE 8/10/80
	Fairlight Instruments Pty Ltd	DRAWN MTB TRACED CHECKED CT		DRAWING NUMBER MQ215L/02

14. MECHANICAL PARTS LIST

14.1 PARTS LIST FOR DRAWING MQ215L/01

Ref No.	Part No.	Description.
1	G5152	Light Pen Socket
2	G5151	Light Pen
3	J0209	Front Panel Assy.
4	J0208	Base Panel
5	G5191	Power Transformer
6	G0073	Power Supply Base Plate
7	G5159	Voltage Selector Switch
8	J0040	Rear Panel Escutcheon
9	G5190	Fuse Holder Cap
10	G5309	Fuse Holder
11	D6768	Power Connector 3 pin
12	D6710	Graphics Connector 5 pin
13	G0128	P.C.B. Bracket
14	G0127	Support strip
15	G0124	Support Panel LH
16	G0126	Support bracket
17	G0125	Support Panel RH
18	MVDU02	CRT Card VDU02
19	MVDU01	Main Card VDU01
20	G5184	Deflection Yoke
21	G5198	Picture Tube 15"
22	G6017	eht cable
23	MVDU03	P.S.U. Card VDU03
24	R6111	Contrast Pot
25	R6110	Brightness Pot
26	G5107	P.C.B. Standoff
27	H0125	Screw 6Gx1/4"
28	H0102	Screw CHD4BAx"
29	H0111	Screw CKS 4BAx15/16"
30	H0118	Screw CKS6BAx3/8"
31	H0115	Screw 4Gx3/8"
32	H0140	Stud 1/4"W
33	H0133	Screw CHD 4BAx1/4"
34	H0008	Washer 4BA star
35	H0021	Washer Pot
36	H0139	Washer 1/4"W Star
37	H0012	Washer 6BA Star
38	H0202	Nut 4BA Hex
39	H0208	Nut Fuseholder
40	H0201	Nut 6BA Hex
41	H0020	Nut Pot

14. MECHANICAL PARTS LIST (continued)

14.2 PARTS LIST FOR DRAWING MQ215L/02

Ref.No.	Part No.	Description.
1	J0209	Front Panel
2	J0271	Top Cover
3	J0208	Base Panel
4	J0006	Foot
5	H0132	Screw 1/4"x1"
6	H0103	Screw 8Gx3/4" CHD
8	H0209	Nut