Goldstar FC200 service manual

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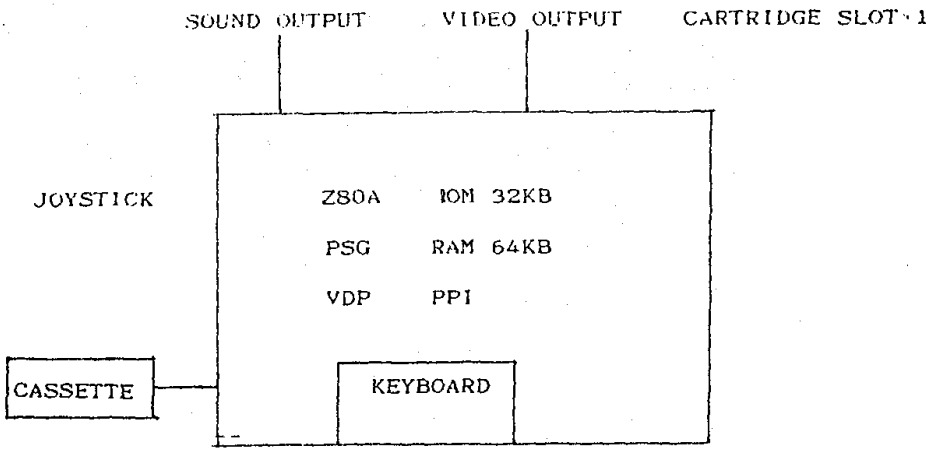
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1. 1 General Specification

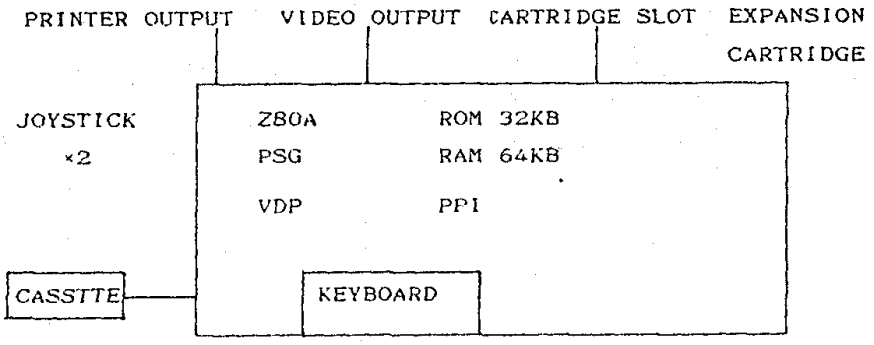
°CPU	*Z-80A or Equivalence*
°MEMORY	ROM 32KB(MSX BASIC)
	RAM 64KB
°CRT DISPLAY	TEXT MODE 40chr×24line
	GRAPHIC MODE 256×192dots
	COLOR 16color
°CMT	FSK METHOD
	1200/2400 baud rate
°SOUND FUNCTION	8 octave,3 tones output
°KEYBOARD	Alphanumeric,graphic symbol
	code symbols
°FLOPPY DISK	5¼" supporting(MSX-DOS formatting)
	3½ "
°PRINTER	8 bit parallel(Centronics)
°ROM Cartridge	I/O bus
	Game cartridge,expansion bus cartridge
°Joystick	1 or 2

1. 2 SYSTEM CONFIGURATION

°MINIMUM



° SOFTWARE SUPPORT AREA



*The number of the slot is maxinum 16 containing system

2. 1 LSI SPEC.

°CPU	Z80A or equivalence
	CLOCK 3.579545MHZ
	1 WAIT SIGNAL is inserted after each M1 cycle.
°VDP	TMS9129NL
°PSG	AY-3-8910
°PPI	INTEL-8255A

2. 2 MEMORY

° ROM　　MSX BASIC INTERPRETER　32KB

° RAM　　USER RAM :64KB

VIDEO RAM:16KB

* There is 4 basic slot in system,and the system can access 256KB ROM,RAM.And it can have maximum 1M byte memory area.

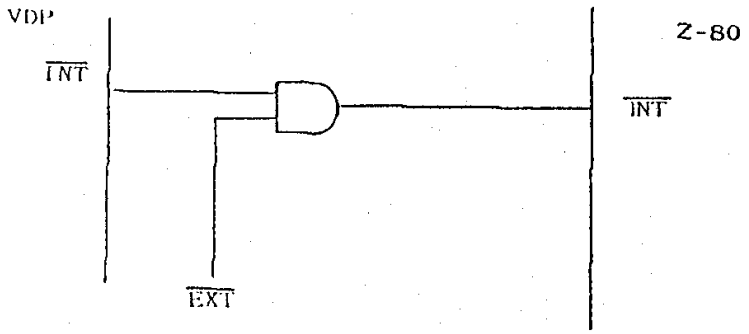
* Basic ROM exists form 0000H to 7FFFFH,and RAM exists from FFFFH to lower address.Refer to Chapter 4. for details.

2. 3 INTERRUPT

* $\overline{NMI}$---Not use,MSX BASIC has RAM HOOK.

* $\overline{INT}$--- VDP or cartridge bus can input external interrupt signal.VDP inputs interrupt signl to CPU on every 1/50 sec, then CPU restarts from 0038H.

°INTERRUPT CIRCUIT EXAMPLE.



2. 4 DISPLAY MODE

* LSI TMS9129NL

* Character:alphanumeric·graphic symbols (8×8 dots)

*Color :16 colors

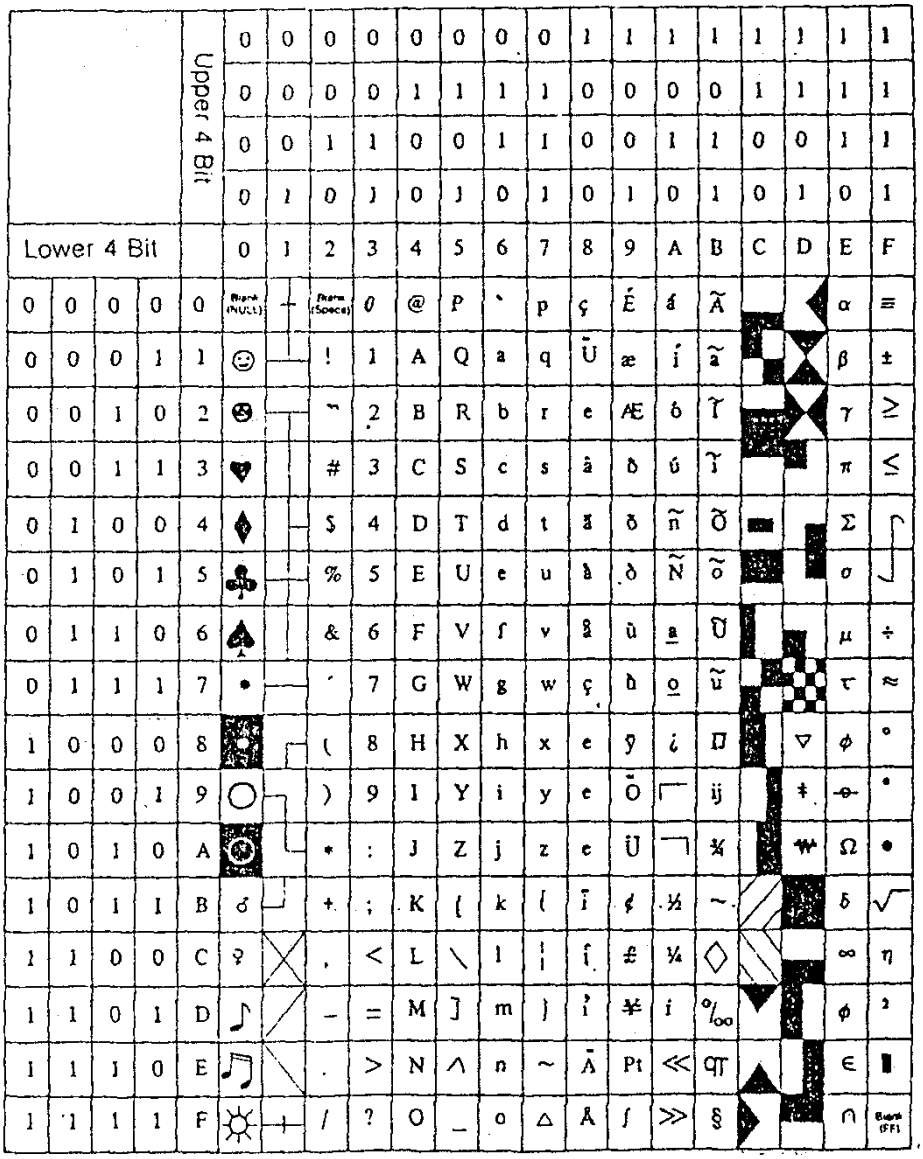
* Sprite :possible

* Display mode table

MODE	RESOLUTION	SIZE	NO	COLOR	SPRITE	DIPLAY
GRAPHIC 1	240×192	8×8	256	16	0	29×24
GRAPHIC 2	240×192	8×8	768	16	0	29×24
MULTICOLOR	64×48blk	4×4	-	16	0	29×24
TEXT	240×192	8×6	256	2of16	×	39×24

* NO: THE NUMBER OF PATTERN

2. 5 DISPLAY CHARACTER CODE



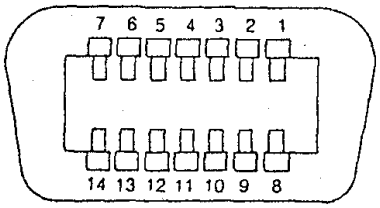
Upper 4 Bit	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Lower 4 Bit	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0 0	Blank (NULL)	─	Blank (Space)	0	@	P	`	p	ç	É	á	Ã			α	≡
0 0 0 1 1	☺	─	!	1	A	Q	a	q	Ü	æ	í	ã			β	±
0 0 1 0 2	☹	─	"	2	B	R	b	r	e	Æ	ó	Ỹ			γ	≥
0 0 1 1 3	♥		#	3	C	S	c	s	â	ð	ú	ỹ			π	≤
0 1 0 0 4	♦	─	$	4	D	T	d	t	ä	ð	ñ	Õ			Σ	⌠
0 1 0 1 5	♣	─	%	5	E	U	e	u	à	ð	Ñ	õ			σ	⌡
0 1 1 0 6	♠		&	6	F	V	f	v	å	ù	ª	Ũ			μ	÷
0 1 1 1 7	•	─	'	7	G	W	g	w	ç	ð	º	ũ			τ	≈
1 0 0 0 8	◘	┌	(	8	H	X	h	x	e	ÿ	¿	Ð		▽	φ	°
1 0 0 1 9	○	└	)	9	I	Y	i	y	e	Õ	⌐	ij		‡	Θ	∙
1 0 1 0 A	◙	┘	*	:	J	Z	j	z	e	Ü	¬	¼		Ψ	Ω	•
1 0 1 1 B	♂	┐	+	;	K	[	k	{	ĩ	¢	½	~			δ	√
1 1 0 0 C	♀	┼	,	<	L	\	l	¦	î	£	¼	◇			∞	η
1 1 0 1 D	♪	╱	-	=	M	]	m	}	ì	¥	i	‰			φ	²
1 1 1 0 E	♫	╲	.	>	N	^	n	~	Ã	Pt	≪	¶			∈	■
1 1 1 1 F	☼	┼	/	?	O	_	o	△	Å	ſ	≫	§			∩	Blank (FF)

2. 9 PRINTER INTERFACE

* STANDARD : 8 bit parallel.
* LEVEL : TTL
* CONNECTOR : AMPHENOL 14 PIN
* SIGNAL TABLE

TERMINAL NO	SIGNAL
1	PSTB
2	PDB0
3	PDB1
4	PDB2
5	PDB3
6	PDB4
7	PDB5
8	PDB6
9	PDB7
10	NC
11	BUSY
12	NC
13	NC
14	GND

PIN CONNECTION

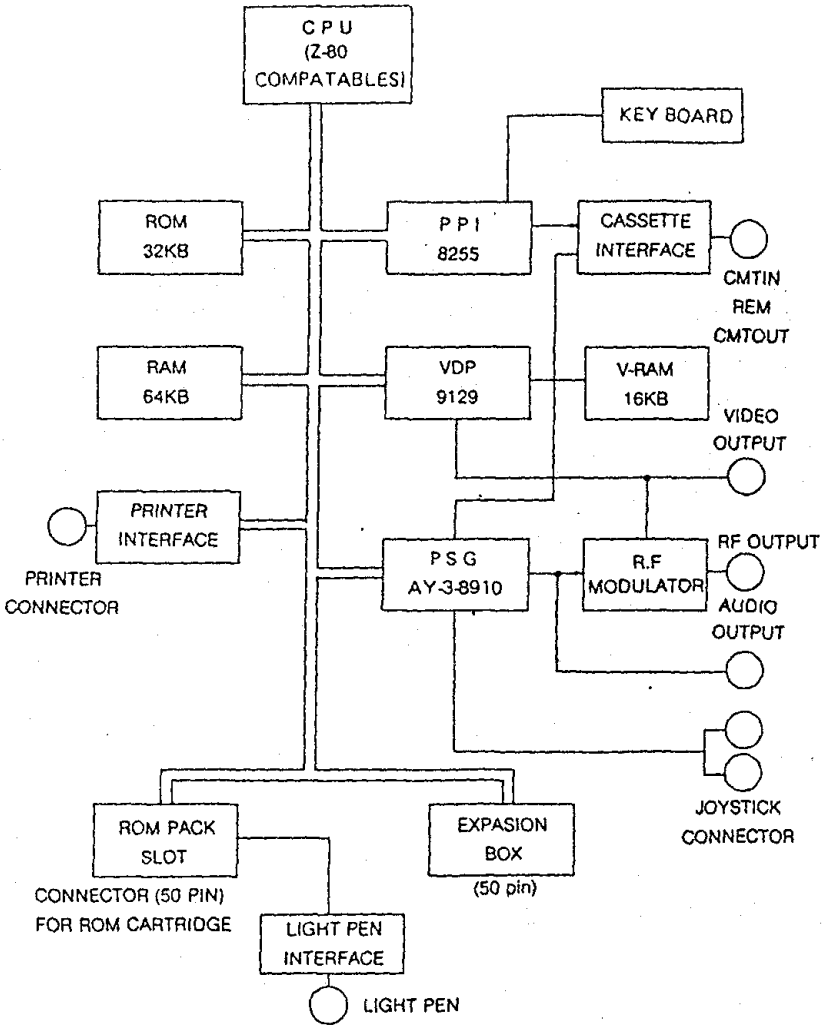


pin arrangement toward the system

2. 10 THE LIST OF CONNECTOR

TERMINAL NAME	SPEC/STANDARD
VIDEO OUTPUT	
COMPOSITE SIGNAL OUTPUT	RCA 2 PIN CONNECTOR
RF SIGNAL	RCA 2 PIN CONNECTOR
CASSETTE	DIN 8 PIN CONNECTOR
GENERAL I/O PORT	AMP 9 PIN CONNECTOR
PRINTER	AMPHENOL 14 PIN CONNECTOR
CARTRIDGE BUS	2.54 PITCH,50 PIN CONNECTOR
AUDIO OUTPUT	RCA 2 PIN CONNECTOR

3. 1 BLOCK DIAGRAM



3.2 CARTRIDGE BUS SIGNAL

NO.	SIGNAL NAME	I/O	NO.	SIGNAL NAME	I/O
1	CS1(N)	O	2	CS2(N)	O
3	CS12(N)	O	4	SLTSL(N)	O
5	Reserved *1	-	6	RFSH(N)	O
7	WAIT(N) *2	I	8	INT(N) *2	I
9	M1(N)	O	10	BUSDIR	I
11	IORQ(N)	O	12	MERQ(N)	O
13	WR(N)	O	14	RD(N)	O
15	RESET(N)	O	16	COMP. VIDEO	O
17	A9	O	18	A15	O
19	A11	O	20	A10	O
21	A7	O	22	A6	O
23	A12	O	24	A8	O
25	A14	O	26	A13	O
27	A1	O	28	A0	O
29	A3	O	30	A2	O
31	A5	O	32	A4	O
33	D1	I/O	34	D0	I/O
35	D3	I/O	36	D2	I/O
37	D5	I/O	38	D4	I/O
39	D7	I/O	40	D6	I/O
41	GND	-	42	CLOCK(3.58MHz)	O
43	GND	-	44	SW1	-
45	+5V	-	46	SW2	-
47	+5V	-	48	+12V	-
49	SUNDIN	I	50	-12V	-

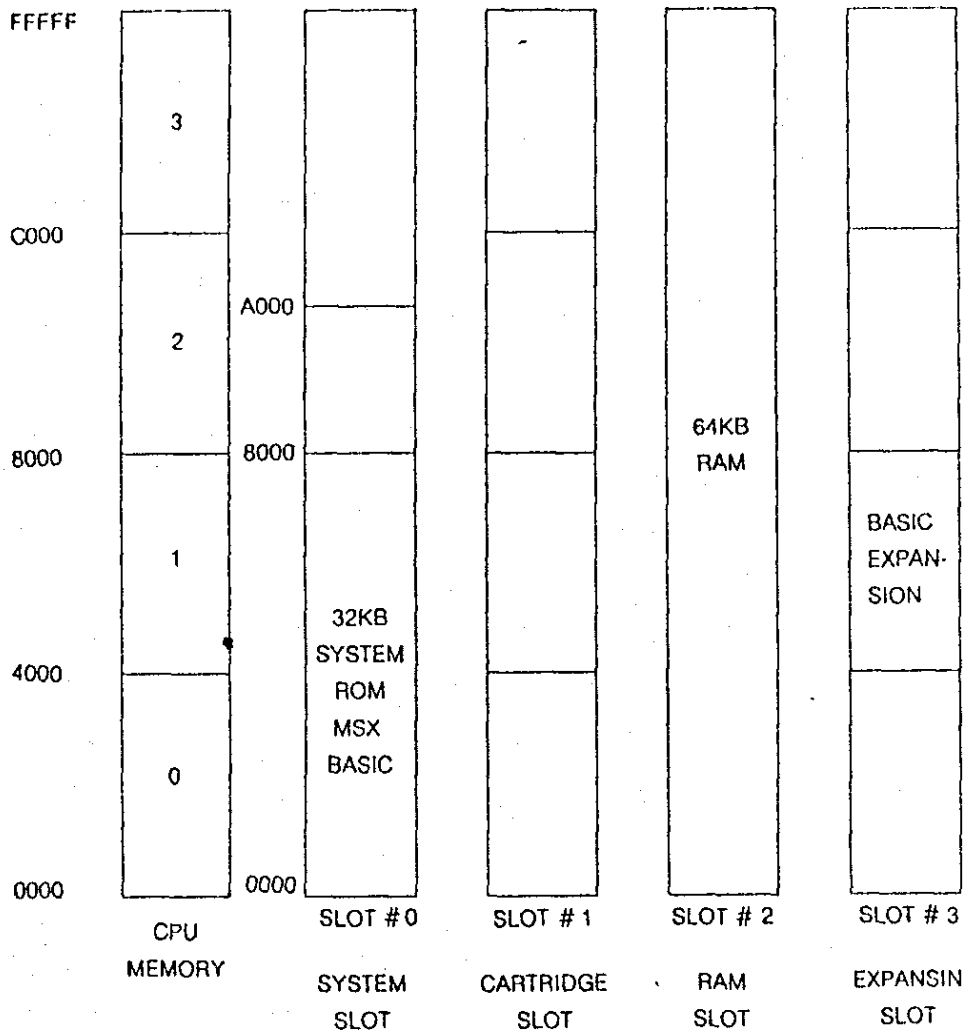
*1 :"Reserved" means that this pin is prohibited to be u
*2 : open collector state

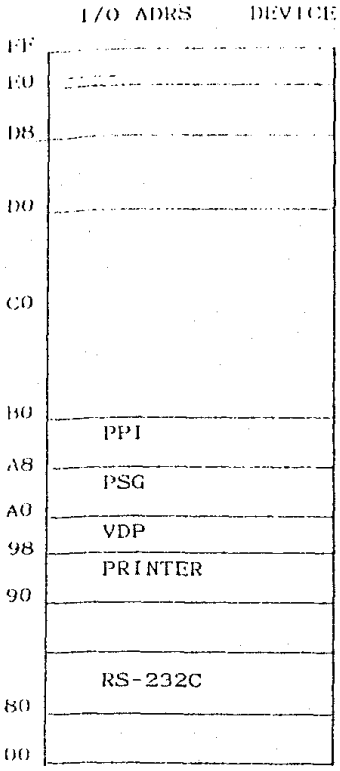
3.3 CARTRIDGE BUS SIGNAL FUNCTION

NO.	SIGNAL NAME	CONTENTS
1	CS1(N)	ROM 4000H~7FFFH ADDR. SELECTION SIGNAL
2	CS2(N)	ROM 8000H~BFFFH ADDR. SELECTION SIGNAL
3	CS12(N)	ROM 4000H~BFFFH ADDR. SELECTION SIGNAL
4	SLTSL(N)	SLOT SELECTION SIGNAL EACH SLOT
5	Reserved	
6	RFSH(N)	REFRESH CYCLE SIGNAL
7	WAIT(N)	WAIT REQUEST SIGNAL TO CPU
8	INT(N)	INTERRUPT REQUEST SIGNAL TO CPU
9	M1(N)	MACHINE LANGUAGE FETCH CYCLE
10	BUSDIR	DATA BUS DIRECTION SIGNAL
11	IORQ(N)	INPUT/OUTPUT REQUEST SIGNAL
12	MERQ(N)	MEMORY REQUEST SIGNAL
13	WR(N)	WRITE CYCLE SIGNAL
14	RD(N)	READ CYCLE SIGNAL
15	RESET(N)	CPU RESET SIGNAL
16	COMP. VIDEO	COMPOSITE VIDEO SIGNAL
17-32	A0~A15	ADDRESS BUS SIGNAL
33-40	D0~D7	DATA BUS SIGNAL
41,43	GND	SIGNAL GROUND
42	CLOCK	CPU CLOCK:3.58MHz
44,46	SW1, SW2	FOR SYSTEM, PROTECTION & AUTO RESET
45,47	+5V	+5V POWER
48	+12V	+12V POWER
49	SUNDIN	EXTERNAL SOUND INPUT(-5dbm)
50	-12V	-12V POWER

4. 1 MEMORY MAP

▼ The following diagram is the memory map.





IO ADR	RW	CONTENT	INDEX
&H98	W	VRAM DATA WRITE	9129
	R	VRAM DATA READ	
&H99	W	COMMAND,ADDRESS SET	
	R	STATUS READ	
&HA0	W	ADDRESS LATCH	AY-3-8910
&HA1	W	DATA WRITE	
&HA2	R	DATA READ	
&HA8	W	PORT-A DATA WRITE	8255a
	R	READ	
&HA9	W	PORT-B DATA WRITE	
	R	read	
&HAA	W	PORT-C DATA WRITE	
	R	READ	
&HAB	W	MODE SET	
&H90	W	STROBE OUTPUT(b0)	LATCH OUT
	R	STATUS INPUT(b1)	BUSY '1'
&H91	W	PRINT DATA	LATCH OUT

4.3 PPI BIT ASSIGNMENT

PORT	BIT	I/O	NAME	FUNCTION
A	0 1	O	CS0L CS0H	SLOT 1 FOR 0000-3FFF
	2	O	CS1L	SLOT ID FOR 4000-7FFF
	3	O	CS1H	
	4	O	CS2L	SLOT ID FOR 8000-BFFF
	5		CS2H	
	6	O	CS3L	SLOT ID FOR C000-FFFF
	7		CS3H	
B	0-7	I		KEYBOARD RETURN
C	0	O	KB0	KEYSCAN OUTPUT
	1		KB1	
	2		KB2	
	3		KB3	
	4	O	CASON	CASSETTE MOTOR ON(L=ON)
	5	O	CASW	CASSETTE WRITE SIGNAL
	6	O	CAPS	DRIVES CAPS INDICATER
	7	O	SOUND	ONE BIT OUTPUT FOR EXTRA SOUND OUTPUT

4.4 PSG BIT ASSIGNMENT

PORT	BIT	I/O	CONNECTOR		JOYSTICK
A	0	I	J3 1	*1	FWD1
			J4 1	*2	FWD2
	1	I	J3 2	*1	BACK1
			J4 2	*2	BACK2
	2	I	J3-3	*1	LEFT1
		I	J4-3	*2	LEFT2
	3	I	J3 4	*1	RIGHT1
			J4-4	*2	RIGHT2
	4	I	J3 6	*1	TRGA1
			J4-6	*2	TRGA2
	5	I	J3-7	*1	TRGB1
			J4-7	*2	TRGB2
	6	I	KEY MATRIX SELECTOR		
	7	I	CSAR (CASSETTE READ SIGNAL)		
B	0	O	J3-6	*3	
	1		J3-7	*3	
	2		J4-6	*3	
	3		J4-7	*3	
	4		J3-8		
	5		J4-8		
	6		PORT-A INPUT SELECT		
	7				

*1 VALID ONLY WHILE PORT-B/BIT-6 IS L

*2 VALID ONLY WHILE PORT-B/BIT-6 IS H

*3 SET H IF NOT USED AS AN OUTPUT.OPEN CLLECTOR OUTPUT.

*OTHER PINS ON J3,J4

J3-5,J4-5 +5V

J3-9,J4-9 GND

*4 is not supplied in the minimum configuration.

5.1 RAM EXPANSION

MSX BASIC requires a continous area in memory from FFFF to the lower memory area.Expansion RAM should be located just under the existing RAM to make a continuous area available to BASIC.

When the minimum memory system configuration contains 8k RAM from E000-FFFF,memory must still be incremented by 16k as the SLOT SELECT SIGNAL works on a 16k unit basis.In this case the original 8k of RAM are not used and the expansion of results in a total of 16k memory not 24k.

There are two kinds of 16k RAM cartridges available.One is for the 8k RAM minimum system and the other for those machine which comes with 16k RAM.While both cartridges contain 16k of RAM they must not be confused with one another and care must be taken that they are installed properly.

Computers with 8k RAM to start with use 16k RAM from FFFF to C000.

Computers with 16k RAM to start with use 16k RAM Expansion Cartridges with RAM from BFFF to 8000.

MSX BASIC OCCUPIES THE RAM from 8000 to FFF and cannot use RAM from 0000 to 7FFF.

5. 2 SLOT EXPANSION

The four slots which come with the minimum system are called , the BASIC SLOTS and from each of these BASIC SLOTS other slots can be added to expand the system.To select an expanded slot, the BASIC SLOT to which is belong must first be selected.

This is not necessary in systems in which there is a function which can inhibit the BASIC SLOT.

Up to four slots can be connected to each BASIC SLOT without using a buffer.Five or more slots can be connected using the buffer for the cartridge bus.

Since the CPU cannot distinguish whether a cartridge is before or after the buffer,a circuit which accepts a signal from the cartridge to distinguish the derection of the buffer is installed.The signal from the cartridge is called BUSDIR. In some cases,however,this signal is not necessary and the cartridge circuit can be simplified using:

In some cases,however,this signal is not necessary and the cartridge circuit can be simplified using:

(1) A cartridge which accepts but never sends data to the CPU.IN this case the buffer always works outward and never inward.

(2) A memory cartridge.
In this case,the bus dorection can be distinguished from the signals available(Slot Select,Memory Request,Read,Write)

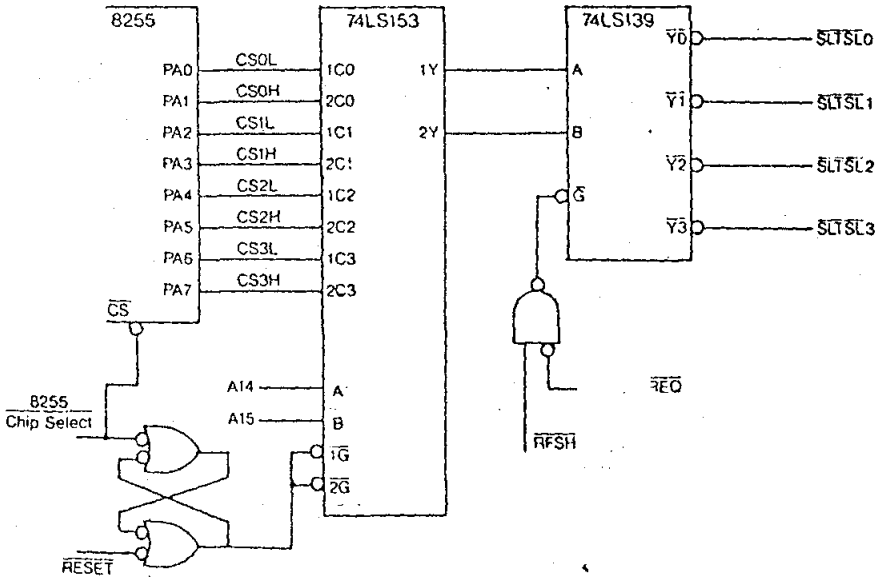
Thus ROM cartridges can be made inexpensively.

5. 3 SLOT

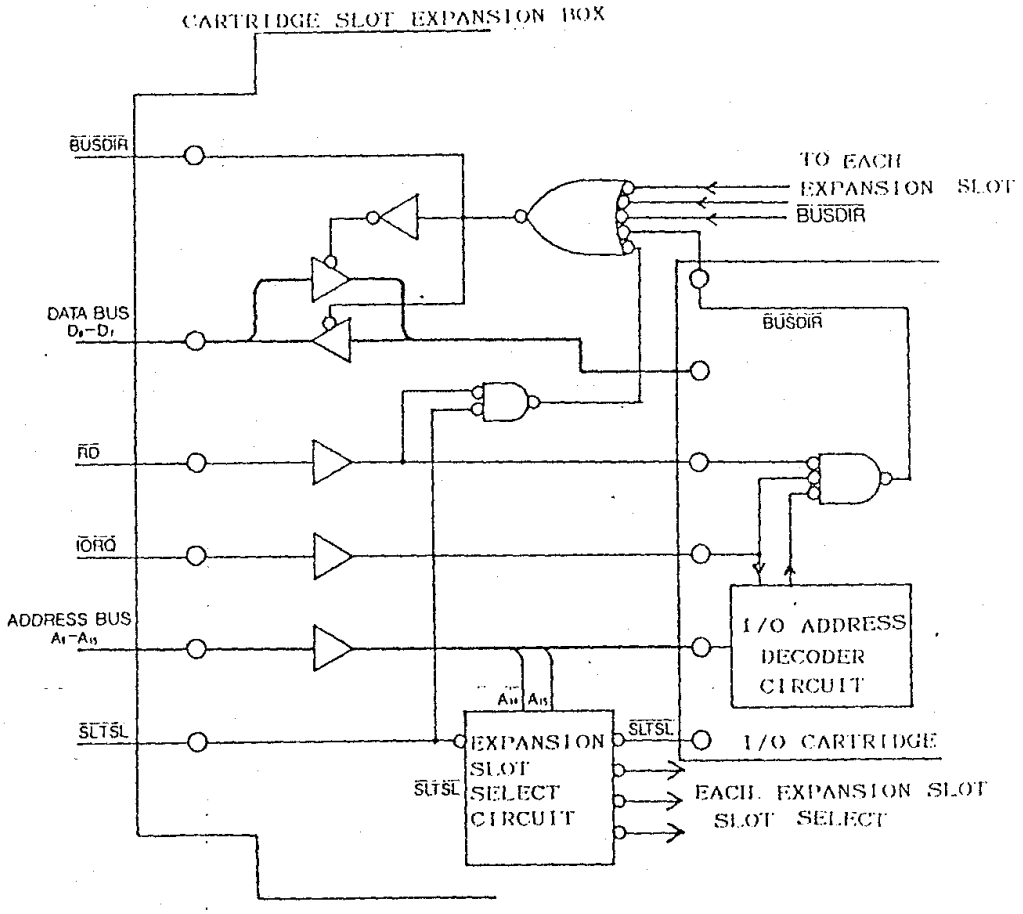
WHAT IS A "SLOT"?

The word "slot" is used here with a special meaning.It does not refer to the cartridge connector slot familiar to Apple 2 users.Slot here is somewhat similar to a memory bank because it is a block of 64k of memory.It is also similar to a "hardware slot" because the CPU names each slot and selects a slot on the cartridge bus is called the "Slot Select Signal".

Note that we are discussing the slot from the point of view of software and the number of physical cartridge slots will be discussed in another section.



5.4 EXPANSION SLOT CIRCUIT EXAMPLE



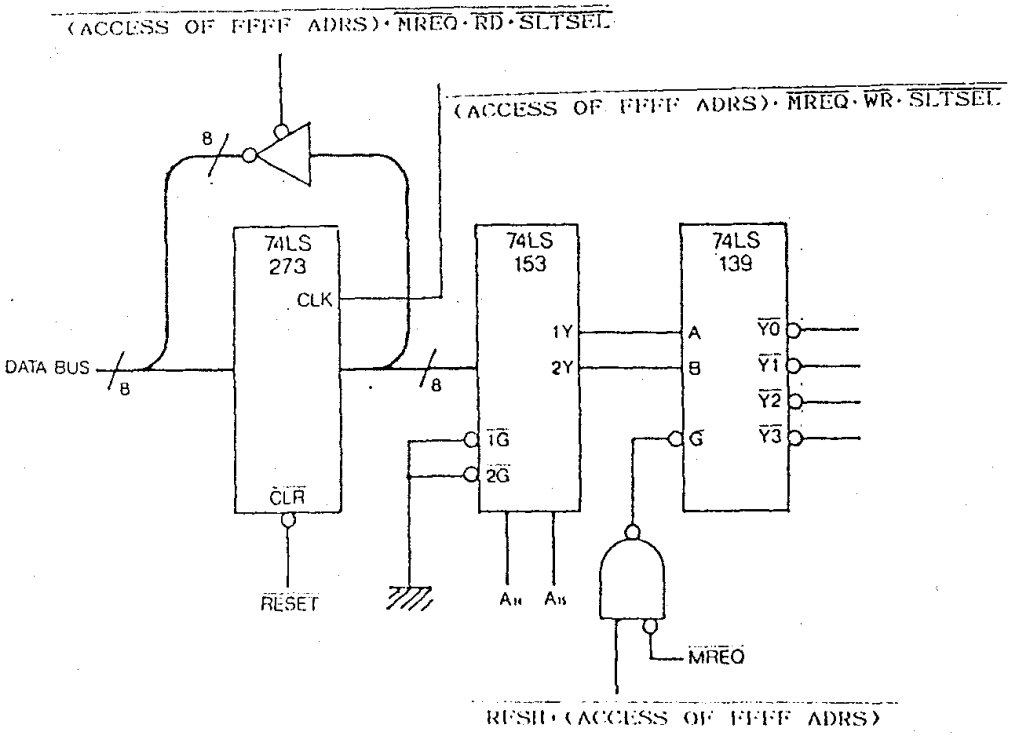
WHY USE SLOTS ?

On a system with an ordinary bank memory setup,every device in the same memory area receives the same select signals. This makes it impossible to put two or more devices on the same operation or even damages it.

Using slots makes it possible to put several edvices in the same address but in different slots.It also makes it possible to put programs in the same area.

As a result,the slot makes for a more flexible environment and adds more expandability to the system.

*** EXPANSION CARTRIDGE
SELECT SIGNAL CIRCUIT



6. 1. CPU-SLOT CIRCUIT

CPU(Z-80A) clock is derived from the video display processor TMS9129.
Using the TR Q3(2SC1815) in main reset circuit, turning the power switch on made negative pulse, set CPU and other processor resetted.
MSX system has four slots by the SLOT SELECTION method. Each slot consists of 64KB.

*SLOT #0 :MSX BASIC INTERPRETER ROM VERSION 32KB
*SLOT #1 :EXTERNAL CARTRIDGE SLOT
*SLOT #2 :MSX SYSTEM INTERNAL D-RAM 64KB
*SLOT #3 :EXTERNAL EXPANSION SLOT

Among the expansion and cartridge slot signals(50 pins), CPU address and control signals are connected through the HEX BUFFER(74LS367*4), but not the DATA BUS(D0-D7).

6. 2. SLOT SELECTION CIRCUIT

Slot selection set through PORT A of the P.P.I chip(INTEL 8255A) by the DATA BUS(D0-D7).
The PORT A in the P.P.I LSI is wired to 8-to-2 ENCODER (74LS153) by the 8-bit parallel line.
SLOT SELECTION is depending on the content of PORT A register in P.P.I
As example, if you want to select the SLOT #3(ADDRESS: 4000HEX-7FFFHEX), you should write a data(ACHEX) to the PORT A register in P.P.I.

CS3H	CS3L	CS2H	CS2L	CS1H	CS1L	CS0H	CS0L
1	0	1	0	1	1	0	0
		A				C	

If you input ACHex data to PORT A of P.P.I chip(INTEL 8255), it allows access of MSX BASIC INTERPRETER in SLOT #0, internal D-RAM in SLOT #2 and external cartridge ROM in SLOT #3. (for example, assembly language OUT PORTA, ACH is inserted)

6. 3. POWER ON RESET

As you turn on the power switch PROGRAM COUNTER's content is set to 0000H.
This register's content set to the system ROM through the address line(A0-A15) and PORT A register in P.P.I is set 00H.
8-bit parallel line of PORT A is connected to 8-to-2 ENCODER(74LS153) and CS0L bit,CS0H bit is selected by 8-to-2 ENCODER(74LS153).
This signal is wired to dual 2-to-4 DECODER(74LS139). In DECODER 1Y0(negative) signal is active,SLOT #0 is selected.
Therefore the content of 0000H address in MSX system ROM is read by the CPU.

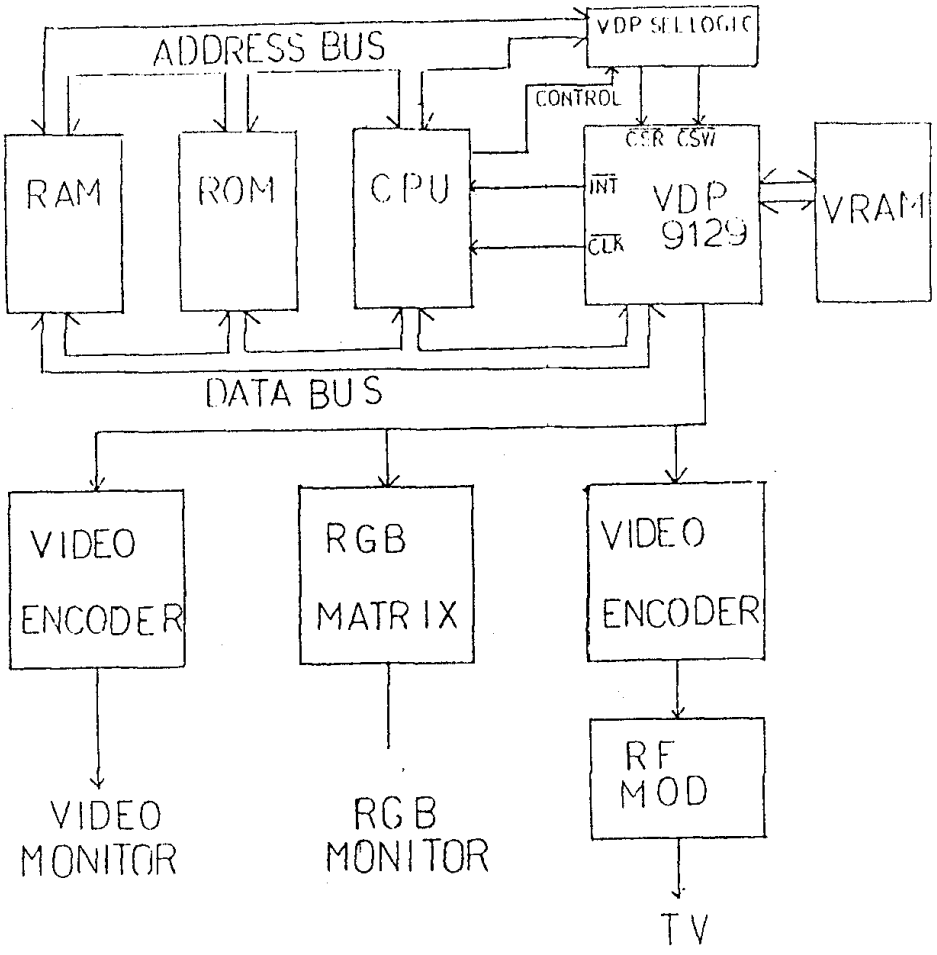
6. 4 VIDEO DISPLAY PROCESSOR: TMS9129NL

*V. D. P. SPECIFICATION

VDP IS DESIGNED TO INTERFACE DIRECTLY WITH THE TMS4416-15(16K*4BIT) D-RAM.
IT IS N-CHANNEL MOS LSI DEVICE USED IN VIDEO SYSTEMS WHERE DATA DISPLAY ON A RASTER-SCANNED HOME COLOR T.V OR COLOR MONITOR IS DESIRED.
THIS DEVICE GENERATES ALL NECESSARY VIDEO, CONTROL AND SYNCHRONIZATION SIGNALS AND ALSO CONTROLS THE STORAGE ,RETRIEVAL AND REFRESH OF DISPLAY DATA IN THE DYNAMIC SCREEN REFRESH MEMORY.
TMS9129NL HAS A 625 LINE FORMAT FOR USE WITH THE EUROPEAN PAL SYSTEM AND OPERATES ONLY IN A NONINTERLACED MODE.
THE VDP HAS FOUR VIDEO DISPLAY MODE

*TEXT MODE, GRAPHIC ONE MODE, GRAPHIC TWO MODE, MULTICOLOR

MODE	RESOLUTION	PATTERN SIZE	PATTERN NO.	COLOR	SPRITE	DISPLAY
GRAPHIC 1	192*256 PIXEL	8*8 DOT	256	16	OK	24LINE* 32 COL.
GRAPHIC 2	192*256 PIXEL	8*8 DOT	768	16	OK	24 LINE *32 COL.
MULTICOLOR	48*64 BLOCK	4*4 DOT	---	16	OK	24 LINE 32 COL.
TEXT	192*256 PIXEL	8*6 DOT	256	16	NO	24 LINE 40 COL.



BLOCK DIAGRAM
OF TMS9129

*V.D.P Interrupt
The VDP interrupt output pin is used to generate an interrupt at the end of each active-display scan, which is about every 1/50 second for the TMS9129. The interrupt output is active when the Interrupt Enable bit(IE) in the VDP register 1 is a "1" and the F bit of the status register is a "1". Interrupts are cleared when the status register is read.

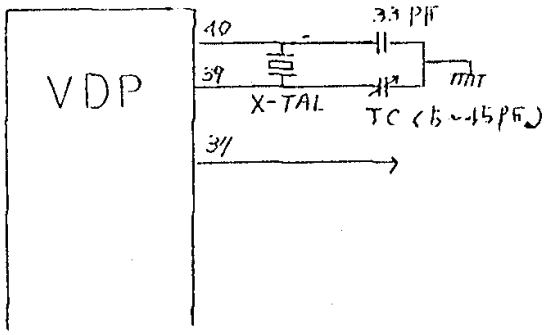
*CPU--VDP INTERFACE
The VDP communicates with the CPU via an 8-bit bidirectional data bus.
Three control lines, decoded from the CPU address and enable lines, determines interrpretation of the bus. Through the bus, CPU can write to V-RAM, read from V-RAM, write to VDP registers, and read the VDP status register. The VDP also generates interrupt signal after every refresh of the TV display if the interrupt is enabled.

*VDP-VRAM INTERFACE

The VDP can use either TMS4116-15(16k*1) or TMS4416-15/20 (16k*4) dynamic RAMs. AD(0) is used for the eighth RAM address bit in the TMS4416-15/20 RAMs, but not for the TMS4116.
Since the early write cycle is used by the VDP, G on the TMS4416 must be tied to ground.

The VDP accesses up to 16.384kbyte of VRAM using a 14-bit VRAM address. The VDP fetches data from the VRAM in order to process the video image.
The VDP also stores data in or read out data from the VRAM during a CPU-VRAM data transfer. The VDP automatically refreshes the VRAM.
THE VDP-VRAM INTERFACE CONSISTS OF A BIDIRECTIONAL 8-BIT DATA BUS AND THREE CONTROL LINES(RAS, CAS, R/W).
THE VDP READS FROM AND WRITES DATA TO THE V-RAM ON THE VRAM DATA BUS. THE VDP OUTPUTS THE ADDRESS TO THE VRAM OF THE VRAM ADDRESS BUS.
THE VRAM LOW ADDRESS IS OUTPUT WHEN RAS IS ACTIVE(LOW)
THE COLUMN ADDRESS IS OUTPUT WHEN CAS IS ACTIVE(LOW).
DATA IS OUTPUT TO THE VRAM WHEN R/W IS ACTIVE(LOW).

*CPU CLOCK GENERATION



The VDP generates CPU clock(3.58MHz).
A fundamental frequency, parallel-mode X-TAL is used as the frequency reference for the internal clock oscillatotr, which is the master time base for all system operations. This master clock is divided by two to generate the pixel clock(5.3MHz) and by three to provide the CPUCLK(3.58MHz).

*CPU INTERFACE
The VDP interface to the CPU using an 8-bit bidirectional data bus, three control lines, and an interrupt.

1. write data bytes to VRAM
2. read data bytes from VRAM
3. write to one of the 8-VDP write only registers
4. read the VDP status register

The type and direction of data transfers are control by the CSW, CSR, and mode inputs.
CSW is the CPU to VDP write select.
When it is active(low), the 8 bits on CD0-CD7 are strobed into the VDP.
CSR is the CPU from VDP read select.
When it is active(low), the VDP outputs 8 bits on CD0-CD7 to the CPU. CSW and CSR should never be simultaneously low at the same time. If both are low , the VDP outputs data on CD0-CD7 and latches invalid data.
Mode determines the source or destination of a read or wri data transfer. Mode is normally tied to a CPU low address, A0.

*CPU-VDP DATA TRANSFERS

OPERATION	DATA BIT 0	1	2	3	4	5	6	7	CSW	CSR	MODE
WRITE TO VDP REG.											
BYTE 1 DATA WRITE	D0	D1	D2	D3	D4	D5	D6	D7	0	1	1
BYTE 2 REG. SELECT	1	0	0	0	0	RS0	RS1	RS2	0	1	1
WRITE TO VRAM											
BYTE 1 ADDR. SETUP	A6	A7	A8	A9	A10	A11	A12	A13	0	1	1
BYTE 2 ADDR. SETUP	0	1	A0	A1	A2	A3	A4	A5	0	1	1
BYTE 3 DATA WRITE	D0	D1	D2	D3	D4	D5	D6	D7	0	1	0
READ FROM VDP REG.											
BYTE 1 DATA READ	D0	D1	D2	D3	D4	D5	D6	D7	1	0	1
READ FROM VRAM											
BYTE 1 ADDR. SETUP	A6	A7	A8	A9	A10	A11	A12	A13	0	1	1
BYTE 2 ADDR. SETUP	0	1	A0	A1	A2	A3	A4	A5	0	1	1
BYTE 3 DATA READ	D0	D1	D2	D3	D4	D5	D6	D7	1	0	0

6.5 PROGRAMMABLE PERIPHERAL INTERFACE

"PPI"

8255A FUNCTIONAL DESCRIPTION

GENERAL

The 8255A is a programmable peripheral interface(PPI)device designed for usein microcomputer systems.Its function is that of a general purpose I/O component to interface peripheral equipment to themicrocomputer system bus.The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

DATA BUS BUFFER

This 3-state bidirectional 8-bit is used to interface the 8255A to the system data bus.Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU.Control words and status information are also transferred through the data bus buffer.

Read/Write and Control logic.

The function of this block is to manage all of th internal and external transfers of both data and control or status words.It accepts inputs from the CPU Address and control busses and in turn,issues commands to both of the control groups.

($\overline{CS}$)

Chip select.A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

READ.A "low"on this input pin enables the 8255A to send the data or statusinformation to the CPU on the data bus.In essence,it allows the CPu to "read from the 8255A

($\overline{WR}$)

WRITE.A "low" on this input pin enables the CPU to write data or control words into the 8255A/

(A0 and A1)

Port select 0 and port select 1.these input signals,in conjunction with the RD and WR inputs,control the selection of one of the three ports or the control word registers.They are normally connected to the least significant bits of the address bus(A0 and A1)

8255A BASIC OPERATION

A1	A0	RD	WR	CS	INPUT OPERATION(READ)
0	0	0	1	0	PORT A DATA BUS
0	1	0	1	0	PORT B DATA BUS
1	0	0	1	0	PORT C DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS--PORT A
0	1	1	0	0	DATA BUS--PORT B
1	0	1	0	0	DATA BUS-- PORT C
1	1	1	0	0	DATA BUS--CONTROL
					DISABLE FNCTION
×	×	×	×	1	DATA BUS--3 STATE
1	1	0	1	0	ILLEGAL CONDITON
×	×	1	1	0	DATA BUS--3 STATE

(RESET)

Reset.A "high on this input clears the control register and all ports(A,B,C) are set to the input mode.

Group A and Group B controls

The functional configuration of each port is programmed by the systems software.In essence,the CPU "outuputs" a control word to the 8255A.The control word contains information such as "mode","bit set","bit reset".etc, that initialize the functional configuration of the 8255A.

Each of th Control blocks(Group A dnd Group B) accepts "commands" from the internal data bus and issues the proper commands to its associated ports.

Control Group A-Port A and Port C upper(C7-C4)

Control Group B-Port B and Port C lower(C3-C0)

The Control Word Register can only be writteen into.No read operation of the congfol word register is allowed.

Ports A,B,and C

The 8255A contains three 8-bit ports(A,B, and C).All can

be configured in swide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A.One 8-bit data output latch/buffer and one 8-bit data input latch.
Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input).This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

8255A OPERATIONAL DESCRIPTION.

MODE SELECTION

There are three basic modes of operation that cab be selected by the system software:

Mode 0-Basic Input/Output
Mode 1-Strobed Input /Output
Mode 2-Bi-Directional bus

When the reset input goes "high" all ports will be set to the input mode(i.e., all 24 lines will be in the high impedence state).After the reset is removed the 8255A can remain in the input mode with no additional initialization required.During the execution of the system program any of the other modes may be selected using a single output instruction.This allows a single 8255A to service a variety of peripheral devices with asimple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions.All of the output registers,including the status flip-flops,will be reset whenever the mode is changed.Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure.For instance ;Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results,Group A could be programmed in mode 1

to monitor a keyboard or tape reader on an interrupt driven basis.The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple,logical I/O approach will surface.The design of the 8255A has taken into account things such as efficient PC layout and complete functional flexibility to support almost any peripheral device with no external logic.Such design represents the maximum use of the available pins.

PSG(Progammable Sound Generator)

FEATURES

•Full software control of sound gener
•Interfaces to most 8 bit microprocessors,
•Three independently Programmed Analog Output
•Two 8-bit General purpose I/O Ports
•Single +5 volt supply

BASIC FUNCTIONS

DA7-DA0 (input/output/high impedance):
Data Address 7--0
These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG.IN the data mode,DA7-DA0 correspond to Register Array bits B7--B0.In the address mode ,DA3--DA0 select the register number ($0--17_8$) and a DA7--DA4 in conjunction with address inputs A9 and A8 for the high order address(chip select)

$\overline{\text{RESET}}$(input)
For initialization/power-on purposes,applying a logic "0"(ground) to the RESET pin will reset all registers to "0".The reset pin is provided with an on-chip pull-up resistor.

CLOCK(input)
This TTL-compatible input supplies the timing reference for the TONE,NOISE and ENVELOPE GENERATORS.

BDIR,BC2,BC1(input):
Bus Direction,Bus control 2,1

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE
0	1	1	READ FROM PSG
1	1	0	WRITE TO PSG
1	1	1	LATCH ADDRESS

ANALOG CHANNEL A,B,C(output)
Each of these signals is the output of its corresponding D/A converter. and complex sound waveshape generated by the PSG.

IOA7-IOA0(input output);IOB7-IOB0(input/output)
Input/Output A7-A0,B7-B0
Each of these two parallel input-output ports provides 8 bits of parall data to/from the PSG/CPU bus from/to any external devices

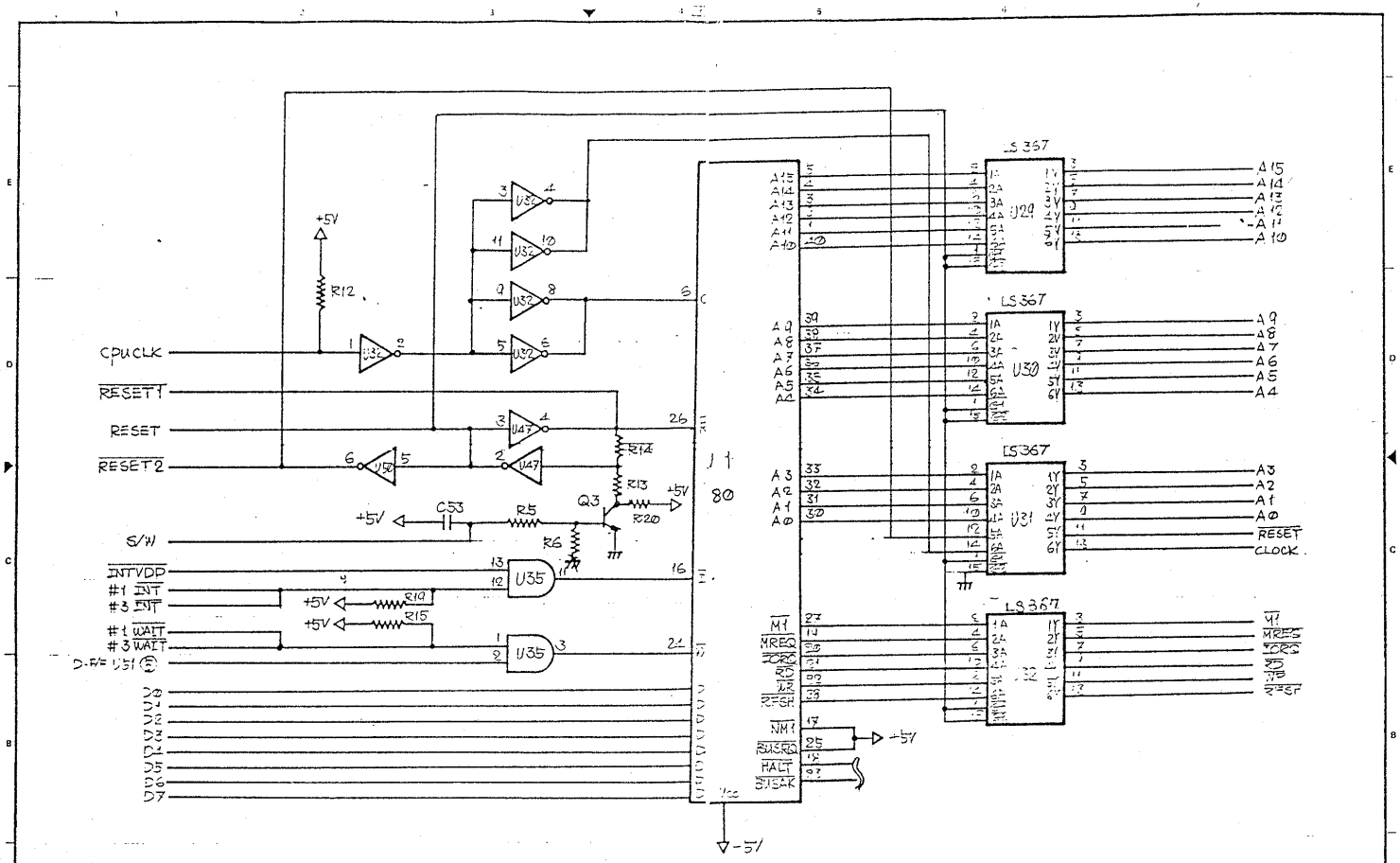
connected to the IOA or IOB pins.Each pin is provided with an on-chip pull-up resistor,so that when in the "input" mode,all pins will read normally high.Therefore,the recommended method for scanning external switches would be to ground the input bit.

FC-200 POWER PART LIST

C'CT NO.	DESCRIPTION & SPECIFICATION
IC1	IC, REGULATOR STR 9005
IC2	IC, REGULATOR SI-3122V
IC3	IC, REGULATOR GL-7912
D1	DIODE, BRIDGE RB-401
D2	DIODE, BRIDGE DBA 20B
D3	DIODE, RECTIFIER 1N4001
C1~C2	C, CE 4700MF 16V CE04
C5	C, CE 100MF 16V CE04
C6	C, CE 100MF 25V CE04
C3~C4	C, CE 1000MF 25V CE04
C7	C, CE 470MF 25V CE04
R1	R, CARBON FILM 4.7K-J 1/4W
J1~J4	WIRE, COPPER TIN-COATED
W1	CONN. AY, POWER TO MAIN FC-200
W2	CONN. AY, REMOTE FC-200
F1	FUSE, 250V 2A

C'CT NO.	DESC. & SPEC.	C'CT NO.	DESC. & SPEC.
U1	CPU, Z-80A ZILOG	U2	VDP, TMS9129NL PAL VDP
U3	P.S.G, AY-3-8910 G.I	U4	P.P.I, I8255A INTEL
U5A, B	ROM, M-ROM BASIC	U6~U7	D-RAM, TMS4416-15 T.I
U14~U21	D-RAM, HM4864-2DC 64K*1	U26, 33, 48	QUAD MUX, 74LS157
U34	DECODER, 74LS145	U49	QUAD MUX, 74LS157
U44	DECODER, 74LS139	U27	DUAL MPX, 74LS153
U45	DECODER, 74LS138	U29~U31	HEX BUFFER, 74LS367
U23, 38, 40	D-F/F, 74LS74	U43	HEX BUFFER, 74LS367
U25, 36, 37	OR, 74LS32	U46	NOR, 74LS02
U35, 42	AND, 74LS08	U39	NAND, 74LS00
U32	HEX INVERT., 74HCU04P	U47, 50	HEX INVERT., 74LS04
U41	OPEN COLL., 74LS09	U28	2-OP AMP, MPC4559C NEC
U22	8-D F/F, 74LS374	U24	QUAD BUFFER, 74LS125
HIC5001	HYBRID IC, HIC5001	C53	TRIMMER CAP., TZ03R300E
RELAY	RELAY, DS1M-DC5V	Q1~Q3	TR, KTC1815GR
D2	DIODE, SWITCHING 1N4148	D1	DIODE, ZENER GZB5.1-B

C54	CERAMIC CAP., 33PF	C56	CERAMIC CAP, 470PF 50V
C57	ELECTRO-CAP., 4.7MF 16V	C58	ELECTRO-CAP., 220MF 16V
C4~8, 52	CERAMIC CAP., 0.1MF 50V	R50~59	R ARRAY, 2.2K*10 1/4W
R21~R24	R ARRAY, 10K*4 1/4W	R25~R40	R ARRAY, 10K*8 1/4W
R5, 12, 15	RESISTOR, 10K-J 1/4W	R4, 10	RESISTOR, 4.7K-J 1/4W
R19, 47, 48	RESISTOR, 10K-J 1/4W	R8, 9	RESISTOR, 220-J 1/4W
R1, 2, 18	RESISTOR, 2.2K-J 1/4W	R14	RESISTER, 6.2K-J 1/4W
R3, 13, 16	RESISTER, 1K-J 1/4W	R20	RESISTOR, 3.7K-J 1/4W
R61	RESISTOR, 1K-J 1/4W	R6	RESISTOR, 5.1K-J 1/4W
R42~R44	RESISTOR, 470-J 1/4W	R60	RESISTOR, 22K-J 1/4W
R11	RESISTOR, 120-J 1/4W	R49	RESISTOR, 330-J 1/4W
PCB CONN.	CONN, 50P 980-050-039	EXP. CONN.	CONN, 50P 6201-050-258
PRT CONN.	CONN, 14P 57L-40140-770B	P1~P2	CONN, 2P MLX 5045-02A
KBD CONN.	CONN, 11P MLX 5267-11A	KBD CONN.	CONN, 12P MLX 5267-12A
PWR CONN.	CONN, 4P MLX 5289-04A	JOY CONN.	CONN, 9P SUB-D TYPE
JACK	RCA 1P S-1558	SOCKET	DIN 8P TCS-4480-01
R45	RESISTOR, 8.2K-J 1/4W	F1~F3	EMI FILTER, DSS310-55DL2



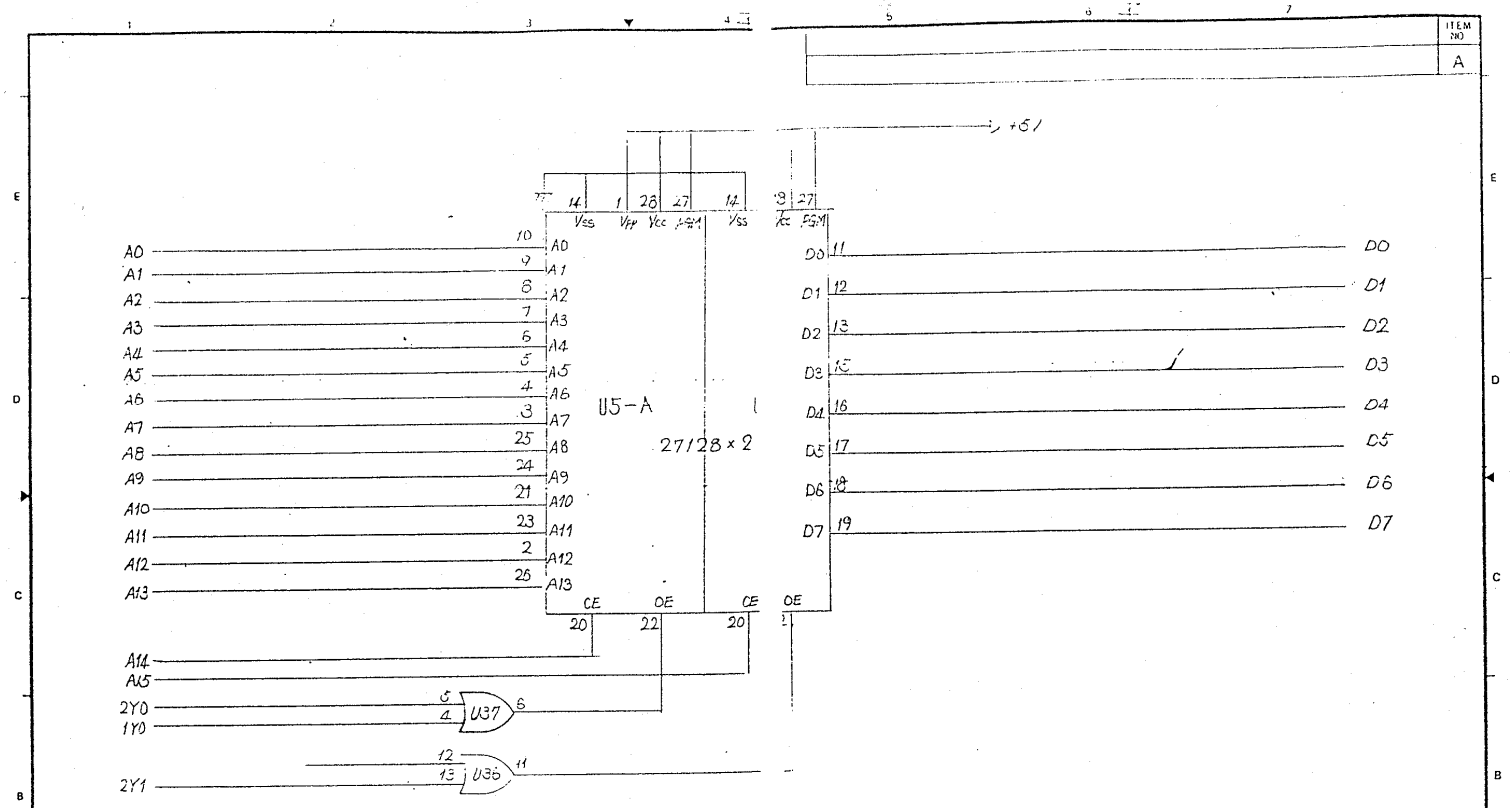
CHANGES	DIMENSIONAL TOLERAN						C	B	A	NO.	PART NO	DESCRIPTION	MATERIAL	COLOR FINISH	REMARK
	공차 / 치수	1	3	11	15	11				QUANTITY					
	0.5	±0.05	12	16	100	13									
	1	0.10	0.15	0.20	0.35	0.1									
	2	0.15	0.20	0.30	0.45	0.2									
	3	0.20	0.30	0.15	0.70	1.1									
	4	0.30	0.15	0.70	1.0	1.5									
	5	0.15	0.70	1.0	1.5	2.0									
	ANGULAR														
	UNLESS OTHERWISE SPE														

GoldStar

SCALE | UNIT mm | DRAWN | CHECKED | APPROVED | ISSUE

FC-200 CIRCUITS (1)
C P U

A3 297 · 420 또 공심양식F 143 Stock No 91160143



ITEM NO A

CHANGES

VIDEOTEX BURO
Kannerburg 506
7929 AS Dessenter
tel. 05... 10 - 3 07 59

DIMENSIONAL TOLERAN

구분	1 ~3	5 ~12	13 ~30	31 ~120	121 ~330
등급	±0.05				
1	0.10	0.15	0.20	0.30	0.5
2	0.15	0.20	0.30	0.45	0.7
3	0.20	0.30	0.45	0.70	1.0
4	0.30	0.45	0.70	1.0	1.5
5	0.45	0.70	1.0	1.5	2.0

ANGULAR

UNLESS OTHERWISE SPEC

NO.	PART NO.	DESCRIPTION	MATERIAL	COLOR FINISH	NOTE
QUANTITY					

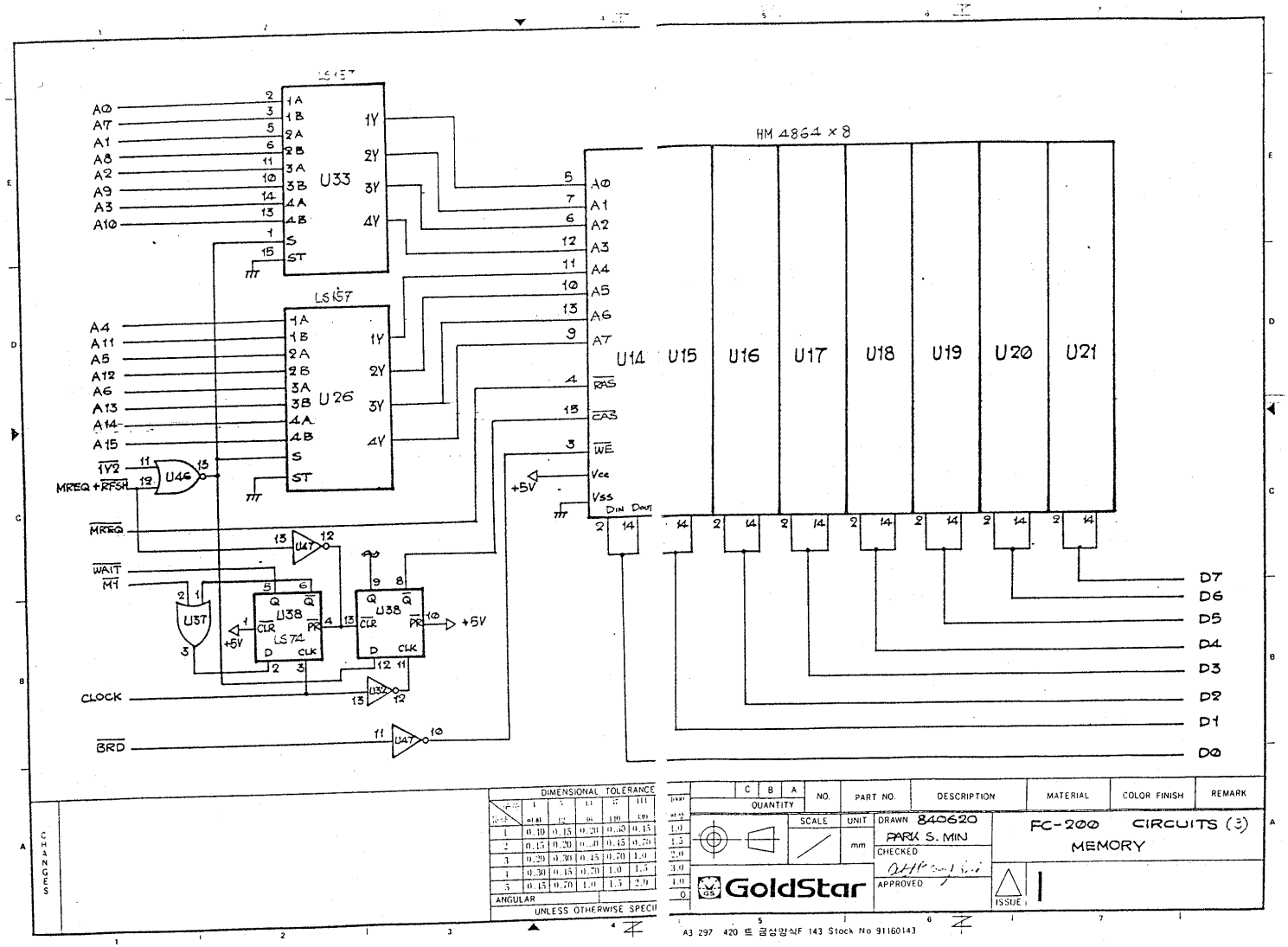
SCALE | UNIT mm | DRAWN 84 9 20 PARK H. D | CHECKED | APPROVED

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FC-200 CIRCUITS (2)
MONITOR

ISSUE 1

A3 297 × 420 트 금성왕식F 143 Stock No 91160143



DIMENSIONAL TOLERANCE						
	I	II	III	IV	V	VI
1	0.10	0.15	0.20	0.35	0.45	
2	0.15	0.20	0.30	0.45	0.70	
3	0.20	0.30	0.45	0.70	1.0	
4	0.30	0.45	0.70	1.0	1.5	
5	0.45	0.70	1.0	1.5	2.0	
ANGULAR	UNLESS OTHERWISE SPECIFIED					

C	B	A	NO.	PART NO.	DESCRIPTION	MATERIAL	COLOR FINISH	REMARK
QUANTITY								

CHANGES

SCALE / UNIT mm

DRAWN 840620 PARK S. MIN

CHECKED

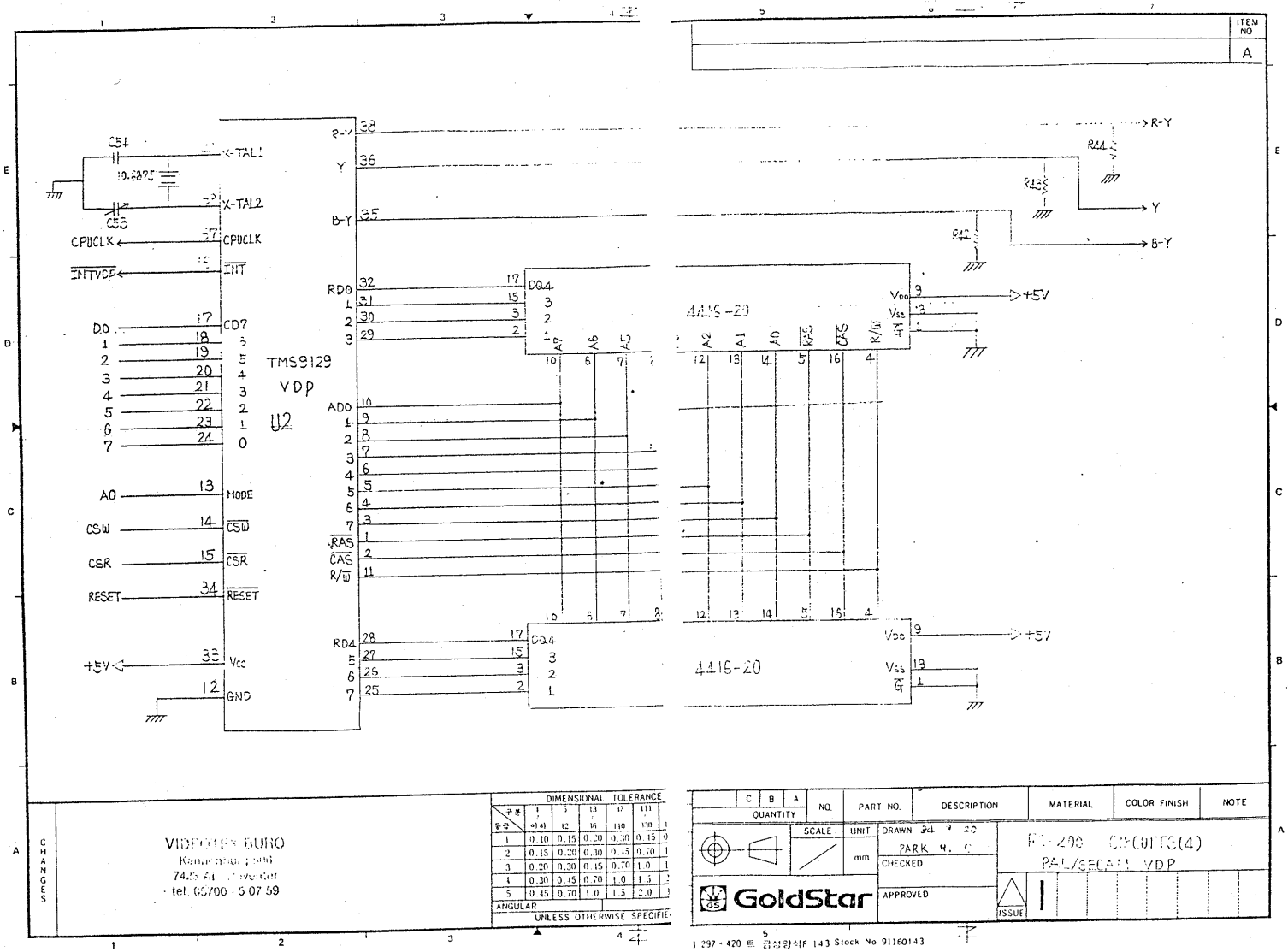
APPROVED

GoldStar

FC-200 CIRCUITS (3)
MEMORY

ISSUE

A3 297 420 트 금성양식F 143 Stock No 91160143



ITEM NO
A

CHANGES

VIDEOTRON BURO
Kamerstraat (post)
7475 AA [illegible] Deventer
- tel. 05700 - 5 07 59

DIMENSIONAL TOLERANCE

FR	1	3	13	17	111	
	±1.0	12	16	110	130	
1	0.10	0.15	0.20	0.30	0.15	0
2	0.15	0.20	0.30	0.45	0.20	1
3	0.20	0.30	0.15	0.70	1.0	1
4	0.30	0.45	0.70	1.0	1.5	2
5	0.45	0.70	1.0	1.5	2.0	3

ANGULAR
UNLESS OTHERWISE SPECIFIE

C	B	A	NO.	PART NO.	DESCRIPTION	MATERIAL	COLOR FINISH	NOTE
QUANTITY								

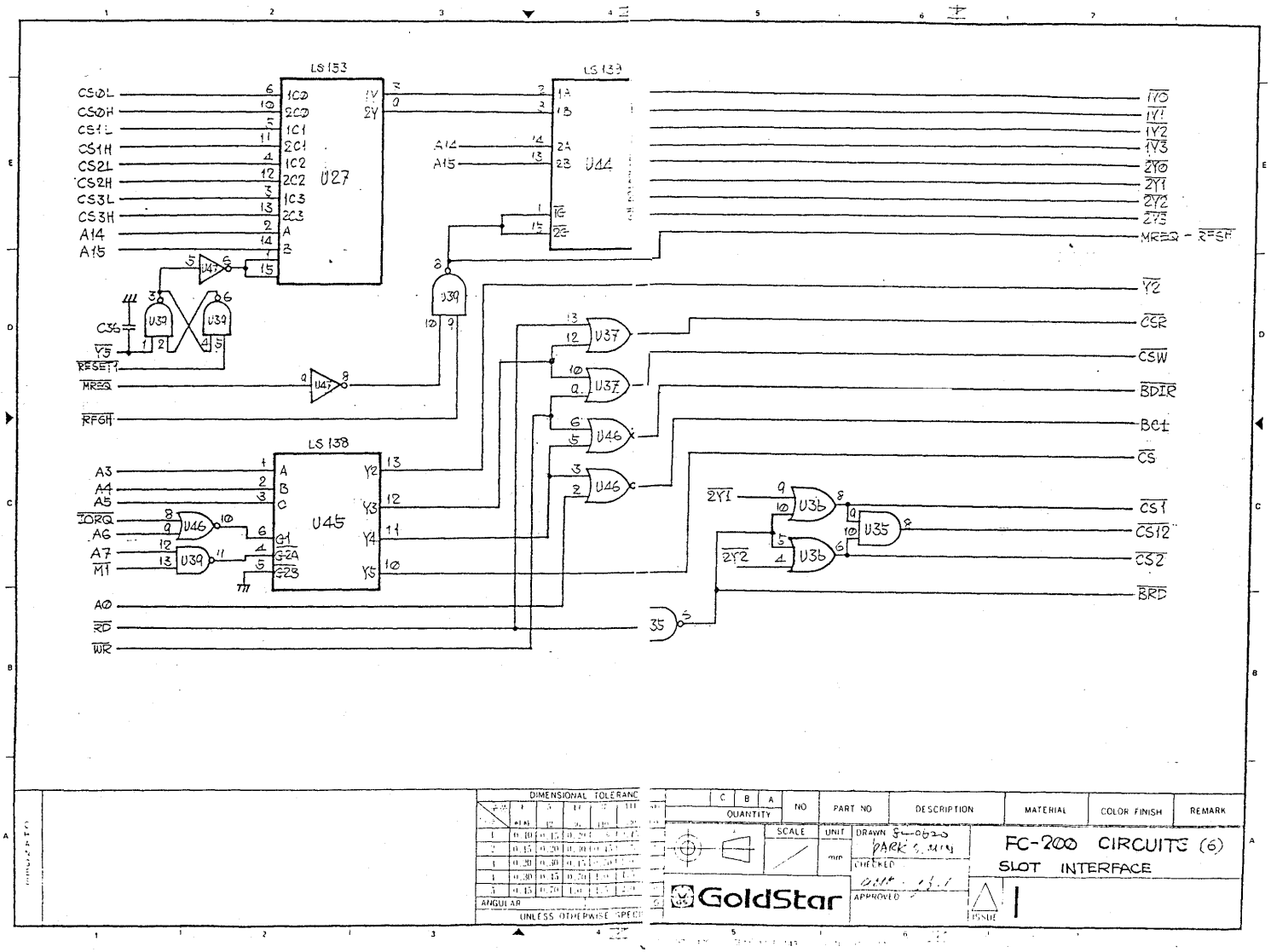
SCALE | UNIT: mm | DRAWN: PARK H. C | CHECKED | APPROVED

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RC-200 CIRCUITS(4)
PAL/SECAM VDP

ISSUE 1

3 297 - 420 톤 금성원사IF 143 Stock No 91160143



DIMENSIONAL TOLERANC					
	1	2	3	4	5
	mm				
1	0.10	0.15	0.20		
2	0.15	0.20	0.30		
3	0.20	0.30	0.50		
4	0.30	0.50	0.80		
5	0.50	0.80	1.20		
ANGULAR					

UNLESS OTHERWISE SPECI

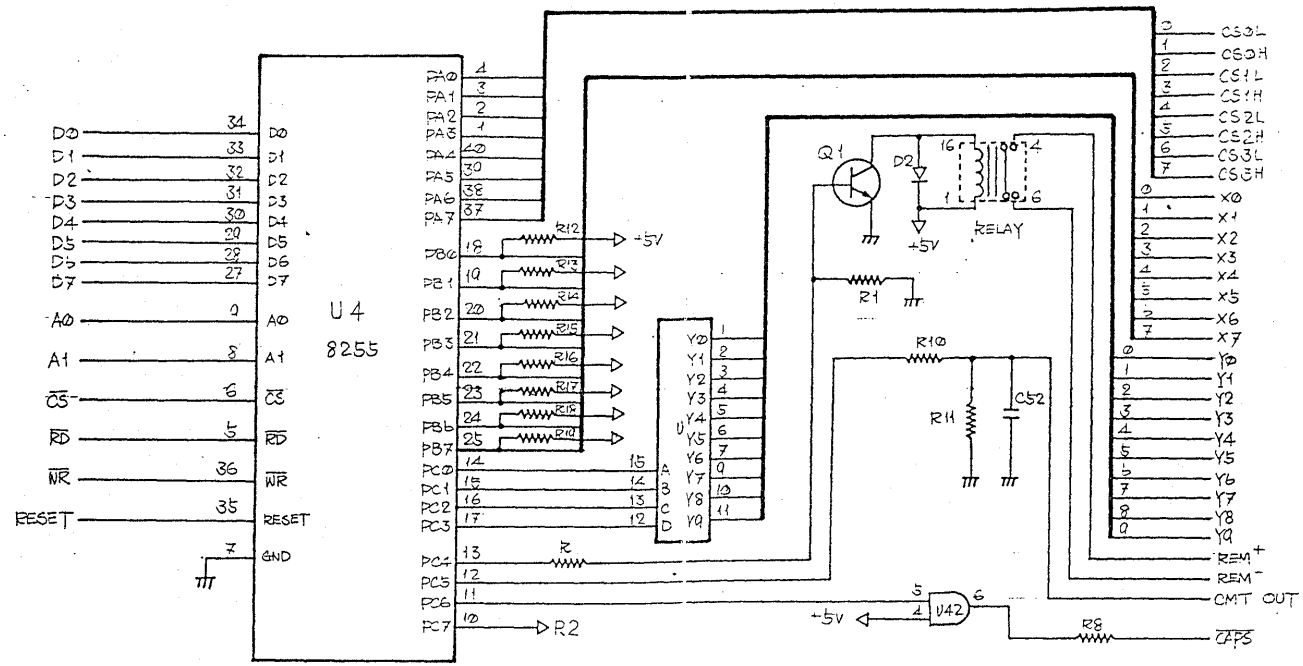
C	B	A	NO	PART NO	DESCRIPTION	MATERIAL	COLOR FINISH	REMARK
QUANTITY								

SCALE | UNIT mm | DRAWN S-0620 PARK S.MIN | CHECKED | APPROVED

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FC-2000 CIRCUITS (6)
SLOT INTERFACE

INSIDE



CHANGES

NO	PART NO.	DESCRIPTION	MATERIAL	COLOR FINISH	REMARK
C B A QUANTITY					

DIMENSIONAL TOLERANCE

부호	1	3	6	30	100
1	0.10	0.15	0.20	0.30	0.45
2	0.15	0.20	0.30	0.45	0.70
3	0.20	0.30	0.45	1.00	1.50
4	0.30	0.45	0.70	1.50	2.50
5	0.45	0.70	1.00	2.50	4.00
ANGULAR					

UNLESS OTHERWISE SPEC

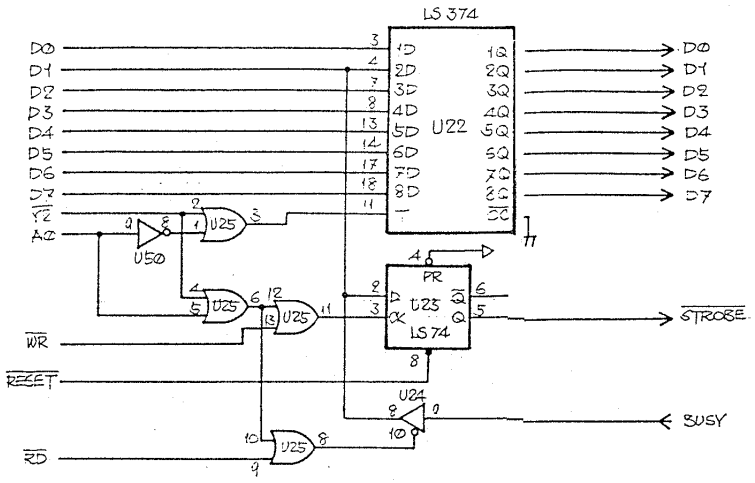
SCALE | UNIT mm | DRAWN | CHECKED | APPROVED

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FC-200 CIRCUITS (7)
PERIPHERAL INTERFACE

ISSUE

A3 297 420 ㎜ 금성알티 143 Stock No 91167



DIMENSIONAL TOLER				
	1	3	6	120
	±0.45	12	30	
1	0.10	0.15	0.20	0.3
2	0.15	0.20	0.30	0.5
3	0.20	0.30	0.45	
4	0.30	0.45	0.70	
5	0.45	0.70	1.0	
ANGULAR				

UNLESS OTHERWISE S

CHANGES

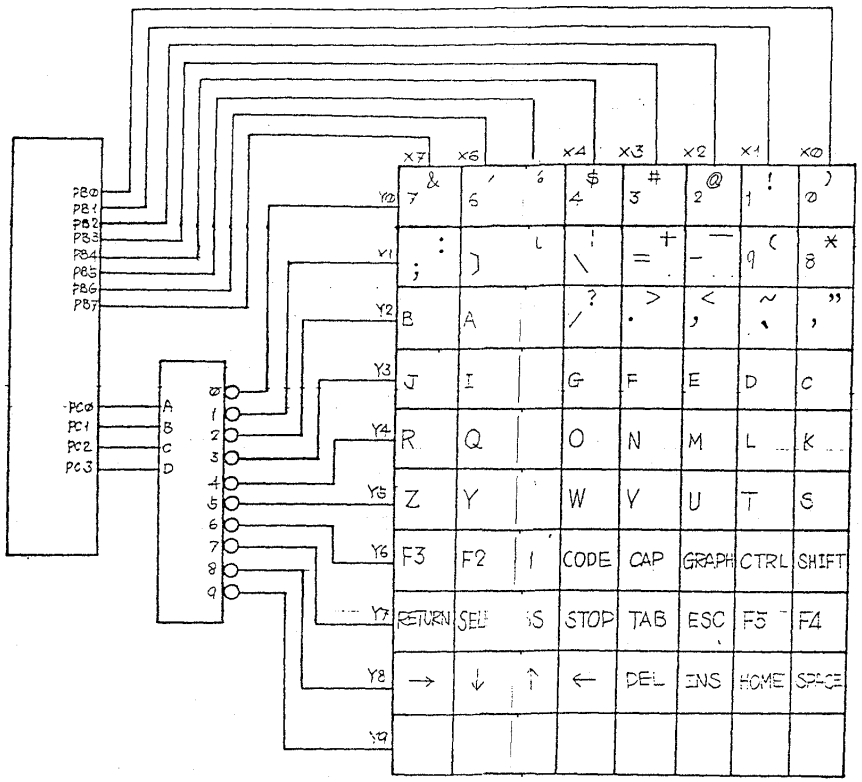
NO	PART NO	DESCRIPTION	MATERIAL
C B A			
QUANTITY			

SCALE | UNIT mm | DRAWN 김상준 DARK.4IN | CHECKED | APPROVED | ISSUE 1

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FC-200 C
PRINTE

A3 297 420 트 금성잉식IF 143 Stock No 91160143



CHANGES

DIMENSIONAL TOLE				
구분 / 등급	1 ±0.05	3 ±0.2	6 ±0.3	12 ±0.5
1	0.10	0.15	0.20	±0.30
2	0.15	0.20	0.30	0.45
3	0.20	0.30	0.45	0.70
4	0.30	0.45	0.70	1.0
5	0.45	0.70	1.0	1.5
ANGULAR				
UNLESS OTHERWISE				

UNIT	
0.5	±0.2
1.0	
1.5	
2.0	
3.0	
4.0	
9	

NO.	PART NO.	DESCRIPTION	MATERIAL	COLOR FINISH	REMARK
QUANTITY					

SCALE | UNIT mm

DRAWN 840620

CHECKED PARK S. MIN

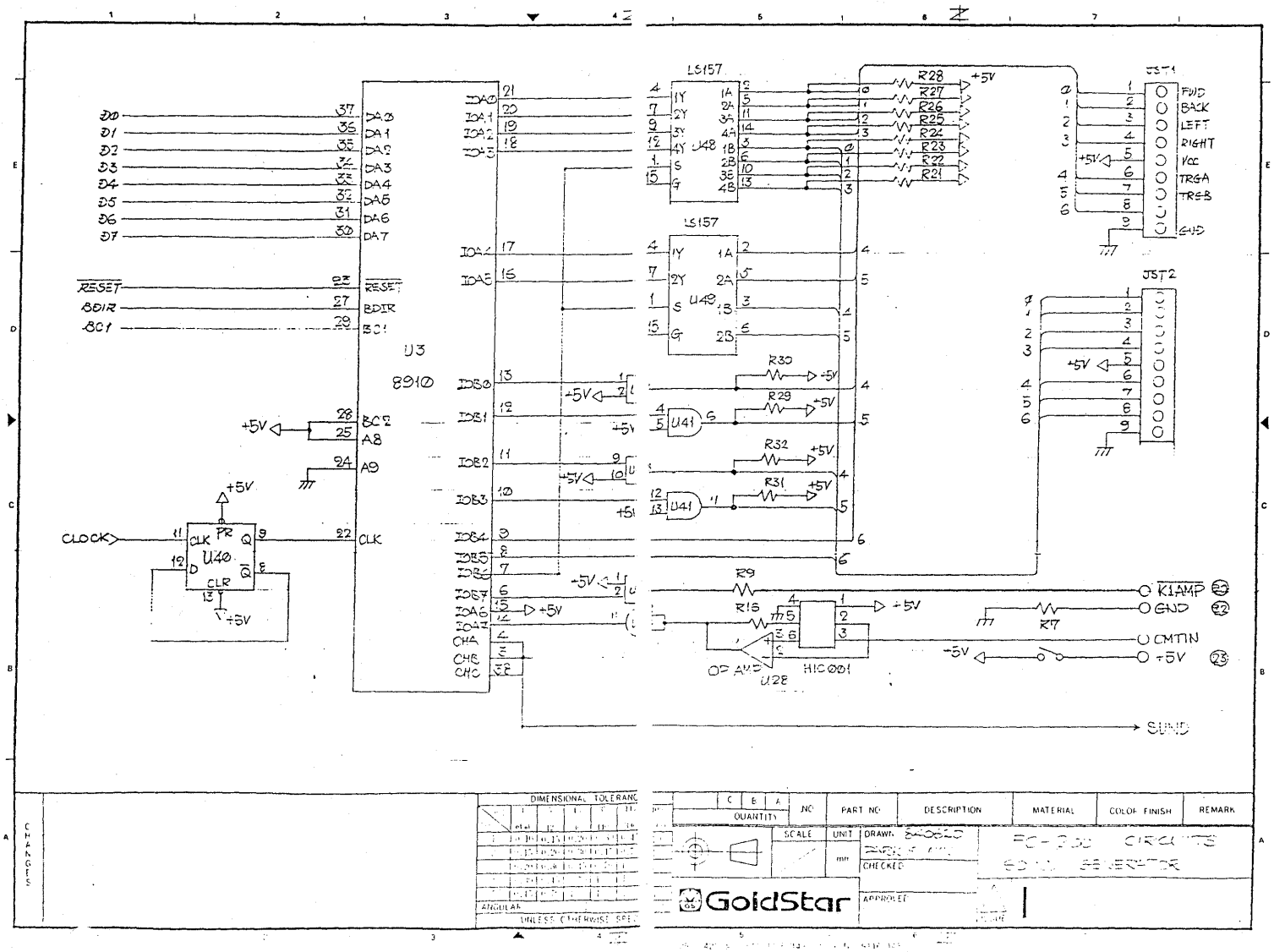
APPROVED

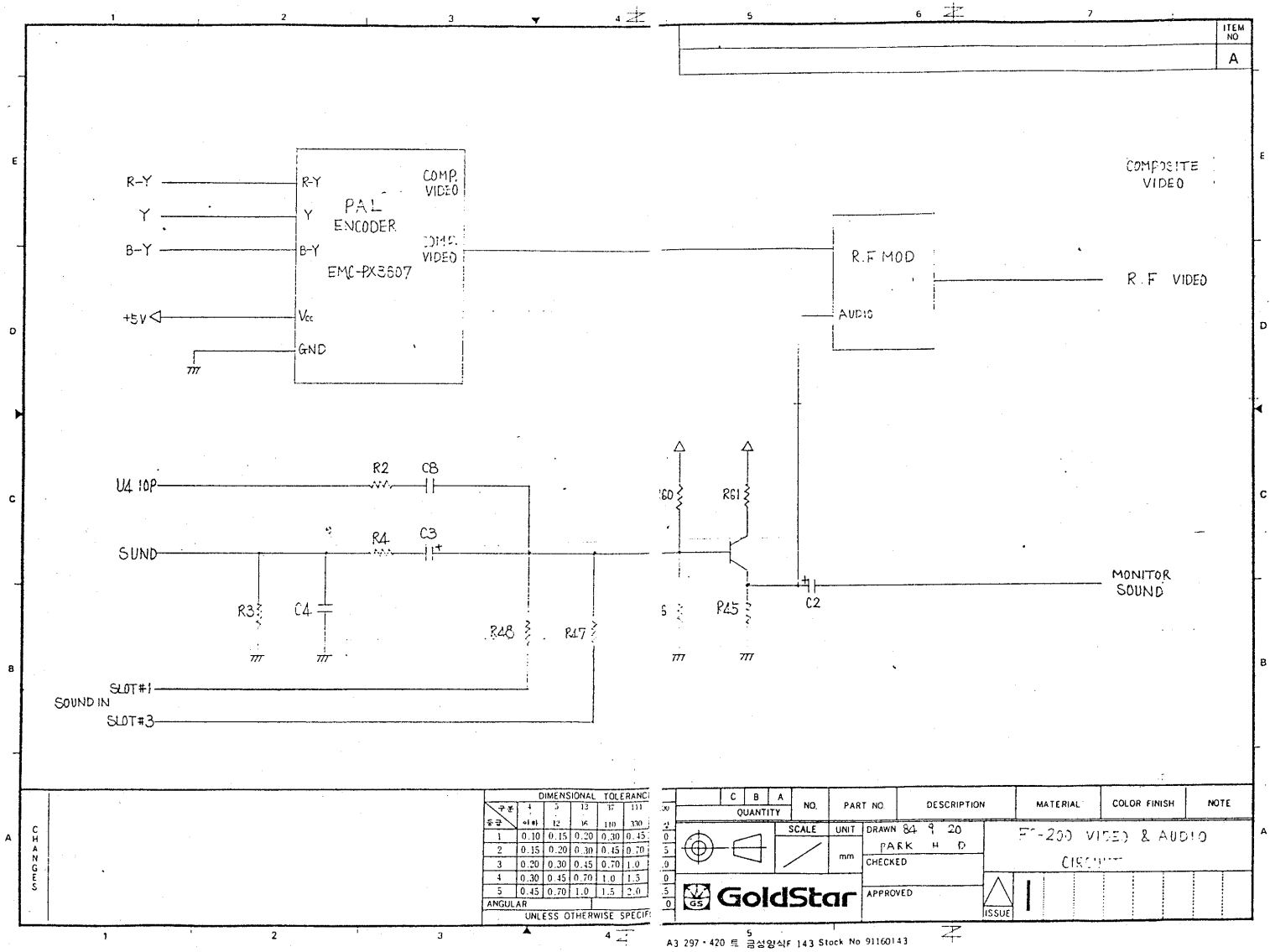
GoldStar

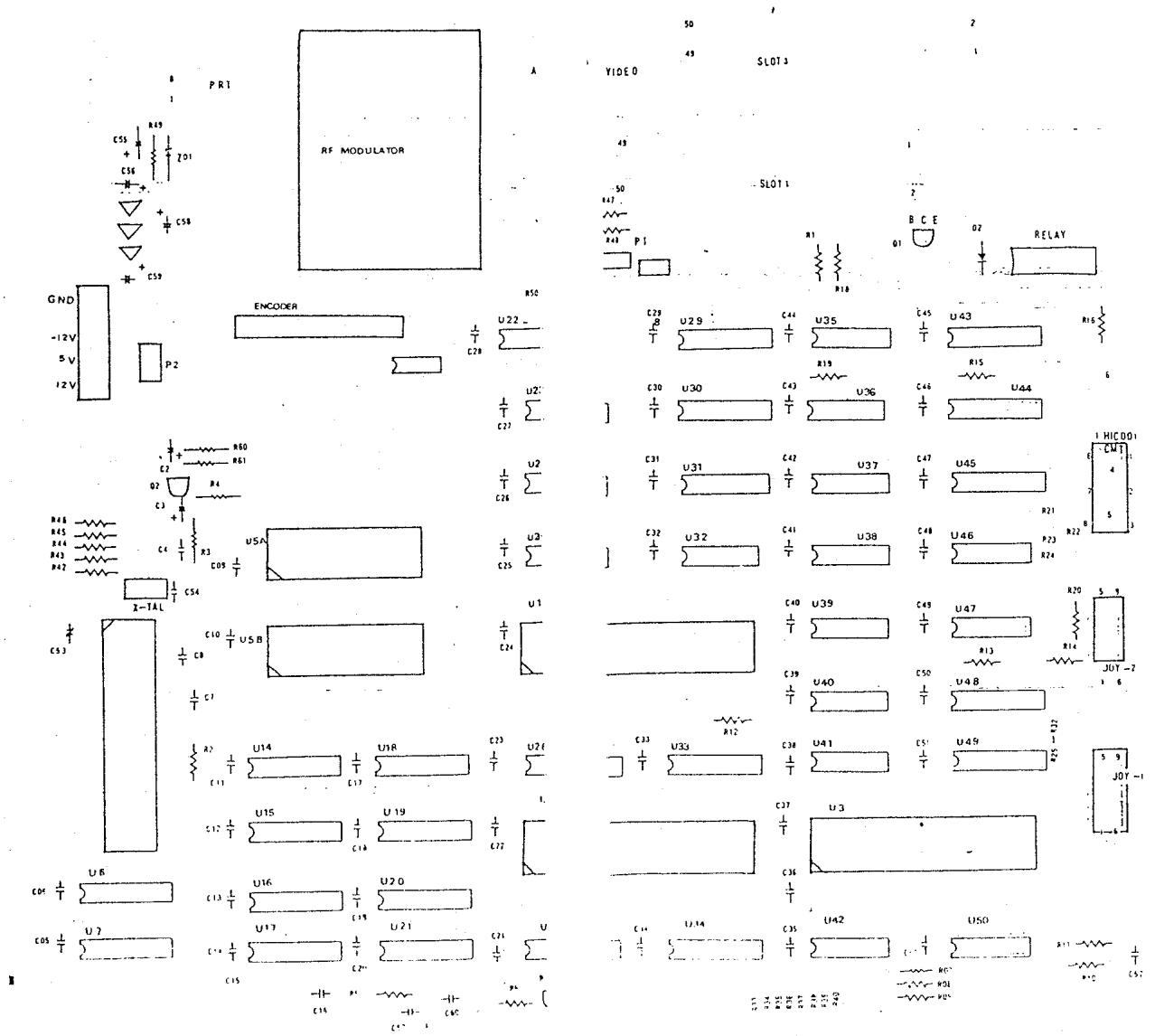
FC-200 CIRCUITS (9)
KBD MATRIX

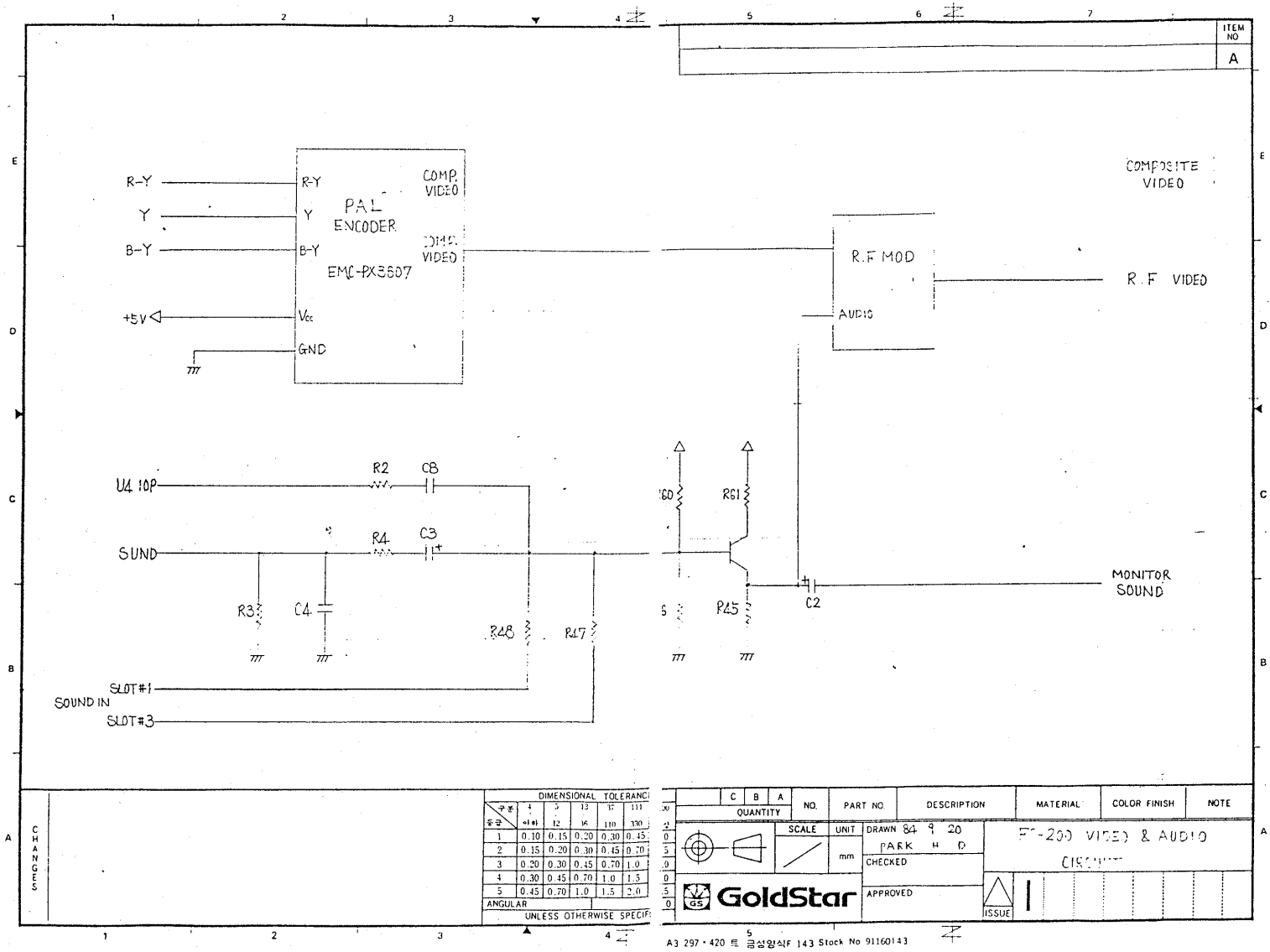
ISSUE 1

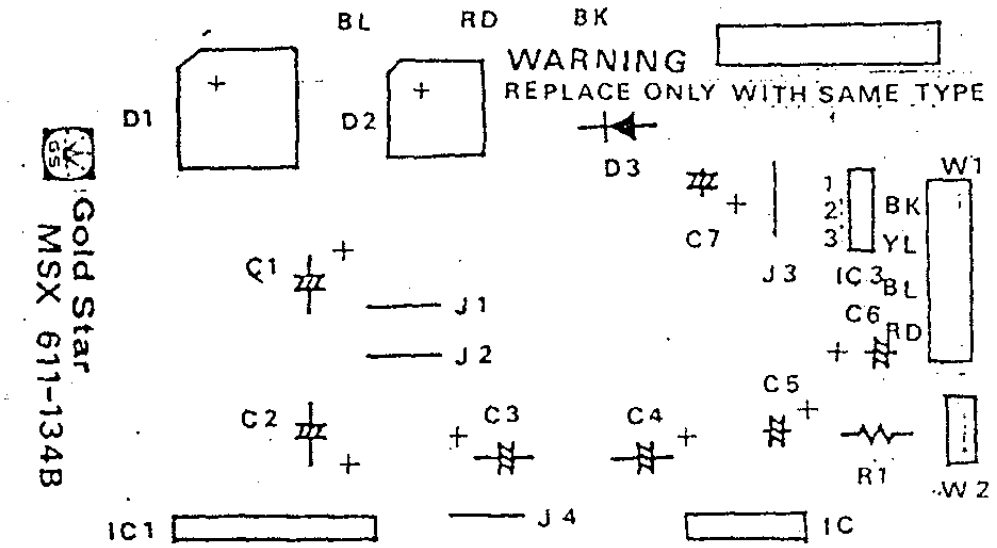
A3 297 · 420 뜨 금성양식F 143 Stock No 91160143


D0
D1
D2
D3
D4
D5
D6
D7
RESET
BDIR
BC1
U3
8910
BC2
A8
A9
CLOCK
U40
CLR
LS157
U48
U41
R28
R27
R26
R25
R24
R23
R22
R21
R30
R29
R32
R31
JST1
FWD
BACK
LEFT
RIGHT
Vcc
TRGA
TRGB
GND
JST2
R9
R15
R17
K1AMP
GND
CMTIN
+5V
OP AMP
U28
HIC0001
SGND
GoldStar


ITEM NO
A
R-Y
Y
B-Y
+5V
R-Y
Y
B-Y
Vcc
GND
PAL
ENCODER
EMC-PX3607
COMP. VIDEO
COMP. VIDEO
COMPOSITE VIDEO
R.F MOD
AUDIO
R.F VIDEO
U4 10P
SUND
R2
C8
R4
C3
R3
C4
R48
R47
R61
R45
C2
MONITOR SOUND
SLOT#1
SOUND IN
SLOT#3
CHANGES
DIMENSIONAL TOLERANCE
ANGULAR
UNLESS OTHERWISE SPECIFI
C B A
QUANTITY
NO.
PART NO.
DESCRIPTION
MATERIAL
COLOR FINISH
NOTE
SCALE
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PARK H D
CHECKED
APPROVED
GoldStar
FC-200 VIDEO & AUDIO
CIRCUIT
ISSUE
1
A3 297 • 420 트 금성양식F 143 Stock No 91160143


PRT
RF MODULATOR
GND
-12V
5V
12V
P2
ENCODER
X-TAL
SLOT 3
SLOT 1
VIDEO
RELAY
P1
JOY -2
JOY -1


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COMP. VIDEO
COMPOSITE VIDEO
R.F MOD
AUDIO
R.F VIDEO
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COMPONENT SIDE