MSX Computer

CX-5M, YIS503F

SERVICE MANUAL



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YAMAHA MSX COMPUTER ACCORDING TO AREA

There are 7 different model of the YAMAHA MSX computer according to area. This manual refer to the computer as only the CX5M, referring to all models. Where reference to a particular model is called for, the specific model number pertaining to the area in question will be used. The different model numbers, and the area to which they pertain, are as follows:

CX5ME ..... United Kingdom ..... (PAL-I)
CX5MA ..... Australia and New Zealand ..... (PAL-B)
CX5MG ..... West Germany and European Countries ..... (SECAM)
CX5MS ..... Scandinavian Countries ..... (SECAM)
CX5MF ..... France ..... (RGB output)
YIS-503F ..... France ..... (RGB output)
YIS-503FB ..... Belgium ..... (PAL-G)

MODEL / UNIT	CX5ME	CX5MA	CX5MG	CX5MS	CX5MF	YIS-503F	YIS-503FB
KEYBOARD UNIT	PB55070					PB55079	
KEY SUB BOARD	NA55171						
CPU BOARD	NA55169				NA55170		NA55169
CLOCK CARD	NA55174				NA55170		NA55174
ENCODER BOARD	PB55077	PB55076	PB55078		NA55176		PB55075
POWER SUPPLY UNIT	NP55140	NP55150	NP55180	NP55130	NP55170		
ACCESSORIES							
CASSETTE CABLE	Mi55117		* Mi55116		Mi55117		
RF CABLE	RCA Type Aerial Type		* RCA Type	RCA Type Aerial Type			RCA Type Aerial Type
RGB CABLE					Mi55115		

* marked : with Core

• SPECIFICATIONS

CPU

CPU	: Z80A compatible
Clock	: 3.579545 MHz
Wait	: 1 wait in M1 cycle
Interrupt	: INT enternal and VDP. NMI interrupt non used. (In MSX-BASIC interpreter 50Hz signal from VDP is used for the interrupt.) (MODE 1)
Reset	: Power on reset

MEMORY

Main memory	: 32 KB (MB81416-12X4)
Video RAM	: 16KB (μPD416C-3X8)
ROM	: 32KB (MSX-BASIC international version)

CRT DISPLAY

Video Display Processor (VDP)	: TMS9929A
Fonts	: Alpha-numerics, graphic patterns other patterns in 8 X 8 dots
Color	: 16 colors
Display capability	: When power is turned on, 37 characters per line X 24 lines Possible upto 40 characters per line by software control
Resolution	: 256 dots x 192 lines (non-interlace)

I/O INTERFACE

Keyboard	: Stroke type step sculpture Alpha numeric characters, special characters and Alpha numeric characters ..... 48 Control and special effect keys . 16 Cursor movement keys 4

Function keys (programmable) . . 5
CAPS lock keys with LED indication

Audio Cassette Interface : 8 pin DIN connector
Baut rate 1200/2400 BPS switchable be software
FSK standard
With remote control (Cassette motor ON/OFF)

Printer Interface : 8 bit parallel centronics standard
TTL level signal
14 pin connector

Universal I/O Interface (JOYSTIC etc.) : 2 ports
9 pin type D connector (male) X 2
TTL level

Audio/Video Output : [CX-5ME, A, G, S, YIS-503FB]
1) MONITOR output
PAL composite video output 75Ω
2) SOUND output
8 octaves/3 tones + noise
SSG is YM-2149
Beep Sound (PPI: μPD8255C-5)
3) RF output
G-PAL (UHF, 36ch) . .CX5MG, CX5MS, YIS-503FB
B-PAL (VHF, 3ch, 4ch).CX5MA
I-PAL (UHF, 36ch) . . . CX5ME
: [CX5MF, YIS-503F]
1) MONITOR output
RGB output
8 pin DIN connector

Upper Slot (SLOT #1) : 50 pins MSX standard female connector

Rear Slot (SLOT #2) : 50 pins card edge connector

Side Slot (SLOT #3) : 60 pins card edge connector

POWER SUPPLY UNIT CAPACITY

+5V ± 5% 1.9A
Slots . . . . . 300mA X 2
Universal I/O ports . . . . . 50mA X 2
A/V output 50mA
+12V ± 10% 0.5A (max)
−12V ±10% 0.16A (max)

GENERAL SPECIFICATIONS

Power supply: [CX5MF, G, S, YIS503F, FB]
AC220V ± 10%
[CX5ME, A]
AC240V ± 10%
Power input: 30 watts maximum
Measurement: 423(W) x 208(D) x 68(H) mm (CPU)
245(W) x 100(D) x 68(H) mm (Power Supply Unit)
Weight: 2.8 kg (CPU)
1.0 kg (Power Supply Unit)

ACCESSORIES

Cassette interface cable:
CPU side . . DIN 8 pin plug
Cassette recorder side:
Earphone plug (White) . . . . . Mini plug (3.5φ)
Mic plug (Red) . . . . . Mini plug (3.5φ)
Rem-Control plug (Black). . . Mini plug (3.5φ)
Length: 1 m
RF cable: Length . . . . 2 m (CX5ME, A, S, YIS503FB)
Length . . . . 0.98 m (CX5MG)
RGB cable: Length . . . . 1.5 m (CX5MF)

• DISPLAY MODE

MODE		Resolution	Size	Number	Specified Color	Sprite	Characters
Graphic I (Screen 1)	MAX	256 X 192	8 X 8	256	16 colors	Possibility	32 X 24
	NORMAL	240 X 192					29 X 24
Graphic II (Screen 2)	MAX	256 X 192	8 X 8	768	16 colors	Possibility	32 X 24
	NORMAL	240 X 192					29 X 24
Multi Color (Screen 3)	MAX	64 X 40blk	4 X 4 per 1block	—	16 colors	Possibility	8 X 6
	NORMAL	60 X 40blk					
TEXT (Screen 0)	MAX	256 X 192	8 X 6	256	2 out of 16 colors	Impossibility	40 X 29
	NORMAL	240 X 192					39 X 24 37 X 24**

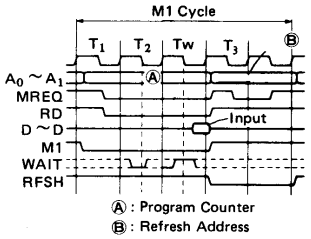
**USE VDP (TMS9929A)

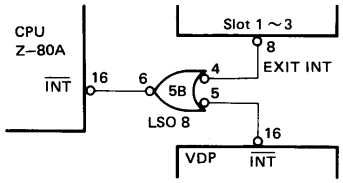
• MSX DESCRIPTION OF OPERATION

CPU (Z80A)

A 3.579545 MHz system clock is fed to the CPU from clock card. Thus one machine cycle is approximately 279 ms. Address bus (16 bits), data bus (8 bits), control bus (6 bits) and other control lines are connected to peripheral devices and units.

The one machine cycle WAIT is inserted per each M1 cycle (instruction fetch cycle). WAIT can be inserted through slots 1 ~ 3 are logically ORed and led to INT line. 50 Hz interrupt signal in output from VDP to initiate each 1/50 second for the screen control or keyboard scan.



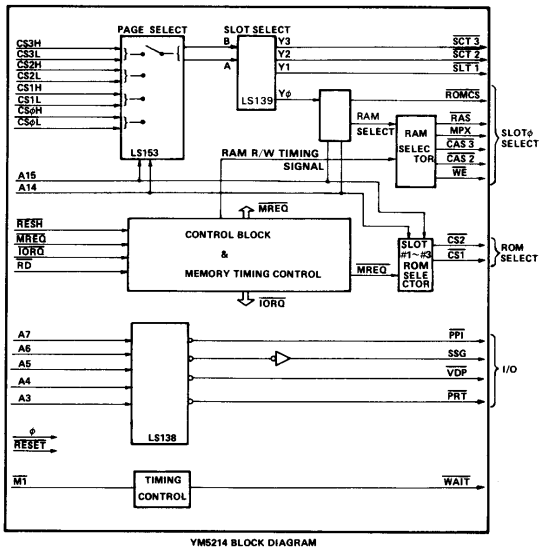


MMC (YM-5214)

It is a dedicated LSI for MSX and developed by YAMAHA.

Based on the MSX specifications it handles the memory bank select, standard I/O control, various access timing generation for ROM and RAM or M1 WAIT instruction generation.

MMC BLOCK DIAGRAM



YM5214 BLOCK DIAGRAM

VDP (TMS9929A)
50 Hz interrupt signal in output from VDP.
It supports 16Kbytes of V-RAM. It produces a PAL video signal for TV display according to the CPU instructions.

SSG (YM–2149)
It is compatible to General Instrument's PSG (AY3-8910) and enhanced.
Designed and developed by YAMAHA.
It produces by program 3 notes and a noise and provided with two 8 bits universal I/O ports for joystick and other peripherals.

PPI (μPD8255AC–5)
Three 8 bits universal I/O ports A, B and C are provided.
Each port may be controlled by software and the following functions are assigned as a specification.
Port A: Memory bank signal output.
Port B: Keyboard scan signal input
Port C: Keyboard strobe signal output, CAPS lock LED switch, cassette data recorder control, etc.

• Memory map and slot

Memory Map and Slot

ROM: 32K bytes MSX BASIC ROM on slot 0, address 0000H ~ 7FFFH.
RAM: DRAM of 16K bytes X 2 (total of 32K bytes) on slot 0, address 8000H ~ FFFFH.

	Slot 0	Slot 1	Slot 2	Slot 3
FFFFH	RAM 16Kb			
C000H	RAM 16Kb			
8000H	MSX BASIC			
4000H	ROM 32Kb			
0000H				

(Memory Map)

VRAM: 16 Kbytes V-RAM are is separated from the system bus and is supported by VDP.

SLOT SELECT SIGNAL OF PPI PORT A

PPI-A8H-PORT

PPI PORT A			PORT A	
CS0	L	Specified bit to select 0000H ~ 3FFFH area from which SLOT	LSB	O
	H		bit 1	O
CS1	L	Specified bit to select 4000H ~ 7FFFH area form which SLOT	bit 2	O
	H		bit 3	O
CS2	L	Specified bit to select 8000H ~ BFFFH area from which SLOT	bit 4	O
	H		bit 5	O
CS3	L	Specified bit to select C000H ~ FFFFH area from which SLOT	bit 6	O
	H		MSB	O

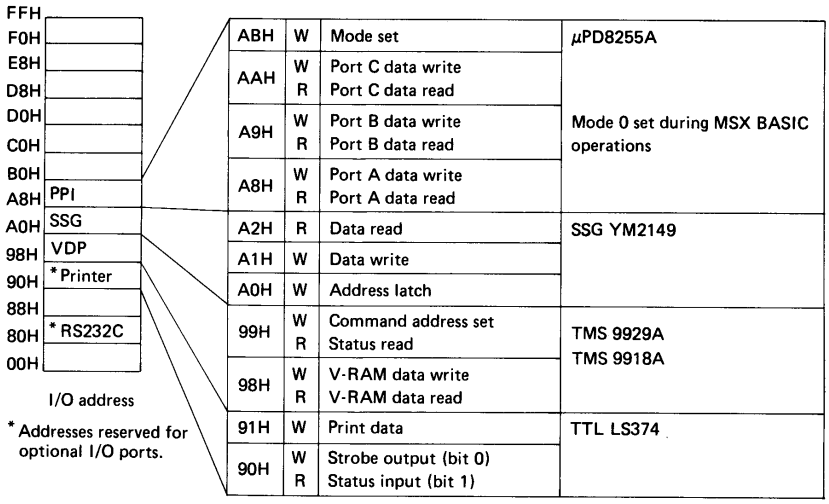
MSX BASIC MODE

SLOT SPECIFICATION BY EACH CSX L, H (X = 0, 1, 2, 3)

L/H	0/0	1/0	0/1	1/1
Slot	ROM, RAM	Slot 1	Slot 2	Slot 3

• I/O port address map

According to the MSX specifications, the 256 byte Z-80A I/O port area from 00H to FFH is reserved for the standard MSX system devices as follows:



ABH	W	Mode set	μPD8255A
AAH	W R	Port C data write Port C data read	Mode 0 set during MSX BASIC operations
A9H	W R	Port B data write Port B data read	
A8H	W R	Port A data write Port A data read	
A2H	R	Data read	SSG YM2149
A1H	W	Data write	
A0H	W	Address latch	
99H	W R	Command address set Status read	TMS 9929A TMS 9918A
98H	W R	V-RAM data write V-RAM data read	
91H	W	Print data	TTL LS374
90H	W R	Strobe output (bit 0) Status input (bit 1)	

PPI input/output port

When MSX-BASIC is operating, the mode is set to MODE 0 (PA0 ~ PA7, PB0 ~ PB7 and PC0 ~ PC7 can be controlled as 8-bit port independently.) and each port controls the following input/output.

PA0 ~ PA7: Output port to MMC, sends out data to produce slot select signal.
PB0 ~ PB7: Input port of keyboard scanning data.
PC0 ~ PC3: Sends scanning signal to keyboard through LS145.
PC4: (Motor ON/OFF control data recorder (cassette) Turns relay ON at "L".
PC5: Output FSK specification data to data recorder (cassette).
PC6: LED lights at CAPS lock LED "L".
PC7: Emits beeping sound through 1 bit output.

SSG input/output port

This LSI produces the programmable triple chord scale as well as noise, and at the same time, controls the next input/output unit by means of the two input/output port.

CHA ~ CHC : Triple chord output terminal and noise output terminal.
IOA0 ~ IOA5: Input port of general purpose input/output port (JOYSTICK 1, 2) scanning data.
IOA6: LED lights at CODE lock LED "L"
IOA7: Input port for data from data recorder (cassette).
IOB0 ~ IOB6: General purpose input/output port (JOYSTICK 1, 2) select and strobe & scanning.
IOB0 ~ IOB3: Port scanning data output
IOB4: JOY 1 strobe signal output
IOB5: JOY 2 strobe signal output
IOB6: JOY 1, 2 select signal
IOB "L" . . . . . JOY 1 select
IOB "H" . . . . . JOY 2 select
IOB7: Non-Used

The specified functions of PPI and SSG input/output ports as described above are all set by the inner monitor when power ON reset and MSX-BASIC in operation (without anything inserted in the slot).

SLOTs #1 and #2 PIN ASSIGNMENT

Pin No.	Pin Name	I/O	Description
1	CS1	O	Select Signal for ROM 4000H-7FFFH
2	CS2	O	Select Signal for ROM 8000H-BFFFH
3	CS1, 2	O	Select Signal for ROM 4000H-BFFFH
4	SLTSL	O	Slot Select Signal
5	N/C	–	Inhibited to use
6	RFSH	O	Dinamic RAM refresh signal
7	EXT WAIT	I	WAIT request, open collector signal
8	EXT INT	I	Maskable interrupt request, open collector signal
9	M1	O	M1 signal from CPU
10	BUSDIR	I	Direction Control for external Bus Buffer
11	IORQ	O	I/O request from CPU
12	MERQ	O	Internal memory request from CPU
13	WR	O	Write request from CPU
14	RD	O	Road request from CPU
15	RES	O	System Preset signal
16	N/C	–	Inhibited to use
17	A9	O	Address Bus signal
18	A15	O	
19	A11	O	
20	A10	O	
21	A7	O	
22	A6	O	
23	A12	O	
24	A8	O	
25	A14	O	
26	A13	O	
27	A1	O	
28	A0	O	
29	A3	O	
30	A2	O	
31	A5	O	
32	A4	O	
33	D1	I/O	Data Bus signal
34	D0	I/O	
35	D3	I/O	
36	D2	I/O	
37	D5	I/O	
38	D4	I/O	
39	D7	I/O	
40	D6	I/O	
41	GND	–	Ground
42	CLOCK	O	System Clock 3.579545MHz
43	GND	–	Ground
44	SW13	–	System protection
45	+5	–	Power Supply +5V
46	SW2	–	System protection (Note: SW1 and SW2 is in connection when Cartridge is inserted.)
47	+5	–	Power Supply +5V
48	+12	–	Power Supply +12V
49	SOUND IN	I	Sound input line (–5dbm) mixed with PSG sound and output
50	–12	–	Power Supply –12V

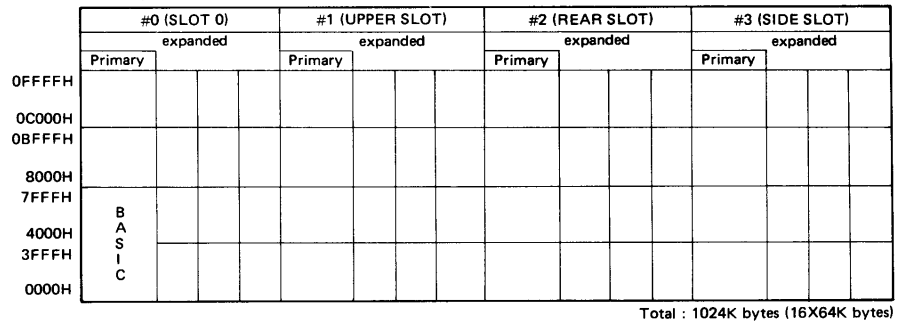
SLOT #3 PIN ASSIGNMENT

Pin No.	Pin Name	I/O	Description
1	SOUND OUT	O	Mixing Sound out of SSG, PP1
2	GND	–	Ground
3	GND	–	Ground
4	PHASE CONTROL	I	Control signal Input for superimpose
5	Y	O	Brightness signal from TMS-9928A
6	B–Y	O	Color difference signal from TMS-9928A
7	C-VIDEO	O	Color difference signal from TMS-9928A
8	R–Y	O	Color difference signal fro TMS-9928A
9	EXT CLOCK	I	External clock input for superimpose
10	CLOCK INT/EX	I	Clock selector for superimpose
11~60			Exactly same as regular slot

Note) Side slot dedicated pins are only applicable to the model equipped with the TMS 9929A VDP. But non used

•MSX BASIC interpreter's slot management mechanism

Memory structure of MSX



Total : 1024K bytes (16X64K bytes)

Terminology: Primary slot . . . . . Slot which is enabled by slot select register within 8255 PPI.
Secondary slot . . . . . Slot which is enabled by expansion slot register placed at 0FFFFH.
Page . . . . . Block of memory (maximum 16K) in each slot.
A slot is divided into 4 pages.
(0000H to 3FFFH, 4000H to 7FFFH, 8000H to 0BFFFH, 0C000H to 0FFFFH)

1. Minimum configuration

a) Microsoft MSX BASIC interpreter at slot #0 from 0000H to 7FFFH.
b) Minimum of 8K RAM from 0E000H to 0FFFH in any slot (including the secondary slot).

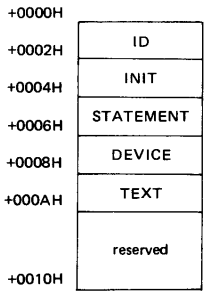
2. RAM search procedure

MSX BASIC first searches for available RAM from 0BFFFH down to 8000H (including the ones in secondary slots), then enables the page containing the largest RAM. If there are more than one such pages, selects the leftmost page in the figure above. MSX BASIC next searches for available RAM from 0FFFFH down to 0C000H, and does the same thing described above. Finally, MSX BASIC searches for continuous RAM block from 0FFFFH down to 8000H and sets the system variable "BOTTOM".

3. PROGRAM CARTRIDGE search procedure

MSX BASIC scans all slots (including secondary slots) from 4000H to 0BFFFH for a valid ID at the beginning of each page, collects information, and passes control to each page. The scan order is from left to right in the figure above. The format of ID and others are as follows.

• Offset from top



- **ID** is a 2 byte code used to distinguish ROM cartridges from empty pages. "AB" (41H, 42H) is used for this purpose.

- **INIT** holds an address of the initialization procedure specific to this cartridge. 0 when no such procedure is necessary. Programs that need to work co-operatively with BASIC interpreter should return control to it by Z80's "RET" instruction (all registers except [SP] can be destroyed). Other programs (such as game programs) need not to do so, however.

- **STATEMENT** holds an address of the expanded statement handler if such is contained in this cartridge. 0 when no such handler is inside. When BASIC encounters a 'CALL' statement, it calls this address with the statement name in the system area. Following are the notes to be remembered. (In the notes below, [HL] register pair is called a 'text pointer')

  1) The cartridge must be placed at 4000H ~ 7FFFH.
  2) Syntax for expanded statement is,
     CALL < statement name > [(< arg > [, < arg >] . .)]
     Key word "CALL" can be substituted with an under score character, " _ ".
  3) Statement name is stroed in the system area terminated by 0. The buffer for statement name is of fixed length (16 bytes) so statement name cannot be longer than 15 characters.
  4) If the handler for that statement is not inside the cartridge, return with carry flag set. Text pointer must be returned unchanged.
  5) If the handler for that statement is inside the cartridge, the cartridge should do the function, update text pointer to the end of the statement (usually, pointing to 0 which indicates the end of line, or " : " which indicates the end of statement), and return with carry flat reset (registers except [SP] can be destroyed). At the entry to the expanded statement handler, text pointer is set up to point to the first non-blank character after the statement name.

- **DEVICE** holds an address of the expanded device handler if such is contained in this cartridge. 0 when no such handler is inside. BASIC calls this address with the device name in the system area. Following are notes to be remembered.

  1) The cartridge must be placed at 4000H ~ 7FFFH.
  2) Device name is stored in the system area terminated by 0. The buffer for statement name is of fixed length (16b bytes) so device name cannot be longer than 15 characters.
  3) A cartridge (16K) can have up to 4 logical devices.
  4) When BASIC encounters a device name which is not known to itself, it calls DEVICE entry with 0FFH is [Acc]. If the handler for that device is not inside the cartridge, carry should be returned set. If it's inside, device ID (from 0 to 3) should be returned in [Acc], and carry reset. All registers can be destroyed.
  5) Real I/O operations take place when a DEVICE entry is entered with one of the following values in [Acc].

     0 Open
     2 Close
     4 Random I/O
     6 Sequential output
     8 Sequential input
     10 LOC function
     12 LOF function
     14 EOF function
     16 FPOS function
     18 Back up a character

  Device ID is passed in the system variable "DEVICE".

- **TEXT** holds the beginning address of BASIC. text contained in the cartridge. 0 when no such text is inside. BASIC regards this as the beginning address of BASIC text, sets pointer there, and begins execution of the program. Following are the notes to be remembered.

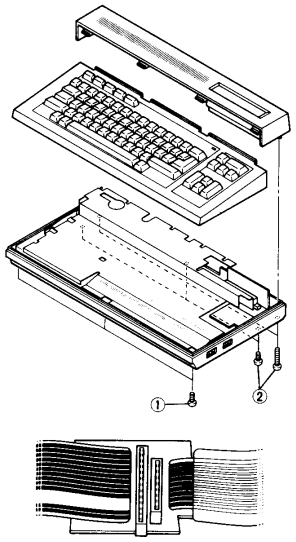
  1) When there are more than one such slots, only the leftmost one (in the figure of Memory structure of MSX above) is enabled and executed.
  2) The cartridge must be placed at 8000H ~ 0BFFFH, thus the maximum length of BASIC text cannot exceed 16 Kbytes.
  3) Even if there is a RAM block equipped at 8000H ~ 0BFFFH, it can never be used.
  4) The address pointed to by the TEXT entry must contain a zero.
  5) The line numbers (for statements which reference line numbers, such as GOTO, GOSUB, etc.) had better be translated to pointers in advance because they are never converted to pointers when executed. The can be line numbers however, but the execution would become slower then.

  NOTE: INIT, STATEMENT, DEVICE and TEST are placed low order byte first.

DISASSEMBLY PROCEDURES

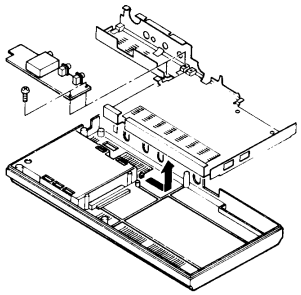
- **Case removal**

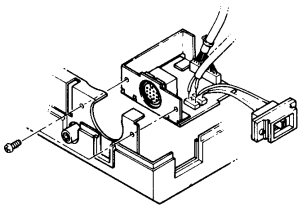
1) Remove three screws 1 in the bottom case.
2) Lift the front end of the keyboard case and remove it.
3) Remove five screws 2 in the bottom case and lift the case.
4) Disconnect the keyboard cable to the CPU boars by pulling it slowly.



- **Power Sub board and lower shield plate removal**

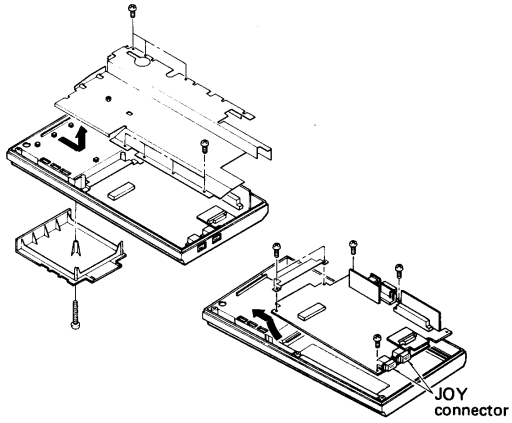
1) Remove two screws and remove the power sub board and power switch.
2) Remove one screw, move the lower shield plate to the left and remove it by lifting it up.





- **CPU board removal**

1) Remove seven screws, move the shield plate to the right a little and lift it up.
2) Remove three connectors of the CPU board.
3) Remove the side slot connector cover shield plate.
4) Remove three screws, lift the slotted side and pull to the left. Then remove the JOYSTICK connector from the bottom case and remove the CPU boards by lifting it up.



• LSI DATA TABLE

CPU (Z80A)

Pin No.	Pin Name	I/O	Active	Function
1 ~ 5	A11, 12, 13, 14, 15	O		Address bus
6	ϕ	I		3.579545 MHz clock input
7 ~ 10	CD4, 3, 5, 6	I/O		Data bus
11	V_{DD}	I		Voltage Supply +5V
12 ~ 15	CD2, 7, 0, 1	I/O		Data bus
16	$\overline{INT}$	I	L	Mask-able interrupt input pin: Mode 1 is used for interrupt which is input by taking the logic OR of the VDP interrupt output (every 1/60s.) and the cartridge interrupt input ($\overline{EXT\ INT}$) (when using MSX-BASIC)
17	$\overline{NMI}$			Non-connect
18	$\overline{HALT}$			Non-connect
19	$\overline{MREQ}$	O	L	Active when the effective address for memory access is on the address bus.
20	$\overline{IORQ}$	O	L	Active when the effective address for the input/output port access is on the address bus (also active when in INT or ACK cycle)
21	$\overline{RD}$	O	L	Active during the period when the CPU can receive data from the memory and input/output port.
22	$\overline{WR}$	O	L	Active when the CPU sends data to be stored in the memory and input/output port to the data bus.
23	$\overline{BUSAK}$			Non-connect
24	$\overline{WAIT}$	I	L	CPU remains in the wait state as long as this signal is active "L". (No refresh signal is generated when in the WAIT state.)
25	$\overline{BUSRQ}$			Non-connect
26	$\overline{RESET}$	I	L	The program counter becomes "0" at the $\overline{RESET}$ input and the CPU is initialized.
27	$\overline{M1}$	O	L	One "L" pulse is output at each instruction fetch cycle (also active when in the INT or ACK cycle)
28	$\overline{RFSH}$	O	L	Active when the low order 7 bit refresh address for D-RAM is on the address bus
29	V_{SS}	I		Ground
30 ~ 40	A0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	O		Address bus

MEMORY CONTROLLER (YM–5214)

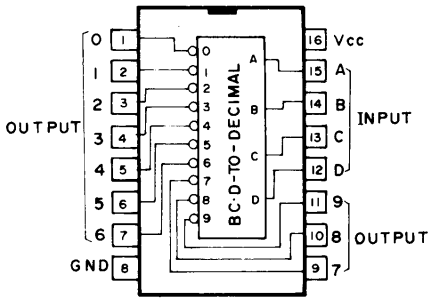
Pin No.	Pin Name	I/O	Active	Function
1	Vss	I		Ground
2	$\overline{RD}$	I	L	CPU (Z80A) $\overline{RD}$ signal input
3	$\overline{IORQ}$	I	L	CPU (Z80A) $\overline{IORQ}$ signal input
4	$\overline{M1}$	I	L	CPU (Z80A) $\overline{M1}$ signal input
5 ~ 9	AD7, 6, 5, 4, 3	I		CPU (Z80A) address 7 ~ 3 signal input
10	V_{DD}			Voltage Supply +5V
11	$\overline{PRT}$	O	L	Printer interface port select
12	$\overline{VDP}$	O	L	VDP port select
13	SSG	O	H	SSG port select
14	$\overline{PPI}$	O	L	PPI port select
15	$\overline{WAIT}$	O	L	1 WAIT signal generated in M1 cycle
16	$\overline{WE}$	O	L	D-RAM $\overline{WE}$ signal
17	$\overline{RAS}$	O	L	D-RAM $\overline{RAS}$ signal, RAS only refresh function by Z80A provided
18	MPX	O	H	D-RAM address multiplex signal
19	$\overline{CAS2}$	O	L	D-RAM (SLOT# 0,8000H-BFFFH) $\overline{CAS}$ signal
20	$\overline{CAS3}$	O	L	D-RAM (SLOT # 0,C000H-FFFFH) $\overline{CAS}$ signal
21	$\overline{ROMCS}$	O	L	MSX-BASIC ROM select signal
22	$\overline{CS1}$	O	L	ROM 4000H-7FFFH select signal
23	$\overline{CS2}$	O	L	ROM 8000H-BFFFH select signal
24	$\overline{RESET}$	I	L	SYSTEM RESET signal input
25	$\overline{SLT3}$	O	L	SLOT #3 select signal
26	$\overline{SLT2}$	O	L	SLOT #2 select signal
27	$\overline{SLT1}$	O	L	SLOT #1 select signal
28	CS3H	I		Slot select register (PPI PORT–A) signal
29	CS3L	I		Slot select register (PPI PORT–A) signal
30	CS2H	I		Slot select register (PPI PORT–A) signal
31	CS2L	I		Slot select register (PPI PORT–A) signal
32	CS1H	I		Slot select register (PPI PORT–A) signal
33	CS1L	I		Slot select register (PPI PORT–A) signal
34	CS0H	I		Slot select register (PPI PORT–A) signal
35	CS0L	I		Slot select register (PPI PORT–A) signal
36, 37	A15, A14	I		CPU (Z80A) ADDRESS 15, 14 signal input
38	$\overline{MREQ}$	I	L	CPU (Z80A) $\overline{MREQ}$ signal input
39	$\overline{RFSH}$	I	L	CPU (Z80A) $\overline{RFSH}$ signal input
40	ϕ	I		CPU (Z80A) CLOCK signal input

VDP Video Display Processor (TMS9929A/TMS9918A)

Pin No.	Pin Name	I/O	Active	Function
1	$\overline{RAS}$	O	L	Low address strobe
2	$\overline{CAS}$	O		VRAM column address strobe
3 ~ 10	AD7, 6, 5, 4, 3, 2, 1, 0 (MSB)	O		VRAM address and data bus (VRAM low and column address and data multiplexed and output) (AD0 is the most significant bit)
11	R/$\overline{W}$	O	H=read	VRAM write strobe
12	Vss	I		Ground
13	MODE	I		CPU interface mode select
14	$\overline{CSW}$	I	L	Write strobe
15	$\overline{CSR}$	I	L	Read strobe
16	$\overline{INT}$	O		Interrupt signal to CPU
17 ~ 24	CD7, 6, 5, 4, 3, 2, 1, 0 (MSB)	I/O		CPU data bus (CD0 is the most significant bit) CPU data bus (CD0 is the most significant bit)
25 ~ 32	RD7, 6, 5, 4, 3, 2 1, 0 (MSB)	I		VRAM read data bus (RD0 is the most significant bit)
33	VDD	I		Voltage Supply +5V
34	$\overline{RESET}$/SYNC	I		3-level input pin (less than 0.6V: $\overline{RESET}$ active → VDP initialized, over 10V:SYNC active → VDP synchronized externally)
35	B–Y/EXTVID	O		B–Y color signal out/external video signal input
36	Y/COMVID	O		Y signal out (brightness and synchronous composite video signal)
37	GROMCLK	O		Output of quartz oscillator (or external clock) signal frequency divided by 24 (ordinarily not used)
38	R–Y/CLOCK	O		R–Y color signal out/clock ϕ output
39	XTAL2	I		Quartz oscillator connecting terminal
40	XTAL1			(10.73864MHz) (When driving external clock, drive both inputs)

● 74LS145 (iG12410)

O.C.BCD to DECIMAL Decorder/Driver



Truth Table

No	INPUTS D	C	B	A	OUTPUTS 0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

SSG Sound Generator (YM-2149)

Pin No.	Pin Names	I/O	Active	Function
1	Vss			Ground
2	NC			Non-connect
3, 4	ANALOG CHANNEL B, A	O		Output of D/A converter
5	NC			Non-connect
6 ~ 13	IOB7, 6, 5, 4, 3, 2, 1, 0	I/O		Parallel data 8 bit port input/output
14 ~ 21	IOA7, 6, 5, 4, 3, 2, 1, 0	I/O		Parallel data 8 bit port input/output
22	CLOCK	I		Supplies reference time for tone, noise and envelope generator
23	$\overline{\text{RESET}}$	I		$\overline{\text{RESET}}$ input
24	A9	I		Fixed to "L"
25	A8	I		Fixed to "H"
26	$\overline{\text{SEL}}$			Selection of CLOCK frequency
27	BDIR	I		Internal operation control command
28, 29	BC2, BC1	I		signal
30 ~ 37	DA7, 6, 5, 4, 3, 2, 1, 0	I/O		Data input/output
38	ANALOG CHANNEL C	O		Output of D/A converter
39	TEST1			Test pin
40	VDD			Voltage Supply +5V

PPI (μPD8255A)

Pin No.	Pin Name	I/O	Active	Function
1 ~ 4	PA3, 2, 1, 0			Port A (BIT)
5	$\overline{\text{RD}}$	I		Read input
6	$\overline{\text{CS}}$			Chip select
7	GND			Ground
8, 9	A1, A0			Internal register select signal input
10 ~ 17	PC7, 6, 5, 4, 0, 1, 2, 3			Port C (BIT)
18 ~ 25	PB0, 1, 2, 3, 4, 5, 6, 7			Port B (BIT)
26	VDD			Power Supply +5V
27 ~ 34	D7, 6, 5, 4, 3, 2, 1, 0			Data bus
35	RESET			RESET input
36	$\overline{\text{WR}}$			Write input
37 ~ 40	PA7, 6, 5, 4			Port A (BIT)

RAM (MB81416-12)

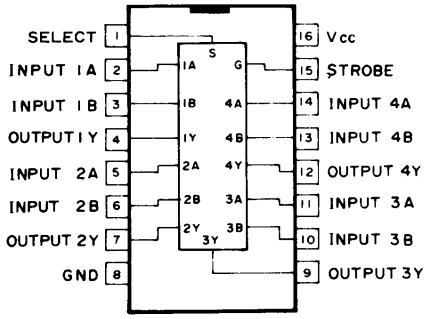
Pin No.	Pin Name	I/O	Active	Function
1	$\overline{OE}$	I		Output enable
2, 3	DQ1, DQ2	I/O		Data output
4	$\overline{WE}$	I		Write enable, write mode at active "L"
5	$\overline{RAS}$	I		Lower address strobe
6 ~ 8	A6, 5, 4	I		Address input
9	VDD			Voltage Supply +5V
10 ~ 14	A7, 3, 2, 1, 0	I		Address input
15	DQ3	I/O		Data output
16	$\overline{CAS}$	I		Column address strobe
17	DQ4	I/O		Data output
18	Vss			Ground Note) MB81416 is an N channel MOS RAM consisting of 16384 word x 4 bit. $\overline{RAS}$ only refresh type, write cycle (early write) type.;

V–RAM (MB8116) (μPD416C)

Pin No.	Pin Name	I/O	Active	Function
1	VBB			–5V
2	DIN	I		Data input
3	$\overline{WE}$	I	L	Write enable, write mode to D-RAM at active "L"
4	RAS	I	L	Lower address strobe
5 ~ 7	A0, 2, 1	I		Address bus
8	VDD			+12V
9	Vcc			+5V
10 ~ 13	A5, 4, 3, 6	I		Address bus
14	DOUT	O		Data output
15	$\overline{CAS}$	I	L	Column address strobe
16	Vss			Ground Note) MB8116 is an M-OS-N channel RAM consisting of 16384 word x 1bit Output is three state. $\overline{RAS}$ only refresh type, write cycle (early write) type. VDD: +12V, Vcc: +5V, VBB: –5V

● 74LS157 (iG059650)

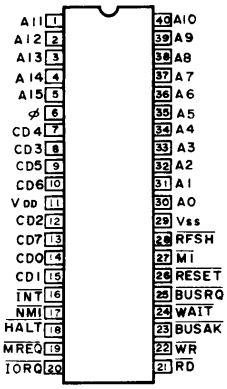
2 to 1 Data Selectors



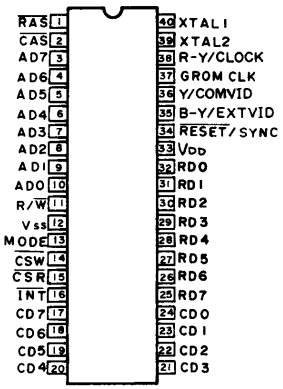
Truth Table

INPUTS		OUTPUT
Select	Strobe G	Y
X	H	L
L	L	A
H	L	B

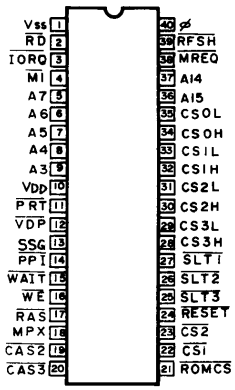
Z–80A



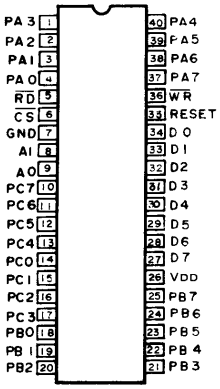
TMS9929A/TMS9918A



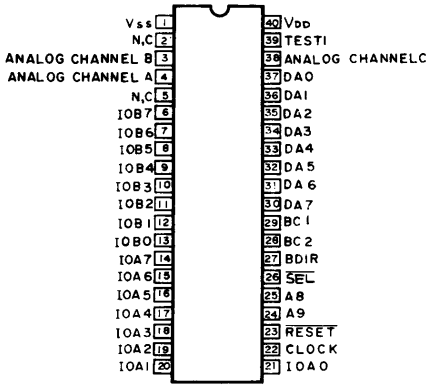
YM-5214



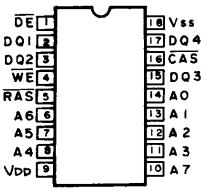
μPD8255A



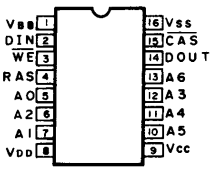
YM2149



MB81416-12

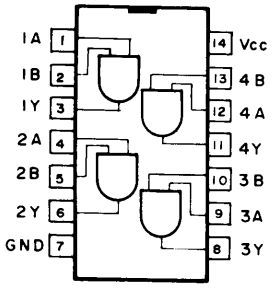


MB8116

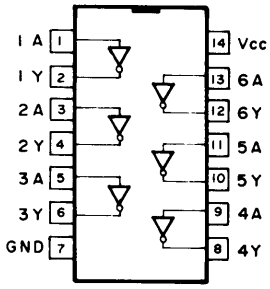


■IC BLOCK DIAGRAM

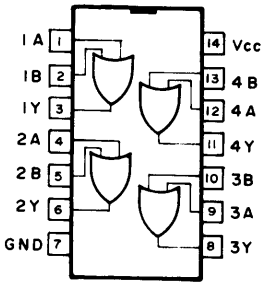
●74LS08 (iG043750)
Quad 2 Input AND



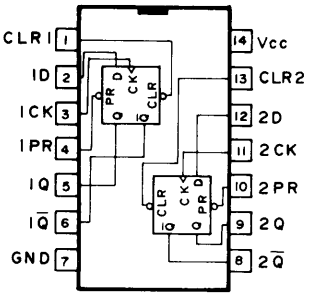
●74LS14 (iG049650)
Hex Schmitt
Trigger Inverters



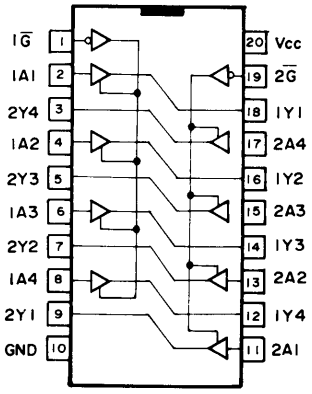
●74LS32 (iG049850)
Quad 2 Input
O.C. NOR Buffer



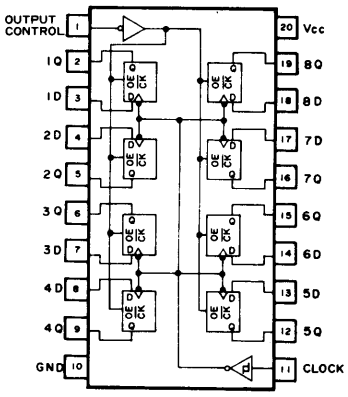
●74LS74 (iG044050)
Dual D-FFs
with preset and clear



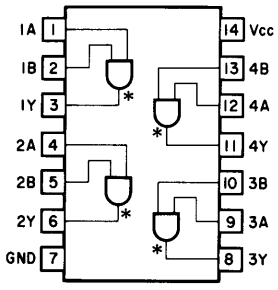
●74LS244 (iG060050)
Octal 3 State Bus Buffers



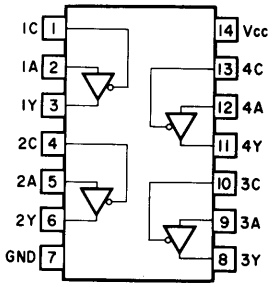
●74LS374
Octal 3 State D FFs



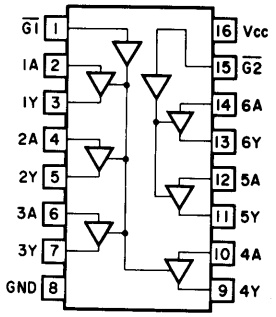
●74LS09(iG122500)
Quad 2 Input O.C.AND



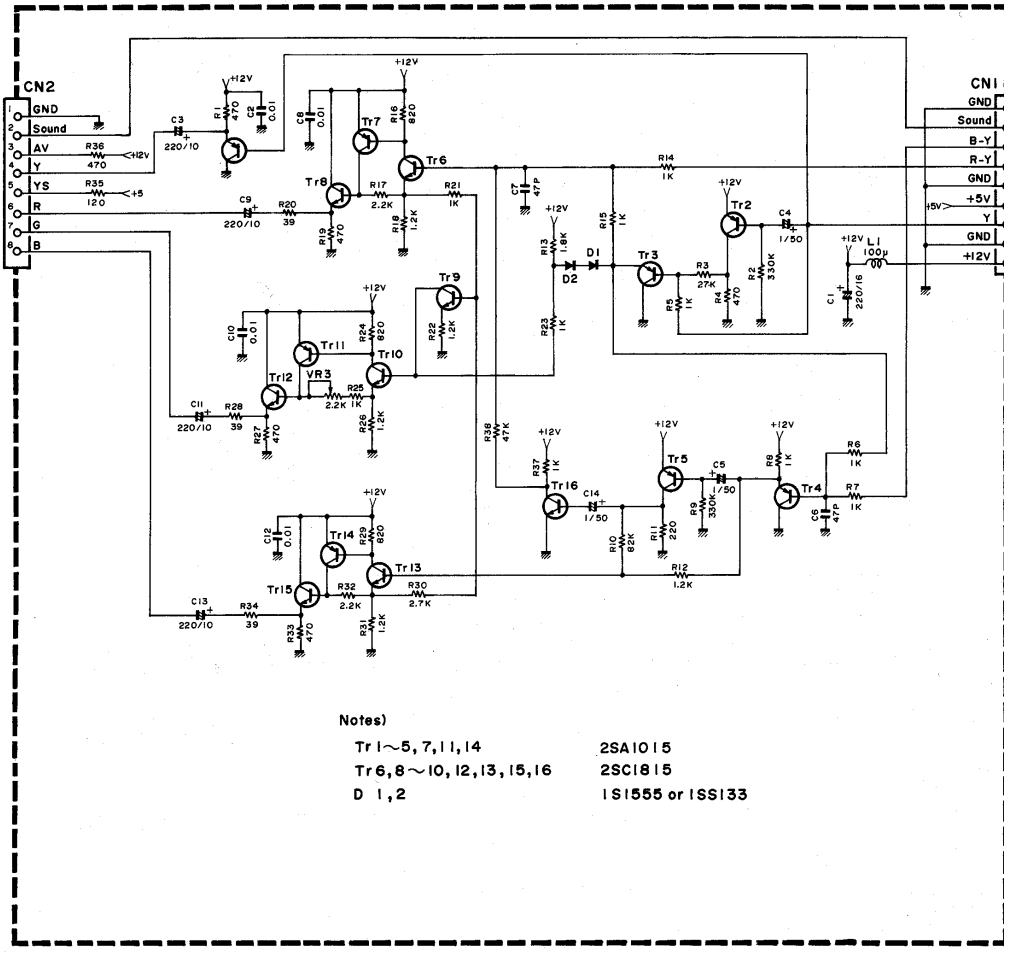
●74LS125(iG059550)
Quad 3 State Bus Buffers



●74LS367(iG071600)
Hex 3 State Bus Buffers

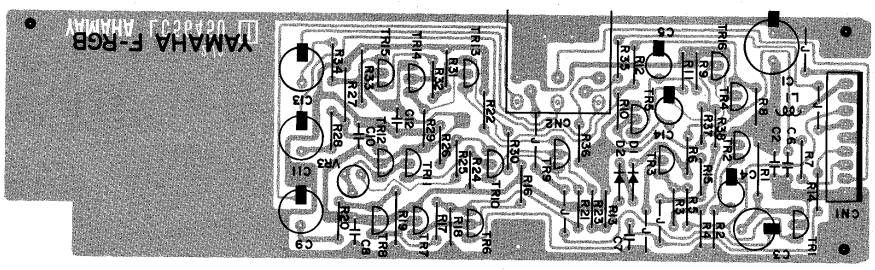


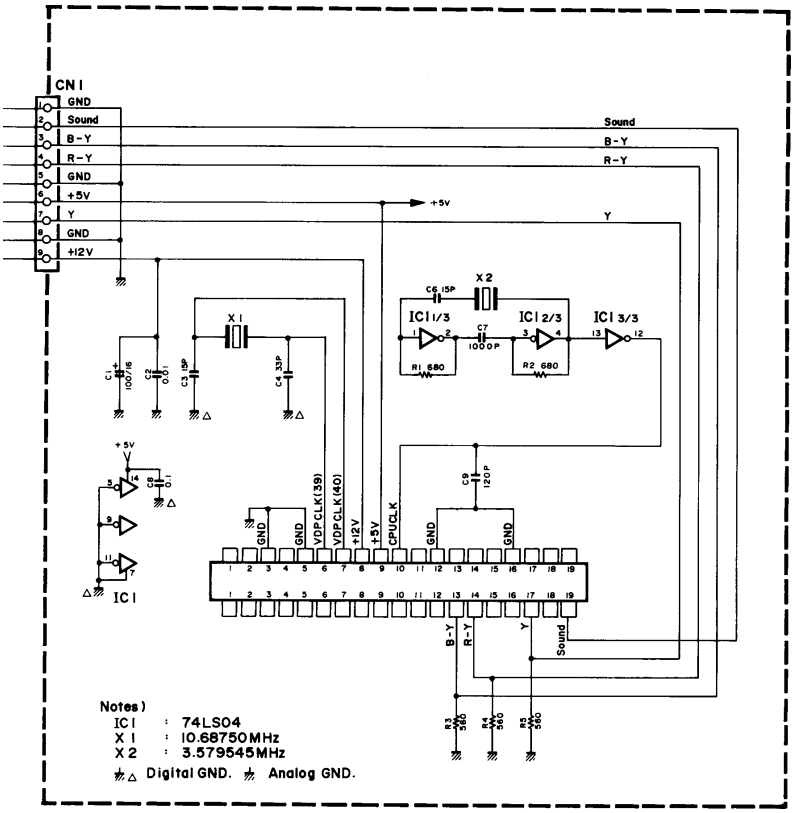
● RGB Circuit Diagram (NA551760)

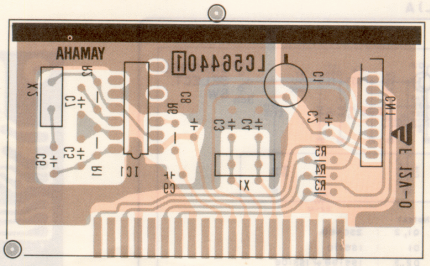


Notes)

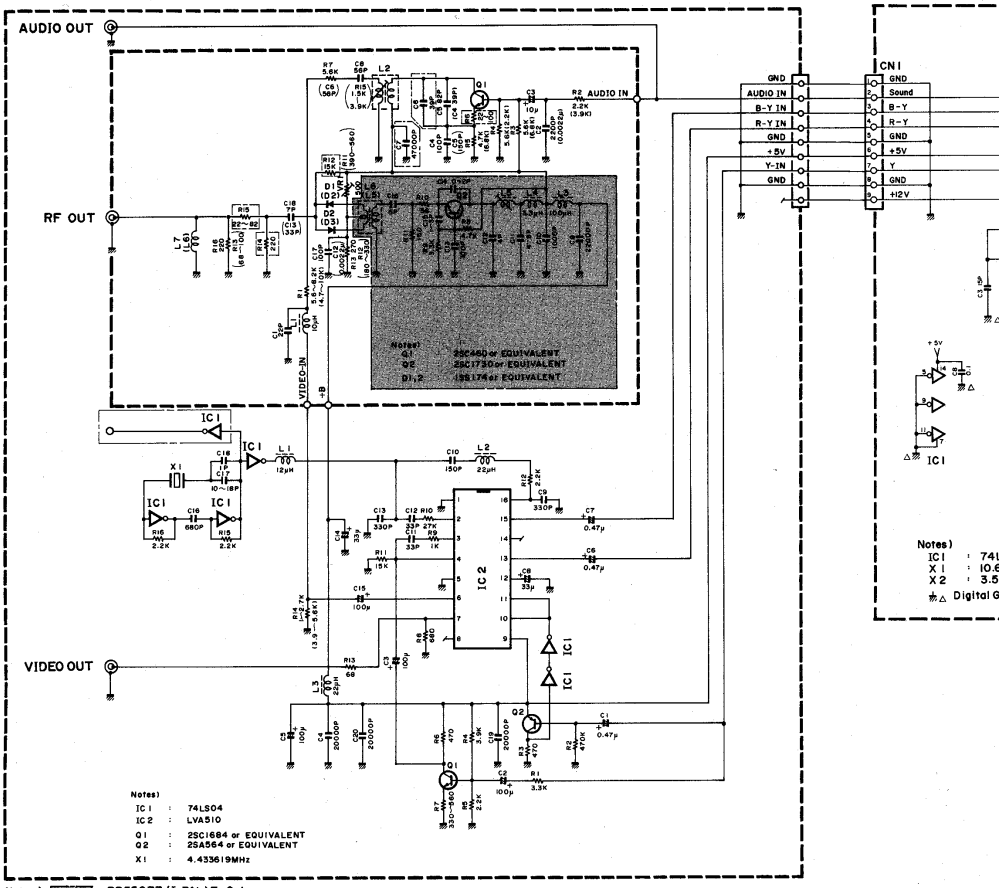
Tr 1~5, 7, 11, 14	2SA1015
Tr 6, 8~10, 12, 13, 15, 16	2SC1815
D 1, 2	1S1555 or 1SS133




CN1
GND
Sound
B-Y
R-Y
GND
+5V
Y
GND
+12V
Sound
B-Y
R-Y
Y
+5V
X1
X2
C6 15P
IC1 1/3
IC1 2/3
IC1 3/3
C7
1000P
R1 680
R2 680
C1
100/16
C2
0.01
C3 15P
C4 33P
C8
0.1
C9
120P
IC1
GND
GND
VDPCLK(39)
VDPCLK(40)
+12V
+5V
CPUCLK
GND
GND
B-Y
R-Y
Y
Sound
R3
560
R4
560
R5
560
Notes)
IC1 : 74LS04
X1 : 10.68750MHz
X2 : 3.579545MHz
Digital GND. Analog GND.

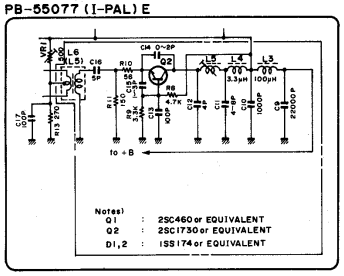

AHAMAY
LC89410

● ENCODER Circuit Diagram (G-PAL) PB55075

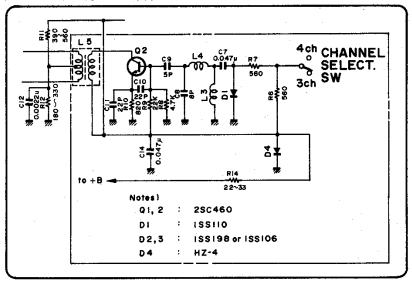


Notes) ■■■ PB55077 (I-PAL) E Only
( ) PB55076 (B-PAL) A

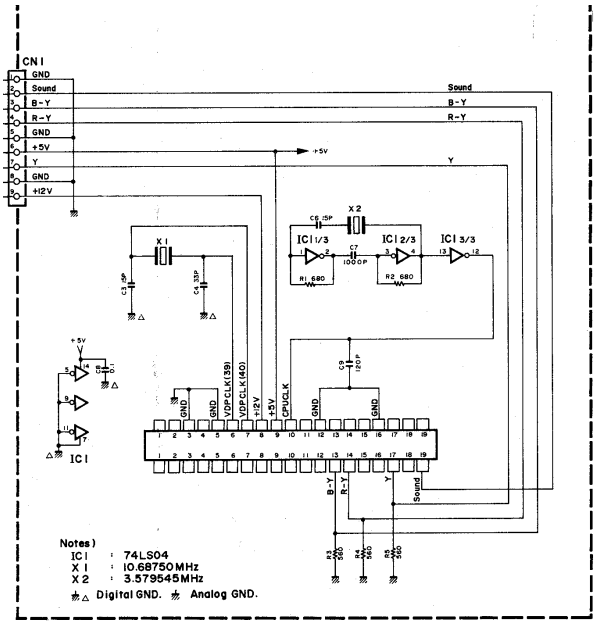
PB-55077 (I-PAL) E

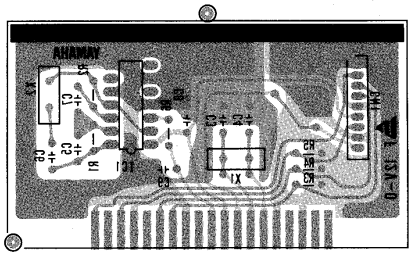


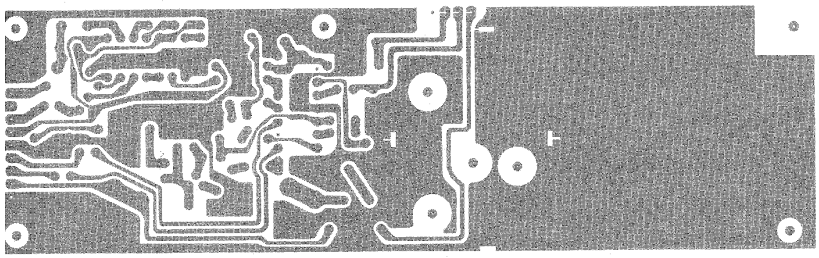
PB-55076 (B-PAL) A



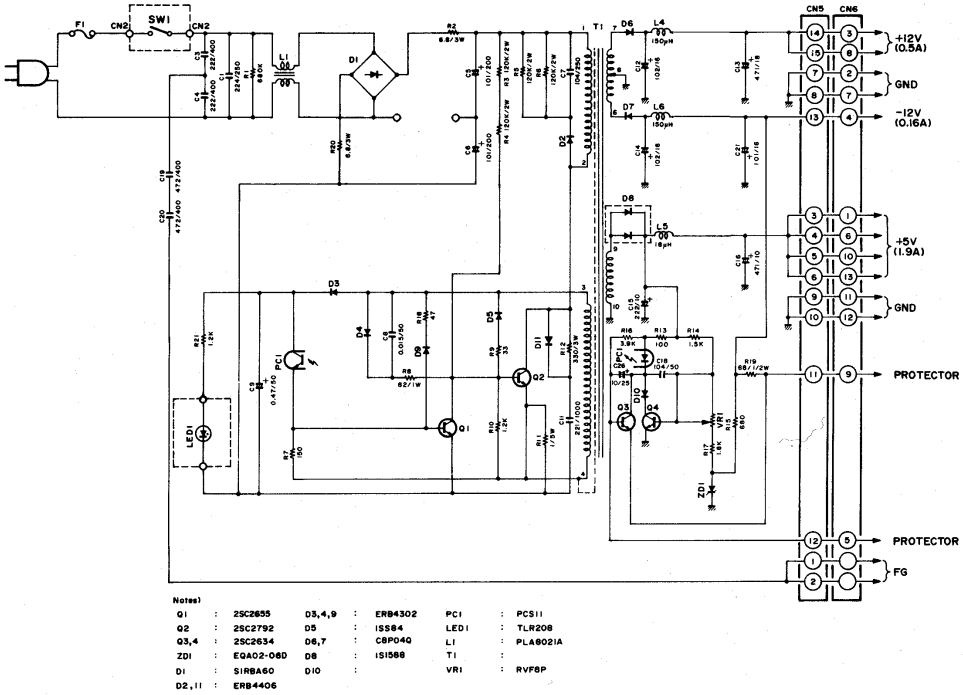



CN1
GND
Sound
B-Y
R-Y
GND
+5V
Y
GND
+12V
X1
X2
IC1 1/3
IC1 2/3
IC1 3/3
R1 680
R2 680
IC1
Notes)
IC1 : 74LS04
X1 : 10.68750MHz
X2 : 3.579545MHz
Digital GND. Analog GND.





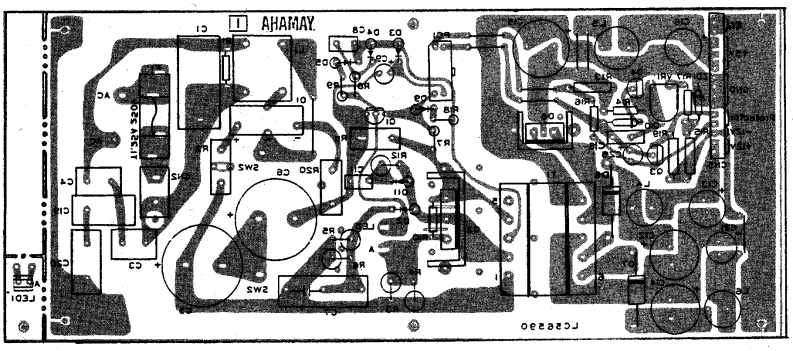
● Power Supply Circuit Diagram (NP55140, NP55150, NP55170)



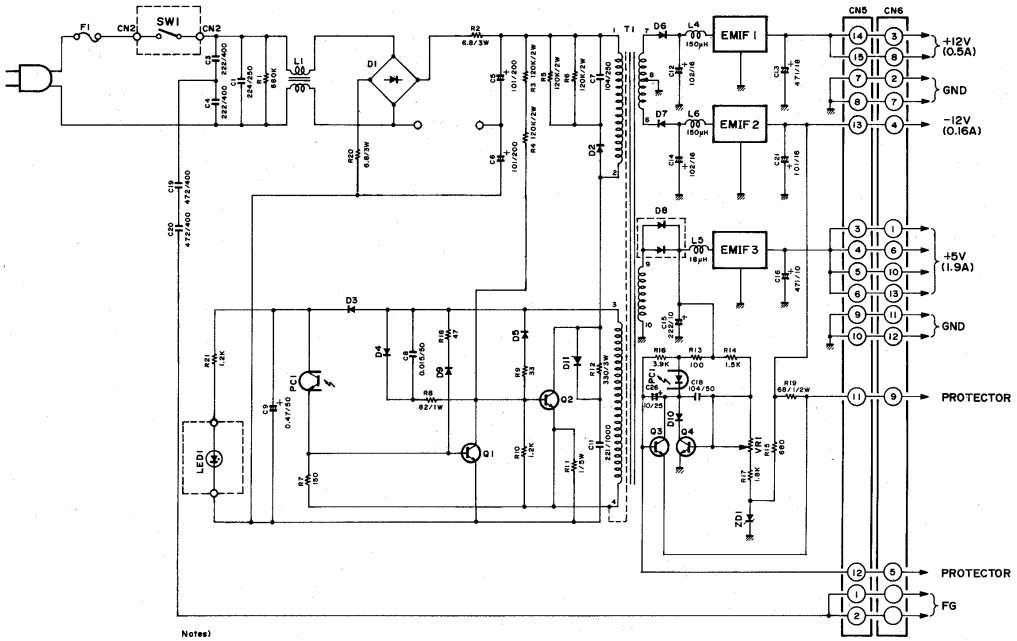
Notes)

Q1	:	2SC2655	D3,4,9	:	ERB4302	PC1	: PC511
Q2	:	2SC2792	D5	:	ISS84	LED1	: TLR206
Q3,4	:	2SC2634	D6,7	:	C8P040	L1	: PLA6021A
ZD1	:	EQA02-06D	D8	:	IS1588	T1	:
D1	:	SIRBA60	D10	:		VR1	: RVF8P
D2,11	:	ERB4406					

● Power Supply Circuit Board



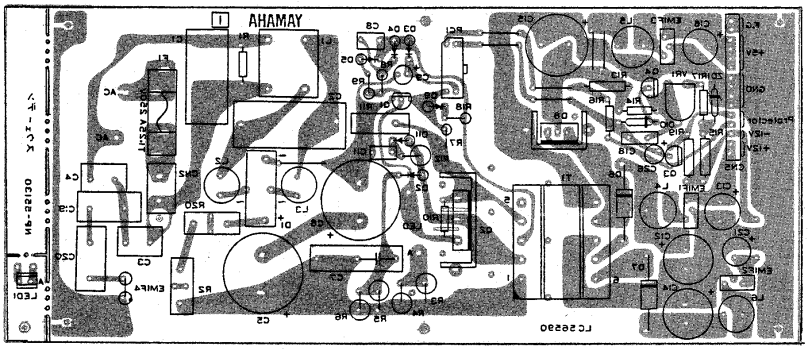
● Power Supply Circuit Diagram (NP55130)



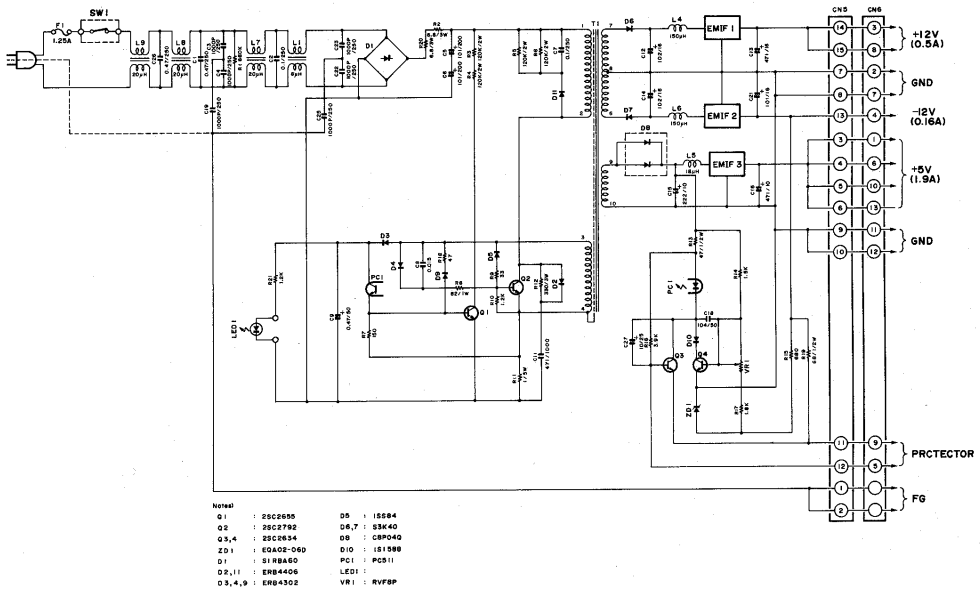
Notes)

Q1	:	2SC2655	D3,4,9	:	ERB4302	PC1	: PC511
Q2	:	2SC2792	D5	:	ISS84	LED1	: TLR208
Q3,4	:	2SC2634	D6,7	:	C8P040	L1	: PLA8021A
ZD1	:	EQA02-06D	D8	:	IS1588	T1	:
D1	:	SIRBA60	D10	:		VR1	: RVF8P
D2,11	:	ERB4406					

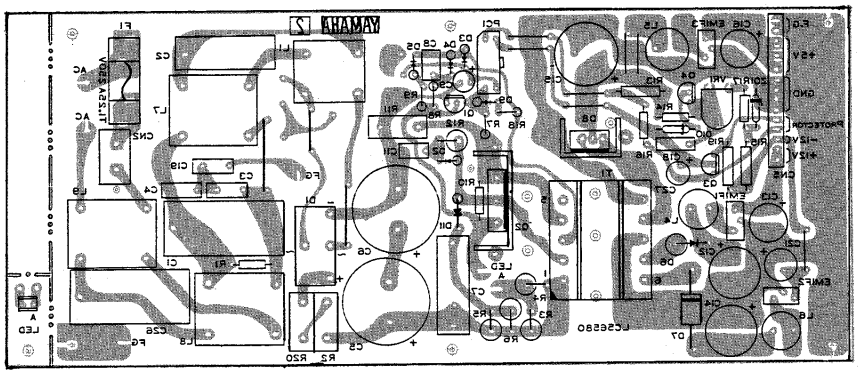
● Power Supply Circuit Board



● Power Supply Circuit Diagram (NP55180)

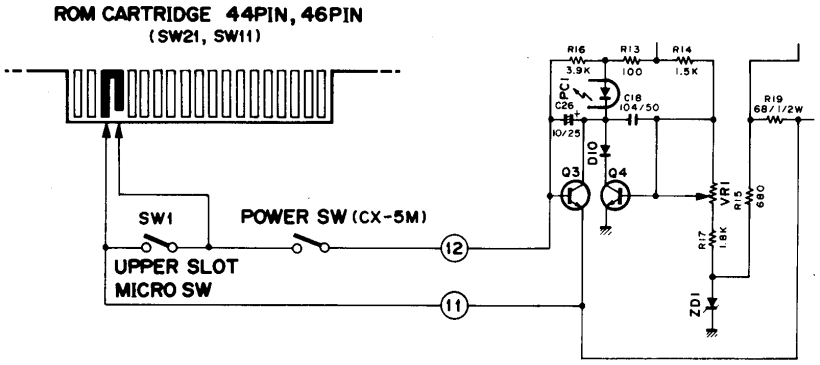


● Power Supply Circuit Board

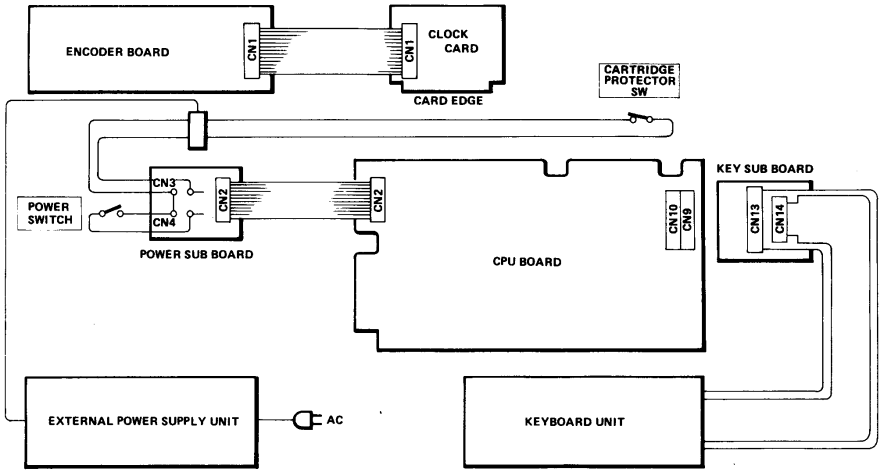


■OPERATION OF CARTRIDGE PROTECTION

The power supply circuit of this unit is the self RC circuit type and specified secondary voltageis is given by the feedback of PC-1 as shown to the figure. In the cartridge protector circuit, SW1 is shorted when the ROM cartridge is not inserted in the upper slot. For this reason, Q3 is non operating. When the cartridge is inserted, SW1 become open, Q3 is ON. In the result, the voltage supply stops. After that, when the cartridge is fully put in, Q3 becomes OFF and power is supplied because pin 44 (SW21) and pin 46 (SW11) are shorted.



■WIRING BLOCK DIAGRAM



ENCODER BOARD ⟷ CLOCK CARD

CN1

1	GND
2	AUDIO IN
3	B - Y
4	R - Y
5	GND
6	+5V
7	Y
8	GND
9	

CN1

1	GND
2	SOUND
3	B - Y
4	R - Y
5	GND
6	+5V
7	Y
8	GND
9	+12V

POWER SUB BOARD ⟷ CPU BOARD

CN2

1	−12
2	+12
3	+12
4	GND
5	GND
6	GND
7	+5
8	+5

CN2

1	−12
2	+12
3	+12
4	GND
5	GND
6	GND
7	+5
8	+5

KEY SUB BOARD ⟷ KEYBOARD UNIT

CN9

12	$\overline{Y3}$
11	$\overline{Y2}$
10	$\overline{Y1}$
9	$\overline{Y0}$
8	$\overline{X7}$
77	$\overline{X6}$
6	$\overline{X5}$
5	$\overline{X4}$
4	$\overline{X3}$
3	$\overline{X2}$
2	$\overline{X1}$
1	$\overline{X0}$
0	GND

CN13

14	POWER
13	+5
12	$\overline{X4}$
11	$\overline{X6}$
10	$\overline{X1}$
9	$\overline{X2}$
8	$\overline{X3}$
7	$\overline{X5}$
6	$\overline{X7}$
5	$\overline{X0}$
4	$\overline{CODE}$
3	+5
2	$\overline{CAPS}$
1	+5

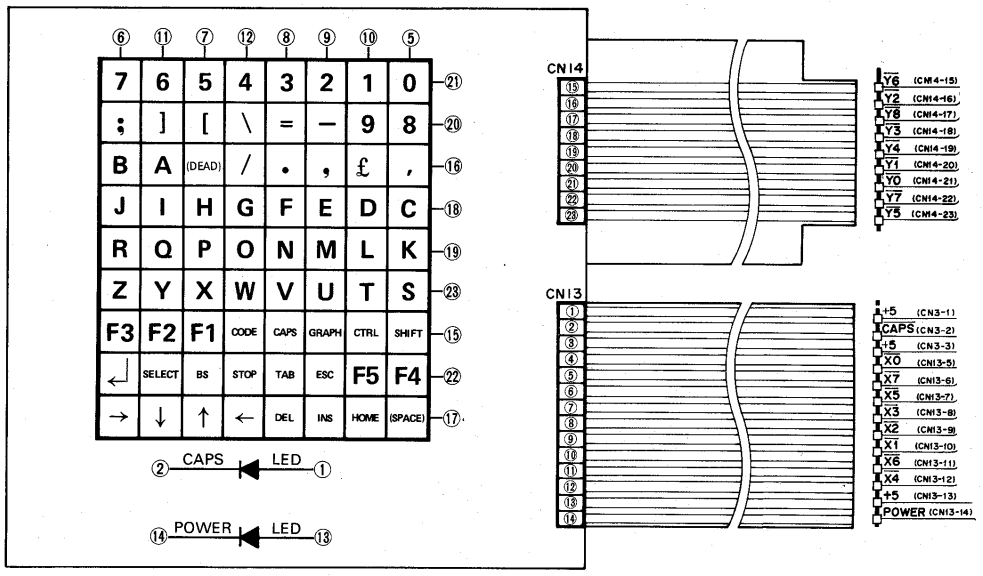
CN10

12	+5
11	+5
10	+5
9	POWER
8	$\overline{CODE}$
7	$\overline{CAPS}$
6	$\overline{Y9}$
5	$\overline{Y8}$
4	$\overline{Y7}$
3	$\overline{Y6}$
2	$\overline{Y5}$
1	$\overline{Y4}$
0	GND

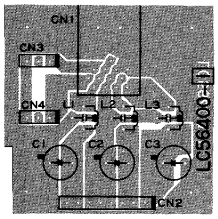
CN14

23	$\overline{Y5}$
22	$\overline{Y7}$
21	$\overline{Y0}$
20	$\overline{Y1}$
19	$\overline{Y4}$
18	$\overline{Y3}$
17	$\overline{Y8}$
16	$\overline{Y2}$
15	$\overline{Y6}$

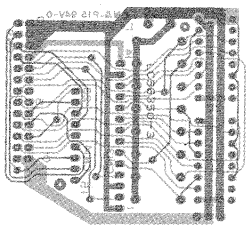
■KEYBOARD MATRIX TABLE

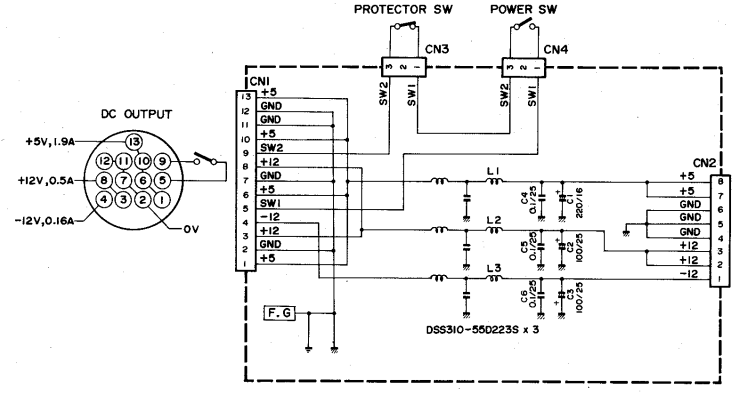


● Power Sub Circuit Board & Diagram

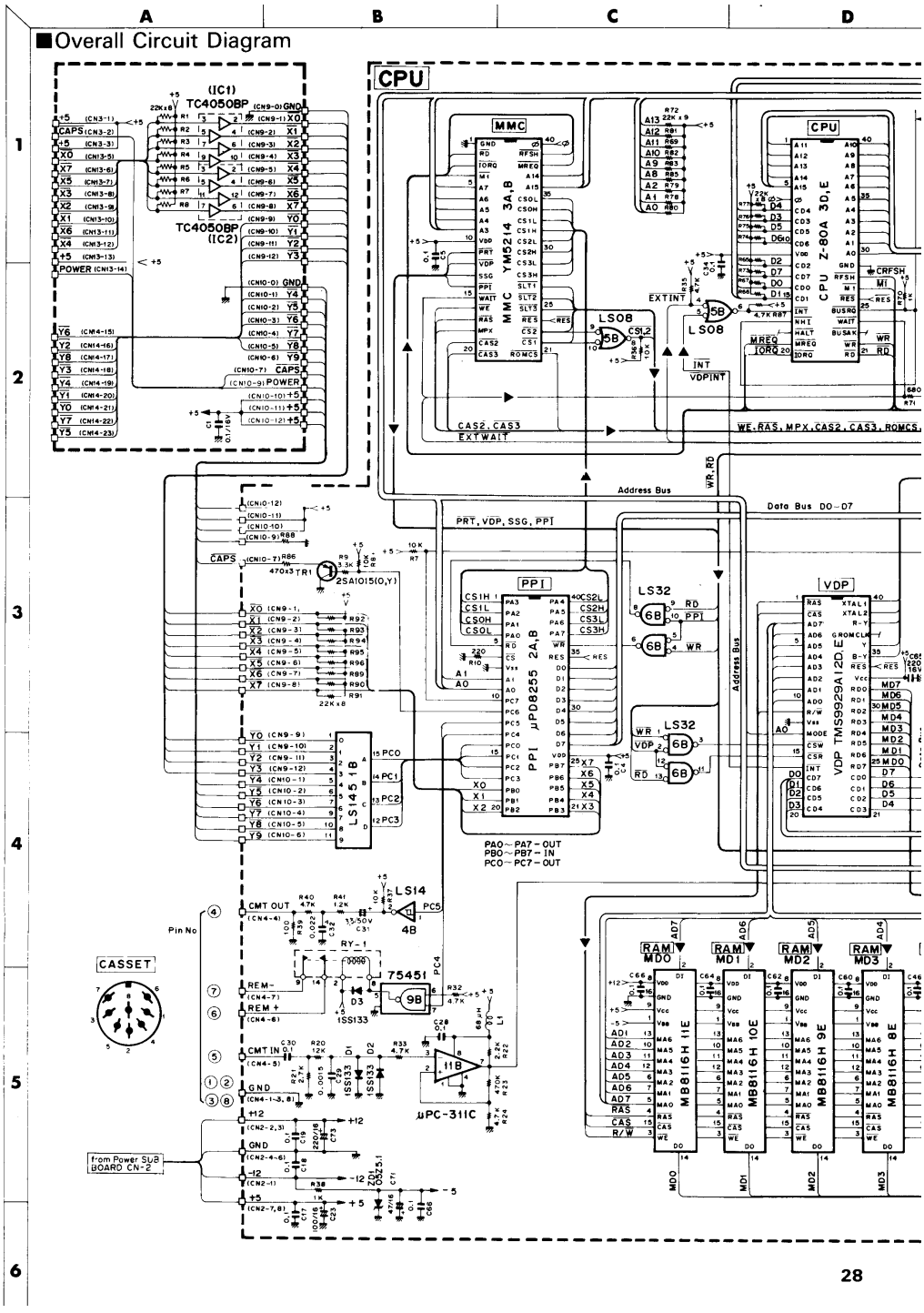


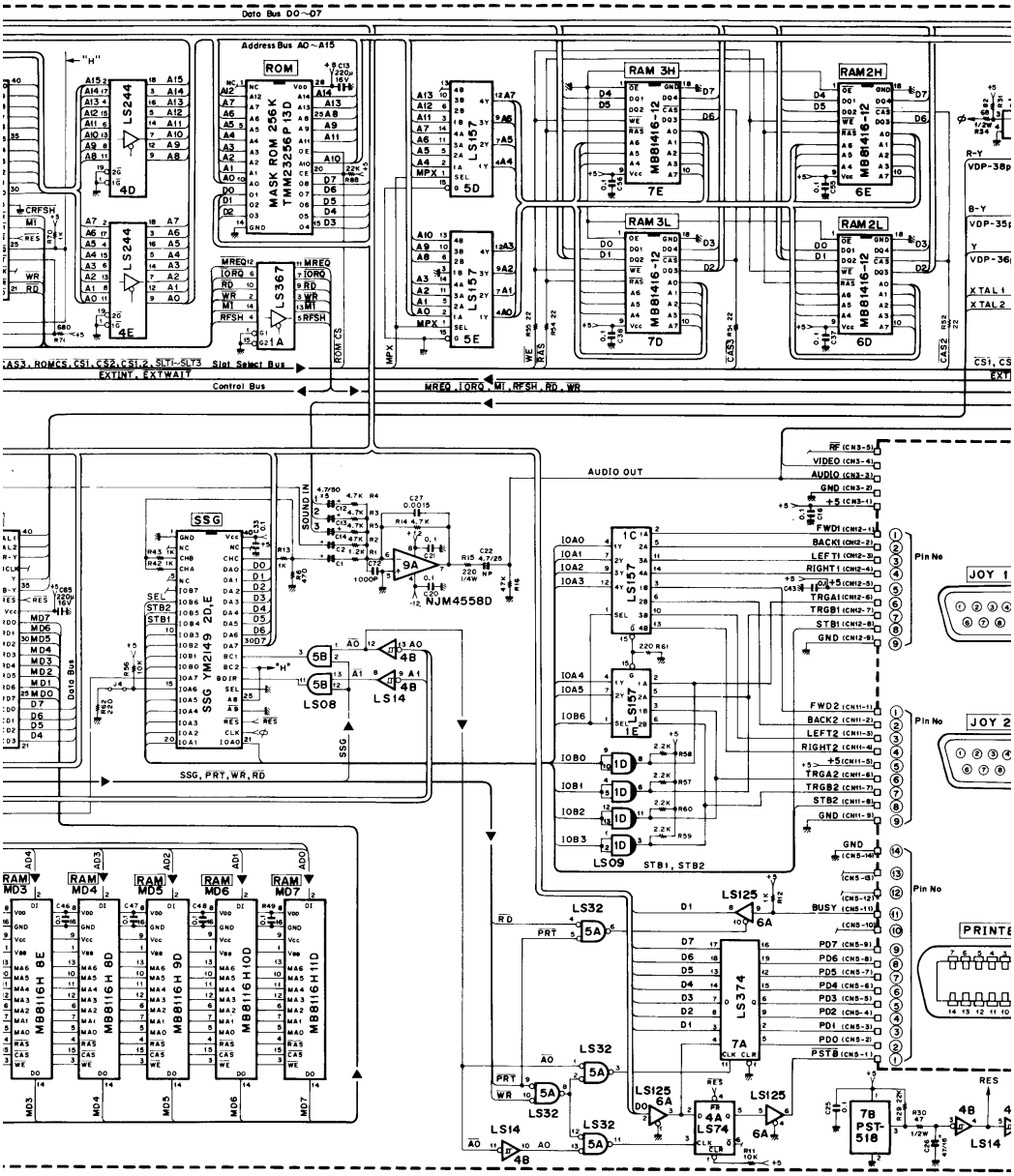
● Key Sub Circuit Board

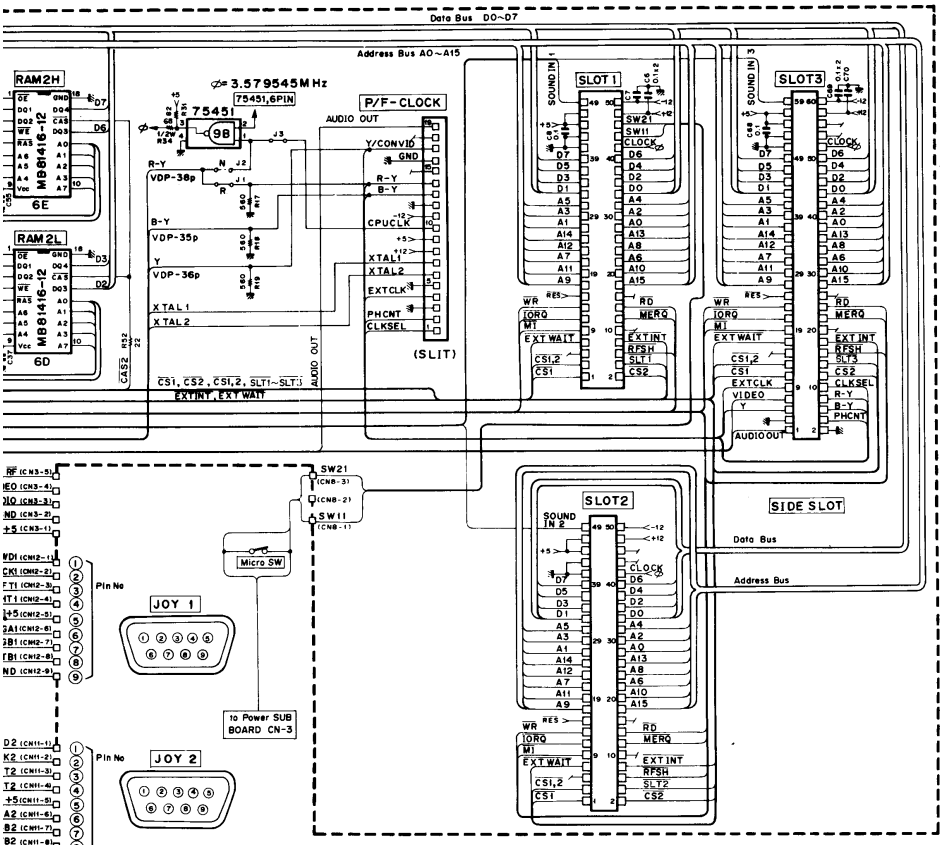




■Overall Circuit Diagram




Data Bus D0~D7
Address Bus A0~A15
ROM
MASK ROM 256K TMM23256P-13D
LS244
4D
4E
LS367
4A
LS157
5D
5E
RAM 3H
RAM 3L
RAM2H
RAM2L
MB81416-12
7E
7D
6E
6D
MREQ IORQ RD WR M1 RFSH
Slot Select Bus
Control Bus
MREQ, IORQ, MT, RFSH, RD, WR
SSG
SSG YM2149 20,E
SOUND IN
NJM4558D
AUDIO OUT
LS157
LS09
LS08
LS14
LS32
LS125
LS374
LS74
7B PST-518
JOY 1
JOY 2
PRINTE
Pin No
VDP-38p
VDP-35
VDP-36
XTAL1
XTAL2
RF (CN3-5)
VIDEO (CN3-4)
AUDIO (CN3-3)
GND (CN3-2)
+5 (CN3-1)
FWD1 (CN12-1)
BACK1 (CN12-2)
LEFT1 (CN12-3)
RIGHT1 (CN12-4)
TRGA1 (CN12-6)
TRGB1 (CN12-7)
STB1 (CN12-8)
GND (CN12-9)
FWD2 (CN11-1)
BACK2 (CN11-2)
LEFT2 (CN11-3)
RIGHT2 (CN11-4)
TRGA2 (CN11-6)
TRGB2 (CN11-7)
STB2 (CN11-8)
GND (CN11-9)
GND (CN5-14)
BUSY (CN5-11)
PD7 (CN5-9)
PD6 (CN5-8)
PD5 (CN5-7)
PD4 (CN5-6)
PD3 (CN5-5)
PD2 (CN5-4)
PD1 (CN5-3)
PD0 (CN5-2)
PSTB (CN5-1)
SSG, PRT, WR, RD
STB1, STB2



P/F-CLOCK CARD

→	19	SOUND (AUDIO)
	18	NC
→	17	Y
*	16	D-GND
	15	NC
→	14	R-Y
→	13	B-Y
*	12	D-GND
	11	NC
←	10	CPU CLOCK(3.579545MHz)
→	9	+5V
→	8	+12V
←	7	VDPCLK(40)
←	6	VDPCLK(39)
*	5	GND
	4	NC
*	3	GND
	2	NC
	1	NC

ENCODER BOARD A/V OUTPUT

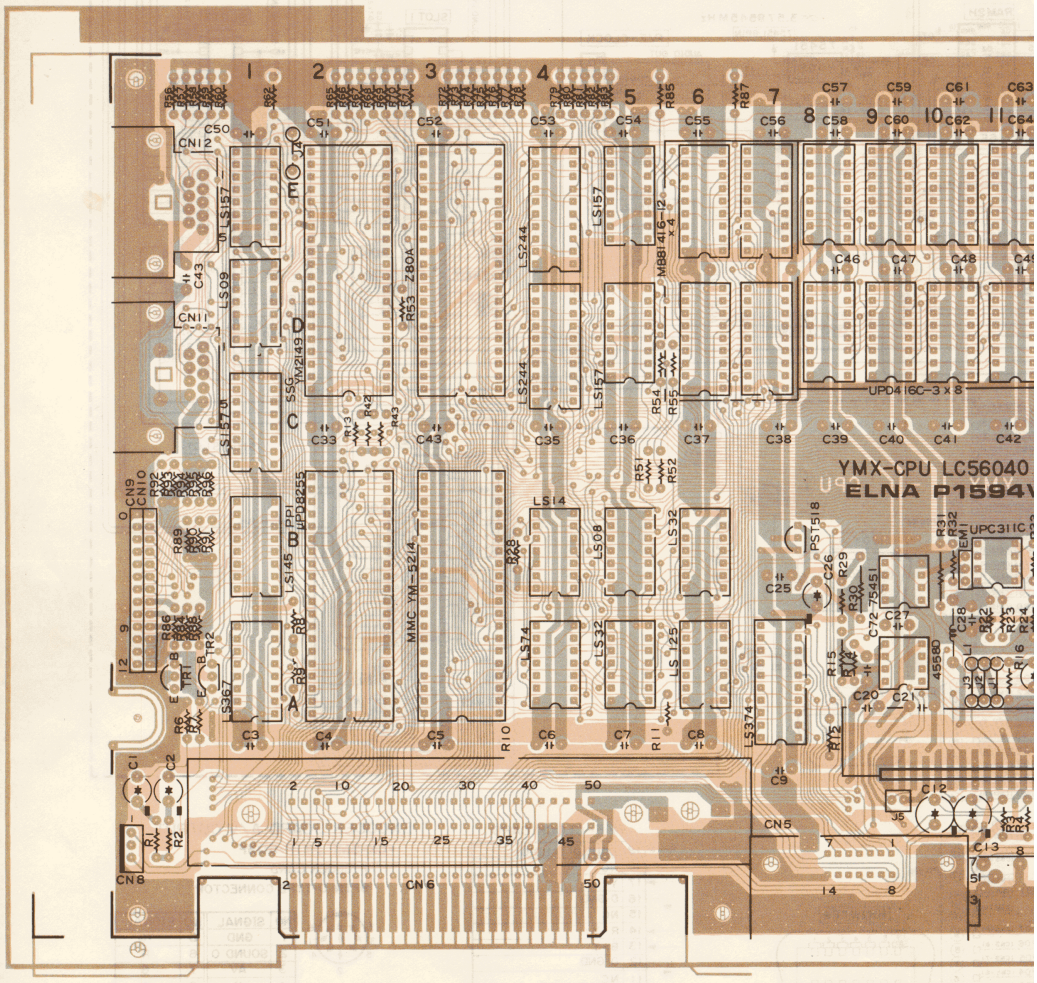
- **CX-5MF, YIF-503F**
  - F-CLOCK CARD
  - 8PIN D-TYPE CONNECTOR

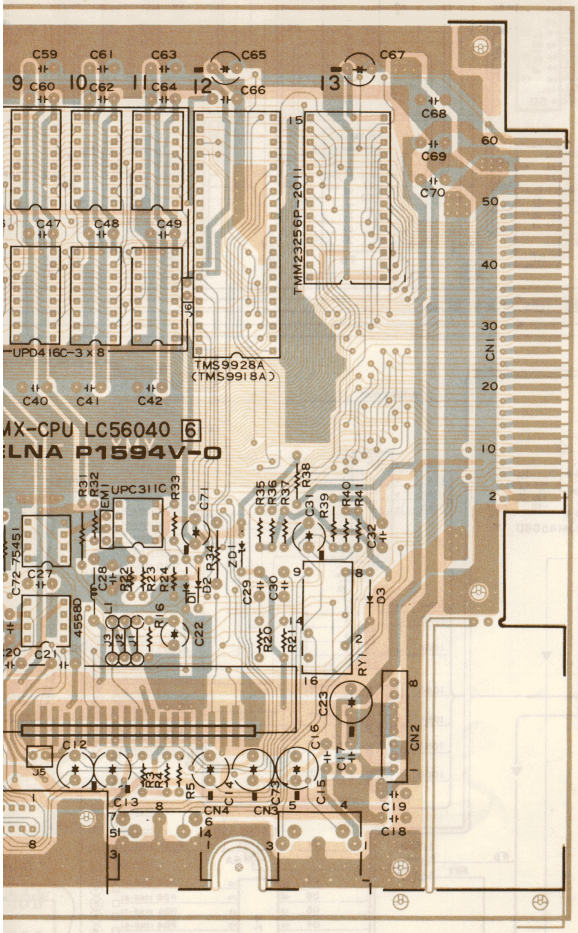


NO	SIGNAL	NO	SIGNAL
1	GND	5	YS
2	SOUND O	6	R
3	AV	7	G
4	Y	8	B

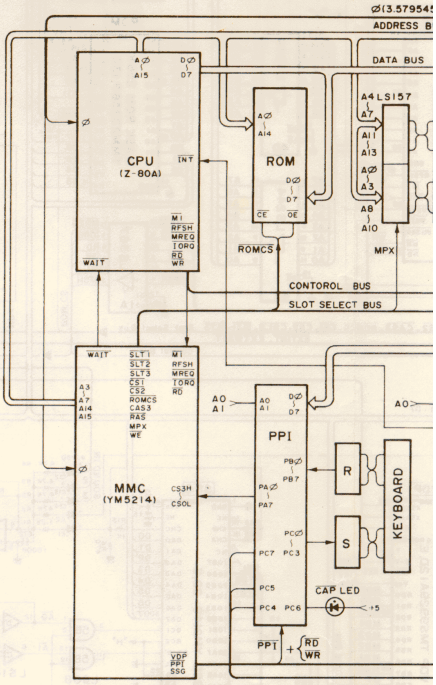
- **CX-5M,E,A,G,S**
  - P-CLOCK CARD
  - RCA-TYPE CONNECTOR
    - RF-OUT
    - MONITOR-OUT
    - SOUND-OUT

■CPU Circuit Board

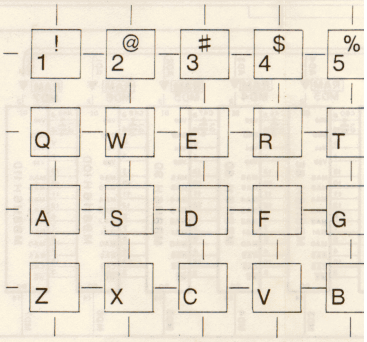


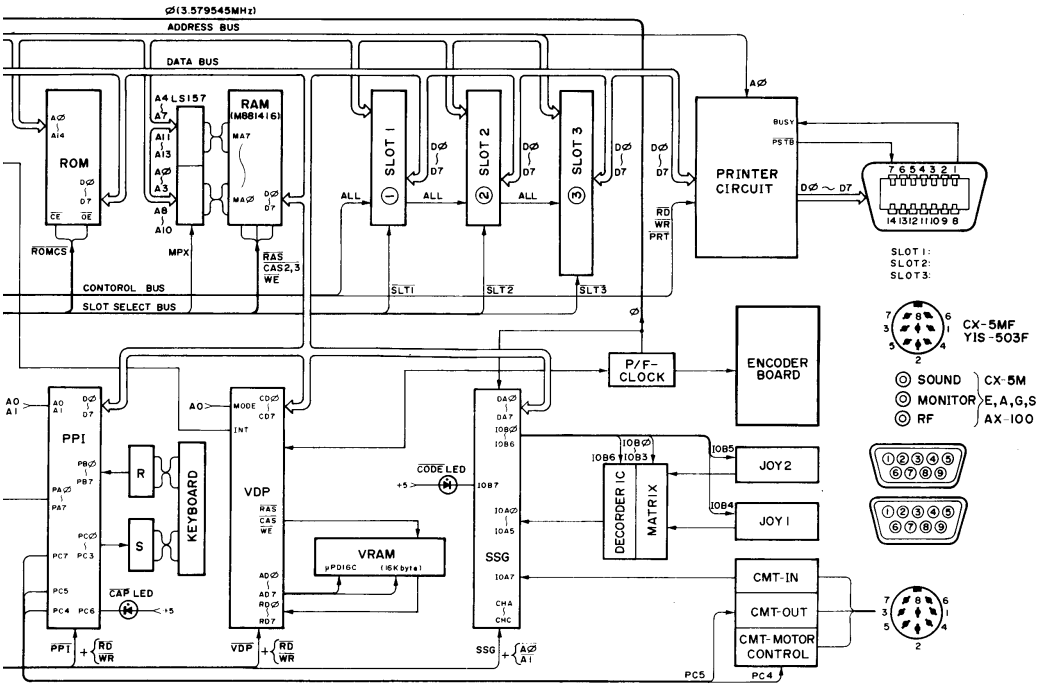


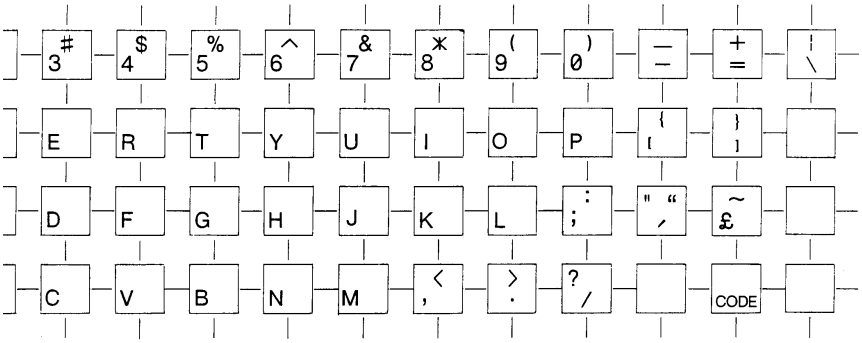
■BLOCK DIAGRAM



■KEYBOARD




ø(3.579545MHz)
ADDRESS BUS
DATA BUS
ROM
RAM (M68I416)
A4 LS157
SLOT 1
SLOT 2
SLOT 3
PRINTER CIRCUIT
BUSY
PSTB
D0 ~ D7
SLOT 1:
SLOT 2:
SLOT 3:
ROMCS
MPX
RAS CAS2,3 WE
CONTOROL BUS
SLOT SELECT BUS
SLT1
SLT2
SLT3
RD WR PRT
P/F-CLOCK
ENCODER BOARD
CX-5MF
YIS-503F
SOUND
MONITOR
RF
CX-5M
E,A,G,S
AX-100
PPI
VDP
VRAM (16Kbyte)
SSG
KEYBOARD
R
S
CAP LED
CODE LED
DECORDER IC
MATRIX
JOY2
JOY1
CMT-IN
CMT-OUT
CMT-MOTOR CONTROL
PC5
PC4


3 # 4 $ 5 % 6 ^ 7 & 8 * 9 (0) - = \
E R T Y U I O P [ ]
D F G H J K L ; : ' " / ~ £
C V B N M , < . > / ?
CODE